Abstract: A receiver circuit comprising first and second antennas; an input amplification stage comprising first and second input amplifier circuits for amplifying first and second signals received at the first and second antennas respectively; a switching stage comprising first and second transconductance components connected respectively to the first and second input amplifier circuits and to a common output, and a switching mechanism arranged to selectively turn on and off the first and second transconductance components so that only one of the first and second transconductance components is in an on state at any time, the first and second transconductance components further amplifying the first and second signals respectively when in an on state; and an output amplification stage connected to the common output of the switching stage and comprising an output amplifier circuit for further amplifying the first and second signals when they are outputted via the common output.
Title

A RECEIVER CIRCUIT

Field

The present invention relates to a receiver circuit and an amplifying and switching circuit for a radar receiver.

Background

Automotive radar systems may be installed in vehicles to assist drivers. These systems may provide the driver with information about distance between the driver's vehicle and other vehicles or obstacles present on the road. In some implementations, radar systems can be used to control aspects of operation of the vehicle, for example to control the braking system to avoid a crash.

In automotive radar systems, the transmitter sends out a signal through a transmit antenna. The propagated signal reaches the target and partially reflects back to the radar system. The reflected signal is picked up by a receive antenna of a receiver circuit (Rx). In order to assist with high resolution detection, the receiver can have a plurality of antennas, each with its own receive channel as shown in Figure 1. A drawback of this architecture is that it requires a complex local oscillation (LO) distribution network to provide LO signals for mixers in the Rx circuits that are used to recover information from the reflected signal.
It would be advantageous to provide an alternative receiver circuit.

Summary of the Invention

In a first aspect, the invention provides a receiver circuit comprising:

- a first antenna;
- a second antenna;
- an input amplification stage comprising a first input amplifier circuit for amplifying a first signal received at the first antenna, and second input amplifier circuit for amplifying a second signal received at the second antenna;
- a switching stage comprising first and second transconductance components connected respectively to the first and second input amplifier circuits and to a common output, and a switching mechanism arranged to selectively turn on and off the first and second transconductance components so that only one of the first and second transconductance components is in an on state at any time, the first and second transconductance components further amplifying the first and second signals respectively when in an on state; and
- an output amplification stage connected to the common output of the switching stage and comprising an output amplifier circuit for further amplifying the first and second signals when they are outputted via the common output.

In an embodiment, the first and second transconductance components comprise first and second transistors arranged in a common source topology.
In an embodiment, the common output is formed by connecting the drains of the first and second transistors.

In an embodiment, the receiver circuit comprises a third antenna and wherein the input amplification stage a third input amplifier circuit for amplifying a third signal received at the third antenna, and wherein the switching stage comprises a third transconductance component connected to the third input amplifier circuit and the common output for further amplifying the third signal, and wherein the switching mechanism is further arranged to turn the third transconductance component on and off.

In an embodiment, the third transconductance component comprise a third transistor arranged in a common source topology.

In an embodiment, the switching mechanism comprises fourth and fifth transistors connected respectively to the first and second transistors and which when switched on respectively turn on the first and second transistors.

In an embodiment, the switching mechanism comprises fourth, fifth and sixth transistors connected respectively to the first, second and third transistors and which when switched on respectively turn on the first, second and third transistors.

In an embodiment, the first and second input amplifier circuits each comprise a plurality of common source amplifiers.
In an embodiment, the first and second input amplifiers each comprise at least one input matching component.

In an embodiment, the first and second input amplifier circuits each comprise three common source amplifiers.

In an embodiment, the output amplifier circuit comprises a plurality of common source amplifiers.

In an embodiment, the receiver circuit comprises two common source amplifiers.

In a second aspect, the invention provides an amplifying and switching circuit for a radar receiver, the circuit comprising:

- an input amplification stage comprising a first input for connection to a first antenna, a second input for connection to a second antenna, a first input amplifier circuit for amplifying a first signal received at the first input, and second input amplifier circuit for amplifying a second signal received at the second input;
- a switching stage comprising first and second transconductance components connected respectively to the first and second input amplifier circuits and to a common output, and a switching mechanism arranged to selectively turn on and off the first and second transistors so that only one of the first and second transconductance components is in an on state at any time, the first and second transconductance components further amplifying the first and second signals respectively when in an on state; and
- an output amplification stage connected to the common output of the switching stage and comprising an output amplifier circuit for further amplifying the first and
second signals when they are outputted via the common output.

**Brief Description of the Drawings**

Embodiments of the invention will now be described in relation to the following drawings, in which:

- Figure 1 is a schematic diagram of a prior art receiver circuit;
- Figure 2 is a schematic diagram of a receiver circuit of an embodiment of the invention;
- Figures 3a and 3b are schematic diagrams illustrating the operation of the receiver of Figure 2;
- Figure 4 shows the operation of the switching stage of the receiver circuit of an embodiment;
- Figure 5 shows how the switching stage can be extended to allow the receiver circuit to accommodate more antennas;
- Figure 6 is a circuit diagram of an amplifying and switching circuit of an embodiment;
- Figures 7a and 7b illustrate common source and Cascode amplifiers respectively;
- Figure 8 shows the simulated S parameter of the selected channel of the receiver circuit; and
- Figure 9 shows the simulated S parameter of the blocked channel of the receiver circuit.

**Detailed Description**

Referring to Figures 2 to 7, a receiver circuit 100 of an embodiment comprises two or more antennas with a switching stage that enables switching between the antennas so as to
reduce the number of components required to form receiver
channels while advantageously balancing power consumption,
silicon area and reductions in Rx sensitivity. The proposed
receiver circuit allows selection between two or more
antennas and incorporates a switching stage that has
conversion gain. The receiver circuit 100 reduces the number
of local oscillation signals that need to be distributed to Rx mixers.

The receiver circuit 100 is intended to be implemented on a
CMOS chip with a 65nm process accordingly it will be
appreciated that other components (such as a mixer) will be
implemented on the same chip and form part of the radar
receiver circuit.

A simplified diagram of a receiver circuit 100 for two
antennas is shown in Figure 2. The receiver circuit 100 has
two antennas 101,102, an input amplification stage 110
comprising two input amplifier circuits 111,112 (InAmp1 and
InAmp2), a switching stage 120 that implements a
transconductance with switching function (TranSw), and an
output amplifier stage 130 (OutAmp) which is then connected
to further components of the receiver channel such as a
mixer (not shown). It will be appreciated that signals
received at the antennas 101,102 are amplified by the input
stage 110 but only one of the signals is amplified by the
output amplifier 130 at any time.

The operation of the proposed receiver circuit 100 is shown
in Figure 3. In Figure 3a, when the input signal from RxAnt1
is selected, as indicated by arrow 141 a first
transconductance component 121 of the TranSw 120 amplifies
the signal received via InAmp 101 from RxAnt1 which is then
further amplified by OutAmp 130. As indicated by arrow 142, TranSW 120 blocks 122 the signal from RxAnt2 102. In Figure 3b, when the input signal from RxAnt2 102 is selected, as indicated by arrow 152, a second transconductance component 124 of the TranSw 120 amplifies the signal from RxAnt2 102. As indicated by arrow 151, TranSW 120 blocks 123 the signal from RxAnt1 101.

A schematic diagram of the switching stage 120 (TranSw) is shown in Figure 4a. The TranSw 120 has a pair of common source amplifiers $M_1$ and $M_2$ whose drains are connected to provide a common output. Transistors $M_3$ and $M_4$ act as switching mechanism under control of switching signals 401, 402 which are the complement of one another and can be provided by a clock signal.

The operation of the TranSw 120 is described in relation to Figs. 4b and c. When the received signal from channel 1 ($v_{in1}$) is wanted (in this embodiment, the signal from InAmpl 111), in Figure 4b, switching signal 401 is set so that $M_3$ is open, $M_1$ is biased as a normal common source amplifier, while switching signal 402 causes $M_4$ to short the signal from channel 2 ($v_{in2}$) to ground as well as making $M_2$ off. As a result, the output current is only caused by $v_{in1}$ and expressed by:

$$i_o = v_{in1} \frac{\mu C}{1}$$  \hspace{1cm} (1)

In another words, the signal from channel 1 is let through while signal from channel 2 is blocked. When the receive
signal from channel 2 \((v_{in2})\) is wanted, in Figure 4c, switching signal 401 is set so \(M_3\) is shorts the signal from channel 1 \((v_{in1})\) to ground as well as making \(M_1\) off, while switching signal 402 is set so that \(M_4\) is open and \(M_2\) is biased as a normal common source amplifier. As a result, the output current is only caused by \(v_{in2}\) and expressed by:

\[
 i_o = v_{in2} \eta_2 \tag{2}
\]

That is, the signal from channel 2 is let though while signal from channel 1 is blocked.

Figure 5 shows how, the receiver circuit can be adapted to select an arbitrary number \((N)\) of channels - i.e., with more than two antennas, for example with three antennas (when \(N=3\)). Note that the switching signals 501 for \(N\) channels that control switching transistors \(M_3, M_4 \ldots M_K\) ensure only one of the amplifiers \(M_1, M_2 \ldots M_N\) acts as a common source amplifier at any time while the other signals are blocked. However, it should be noted that the parasitic capacitance \((C_{pa})\) seen at the common drain is increased as the number of transistors increases. As a result, the gain of TranSw 120A of Figure 5 will be decreased. Provided the gain and noise factor of each channel is within the specified requirements of the design, the number of channels can be increased.

In one embodiment, the receiver circuit 100 is designed for operation at 77GHz. The receiver circuit 100 should provide input matching with both receive antennas at all times (irrespective of whether the channel is selected or
The two inputs to the TranSw 120 could be connected to the receive antennas over a matching network. However, the input impedances of the TranSw 120 vary significantly as transistors $M_1$–$M_4$ are switched on/off.

Thus matching networks that match the receive antennas with the varied impedances are not practical. In order to overcome this issue, the input amplifiers are placed between the TranSw and the receive antennas to provide sufficient isolation between the inputs of the TranSw and the antennas. As a result, the matching networks are not affected by the varied input impedances of the TranSw. The output amplifier (OutAmp) drives the output current of the TranSw and adds more gain.

Amplifiers in low noise amplifiers suitable for a CMOS substrate are usually based on 3 common transconductance components: common gate (CG), common source (CS), and cascode amplifier. To achieve high gain, CS (Figure 7a) and cascode (Figure 7b) topologies are best suited for the transconductance components in the receiver circuit.

Although the cascode structure has the advantages of bandwidth improvement, input-output isolation, and high output impedance, it has more transistors, i.e. more noise sources than a CS transconductance component. Further, at 77 GHz, the gain provided by the CS transistor of the cascode structure is not high, as a result the noise contributed by the cascode transistor is significant. Accordingly, a CS topology is chosen as the transconductance component for the receiver circuit 100 of the embodiment.
A simplified schematic of the proposed receiver circuit with switching for two antennas is shown in Figure 6. The proposed receiver circuit consists of identical InAmpl 111 and InAmp2 112, TranSw 120, and OutAmp 130.

The input amplifiers 111,112 (InAmpl, InAmp2) each have three cascaded common source amplifiers with input matching. In the first stage of InAmpl 111 and InAmp2 112, the transistor (M5/M8) bias is set to optimal $NF_{min}$ current density, which is 0.2 mA/µm. The optimal finger width to maximize $f_{max}$ is chosen and equal to 1 µm. The number of fingers is selected to match the optimal noise impedance, which is 20 fingers. Thus, the transistor's total width is 20 µm with minimum channel length of 65 nm. Degeneration and gate matching inductors $L_S$ and $L_Q$ respectively are added to bring the input impedance of the CS transistor $M_1$ to match a 50 Ohm antenna. The input impedance can be expressed by

$$Z_{IN}=R_Q, R_S, \omega T L_S + j \left( \omega L_S + \omega L_G - \frac{\omega T}{\omega g_m} \right)$$  \hspace{1cm} (3)

where $R_Q$ and $R_S$ are gate and source resistance respectively, $\omega_T$ is the maximum unity current gain frequency, and $g_m$ is the transconductance of $M_5/M_8$.

As expressed in (3), the values of $L_S$ and $L_Q$ are chosen to cancel out the imaginary part of $Z_{in}$ while making the real part of $Z_{in}$ close to 50 Ohm. In this design $L_S$ and $L_Q$ are 70 pH and 80 pH and implemented by micro strip transmission lines, $T_{in}$ and $T_{in}$ respectively. At 77 GHz the capacitive
parasitics due to the input pad of the receiver circuit cannot be neglected, thus a shunt 60 pH \( L_p \) is added to cancel out this parasitic capacitance by a further micro strip transmission line \( T_p \). Furthermore, \( T_p \) acts as electrostatic discharge (ESD) path to protect the gate of \( M_5/M_8 \). The output drain of the first stage is placed very close to the gate of the second stage in a circuit layout of an embodiment. As a result, the 80 pH output load, creates an LC resonance circuit, which maximizes the gain and avoids complex inter-stage matching network. This design is adopted in every stage of the InAmp1/lnAmp2.

The second stage transistor \( M^+/M_8 \) (Figure 6) has the same size and bias point as the transistor \( M_5/M_8 \) of the first stage. In the second stage, because the isolation of the CS topology is low, the input impedance of the second stage will affect the input impedance of the first stage. Therefore, a 50 pH degeneration inductor is adopted in this stage to obtain better input matching which is provided by micro strip transmission line \( T_{s2} \). The output load of this stage is an 80pH inductor.

As shown in Figure 6, the last stage \( M_7/M_{10} \) has the same transistor size as well as bias point as the first two stages. All the matching/loading inductors used in the InAmp1/lnAmp2 111,112 are micro strip transmission lines. The characteristic impedance of all transmission lines is 80 Ohm except \( T_p \) because \( T_p \) is also the ESD path for the input gate of the receiver circuit, its width is made wider to reduce resistance, its characteristic impedance is 50 Ohm.
Consisting of three cascade amplifier, InAmpl/lnAmp2 111,112 provides sufficient isolation between receive antennas and the TranSw 120 thus the input matching are simplified and relaxed. Increasing the number of cascaded amplifiers would improve the isolation but would also decrease efficiency since the architecture would have greater power consumption and silicon area are traded due to the additional amplifiers. Reducing the number of cascaded amplifier makes the isolation lower thus making the input matching design more challenging.

As described above in relation to Figure 4, the TranSw 120 consists of transistors $M^->M^<$. The transistors' lengths are all 65 nm, the width of $M_1$ and $M_2$ are 20 $\mu$m, while the width of $M_3$ and $M_4$ are 16 $\mu$m.

The output amplifier 130 (OutAmp) drives the output of the TranSw consists of an inductive load (80pH) made of micro strip transmission lines, and 2 cascaded identical common source amplifiers. The two transistors $M_{11}$ and $M_{12}$ have length and width of 65nm and 20 pm. All the loads of the two amplifiers are 80pH made of micro strip transmission lines. The output drain of the first stage is placed very close to the gate of the second stage in layout. So the 80 pH output load, creates a LC resonance circuit, which maximizes the gain and avoids complex inter-stage matching network.

**Simulation results**

Figure 8 shows the simulated S parameter of the selected channel 801 of the receiver circuit 100. At 76.5 GHz, the selected channel shows 28.8 dB of forward gain 811, -59 dB
of reverse gain 812 and 4.8 dB of NF. The matching at 2 input ports and output port are -20 dB, -18 dB and -19 dB respectively.

Figure 9 shows the simulated S parameter of the blocked channel 901 of the receiver circuit 100. At 76.5 GHz, the blocked channel shows 8 dB of forward gain 911 (20 dB lower than forward gain 811 of the selected channel), -70 dB of reverse gain 812 and the leakage 913 from the input of selected channel to the input of blocked channel is -30 dB. The proposed receiver circuit, including bias circuit, consumes total 38.5 mA from 1.2 V supply.

It will be understood to persons skilled in the art of the invention that many modifications may be made without departing from the spirit and scope of the invention, in particular it will be apparent that certain features of embodiments of the invention can be employed to form further embodiments. For example, the embodiment is described as a receiver circuit comprising two or more antennas, however, the amplification and switching stages could be formed separately from the antennas as an amplification and switching circuit before being connected to the antennas.

It is to be understood that, if any prior art is referred to herein, such reference does not constitute an admission that the prior art forms a part of the common general knowledge in the art in any country.

In the claims which follow and in the preceding description of the invention, except where the context requires otherwise due to express language or necessary implication, the word "comprise" or variations such as "comprises" or "comprising" is used in an inclusive sense, i.e. to specify the presence of the stated features but not to preclude the
presence or addition of further features in various embodiments of the invention.
CLAIMS:

1. A receiver circuit comprising:
a first antenna;
a second antenna;
an input amplification stage comprising a first input amplifier circuit for amplifying a first signal received at the first antenna, and second input amplifier circuit for amplifying a second signal received at the second antenna;
a switching stage comprising first and second transconductance components connected respectively to the first and second input amplifier circuits and to a common output, and a switching mechanism arranged to selectively turn on and off the first and second transconductance components so that only one of the first and second transconductance components is in an on state at any time, the first and second transconductance components further amplifying the first and second signals respectively when in an on state; and
an output amplification stage connected to the common output of the switching stage and comprising an output amplifier circuit for further amplifying the first and second signals when they are outputted via the common output.

2. A receiver circuit as claimed in claim 1, wherein the first and second transconductance components comprise first and second transistors arranged in a common source topology.

3. A receiver circuit as claimed in claim 2, wherein the common output is formed by connecting the drains of the first and second transistors.
4. A receiver circuit as claimed in any one of claims 1 to 3, comprising a third antenna and wherein the input amplification stage a third input amplifier circuit for amplifying a third signal received at the third antenna, and wherein the switching stage comprises a third transconductance component connected to the third input amplifier circuit and the common output for further amplifying the third signal, and wherein the switching mechanism is further arranged to turn the third transconductance component on and off.

5. A receiver circuit as claimed in claim 3, wherein the third transconductance component comprise a third transistor arranged in a common source topology.

6. A receiver circuit as claimed in claim 2 or claim 3, wherein the switching mechanism comprises fourth and fifth transistors connected respectively to the first and second transistors and which when switched on respectively turn on the first and second transistors.

7. A receiver circuit as claimed in claim 5, wherein the switching mechanism comprises fourth, fifth and sixth transistors connected respectively to the first, second and third transistors and which when switched on respectively turn on the first, second and third transistors.

8. A receiver circuit as claimed in any one of claims 1 to 7, wherein the first and second input amplifier circuits each comprise a plurality of common source amplifiers.
9. A receiver circuit as claimed in claim 8, wherein the first and second input amplifiers each comprise at least one input matching component.

10. A receiver circuit as claimed in claim 8 or claim 9, wherein the first and second input amplifier circuits each comprise three common source amplifiers.

11. A receiver circuit as claimed in any one of claims 1 to 10, wherein the output amplifier circuit comprises a plurality of common source amplifiers.

12. A receiver circuit as claimed in claim 11, comprising two common source amplifiers.

13. An amplifying and switching circuit for a radar receiver, the circuit comprising:
   an input amplification stage comprising a first input for connection to a first antenna, a second input for connection to a second antenna, a first input amplifier circuit for amplifying a first signal received at the first input, and second input amplifier circuit for amplifying a second signal received at the second input;
   a switching stage comprising first and second transconductance components connected respectively to the first and second input amplifier circuits and to a common output, and a switching mechanism arranged to selectively turn on and off the first and second transistors so that only one of the first and second transconductance components is in an on state at any time, the first and second transconductance components further amplifying the first and second signals respectively when in an on state; and
an output amplification stage connected to the common output of the switching stage and comprising an output amplifier circuit for further amplifying the first and second signals when they are outputted via the common output.
Figure 3
Figure 4
Figure 5
Figure 6
Figure 7: (a) Common source (CS), (b) Cascode
INTERNATIONAL SEARCH REPORT

INTERNATIONAL SEARCH REPORT

PCT/AU2013/001483

A. CLASSIFICATION OF SUBJECT MATTER

H04B 1/16 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC.

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database consulted during the international search (name of data base and, where practicable, search terms used)

Searched databases EPODOC, WPI with IPC mark H04B 1/16/low and keywords: "second antenna", amplifier, switch, transconductance and other similar terms.

Searched databases TXTUS3, TXTUS4, TXTUS5, TXTUS6, TXTUS7, TXTUS8, TXTUS9, TXTUS10, TXTUS11, TXTUS12, TXTSG1 with keywords: "receiver circuit", "second antenna", amplifier, switch, transconductance, radar and other similar terms.

Searched database INSPEC with keywords: "receiver circuit", "second antenna", amplifier, switch and other similar terms.

Searched Google Patents, Google Scholar, Google Images and IEEEExplore with keywords: receiver, antennas, amplifier, switch, "common source", radar, transconductance, CMOS and other similar terms.

Searched Google Scholar with R. J. Evans, E. Skafidas, H. T. Duong, V. H. Le, J. Li and "The University of Melbourne".

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
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Date of the actual completion of the international search

24 February 2014

Date of mailing of the international search report

24 February 2014

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FormPCT/ISA/210 (fifth sheet) (July 2009)
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<td>US 7957333 B2 (WALKER et al.) 07 June 2011 See the whole document in particular, the abstract, fig. 3, col. 3 lines 7-19, col. 4 lines 50-62, col. 6 lines 15-32.</td>
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<td>A</td>
<td>US 7123898 B2 (BURGENER et al.) 17 October 2006 See the whole document.</td>
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End of Annex

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.