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(54) ELECTROMECHANICAL MICROMIRROR DEVICES AND METHODS OF MANUFACTURING THE SAME

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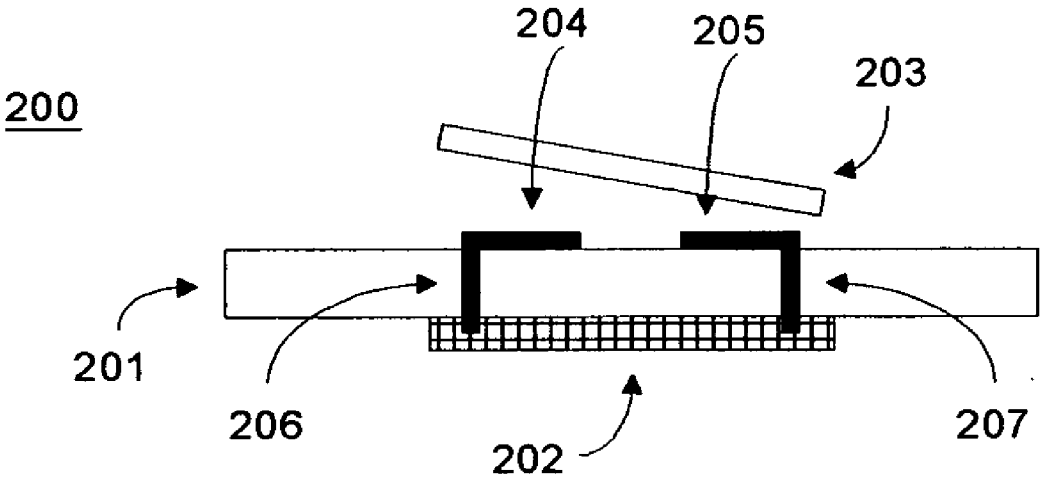
(57) **ABSTRACT**

An electromechanical micromirror device comprises a device substrate with a 1st surface and a 2nd surface, control circuitry disposed on said 1st surface, and a micromirror disposed on said 2nd surface. Arrays of such micromirror devices are also described and may be used as a spatial light modulators (SLMs). The arrays may be 1 dimensional (linear) or 2 dimensional. Methods of fabricating micromirror devices and arrays of such devices are also disclosed. Such methods generally involve providing a device substrate with a 1st surface and a 2nd surface, fabricating control circuitry on the 1st surface, and fabricating micromirror(s) on the 2nd surface.



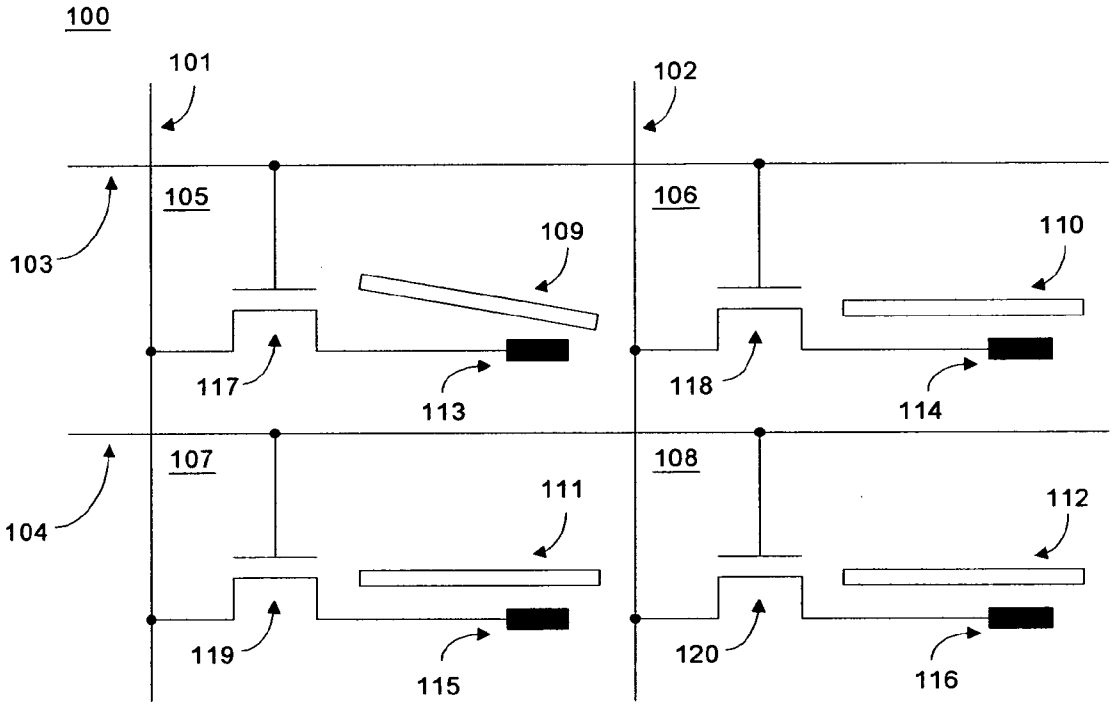

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Fig. 1

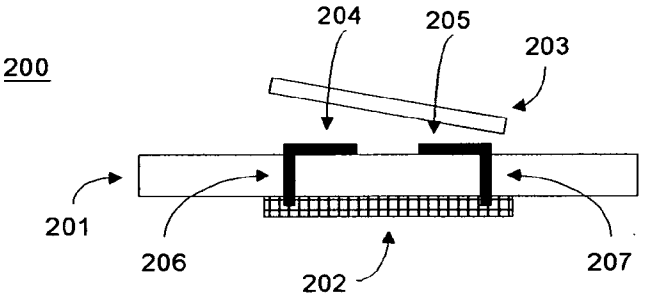
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Fig. 2

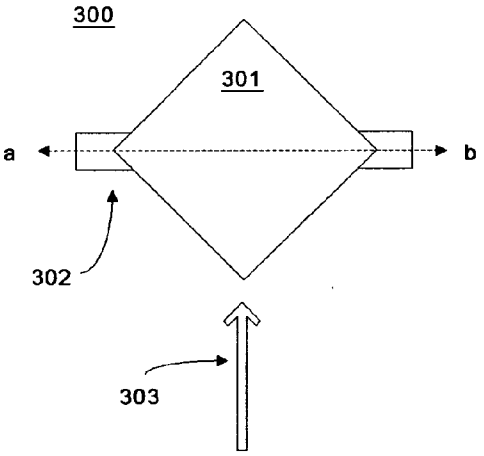


Fig. 3A

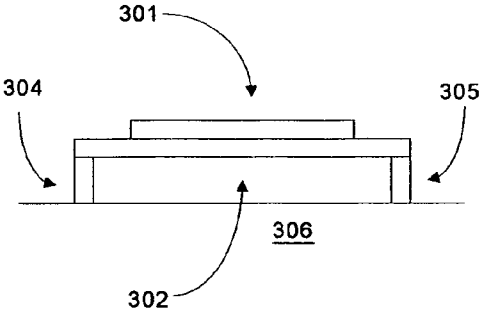


Fig. 3B

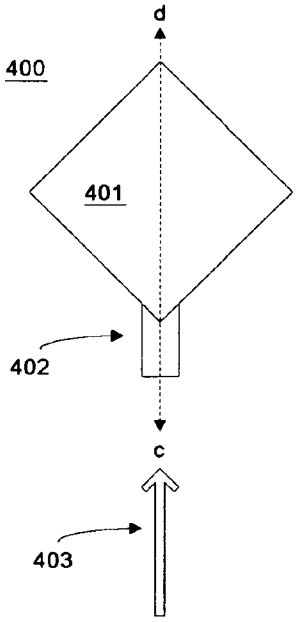


Fig. 4A

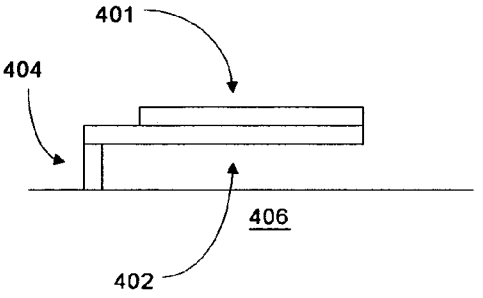


Fig. 4B

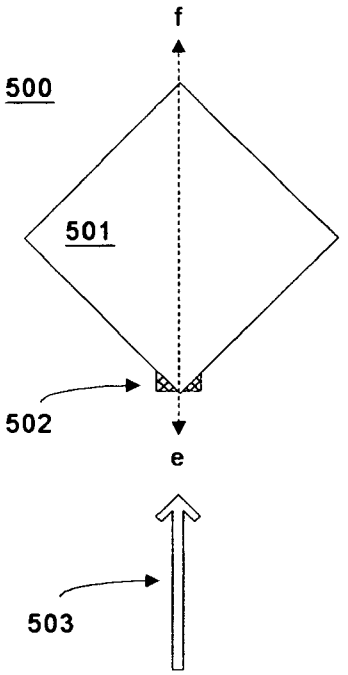


Fig. 5A

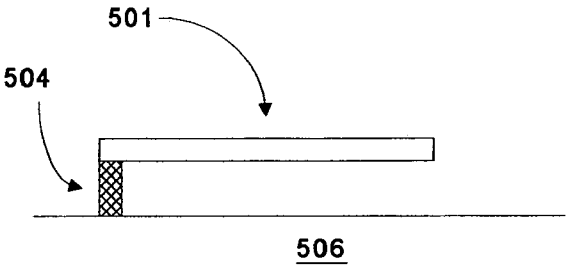


Fig. 5B

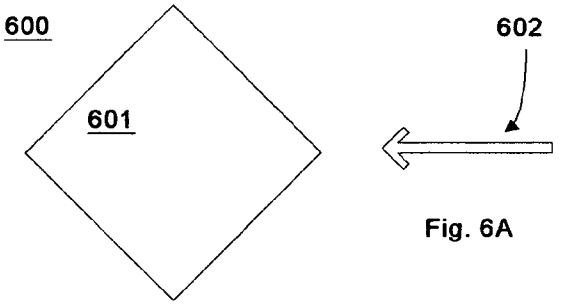


Fig. 6A

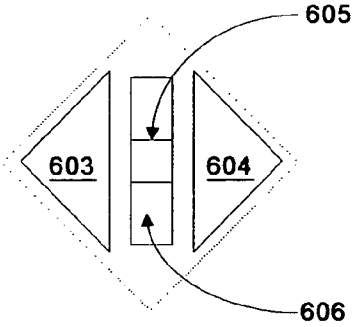


Fig. 6B

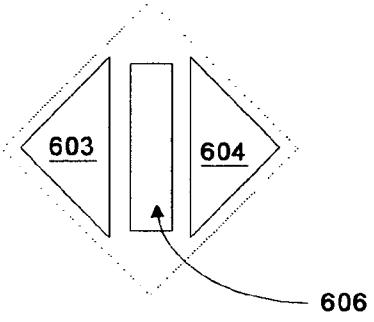


Fig. 6C

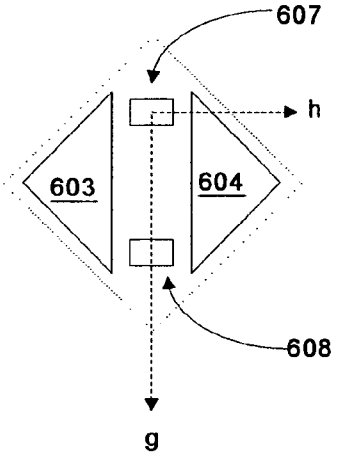


Fig. 6D

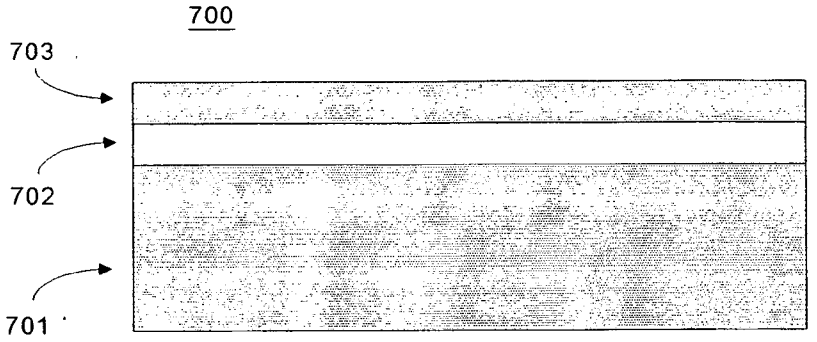


Fig. 7A

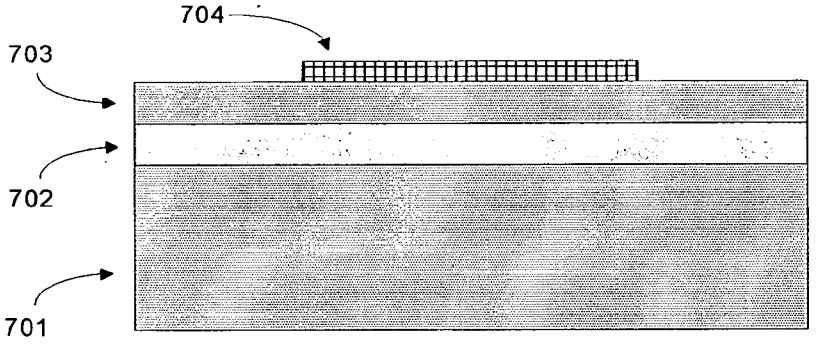


Fig. 7B

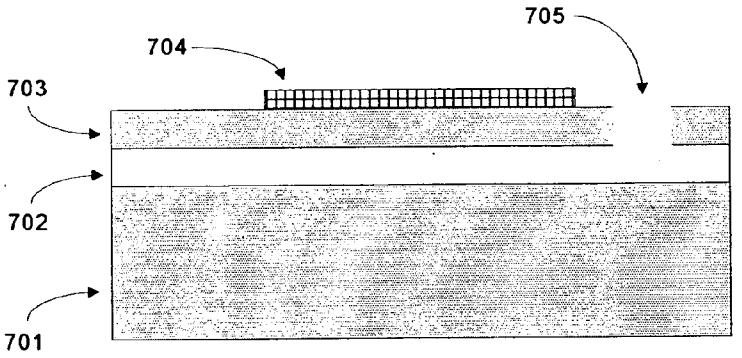


Fig. 7C

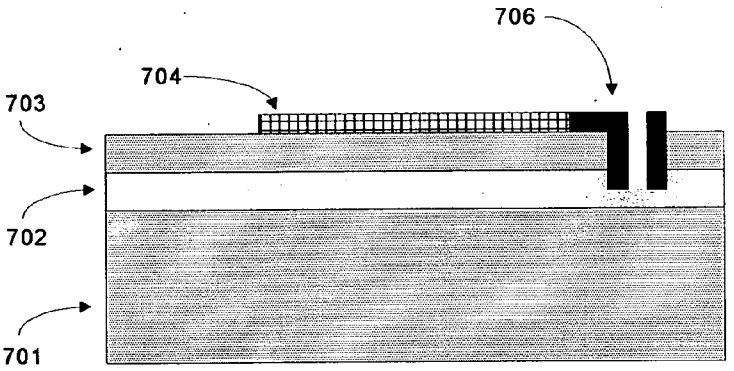


Fig. 7D

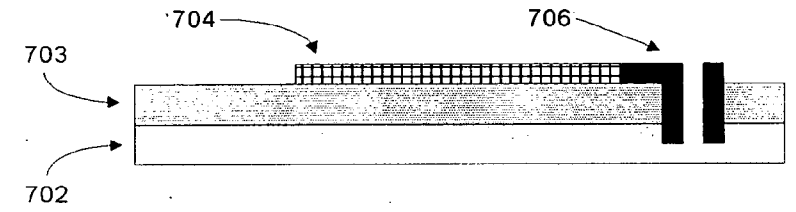


Fig. 8A

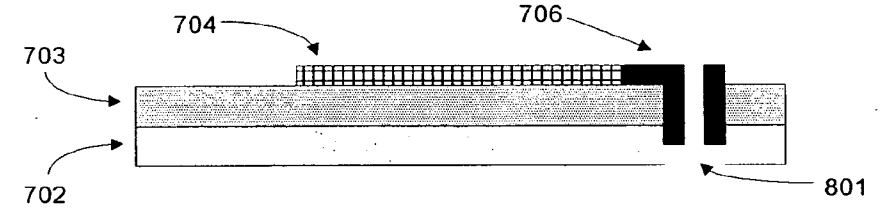


Fig. 8B

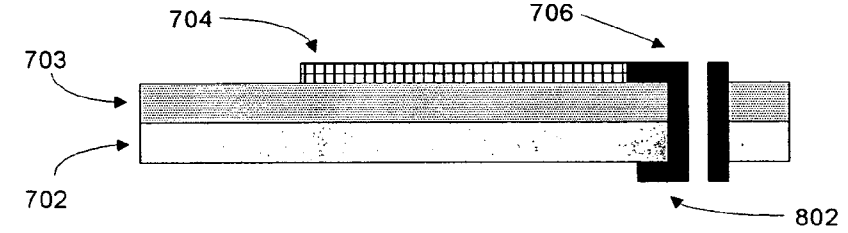
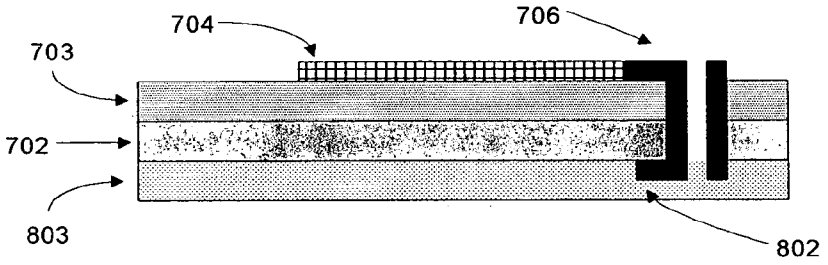


Fig. 8C



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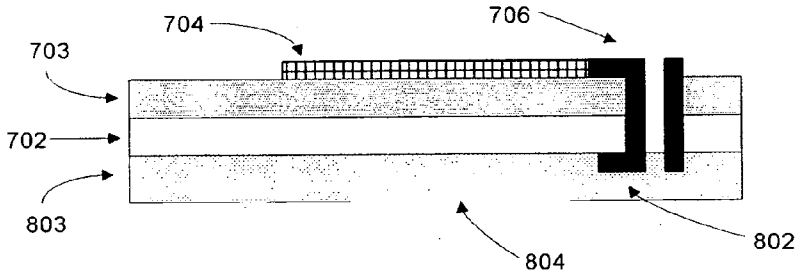
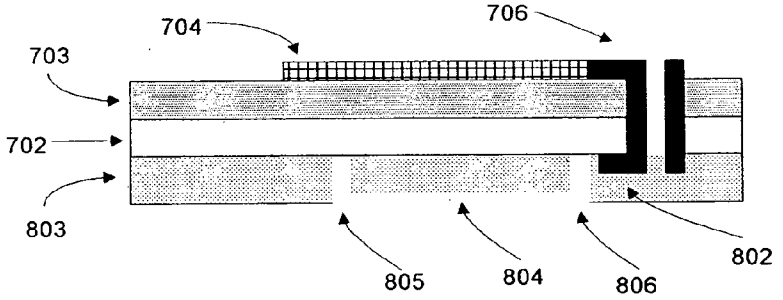


Fig. 8E



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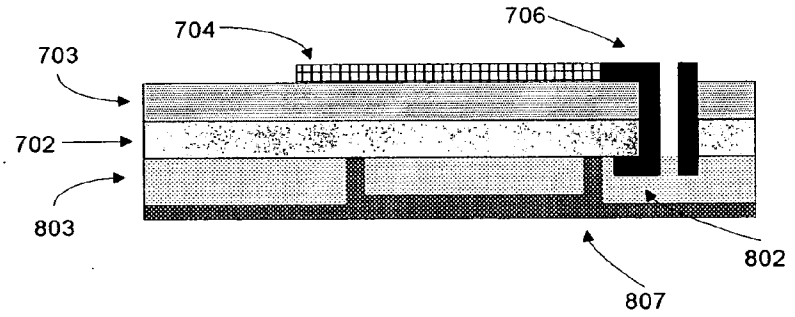

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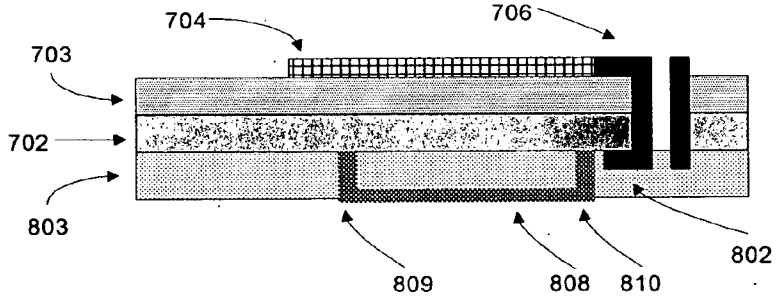

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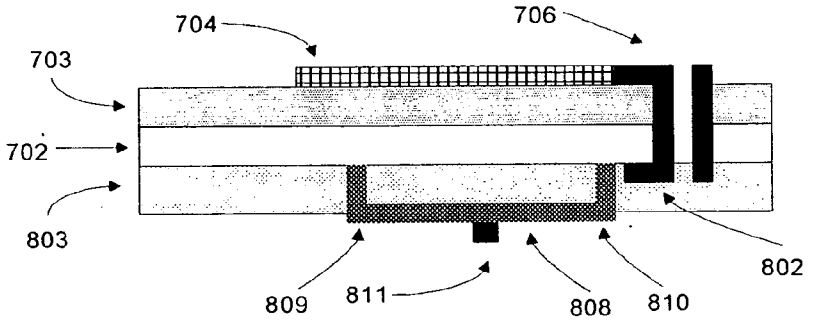


Fig. 8I

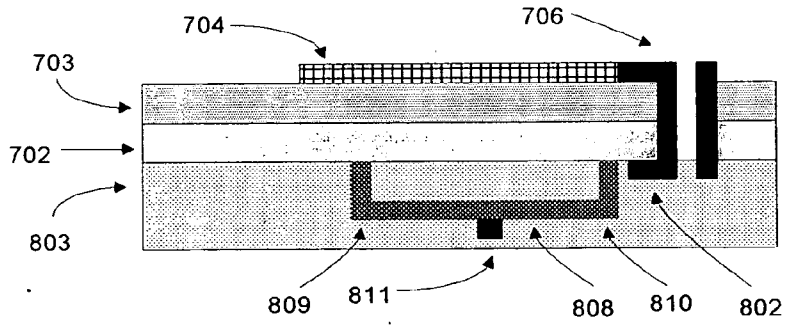
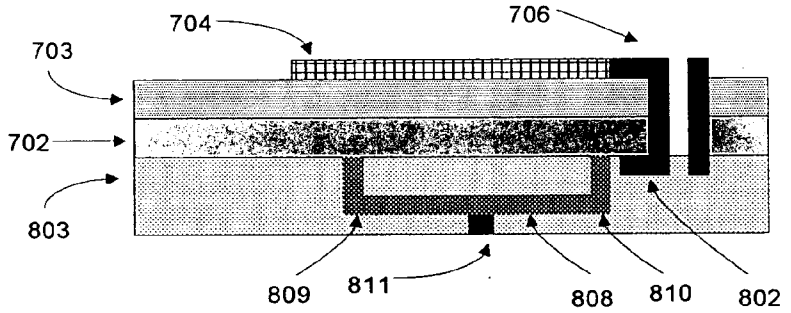


Fig. 8J



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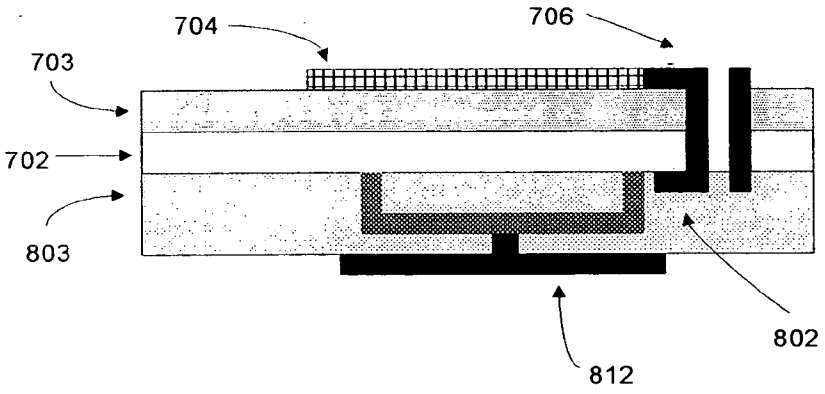

Fig. 8L

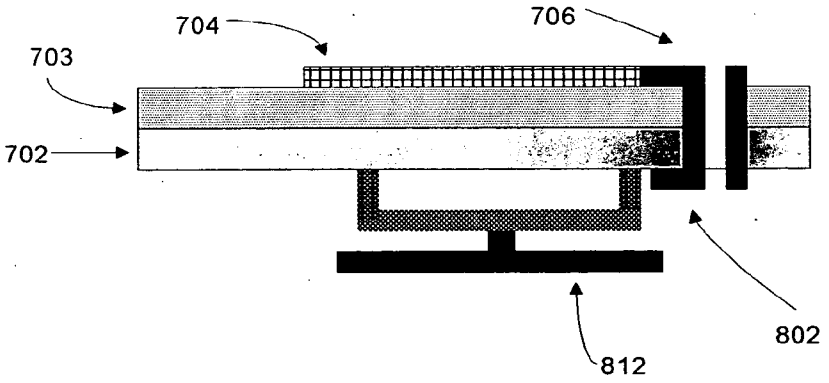

Fig. 8M

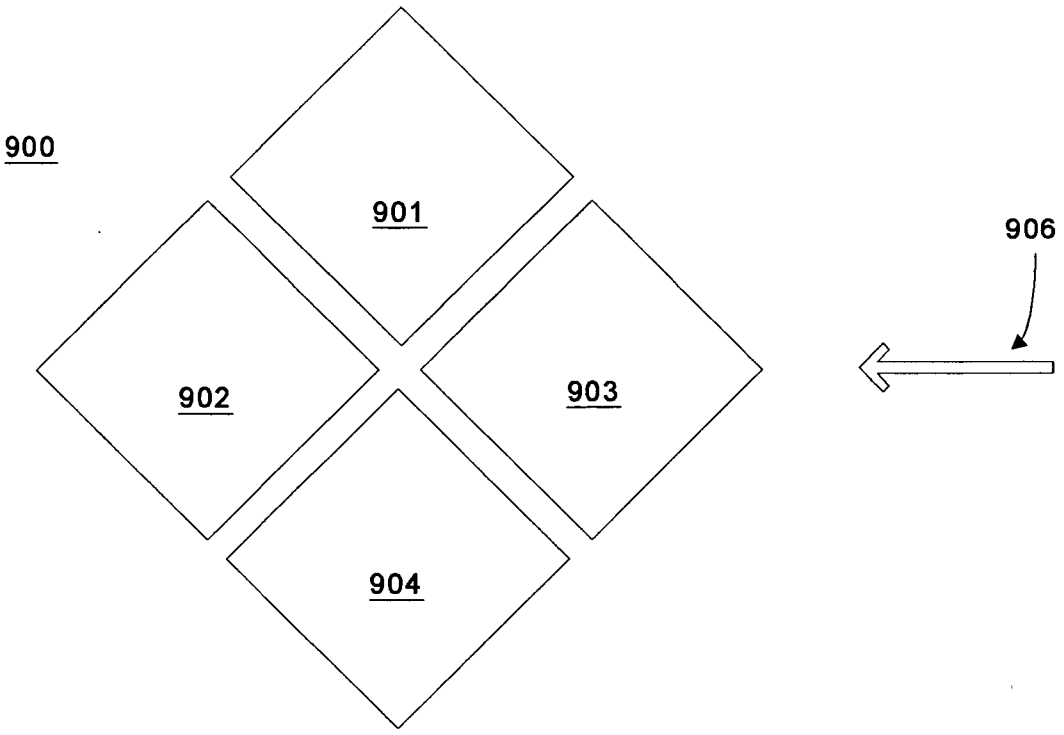

Fig. 9

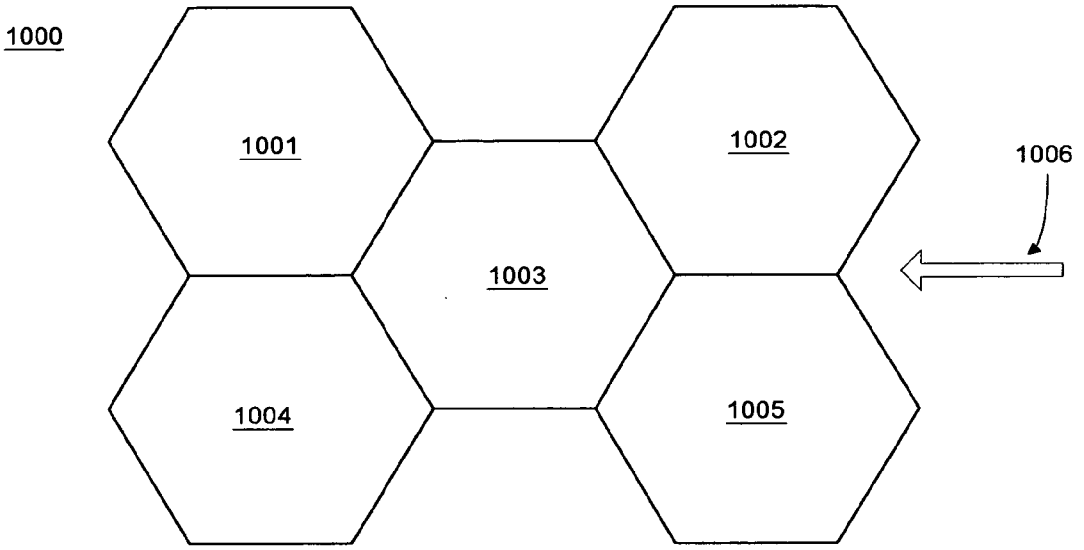

Fig. 10

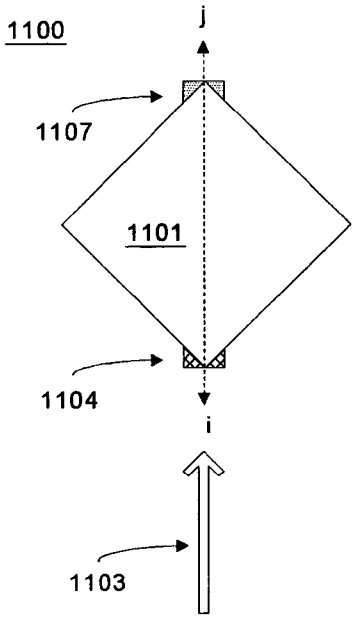

Fig. 11A

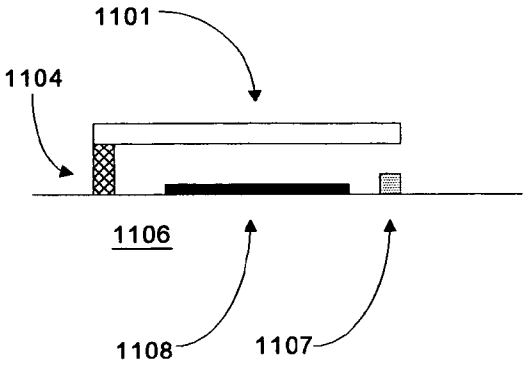

Fig. 11B

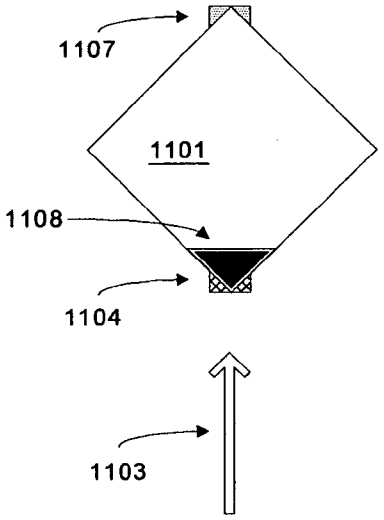

Fig. 11C

ELECTROMECHANICAL MICROMIRROR DEVICES AND METHODS OF MANUFACTURING THE SAME

TECHNICAL FIELD

[0001] This invention relates to electromechanical micromirror devices and methods of manufacturing the same. When fabricated in an array, such devices can be used as a spatial light modulator.

BACKGROUND ART

[0002] Electromechanical micromirror devices have drawn considerable interest because of their application as spatial light modulators (SLMs). A spatial light modulator requires an array of a relatively large number of such micromirror devices. In general, the number of devices required ranges from 60,000 to several million for each SLM. Despite significant advances that have been made in recent years, there is still a need for improvement in the performance and manufacturing yields of electromechanical micromirror devices.

[0003] An example of an early generation prior art device is disclosed in U.S. Pat. No. 4,592,628. U.S. Pat. No. 4,592,628 describes an array of light reflecting devices on a substrate. Each device comprises a hollow post and a deflectable polygonal mirror attached thereto. Each mirror acts as a deflectable cantilever beam. The mirrors are deflected by a beam of electrons from a cathode ray tube. As a result, the substrate does not contain any addressing circuits.

[0004] Another early generation device is disclosed in U.S. Pat. No. 4,229,732. In this case, addressing circuits using MOSFETs were fabricated on the surface of the substrate. Deflectable metallic mirrors were also fabricated on the surface of the substrate. Since the MOSFET circuits and mirrors could not overlap, the fill factor of the array was not as high as if the mirrors could cover the entire surface area.

[0005] As an alternative to mirrors that operate by deflection of cantilever beams, those that operate by torsion were proposed. U.S. Pat. No. 4,317,611 describes an early generation micromirror with a torsional structure. Note that this patent does not describe any methods or architectures for placing addressing circuits on the substrate.

[0006] A 1st generation Texas Instruments, Inc. (TI) device is described in U.S. Pat. No. 4,662,746. A micromirror is suspended by 1 or 2 hinges. If suspended by 1 hinge, the micromirror deflects like a cantilever beam. If suspended by 2 hinges, the micromirror deflects like a torsion beam. Addressing electrodes are located below the micromirrors and addressing circuits are located at the same level in the substrate as the addressing electrodes.

[0007] An improved 1st generation TI device is described in U.S. Pat. No. 5,061,049. In this patent, each mirror is provided with 2 addressing electrodes and 2 landing electrodes. The landing electrodes soften the landing of the mirrors and are also used to reset the mirrors by a suitable voltage sequence. The use of these landing electrodes allows the mirrors to function as a bistable device.

[0008] A 2nd generation TI device is described in U.S. Pat. No. 5,583,688. A 2nd generation TI device is one in which the torsion hinge is at a different level than the reflective mirror. As described more fully in U.S. Pat. No. 5,583,688, the mirror is supported by a mirror support post, which is attached to the torsion hinge by a yoke. In U.S. Pat. No. 5,583,688, the mirrors are actuated by electrostatic forces between the mirror and address electrodes.

[0009] An improved 2nd generation TI device is described in U.S. Pat. No. 5,535,047. In this case, the mirrors are actuated by 2 sets of electrostatic forces. As a result the forces are greater and actuation performance is improved. The 1st force is between the mirror and the elevated address electrode. The 2nd force is between the yoke and substrate-level address electrode.

[0010] Micromirrors that are described in U.S. Pat. No. 4,662,746, U.S. Pat. No. 5,061,049, U.S. Pat. No. 5,583,688, and U.S. Pat. No. 5,535,047 are fabricated on top of CMOS circuits. There may be manufacturing problems associated with the fabrication of micromirrors on top of CMOS circuits. This issue is discussed in U.S. Pat. No. 5,216,537. In this patent, it is discussed that the surface of the CMOS chip has certain manufacturing artifacts, namely aluminum hillocks, pinholes, nonplanar surfaces, and steep sidewalls in the protective oxide at edges of aluminum leads. In response to these problems, U.S. Pat. No. 5,216,537 discloses an improved architecture in which an air gap is provided between the top surface of the CMOS chip and the mirror addressing electrodes. A further advantage of this approach is that because of the low dielectric constant of air, parasitic coupling between the CMOS and the micromirror is reduced.

[0011] The placement of CMOS circuits directly under the micromirrors is also responsible for problems of photosensitivity. As discussed in U.S. Pat. No. 6,344,672, it was found that the CMOS memory cells are unstable in a high-intensity light environment. The patent provided an active collector region in which photogenerated carriers could recombine before reaching the addressing electrode.

[0012] Reflectivity, Inc. (Sunnyvale, Calif.) is also known to be developing micromirror devices. As disclosed in U.S. Pat. No. 5,835,256, the aforementioned problems associated with placing CMOS and micromirrors on the same substrate are solved by placing the micromirrors and CMOS on different substrates. In other words, a hinge and a micromirror are fabricated on an optically transparent substrate, such that the optically reflective surface of the micromirror is proximate the optically transparent substrate. Addressing circuits including mirror addressing electrodes are fabricated on a 2nd substrate (typically silicon) and the 2 substrates are bonded together with a predetermined gap between the micromirror and the addressing electrodes.

[0013] In order to reduce scattering by non-lanar surfaces and increase the fill factor, it was necessary to provide a light shield on the optically transparent substrate in the hinge areas. In an improved device, the hinges are placed on the side of the mirror opposite to the side that is proximate the optically transparent substrate.

[0014] However, another difficulty with the architecture of U.S. Pat. No. 5,835,256 is that the gap between the mirror and mirror addressing electrodes is difficult to control. Since the actuation force is superlinearly dependent on this gap, it is imperative to achieve uniform gap over the entire array to

obtain uniform performance characteristics. As discussed in U.S. Ser. No. 2003/0,134,449, 2nd and higher order adjustments in the gap may be needed in the manufacturing process.

[0015] U.S. Pat. No. 6,538,800 also discusses the use of amorphous silicon as a sacrificial layer. It is shown that amorphous silicon can be deposited for this purpose by LPCVD in a quartz tube of a Tylan furnace. It is also shown that a xenon difluoride etch process can be used to etch amorphous silicon with a selectivity of 100 to 1. Therefore, amorphous silicon can be used successfully as a sacrificial layer in addition to photoresists, silicon oxide, silicon nitride, and silicon oxynitride.

SUMMARY OF THE INVENTION

[0016] The present invention provides micromirror devices, arrays of micromirror devices, and fabrication methods for said devices and arrays that overcome some of the limitations of the prior art. According to the present invention, an electromechanical micromirror device comprises a device substrate with a 1st surface and a 2nd surface, control circuitry disposed on said 1st surface, and a micromirror disposed on said 2nd surface. The present invention also relates to arrays of such micromirror devices. Such arrays may be used as a spatial light modulators (SLMs). The arrays may be 1-dimensional (linear) or 2-dimensional. According to the present invention, methods of fabricating micromirror devices and arrays of such devices generally involve providing a device substrate with a 1st surface and a 2nd surface, fabricating control circuitry on the 1st surface, and fabricating micromirror(s) on the 2nd surface. In a preferred embodiment, control circuits are fabricated using CMOS technology. In another preferred embodiment, the control circuits on the 1st surface are protected by a protective layer during the fabrication of micromirrors on the 2nd surface. In yet another preferred embodiment, the device substrate is a silicon-on-insulator (SOI) substrate.

[0017] A 1st advantage of the present invention is that it provides improved dielectric isolation between the control circuit and the micromirror. A 2nd advantage of the present invention is that provides improved optical isolation of the control circuit area. This is particularly advantageous when the micromirror array is used as a spatial light modulator (SLM) and the 1st surface (the micromirror side) is exposed to high intensity radiation. A 3rd advantage of the present invention is that it provides improved manufacturing yields because the control circuit manufacturing processes and micromirror manufacturing processes can be substantially isolated from each other. In other words, manufacturing artifacts arising from the control circuit process will not damage the micromirror because the micromirror is not built on top of the control circuit. These and other advantages of the present invention will become apparent from the detailed description and the claims below.

BRIEF DESCRIPTION OF THE FIGURES

[0018] **FIG. 1** is a schematic diagram of a 4-pixel array of micromirror devices, comprising control circuits, addressing electrodes, and micromirrors.

[0019] **FIG. 2** is a schematic cross sectional view of a micromirror device in accordance with the present invention.

[0020] **FIG. 3A** is a schematic plan view of a micromirror device in accordance with a 1st embodiment of the present invention.

[0021] **FIG. 3B** is a schematic cross sectional view along line a-b of **FIG. 3A**.

[0022] **FIG. 4A** is a schematic plan view of a micromirror device in accordance with a 2nd embodiment of the present invention.

[0023] **FIG. 4B** is a schematic cross sectional view along line c-d of **FIG. 4A**.

[0024] **FIG. 5A** is a schematic plan view of a micromirror device in accordance with a 3rd embodiment of the present invention.

[0025] **FIG. 5B** is a schematic cross sectional view along line e-f of **FIG. 5A**.

[0026] **FIGS. 6A through 6D** are schematic plan views of a micromirror device according to a 4th embodiment of the present invention, at varying levels of elevation.

[0027] **FIGS. 7A through 7D** are cross sectional views illustrating the fabrication steps on a 1st device substrate surface, in accordance with a 4th embodiment of the present invention.

[0028] **FIGS. 8A through 8M** are cross sectional views illustrating the fabrication steps on a 2nd device substrate surface, in accordance with a 4th embodiment of the present invention.

[0029] **FIG. 9** is a schematic plan view illustrating a micromirror array of rectangular micromirrors according to a 5th embodiment of the present invention.

[0030] **FIG. 10** is a schematic plan view illustrating an array of hexagonal micromirrors in accordance with a 6th embodiment of the present invention.

[0031] **FIG. 11A** is a schematic plan view of a micromirror device in accordance with a 7th embodiment of the present invention.

[0032] **FIG. 11B** is a schematic cross sectional view along line i-i of **FIG. 11A**.

[0033] **FIG. 11C** is a schematic plan view of a micromirror device in accordance with an 8th embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0034] The present invention relates to electromechanical micromirror devices and arrays of such devices. Shown schematically in **FIG. 1** is an array **100** comprising vertical data lines (**101** and **102**) and horizontal addressing lines (**103** and **104**), with each intersection of these data and addressing lines forming an electromechanical micromirror device (**105**, **106**, **107**, and **108**). Each micromirror device comprises a micromirror (**109**, **110**, **111**, and **112**), an addressing electrode (**113**, **114**, **115**, and **116**), and an NMOS transistor (**117**, **118**, **119**, and **120**). Micromirror **109** is shown to be in a deflected state while the other micromirrors are in their undeflected states. A possible scheme for addressing the micromirrors is as follows: The micromirrors (**109**, **110**, **111**, and **112**) are electrically connected to ground. The deflection

of a micromirror is determined by the bias voltage between the micromirror and its addressing electrode. The desired bias voltage is set by the voltages on the vertical data lines (**101** and **102**). The NMOS transistors are turned on by sending a low-high-low pulse on the addressing lines (**103** and **104**), which results in the bias voltages being stored between the micromirrors and addressing electrodes.

[**0035**] While array **100** (**FIG. 1**) has been shown to consist of 4 micromirror devices, an array may typically consist of greater than 60,000 micromirror devices and may be used as a spatial light modulator (SLM). Furthermore, while **FIG. 1** shows a plurality of micromirror devices disposed in a 2-dimensional array, 1-dimensional (linear) array are also possible.

[**0036**] The circuitry as shown in **FIG. 1** comprises the following:

[**0037**] 1) micromirrors;

[**0038**] 2) micromirror addressing electrodes; and

[**0039**] 3) control circuitry.

[**0040**] In the particular case of **FIG. 1**, control circuitry consists of the vertical data lines (**101** and **102**), horizontal addressing lines (**103** and **104**), NMOS transistors (**117**, **118**, **119**, and **120**), and electrical connections among them. In general, control circuitry is understood to mean any circuitry that is provided to control the application of bias voltages between a micromirror and its addressing electrode. As shown in **FIG. 1**, the control circuitry comprised NMOS transistors. However, it should be understood that the control circuitry could comprise other types of circuits, including CMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits.

[**0041**] Some of the important concepts of the present invention are illustrated schematically in **FIG. 2**. A device substrate **201** has a bottom surface on which control circuitry **202** is fabricated. Micromirror **203** and addressing electrodes **204** and **205** are fabricated on the top surface of substrate **201**. For simplicity, support structures for supporting micromirror **203** are not shown. Electrical connections between the addressing electrodes (**203** and **204**) and control circuitry **202** are provided by electrical routing lines **206** and **207**. The electrical routing lines **206** and **207** may be in the form of vias in the device substrate **201** with metallization in these vias. The device substrate may be selected from among the following: silicon-on-insulator (SOI), silicon, polycrystalline silicon, glass, plastic, ceramic, germanium, SiGe, SiC, sapphire, quartz, GaAs, and InP. In general, the choice of device substrate should be consistent with the choice of control circuit technology. For example, a silicon-on-insulator substrate may be suitable for CMOS circuits, and a glass substrate may be suitable for amorphous silicon thin film transistor circuits.

[**0042**] As discussed with reference to **FIG. 1**, a micromirror device comprises a control circuitry, a micromirror, and addressing electrodes. **FIG. 3A** is a schematic plan view of a portion of a micromirror device **300** in accordance with a 1st embodiment of the present invention. Micromirror **301** is shown with its reflective side facing towards the reader. The reflective side of micromirror **301** is substantially planar, with neither recessions nor protrusions. Micromirror **301** is supported by a torsion hinge **302**. In the case that micromirror portion **300** is disposed in an array for a spatial light modulator (SLM), arrow **303** indicates the projection of the incident light propagation direction on the device substrate plane. Note that micromirror **301** has 4 edges and no edge is perpendicular to arrow **303**. **FIG. 3B** is a schematic cross sectional view along line a-b through torsion hinge **302**. Micromirror **301** and torsion hinge **302** are supported by support structures **304** and **305**, which are disposed on device substrate **306**. Since the micromirror deflects by torsion, the axis of rotation of the micromirror is approximately perpendicular to arrow **303**.

[**0043**] **FIG. 4A** is a schematic plan view of a portion of a micromirror device **400** in accordance with a 2nd embodiment of the present invention. Micromirror **401** is shown with its reflective side facing towards the reader. The reflective side of micromirror **401** is substantially planar, with neither recessions nor protrusions. Micromirror **401** is supported by a beam **402**. In the case that micromirror device **400** is disposed in an array for a spatial light modulator (SLM), arrow **403** indicates the projection of the incident light propagation direction on the device substrate plane. Note that micromirror **401** has 4 edges and no edge is perpendicular to arrow **403**. **FIG. 4B** is a schematic cross sectional view along line c-d through beam **402**. Beam **402** is supported by support structure **404**, which is disposed on device substrate **406**. In contrast to micromirror **301** (**FIGS. 3A and 3B**), the axis of rotation of micromirror **401** is approximately parallel to arrow **403**.

[**0044**] **FIG. 5A** is a schematic plan view of a portion of a micromirror device **500** in accordance with a 3rd embodiment of the present invention. Micromirror **501** is shown with its reflective side facing towards the reader. The reflective side of micromirror **501** is substantially planar, with neither recessions nor protrusions. In the case that micromirror device **500** is disposed in an array for a spatial light modulator (SLM), arrow **503** indicates the projection of the incident light propagation direction on the device substrate plane. **FIG. 5B** is a schematic cross sectional view along line e-f. Micromirror **501** is supported by a support structure **504**, which is disposed on device substrate **506**. The axis of rotation of micromirror **501** is approximately parallel to arrow **503**.

[**0045**] An important difference between between micromirror device **400** (**FIGS. 4A and 4B**) and micromirror device **500** (**FIGS. 5A and 5B**) is that in device **400**, there is a beam **402** which supports the micromirror **401** on the support structure **404**, whereas in device **500**, the micromirror is positioned directly on support structure **504**. Therefore, in **FIG. 5A**, the top side **502** of support structure **504** is visible in the plan view.

[**0046**] **FIGS. 6A through 6D** are schematic plan views of a micromirror device **600** accoding to a 4th embodiment of the present invention, at varying levels of elevation. **FIG. 6A** shows the reflective side (top side) of a micromirror **601**. In the case that micromirror device **600** is disposed in an array for a spatial light modulator (SLM), arrow **602** indicates the projection of the incident light propagation vector

on the device substrate plane. Arrow **602** is not perpendicular to any of the 4 sides of micromirror **601**. Arrow **602** is shown to be approximately 45 degrees from the leading edges of micromirror **601**. The reflective side of micromirror **601** is is substantially flat, with neither recesses nor protrusions. As a result, there are no diffraction effects that would be caused by recesses or protrusions in the micromirror.

[**0047**] **FIG. 6B** shows a plan view that is analogous to **FIG. 6A** except that micromirror **601** has been removed. Addressing electrodes **603** and **604**, micromirror support structure **605**, and torsion hinge **606** are visible. Torsion hinge **606** supports micromirror support structure **605**. Addressing electrodes **603** and **604** are electrically connected to control circuitry which is not shown. Micromirror **601** is actuated by electrostatic forces between it and one or both of the addressing electrodes **603** and **604**. **FIG. 6C** shows the result of removing the mirror support structure **605**.

[**0048**] **FIG. 6D** shows the result of removing torsion hinge **606**. Torsion hinge support structures **607** and **608** are shown. **FIGS. 7A through 7D** and **8**A through **8**M show a fabrication sequence of a micromirror device using a cross sectional view along the line g-h. In many cases, the micromirror device would be fabricated in an array for use as a spatial light modulator. Therefore, although **FIGS. 7A through 7D** and **8**A through **8**M illustrate the fabrication of a single micromirror device, it should be understood that the teachings can be extended to the fabrication of an array of micromirror devices.

[**0049**] **FIGS. 7A through 7D** illustrate a fabrication sequence on the control circuitry side. **FIG. 7A** shows a silicon-on-insulator (SOI) substrate **700** comprising an epitaxial top silicon layer **703** with a thickness typically ranging from 50 nm to 600 nm, an intermediate insulator layer **702** with a thickness typically ranging from 50 nm to 2 μm, and a bottom silicon layer **701** with a thickness of around 775 μm. One of the advantages of SOI over silicon substrates is the improved dielectric isolation. In the case of the present invention, the SOI substrate is used to improve the dielectric isolation of the control circuitry and micromirror portion.

[**0050**] **FIG. 7B** shows the formation of control circuitry **704** on epitaxial layer **703** of the SOI substrate **700**. In general, any integrated circuit technology can be considered for fabricating the control circuitry. For example, CMOS circuitry may be used. However, for applications requiring high frequency or high voltages, BiCMOS or DMOS circuitry may be used.

[**0051**] **FIG. 7C** shows the step of forming a trench **705** through the top epitaxial silicon layer **703** and insulator layer **702**, using standard patterning and an anisotropic etch. The anisotropic etch is stopped before the trench **705** reaches the bottom silicon layer **701**. This is followed by a metal deposition and patterning step (**FIG. 7D**) which forms an electrical connection **706** between the control circuitry and the trench. It should be understood that this metal could be any metal that is used in semiconductor fabrication, such as Al alloy, and methods of metal deposition include sputtering, thermal evaporation, and CVD.

[**0052**] At this point the process steps on the control circuitry side are complete. It may be preferable to form a protective layer on the control circuitry side. **FIGS. 8A through 8M** illustrate a fabrication sequence on the micromirror side. The control circuitry side is mounted on a carrier to securely hold the substrate for the subsequent step (**FIG. 8A**) of backgrinding and chemical mechanical polishing (CMP) of the back silicon layer **701** to expose the intermediate insulator layer **702**.

[**0053**] As shown in **FIG. 8B**, insulator layer **702** is pattered to form a trench **801**, thereby completing the via that had been started in the step of **FIG. 7C**. Another metallization (deposition and patterning) step (**FIG. 8C**) forms addressing electrodes **802** that are electrically connected, through via **801**, to control circuitry **704**.

[**0054**] After the formation of the addressing electrodes **802**, the torsion hinge and its support structures are formed. An embodiment of this process is illustrated in **FIGS. 8D through 8H**. An amorphous silicon sacrificial layer **803** is deposited by LPCVD (**FIG. 8D**). Other suitable methods of depositing amorphous silicon are PECVD, catalytic CVD (also known as hot wire CVD), and sputtering. As discussed in the Background Art section, xenon difluoride can be used to etch amorphous silicon with a selectivity of 100 to 1. Other possible sacrificial layers are photoresists, silicon oxide, silicon nitride, and silicon oxynitride. As shown in **FIG. 8E**, a photolithographic patterning and anisotropic etching step is carried out to form a recess **804** where the torsion hinge will be formed. Then, another photolithographic patterning and anisotropic etching step (**FIG. 8F**) is carried out to form holes **805** and **806** where the torsion hinge support structures will be formed. The holes **805** and **806** for the torsion hinge support structures reach the intermediate insulator layer.

[**0055**] As shown in **FIG. 8G**, a layer **807** of structural material is deposited. For example, the structural material may be an Al alloy comprising 0.2% Ti, 1% Si, and the remainder Al. A preferred method of depositing this Al alloy is sputter deposition. A metal is chosen for the structural material because the micromirror is typically held at ground potential. As shown in **FIG. 8H**, structural material layer **807** is patterned to form a torsion hinge **808** and torsion hinge support structures **809** and **810**. Torsion hinge **808** and torsion hinge support structures **809** and **810** are at least partially embedded in sacrificial layer **803**.

[**0056**] A micromirror support structure is placed between the torsion beam and the micromirror. As shown in **FIG. 81**, a metal layer is deposited and then patterned to provide a micromirror support structure **811** on torsion beam **808**. The metal may be an Al alloy comprising 0.2% Ti, 1% Si, and the remainder Al. A preferred method of depositing this Al alloy is sputter deposition. Another layer of sacrificial amorphous silicon is deposited (**FIG. 8J**) such that the micromirror support structure **811** is fully covered by sacrificial layer **803**. A chemical mechanical polishing (CMP) process is carried out to planarize the surface such that the following requirements are satisfied:

[**0057**] 1) the top of the micromirror support structure **811** is exposed and planar;

[**0058**] 2) the sacrificial layer **803** is planar; and

[**0059**] 3) the top of the micromirror support structure **811** and the top of the sacrificial layer **803** are at the same level.

[0060] In this description, top is understood to mean bottom on the drawing page. The result of the planarization step is shown schematically in **FIG. 8K**.

[0061] A metallic layer is deposited and patterned to form a micromirror **812** as shown in **FIG. 8L**. The metal may be an Al alloy comprising 0.2% Ti, 1% Si, and the remainder Al. A preferred method of depositing this Al alloy is sputter deposition. The micromirror **812** is connected to the micromirror support structure **811**. A xenon difluoride etch is carried out to remove the amorphous silicon sacrificial layer (**FIG. 8M**).

[0062] In the foregoing discussion the preferred micromirror comprised a metallic coating. However, it is also possible to construct a micromirror out of multiple alternating layers of higher refractive index and lower refractive index dielectrics. This may be accomplished by using silicon oxide and silicon nitride. Therefore, if an Al mirror has a reflectivity of 92%, the reflectivity can be increased to over 95% by first depositing 68 nm of silicon nitride (n=2.0) and then depositing 96 nm of silicon dioxide (n=1.46).

[0063] In the foregoing discussion of **FIGS. 8G** to **8M**, all of the structural members (torsion hinge, torsion hinge support structures, micromirror, micromirror support structures) were metallic. Alternatively, it is possible to use a dielectric (e.g. hardened photoresist, silicon oxide, silicon nitride, silicon oxynitride) that has been covered with a metallic sheath as a structural member, as described more fully in U.S. Pat. No. 5631782.

[0064] Typically, micromirror devices are incorporated into an array. **FIG. 9** shows a 2-dimensional array **900** of rectangular micromirrors (**901**, **902**, **903**, and **904**), according to a 5th embodiment of the present invention. Arrow **906** indicates the projection of the incident light propagation vector on the mirror plane (device substrate plane). The reflective side of the micromirror has no edges that are perpendicular to arrow **906**. This is a configuration that reduces diffraction into the acceptance cone of the optical system. Another possible shape for a micromirror is a hexagon, shown being disposed in an array **1000** in **FIG. 10**, according to a 6th embodiment of the present invention. There are micromirrors **1001**, **1002**, **1003**,**1004**, and **1005**. Arrow **1006** indicates the projection of the incident light propagation vector on the mirror plane (device substrate plane). The reflective side of the micromirrors has no edges that are perpendicular to arrow **1006**.

[0065] A 7th embodiment of the present invention is explained with reference to **FIGS. 11A and 11B**. **FIG. 11A** is a schematic plane view of a micromirror device **1100**, comprising a micromirror **1101** and a micromirror support structure **1104**. Arrow **1103** indicates the projection of the incident light propagation vector on the micromirror plane (device substrate plane). The reflective side of the micromirror has no edges that are perpendicular to arrow **1103**. The reflective side of micromirror **1101** is substantially planar, with neither recessions nor protrusions. **FIG. 11B** is a schematic cross sectional view along line i-j of **FIG. 11A**. An addressing electrode **1108** is located under micromirror **1101** and on top of device substrate **1106**. Furthermore, a stopper **1107** has been provided. The purpose of stopper **1107** is to prevent micromirror **1101** from contacting addressing electrode **1108** under deflection. This may cause an electrical short. Instead, micromirror **1101** contacts stopper **1107**. In cases where a micromirror deflects in 2 directions from its undeflected state, it is possible to provide 2 stoppers with 1 stopper for each direction of deflection.

[0066] **FIG. 11C** illustrates a modification to micromirror device **1100** in accordance with an 8th embodiment of the present invention. **FIG. 11C** is a plan view of a micromirror device **1100** comprising a micromirror **1101**, a support structure **1104**, and a stopper **1107**. In its undeflected state, the reflective side of micromirror **1101** has no edges that are perpendicular to arrow **1103**. When the micromirror **1101** is actuated, the region **1108** of micromirror **1101** that is adjacent to support structure **1104** gets deflected. Therefore, an edge that is perpendicular to arrow **1103** may appear in region **1108**. In order to reduce diffraction effects from this edge, it is possible to coat region **1108** with a light absorbing material. A preferred light absorbing material is a black dye.

1. An electromechanical micromirror device, comprising:

a single substrate with a 1st surface and a 2nd surface;

a control circuitry disposed on said 1st surface of said single substrate; and

a micromirror section disposed on said 2nd surface of said single substrate;

wherein said micromirror section comprises:

a micromirror; and

at least one support structure for supporting said micromirror.

2. The device of claim 1, wherein:

said control circuitry comprising a circuit selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits.

3. The device of claim 1, wherein:

said single substrate comprising a substrate selected from the group consisting of a silicon-on-insulator (SOI) substrate, a silicon substrate, a polycrystalline silicon substrate, a glass substrate, a plastic substrate, a ceramic substrate, a germanium substrate, a SiGe substrate a SiC substrate, a sapphire substrate a quartz substrate, a GaAs substrate, and an InP substrate.

4. The device of claim 1, wherein:

said micromirror section additionally comprises at least one addressing electrode for actuating said micromirror.

5. The device of claim 4, additionally comprising:

at least one electrically conductive routing line integral with said single substrate that connects said control circuitry to said at least one addressing electrode.

6. The device of claim 5, wherein:

said at least one electrically conductive routing line comprises a via through said single substrate and a metallization in said via.

7. The device of claim 1, wherein:

said single substrate additionally comprises an insulating layer between said first surface and said second surface.

8. The device of claim 1, wherein:

said micromirror further comprising a metallic mirror.

9. The device of claim 1, wherein:

said micromirror further comprising a multilayer dielectric mirror.

10. The device of claim 1, wherein:

said micromirror further comprising a substantially planar reflective side with neither recesses nor protrusions.

11. The device of claim 1, wherein:

said micromirror further comprising a reflective surface having no edges perpendicular to a projection direction of an incident light propagation vector onto said single substrate.

12. The device of claim 11, wherein:

said reflective surface of said micromirror further comprising a polygon-shaped reflective surface.

13. The device of claim 12, wherein:

said polygon-shaped reflective surface is selected from the group consisting of a rectangle-shaped reflective surface and a hexagon-shaped reflective surface.

14. The device of claim 1, wherein:

said micromirror section additionally comprises a torsion hinge disposed underneath and supporting said micromirror support structure; and

said torsion hinge further comprising a pair of supporting structures for supporting said torsion hinge on said substrate.

15. The device of claim 1, wherein:

said micromirror section additionally comprises at least one stopping member for limiting a rotation of said micromirror.

16. The device of claim 15, wherein:

said at least one stopping member comprises a 1st stopping member for limiting the rotation of said micromirror in a 1st direction; and

a 2nd stopping member for limiting the rotation of said micromirror in a direction opposite to said 1st direction.

17. An array of electromechanical micromirror devices comprising:

single substrate with a 1st surface and a 2nd surface;

a control circuitry disposed on said 1st surface of said substrate; and an array of micromirror sections disposed on said 2nd surface of said single substrate wherein each said micromirror section comprises a micromirror; and

a support structure for supporting said micromirror.

18. The array of claim 17, wherein:

said control circuitry comprising a circuit selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits.

19. The array of claim 17, wherein:

said single substrate comprising a substrate selected from the group consisting of a silicon-on-insulator (SOI) substrate, a silicon substrate, a polycrystalline silicon substrate a glass substrate, a plastic substrate a ceramic substrate, a germanium substrate, a SiGe substrate, a SiC substrate, a sapphire substrate, a quartz substrate, a GaAs substrate and an InP substrate.

20. The array of claim 17, wherein:

said micromirror section additionally comprises at least one addressing electrode for actuating said micromirror.

21. The array of claim 20, additionally comprising:

at least one electrically conductive routing line integral with said single substrate that connects said control circuitry to said at least one addressing electrode of at least one of said micromirror sections.

22. The array of claim 21, wherein:

said at least one electrically conductive routing line comprises a via through said single substrate and a metallization in said via.

23. The array of claim 17, wherein:

said single substrate additionally comprises an insulating layer between said first surface and said second surface.

24. The array of claim 17, wherein:

said micromirror further comprising a metallic mirror.

25. The array of claim 17, wherein:

said micromirror further comprising a multilayer dielectric mirror.

26. The array of claim 17, wherein:

said micromirror further comprising a substantially planar reflective side with neither recesses nor protrusions.

27. The array of claim 17, wherein:

said micromirror further comprising a reflective surface of having no edges perpendicular to a projection direction of an incident light propagation vector onto said single substrate.

28. The array of claim 27, wherein:

said reflective surface of said micromirror further comprising a polygon-shaped reflective surface.

29. The array of claim 28, wherein:

said polygon-shaped reflective surface is selected from the group consisting of a rectangle-shaped reflective surface and a hexagon-shaped reflective surface.

30. The array of claim 17, wherein:

said micromirror section additionally comprises a torsion hinge disposed underneath and supporting said micromirror support structure; and

said torsion hinge further comprising a pair of supporting structures for supporting said torsion hinge on said substrate.

31. The array of claim 17, wherein:

said micromirror section additionally comprises at least one stopping member for limiting a rotation of said micromirror.

32. The array of claim 17, wherein:

said at least one stopping member comprises a 1st stopping member for limiting the rotation of said micromirror in a 1st direction; and

a 2nd stopping member for limiting the rotation of said micromirror in a direction opposite to said 1st direction.

33. A spatial light modulator (SLM) comprising an array of electromechanical micromirror devices wherein said micro-mirror devices further comprising:

a single substrate with a 1st surface and a 2nd surface;

a control circuitry disposed on said 1st surface of said single substrate; and

an array of micromirror sections disposed on said 2nd surface of said single substrate wherein each said micromirror section comprises a micromirror; and

a support structure for supporting said micromirror.

34. A method of fabricating an array of electromechanical micromirrors comprising the steps of:

providing a single substrate with a 1st surface and a 2nd surface;

forming control circuitry on said 1st surface of said single substrate; and

forming a plurality of support structures on said second surface of said single substrate and forming a plurality of micromirrors on top of and supported by said support structures.

35. The method of claim 34, wherein:

said step of forming said control circuitry comprises a step of fabricating said control circuits selected from the group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, DMOS circuits, HEMT circuits, amorphous silicon thin film transistor circuits, polysilicon thin film transistor circuits, SiGe transistor circuits, SiC transistor circuits, GaN transistor circuits, GaAs transistor circuits, InP transistor circuits, CdSe transistor circuits, organic transistor circuits, and conjugated polymer transistor circuits.

36. The method of claim 34, wherein:

said step of providing said single substrate further comprising a step of providing said single substrate is selected from a group consisting of a silicon-on-insulator (SOI) substrate, a silicon substrate, a polycrystalline silicon substrate, a glass substrate, a plastic substrate, a ceramic substrate, a germanium substrate, a SiGe substrate, a SiC substrate, a sapphire substrate, a quartz substrate, a GaAs substrate, and an InP substrate.

37. The method of claim 34, wherein:

said step of forming said micromirrors additionally comprises a step of forming a plurality of addressing electrodes for actuating said micromirrors.

38. The method of claim 37, additionally comprising a step of:

forming a plurality of electrically conductive routing lines integrated with said single substrate for connecting said control circuitry to said plurality of addressing electrodes.

39. The method of claim 38, wherein said step of:

forming said plurality of electrically conductive routing lines comprises the steps of:

forming at least one via through said substrate; and

forming a metallization in said at least one via.

40. The method of claim 34, wherein:

said step of providing said single substrate further comprising a step of providing a single substrate comprises an insulating layer between said 1st surface and said 2nd surface.

41. The method of claim 34, wherein:

said step of forming a plurality of micromirrors comprises a step of forming a reflective metallic coating on said micromirrors.

42. The method of claim 34, wherein:

said step of forming a plurality of micromirrors comprises a step of forming a reflective multilayer dielectric coating on said micromirrors.

43. The method of claim 34, wherein said step of forming said micromirrors comprises the steps of:

forming said plurality of micromirror support structures embedded in a sacrificial layer;

planarizing a top surface of said sacrificial layer and said micromirror support structures

depositing a micromirror material on said top-surface;

patterning said micromirror material to form a plurality of micromirrors; and

removing said sacrificial layer by an etching process.

44. The method of claim 43, wherein:

said step of forming said microstructures in said sacrificial layer further comprising a step of forming said microstructures in a layer composed of a material is selected from the group consisting of a photoresist polymer, a silicon oxide, a silicon nitride, a silicon oxynitride, and an amorphous silicon.

45. The method of claim 43, wherein:

said step of planarizing said top surface further comprising a step of applying a chemical mechanical polishing (CMP) process.

46. The method of claim 34, wherein said step of forming a plurality of micromirrors comprises a step of:

patterning said micromirrors to have no edges perpendicular to a projection direction of an incident light propagation vector onto a plane of said single substrate.

47. The method of claim 46, wherein:

said step of forming said micromirrors further comprising a step of patterning at least one of said micromirror as a polygon-shaped micromirror.

48. The method of claim 47, wherein:

said step of forming said polygon-shaped micromirror is a step of forming said micromirror either as a rectangle-shaped micromirror or a hexagon-shaped micromirror.

49. The method of claim 34, additionally comprising a step of:

forming a torsion hinge for supporting said support structures by forming a hinge support followed by forming a torsion hinge on top of and supported by said hinge support.

50. The method of claim 34, additionally comprising the step of:

forming at least one stopping member for limiting a rotation of said micromirror.

51. The method of claim 50, wherein said step of forming at least one stopping member comprises:

forming a 1st stopping member for limiting a rotation of said micromirror in a 1st direction; and

forming a 2nd stopping member for limiting a rotation of said micromirror in a direction opposite to said 1st direction.

52. A method of fabricating an array of electromechanical micromirrors, comprising the steps of:

providing a single silicon-on-insulator substrate with an epitaxial top silicon layer above an insulator layer, supported by a bottom silicon layer;

forming control circuitry on said epitaxial top silicon layer;

removing said bottom silicon layer, thereby exposing the insulator layer;

forming a plurality of support structures followed by forming a plurality of micromirrors on top of and supported by said support structures.

53. The method of claim 52, wherein:

said step of forming said control circuitry comprises a step of fabricating said control circuits selected from a group consisting of: CMOS circuits, NMOS circuits, PMOS circuits, bipolar transistor circuits, BiCMOS circuits, and DMOS circuits.

54. The method of claim 52, wherein:

said step of removing said bottom silicon layer comprises a step of applying a backgrinding step to remove said bottom silicon layer.

55. The method of claim 52, wherein:

said step of removing said bottom silicon layer comprises a step of applying a chemical mechanical polishing (CMP) step to remove said bottom silicon layer.

56. The method of claim 52, additionally comprises a step of:

forming a plurality of addressing electrodes for actuating said plurality of micromirrors.

57. The method of claim 56, additionally comprising a step of:

forming a plurality of electrically conductive routing lines integrated with said single substrate for connecting said control circuitry to said plurality of addressing electrodes.

58. The method of claim 57, wherein said step of forming said plurality of electrically conductive routing lines comprises the steps of:

forming at least one via through said substrate; and

forming a metallization in said via.

59. The method of claim 52, wherein said step of forming said micromirrors the steps of:

forming said plurality of micromirror support structures embedded in a sacrificial layer;

planarizing a top surface of said sacrificial layer and said micromirror support structures;

depositing a micromirror material on said top-surface;

patterning said micromirror material to form a plurality of micromirrors; and

removing said sacrificial layer by an etching process.

60. The method of claim 59, wherein:

said step of planarizing said top surface further comprising a step of applying a chemical mechanical polishing (CMP) process.

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