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(74) Agent: YAO, Shun; 2820 Fifth Street, Davis, California 95618 (US).

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(54) Title: PHOTOVOLTAIC DEVICES WITH ELECTROPLATED METAL GRIDS

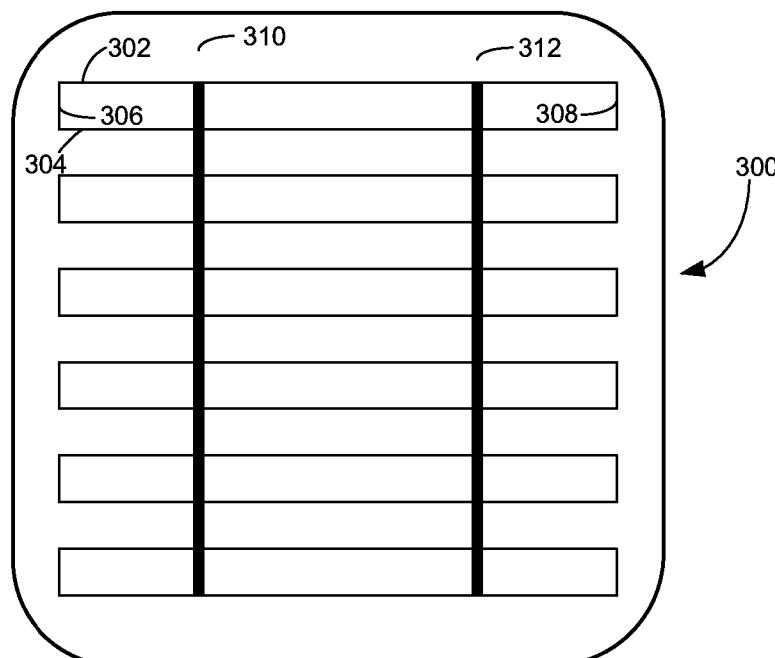


FIG. 3A

(57) Abstract: One embodiment of the present invention provides a solar cell. The solar cell includes a photovoltaic structure and a front-side metal grid (300) situated above the photovoltaic structure. The front-side metal grid also includes one or more electroplated metal layers. The front-side metal grid includes one or more finger lines (302, 304), and each end of a respective finger line is coupled to a corresponding end of an adjacent finger line via an additional metal line (306, 308, 314, 316, 318, 320), thus ensuring that the respective finger line has no open end.



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PHOTOVOLTAIC DEVICES WITH ELECTROPLATED METAL GRIDS

Inventors: Jianming Fu, Jiunn Benjamin Heng, Christopher J. Beitel, and Zheng Xu

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BACKGROUND

Field

[0001] This disclosure is generally related to solar cells. More specifically, this disclosure is related to a solar cell that includes a metal grid fabricated by an electroplating technique.

Related Art

[0002] The negative environmental impact caused by the use of fossil fuels and their rising cost have resulted in a dire need for cleaner, cheaper alternative energy sources. Among 15 different forms of alternative energy sources, solar power has been favored for its cleanliness and wide availability.

[0003] A solar cell converts light into electricity using the photovoltaic effect. There are several basic solar cell structures, including a single p-n junction solar cell, a p-i-n/n-i-p solar cell, and a multi-junction solar cell. A typical single p-n junction structure includes a p-type 20 doped layer and an n-type doped layer. Solar cells with a single p-n junction can be homojunction solar cells or heterojunction solar cells. If both the p-doped and n-doped layers are made of similar materials (materials with equal bandgaps), the solar cell is called a homojunction solar cell. In contrast, a heterojunction solar cell includes at least two layers of materials of 25 different bandgaps. A p-i-n/n-i-p structure includes a p-type doped layer, an n-type doped layer, and an intrinsic (undoped) semiconductor layer (the i-layer) sandwiched between the p-layer and the n-layer. A multi-junction structure includes multiple single-junction structures of different bandgaps stacked on top of one another.

[0004] In a solar cell, light is absorbed near the p-n junction, generating carriers. The carriers diffuse into the p-n junction and are separated by the built-in electric field, thus 30 producing an electrical current across the device and external circuitry. An important metric in determining a solar cell's quality is its energy-conversion efficiency, which is defined as the ratio between power converted (from absorbed light to electrical energy) and power collected when the solar cell is connected to an electrical circuit.

[0005] FIG. 1 presents a diagram illustrating an exemplary homojunction solar cell based on a crystalline-Si (c-Si) substrate (prior art). Solar cell 100 includes a front-side Ag electrode grid 102, an anti-reflection layer 104, an emitter layer 106, a substrate 108, and an aluminum (Al) back-side electrode 110. Arrows in FIG. 1 indicate incident sunlight.

5 [0006] In conventional c-Si based solar cells, the current is collected by front-side Ag grid 102. To form Ag grid 102, conventional methods involve printing Ag paste (which often includes Ag particle, organic binder, and glass frit) onto the wafers and then firing the Ag paste at a temperature between 700°C and 800°C. The high-temperature firing of the Ag paste ensures good contact between Ag and Si, and lowers the resistivity of the Ag lines. The resistivity of the 10 fired Ag paste is typically between 5×10^{-6} and 8×10^{-6} ohm-cm, which is much higher than the resistivity of bulk silver.

15 [0007] In addition to the high series resistance, the electrode grid obtained by screen-printing Ag paste also has other disadvantages, including higher material cost, wider line width, and limited line height. As the price of silver rises, the material cost of the silver electrode has exceeded half of the processing cost for manufacturing solar cells. With the state-of-the-art printing technology, the Ag lines typically have a line width between 100 and 120 microns, and it is difficult to reduce the line width further. Although inkjet printing can result in narrower lines, inkjet printing suffers other problems, such as low productivity. The height of the Ag lines is also limited by the printing method. One print can produce Ag lines with a height that is less 20 than 25 microns. Although multiple printing can produce lines with increased height, it also increases line width, which is undesirable for high-efficiency solar cells. Similarly, electroplating of Ag or Cu onto the printed Ag lines can increase line height at the expense of increased line width. In addition, the resistance of such Ag lines is still too high to meet the requirement of high-efficiency solar cells.

25 [0008] Another solution is to electroplate a Ni/Cu/Sn metal stack directly on the Si emitter. This method can produce a metal grid with lower resistance (the resistivity of plated Cu is typically between 2×10^{-6} and 3×10^{-6} ohm-cm). However, the adhesion of Ni to Si is less than ideal, and stress from the metal stack may result in peeling of the whole metal lines.

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SUMMARY

[0009] One embodiment of the present invention provides a solar cell. The solar cell includes a photovoltaic structure and a front-side metal grid situated above the photovoltaic structure. The front-side metal grid also includes one or more electroplated metal layers. The

front-side metal grid also includes one or more finger lines, and each end of a respective finger line is coupled to a corresponding end of an adjacent finger line via an additional metal line, thus ensuring that the respective finger line has no open end.

[0010] In a variation on the embodiment, the additional metal line is located near an edge 5 of the solar cell and has a width that is larger than a width of the respective finger line.

[0011] In a variation on the embodiment, an intersection between the additional metal line and the respective finger line is rounded or chamfered.

[0012] In a variation on the embodiment, the metal grid further includes a metal adhesive 10 layer situated between the electroplated metal layer and the photovoltaic structure. The metal adhesive layer further comprises one or more of: Cu, Al, Co, W, Cr, Mo, Ni, Ti, Ta, titanium nitride (TiN_x), titanium tungsten (TiW_x), titanium silicide (TiSi_x), titanium silicon nitride (TiSiN), tantalum nitride (TaN_x), tantalum silicon nitride (TaSiN_x), nickel vanadium (NiV), tungsten nitride (WN_x), and their combinations.

[0013] In a further variation, the photovoltaic structure comprises a transparent 15 conducting oxide (TCO) layer, and the metal adhesive layer is in direct contact with the TCO layer.

[0014] In a variation on the embodiment, the electroplated metal layers include one or more of: a Cu layer, an Ag layer, and a Sn layer.

[0015] In a variation on the embodiment, the metal grid further includes a metal seed 20 layer situated between the electroplated metal layer and photovoltaic structure.

[0016] In a further variation, the metal seed layer is formed using a physical vapor deposition (PVD) technique, including one of: evaporation and sputtering deposition.

[0017] In a variation on the embodiment, a predetermined edge portion of the respective finger line has a width that is larger than a width of a center portion of the respective finger line.

[0018] In a variation on the embodiment, the photovoltaic structure includes a base layer, 25 and an emitter layer situated above the base layer. The emitter layer includes at least one of: regions diffused with dopants located within the base layer, a poly silicon layer diffused with dopants situated above the base layer, and a doped amorphous silicon (a-Si) layer situated above the base layer.

[0019] In a further variation, the dopants include one of: phosphorus and boron.

BRIEF DESCRIPTION OF THE FIGURES

[0020] FIG. 1 presents a diagram illustrating an exemplary solar cell (prior art).

[0021] FIG. 2 presents a diagram illustrating an exemplary electroplated metal grid situated on the front surface of a solar cell (prior art).

[0022] FIG. 3A presents a diagram illustrating an exemplary electroplated metal grid situated on the surface of a solar cell, in accordance with an embodiment of the present invention.

5 [0023] FIG. 3B presents a diagram illustrating an exemplary electroplated metal grid situated on the surface of a solar cell, in accordance with an embodiment of the present invention.

[0024] FIG. 3C presents a diagram illustrating an exemplary electroplated metal grid situated on the surface of a solar cell, in accordance with an embodiment of the present invention.

10 [0025] FIG. 3D presents a diagram illustrating an exemplary electroplated metal grid situated on the surface of a solar cell, in accordance with an embodiment of the present invention.

[0026] FIG. 4 presents a diagram illustrating an exemplary electroplated metal grid situated on the surface of a solar cell, in accordance with an embodiment of the present invention.

15 [0027] FIG. 5 presents a diagram illustrating an exemplary process of fabricating a solar cell in accordance with an embodiment of the present invention.

[0028] In the figures, like reference numerals refer to the same figure elements.

DETAILED DESCRIPTION

20 [0029] The following description is presented to enable any person skilled in the art to make and use the embodiments, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present disclosure. Thus, the present invention is not limited to the embodiments shown, but is to be 25 accorded the widest scope consistent with the principles and features disclosed herein.

Overview

30 [0030] Embodiments of the present invention provide a solution to avoid metal peeling in a solar cell that includes an electroplated metal grid. The solar cell includes a crystalline-Si (c-Si) substrate, an emitter layer, a passivation layer, a metal-adhesion layer, and front- and back-side electrode metal grids. The metal-adhesion layer is formed using a physical vapor deposition (PVD) technique, such as sputtering or evaporation. The front-side metal grid is formed by selectively electroplating a metal stack, which can be a single-layer or a multi-layer structure, on the metal-adhesion layer. To mitigate the stress that can lead to the peeling of the metal lines, the

grid pattern is specially designed to ensure that no open end or discontinuous point exists. The back-side electrode metal grid can be formed using a same method that is used to form the front-side electrode metal grid. Additionally, it is possible to form the back-side electrode by screen-printing, electroplating, or aerosol-jet printing of a metal grid.

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Electroplated Metal Grid

[0031] Electroplated metal grids used as solar cell electrodes have shown lower resistance than printed Al grids. However, adhesion between the electroplated metal lines and the underlying transparent conducting oxide (TCO) layers or semiconductor layers can be an issue.

10 Even with the introduction of an adhesion layer, as the thickness of the electroplated metal lines increases (to ensure lower resistance), metal line peeling can still occur when the stress is too high. The peeling of metal lines can be a result of stress buildup at the interface between the electroplated metal and the underlying structures (which can be the TCO layer or the semiconductor structure). The difference in thermal expansion coefficients between the metal 15 and the silicon substrate and the thermal cycling of the environment where the solar cells are situated often lead to such stress. If the amount of the stress exceeds the adhesion strength provided by the adhesion layer, the bonding between the metal and the underlying layers will break.

[0032] FIG. 2 presents a diagram illustrating an exemplary electroplated metal grid 200 situated on the front surface of a solar cell (prior art). In FIG. 2, metal grid 200 includes a number of finger strips, such as finger strips 202 and 204, and busbars 206 and 208. Note that busbars are thicker metal strips connected directly to external leads, and fingers are finer metal strips that collect photo current for delivery to the busbars.

[0033] When designing solar cells, to reduce losses due to emitter resistance and shading, 25 it is desirable to design a high metal height-to-width aspect ratio. However, the height-to-width aspect ratio of the finger lines is often limited by the fabrication technology used for forming the metal grid. Conventional printing technologies, such as screen-printing, often result in metal lines with relatively low height-to-width aspect ratio. Electroplating technologies can produce metal lines with higher height-to-width aspect ratio. However, electroplated metal lines may 30 experience peeling when placed in an environment with changing temperatures. As previously discussed, the difference in thermal expansion coefficients between the metal and the silicon substrate, and the changing temperature can lead to stress buildup and the eventual breaking of the adhesion between the metal and the underlying layers. Even though the breaking may happen

at a single location, the good malleability of the plated metal, such as plated Cu, can lead to peeling of the entire metal line.

[0034] Note that the amount of stress is related to the height-to-width aspect ratio of the metal lines; the larger the aspect ratio, the larger the stress. Hence, assuming the metal lines have 5 uniform width (which can be well controlled during fabrication), the thicker portion of the line will experience greater stress. For electroplated metal grid, due to the current crowding effect occurring at the edge of the wafer, metals deposited at the wafer edge tend to be thicker than metals deposited at the center of the wafer. In the example shown in FIG. 2, electroplated metals located in edge regions, such as regions 210 and 212, tend to have a larger thickness. As one can 10 see from FIG. 2, conventional metal grid 200 includes finger strips that have open ends at edge regions 210 and 212. These end portions tend to have larger thicknesses and, thus, may experience larger amounts of thermal stress.

[0035] To make matters worse, in addition to thermal stress, additional handling of the devices during fabrication of the solar module, such as storing, tabbing, and stringing, can also 15 lead to peeling of the metal grid. For example, while the solar cells are being handled by machines or people, it is possible that finger lines may be pushed from side to side by other objects, such as edges of different wafers or metal lines on a wafer stacked above.

Coincidentally, the end portions of the finger strips are often the weakest point in terms of 20 resisting external forces. As one can see in FIG. 2, the end portion of a finger strip is not connected to other portions of the metal line, and thus is less supported. While being pushed from side to side, it is easier for the end of a finger strip than the middle of the finger strip to break away from the underlying layers. Once the end portion breaks away, the good malleability 25 of the metal often leads to the peeling of the entire metal line. Note that the metal peeling often happens to the finger strip due to its high height-to-width aspect ratio. The busbar, on the other hand, is much wider and usually does not experience peeling.

[0036] Hence, to prevent the peeling of the metal lines, it is important to strengthen the bond between the end portions of the finger strip and the underlying layers. Based on the 30 previous analysis, to strengthen the bond between the metal at the line end and the underlying layers, one can reduce the height of the end portions to make it the same as the rest of the portions of the line. One way to do so is to increase the width of the line at the end region. The increased line width means that the collected current is now spread over a larger area, hence mitigating the current crowding at the line end. However, to avoid shading loss, the increase in line width has to be small, and the overall effect is limited. In addition, this still cannot prevent end peeling caused by external forces.

[0037] Embodiments of the present invention provide a solution that makes the finger strips more resistant to peeling by redesigning the grid pattern. FIG. 3A presents a diagram illustrating an exemplary electroplated metal grid situated on the surface of a solar cell, in accordance with an embodiment of the present invention. In FIG. 3A, metal grid 300 includes a number of horizontally oriented finger strips, such as finger strips 302 and 304, and busbars 310 and 312. However, unlike metal grid 200 where each finger strip is a line segment disconnected from other finger strips, in FIG. 3A, both end points of each finger strip are connected to end points of an adjacent finger strip. For example, the end points of finger strip 302 are connected to end points of finger strip 304 via two short lines 306 and 308.

[0038] Note that two goals can be simultaneously achieved by adding short lines that bridge two adjacent finger strips. The first goal is to divert current at the wafer edge during electroplating, thus reducing the thickness of the metal deposited at the ends of the finger strips. Compared with the example shown in FIG. 2, during the electroplating process where only the finger patterns are conductive, the added short lines, such as lines 306 and 308, can cause the current that was originally concentrated at the tips of the finger strips, such as finger strips 302 and 304, to be diverted away through these added short lines. Consequently, current densities at the tips of the finger strips are reduced. This can further lead to a more uniform height of the deposited metal. The increased height uniformity of the metal lines means that there will be less additional stress buildup at the ends of the finger strips when the temperature changes.

[0039] The second goal achieved by the additional short lines is to eliminate the existence of open ends. By bridging an open end point on one finger strip to an end point on an adjacent finger strip, the original discontinued finger strips become continuous lines without any open ends. Note that, as discussed previously, open or discontinued ends may break off when external forces are applied due to lack of structural support. In contrast, in the example shown in FIG. 3A, when external forces are applied to finger strip 302, such as when finger strip 302 is pushed from side to side, because the end portions are now connected to and supported by additional lines 306 and 308, it is less likely for the end portions of finger strip 302 to break away from the underlying layers. Note that the support to the end portions is provided by adhesion forces between those additional lines and the underlying layers. The elimination of the open ends also eliminates the weakest point in terms of resisting external forces. Note that because the metal peeling is not a concern for busbars, there is no need to eliminate the open ends on the busbars. In one embodiment, the ends of the busbars are configured to align with the finger strips at the upper and lower edge of the wafer, as shown in FIG. 3A. In other words, the ends of the busbars can

merge into the end finger strips, which results in the busbars also have no open ends.

[0040] By simultaneously increasing thickness uniformity and eliminating open ends, embodiments of the present invention effectively reduce the possibility of peeling of the finger strips. In addition to the example shown in FIG. 3A, other grid patterns can also be used to reduce the chances of peeling as long as they add additional metal lines at the wafer edge and the fingers consist of continuous lines without any open ends. FIG. 3B presents a diagram illustrating an exemplary electroplated metal grid situated on the surface of a solar cell, in accordance with an embodiment of the present invention. In the example shown in FIG. 3B, instead of merely creating connections between two adjacent finger strips, short lines are added to connect the end points of more than two finger strips. In FIG. 3B, a number of short lines, such as lines 314 and 316, are added at the wafer edge to couple more than two finger strips. Like the one shown in FIG. 3A, the resulting grid pattern includes continuous finger lines that have no open ends.

[0041] FIG. 3C presents a diagram illustrating an exemplary electroplated metal grid situated on the surface of a solar cell, in accordance with an embodiment of the present invention. In FIG. 3C, on each edge of the wafer, an vertically oriented long line, such as lines 318 and 320, is added to join together end points of all horizontally oriented finger strips. FIG. 3D presents a diagram illustrating an exemplary electroplated metal grid situated on the surface of a solar cell, in accordance with an embodiment of the present invention. In FIG. 3D, short lines are added alternatively (with the exception of the upper and lower edges) at the left and right edges of the wafer between two adjacent finger strips to ensure that each end point of a finger strip is at least coupled to an end point of an adjacent finger strip via a short metal line. Note that the finger patterns shown in FIGs. 3A-3D are merely examples, and they are not intended to be exhaustive or to limit the present invention to the finger patterns disclosed in these figures. Embodiments of the present invention can include any finger patterns that add metal lines at the wafer edge to connect the otherwise discrete finger strips. Such additional lines play important roles in mitigating the problem of metal peelings facing the electroplated metal grid because they help to divert current from and provide structural support to the end portions of the finger strips.

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[0042] Note that, although the additional lines at the wafer edge may increase shading, such an effect can be negligible in most cases. For example, in FIG. 3A, the total effect of the additional lines can be equivalent to the addition of a single finger strip. For a wafer with a size of 125×125 mm², an additional finger strip with a width of about 75 μm only adds about 0.05%

shading, which is negligible. Moreover, the additional shading may also be offset by the additional current collected by these additional lines.

[0043] In the examples shown in FIGs. 3A-3D, sharp corners are created where the additional vertical lines connected to the horizontal finger strips. These sharp corners may also accumulate lateral stress that may cause metal breaking. To further improve the adhesion of the metal lines, in one embodiment, the finger strips are connected by lines with rounded corner. FIG. 4 presents a diagram illustrating an exemplary electroplated metal grid situated on the surface of a solar cell, in accordance with an embodiment of the present invention. In FIG. 4, metal grid 400 includes finger strips that include continuous, non-broken lines. More specifically, every two adjacent parallel finger strips are joined together at the ends by additional short lines to form a continuous loop. To further reduce the stress, straight angles or sharp turns are avoided when designing the finger patterns. For example, the straight angle can be rounded with an arc or chamfered with straight lines. In FIG. 4, regions 402 and 404 illustrate exemplary detailed views of the turning locations of a finger strip.

[0044] The detailed view shown in region 402 illustrates that arcs are used to connect two perpendicular metal lines, one being the horizontal finger strip, and the other the vertical short line that bridges two adjacent fingers. This results in a rounded corner. In one embodiment, the radius of the arc can be between 0.05 mm and one-half of the finger spacing. Note that the finger spacing can be between 2 and 3 mm. The detailed view shown in region 404 illustrates that chamfers are created at the turning corners to eliminate the right angle formed by the two perpendicular metal lines.

[0045] In one embodiment, the metal lines at the wafer edge, such as the short lines (including the rounded or chamfered sections) that connect the two adjacent finger strips, are slightly widened in order to further reduce current density at those locations. As a result, during electroplating, the thickness of metal deposited at those edge locations is reduced, and the increased contact area also ensures better adhesion between the electroplated metal and the underlying layers. In FIG. 4, region 406 illustrates an exemplary detailed view of the edge portions of a finger strip, showing that the width of the edge portion is larger than that of the center portion of the finger strip. In one embodiment, the width of the edge portion of the finger can be at least 20% - 30% larger than that of the center portion. In a further embodiment, the width of the edge portion of the finger can be up to 0.2 mm. The length of this widened portion (denoted as L in FIG. 4) can be between 1 and 30 mm. Note that the longer the widened finger edge, the better the adhesion, and the more shading effect. In some embodiments, the interface

between the center portion of the finger and the widened edge portion of the finger may be tapered.

[0046] FIG. 5 presents a diagram illustrating an exemplary process of fabricating a solar cell in accordance with an embodiment of the present invention.

5 **[0047]** In operation 5A, a substrate 500 is prepared. In one embodiment, substrate 500 can be a crystalline-Si (c-Si) wafer. In a further embodiment, preparing c-Si substrate 500 includes standard saw damage etch (which removes the damaged outer layer of Si) and surface texturing. The c-Si substrate 500 can be lightly doped with either n-type or p-type dopants. In one embodiment, c-Si substrate 500 is lightly doped with p-type dopants. Note that in addition to 10 c-Si, other materials (such as metallurgical-Si) can also be used to form substrate 500.

15 **[0048]** In operation 5B, a doped emitter layer 502 is formed on top of c-Si substrate 500. Depending on the doping type of c-Si substrate 500, emitter layer 502 can be either n-type doped or p-type doped. In one embodiment, emitter layer 502 is doped with n-type dopant. In a further embodiment, emitter layer 502 is formed by diffusing phosphorous. Note that if phosphorus diffusion is used for forming emitter layer 502, phosphosilicate glass (PSG) etch and edge 20 isolation is needed. Other methods are also possible to form emitter layer 502. For example, one can first form a poly Si layer on top of substrate 500, and then diffuse dopants into the poly Si layer. The dopants can include either phosphorus or boron. Moreover, emitter layer 502 can also be formed by depositing a doped amorphous Si (a-Si) layer on top of substrate 500.

25 **[0049]** In operation 5C, an anti-reflection layer 504 is formed on top of emitter layer 502. In one embodiment, anti-reflection layer 504 includes, but not limited to: silicon nitride (SiN_x), silicon oxide (SiO_x), titanium oxide (TiO_x), aluminum oxide (Al_2O_3), and their combinations. In one embodiment, anti-reflection layer 504 includes a layer of a transparent conducting oxide (TCO) material, such as indium tin oxide (ITO), aluminum zinc oxide (AZO), gallium zinc oxide (GZO), tungsten doped indium oxide (IWO), and their combinations.

[0050] In operation 5D, back-side electrode 506 is formed on the back side of Si substrate 500. In one embodiment, forming back-side electrode 506 includes printing a full Al layer and subsequent alloying through firing. In one embodiment, forming back-side electrode 506 includes printing an Ag/Al grid and subsequent furnace firing.

30 **[0051]** In operation 5E, a number of contact windows, including windows 508 and 510, are formed in anti-reflection layer 504. In one embodiment, heavily doped regions, such as regions 512 and 514 are formed in emitter layer 502, directly beneath contact windows 508 and 510, respectively. In a further embodiment, contact windows 508 and 510 and heavily doped regions 512 and 514 are formed by spraying phosphorous on anti-reflection layer 504, followed

by a laser-groove local-diffusion process. Note that operation 5E is optional, and is needed when anti-reflection layer 504 is electrically insulating. If anti-reflection layer 504 is electrically conducting (e.g., when anti-reflection layer 504 is formed using TCO materials), there is no need to form the contact windows.

5 [0052] In operation 5F, a metal adhesive layer 516 is formed on anti-reflection layer 504. In one embodiment, materials used to form adhesive layer 516 include, but are not limited to: Ti, titanium nitride (TiN_x), titanium tungsten (TiW_x), titanium silicide ($TiSi_x$), titanium silicon nitride ($TiSiN$), Ta, tantalum nitride (TaN_x), tantalum silicon nitride ($TaSiN_x$), nickel vanadium (NiV), tungsten nitride (WN_x), Cu, Al, Co, W, Cr, Mo, Ni, and their combinations. In a further 10 embodiment, metal adhesive layer 516 is formed using a physical vapor deposition (PVD) technique, such as sputtering or evaporation. The thickness of adhesive layer 516 can range from a few nanometers up to 100 nm. Note that Ti and its alloys tend to form very good adhesion with Si material, and they can form good ohmic contact with heavily doped regions 512 and 514. Forming metal adhesive layer 514 on top of anti-reflection layer 504 prior to the electroplating 15 process ensures better adhesion to anti-reflection layer 504 of the subsequently formed layers.

[0053] In operation 5G, a metal seed layer 518 is formed on adhesive layer 516. Metal seed layer 518 can include Cu or Ag. The thickness of metal seed layer 518 can be between 5 nm and 500 nm. In one embodiment, metal seed layer 518 has a thickness of 100 nm. Like metal adhesive layer 516, metal seed layer 518 can be formed using a PVD technique. In one 20 embodiment, the metal used to form metal seed layer 518 is the same metal that used to form the first layer of the electroplated metal. The metal seed layer provides better adhesion of the subsequently plated metal layer. For example, Cu plated on Cu often has better adhesion than Cu plated on to other materials.

[0054] In operation 5H, a patterned masking layer 520 is deposited on top of metal seed 25 layer 518. The openings of masking layer 520, such as openings 522 and 524, correspond to the locations of contact windows 508 and 510, and thus are located above heavily doped regions 512 and 514. Note that openings 522 and 524 are slightly larger than contact windows 508 and 510. Masking layer 520 can include a patterned photoresist layer, which can be formed using a photolithography technique. In one embodiment, the photoresist layer is formed by screen- 30 printing photoresist on top of the wafer. The photoresist is then baked to remove solvent. A mask is laid on the photoresist, and the wafer is exposed to UV light. After the UV exposure, the mask is removed, and the photoresist is developed in a photoresist developer. Openings 522 and 524 are formed after developing. The photoresist can also be applied by spraying, dip coating, or curtain coating. Dry film photoresist can also be used. Alternatively, masking layer 520 can

include a layer of patterned silicon oxide (SiO₂). In one embodiment, masking layer 520 is formed by first depositing a layer of SiO₂ using a low-temperature plasma-enhanced chemical-vapor-deposition (PECVD) technique. In a further embodiment, masking layer 520 is formed by dip-coating the front surface of the wafer using silica slurry, followed by screen-printing an etchant that includes hydrofluoric acid or fluorides. Other masking materials are also possible, as long as the masking material is electrically insulating.

[0055] Note that masking layer 520 defines the pattern of the front metal grid because, during the subsequent electroplating, metal materials can only be deposited on regions above the openings, such as openings 522 and 524, defined by masking layer 520. To ensure better thickness uniformity and better adhesion, the pattern defined by masking layer 520 includes finger strips that are formed with continuous, non-broken lines. Exemplary patterns formed by masking layer 520 include patterns shown in FIGs. 3A-3D. In a further embodiment, openings that define lines located close to the wafer edge are widened. Exemplary patterns at the wafer edge include patterns shown in FIG. 4. FIG. 5G illustrates a top view of the patterned masking layer in accordance with an embodiment of the present invention. As one can see in FIG. 5G, the shaded area on the surface of the wafer is covered with masking layer 520, hence is not electrically conductive. The openings expose the underlying metal seed layer 518, which is electrically conductive. In the exemplary pattern shown in FIG. 5I, openings with smaller width define the finger pattern, which includes continuous lines without any open end. On the other hand, openings with larger width define the busbars, which may include line segments with open ends because, for busbars, metal peeling is not a concern.

[0056] In operation 5J, one or more layers of metal are deposited at the openings of masking layer 520 to form a front-side metal grid 526. Front-side metal grid 526 can be formed using an electroplating technique, which can include electrodeposition, light-induced plating, and/or electroless deposition. In one embodiment, metal seed layer 518 and/or adhesive layer 516 are coupled to the cathode of the plating power supply, which can be a direct current (DC) power supply, via an electrode. Metal seed layer 518 and masking layer 520, which includes the openings, are submerged in an electrolyte solution which permits the flow of electricity. Note that, because masking layer 520 is electrically insulating, metals will be selectively deposited into the openings, thus forming a metal grid with a pattern corresponding to the one defined by those openings. Depending on the material forming metal seed layer 518, front-side metal grid 526 can be formed using Cu or Ag. For example, if metal seed layer 518 is formed using Cu, front-side metal grid 526 is also formed using Cu. In addition, front-side metal grid 526 can include a multilayer structure, such as a Cu/Sn bi-layer structure, or a Cu/Ag bi-layer structure. The Sn or

Ag top layer is deposited to assist a subsequent soldering process. When depositing Cu, a Cu plate is used at the anode, and the solar cell is submerged in the electrolyte suitable for Cu plating. The current used for Cu plating is between 0.1 ampere and 2 amperes for a wafer with a dimension of 125 mm × 125 mm, and the thickness of the Cu layer is approximately tens of 5 microns. In one embodiment, the thickness of the electroplated metal layer is between 30 μm and 50 μm .

[0057] In operation 5K, masking layer 520 is removed.

[0058] In operation 5L, portions of adhesive layer 516 and metal seed layer 518 that are 10 originally covered by masking layer 520 are etched away, leaving only the portions that are beneath front-side metal grid 526. In one embodiment, wet chemical etching process is used. Note that, because front-side metal grid 526 is much thicker (by several magnitudes) than adhesive layer 516 and metal seed layer 518, the etching has a negligible effect on front-side metal grid 526. In one embodiment, the thickness of the resulting metal grid can range from 30 μm to 50 μm . The width of the finger strips can be between 10 μm to 100 μm , and the width of 15 the busbars can be between 0.5 to 2 mm. Moreover, the spacing between the finger strips can be between 2 mm and 3 mm.

[0059] During fabrication, after the formation of the metal adhesive layer and the seed 20 metal layer, it is also possible to form a patterned masking layer that covers areas that correspond to the locations of contact windows and the heavily doped regions, and etch away portions of the metal adhesive layer and the metal seed layer that are not covered by the patterned masking layer.

In one embodiment, the leftover portions of the metal adhesive layer and the metal seed layer 25 form a pattern that is similar to the ones shown in FIGs. 3A-3D and FIG. 4. Note that such patterns include finger strips that consist of continuous, non-broken lines. Once the patterned masking layer is removed, one or more layers of metals can be electroplated to the surface of the solar cell. On the solar cell surface, only the locations of the leftover portions of the metal seed 30 layer are electrically conductive, a plating process can selectively deposit metals on top of the leftover portions of metal seed layer.

[0060] In the example shown in FIG. 5, the back-side electrode is formed using a conventional printing technique (operation 5D). In practice, the back-side electrode can also be 30 formed by electroplating one or more metal layers on the backside of the solar cell. In one embodiment, the back-side electrode can be formed using operations that are similar to operations 5F-5L, which include forming a metal adhesive layer, a metal seed layer, and a patterned masking layer on the backside of the substrate. Note that the patterned masking layer on the backside defines the pattern of the back-side metal grid. In one embodiment, the back-side

metal grid includes finger strips that are formed with continuous, non-broken lines. In a further embodiment, the back-side metal grid may include exemplary patterns shown in FIGs. 3A-3D and FIG. 4.

[0061] The foregoing descriptions of various embodiments have been presented only for 5 purposes of illustration and description. They are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. Additionally, the above disclosure is not intended to limit the present invention.

What Is Claimed Is:

1. A solar cell, comprising:
 - a photovoltaic structure; and
 - 5 a front-side metal grid situated above the photovoltaic structure, wherein the front-side metal grid includes one or more electroplated metal layers, wherein the front-side metal grid includes one or more finger lines, and wherein each end of a respective finger line is coupled to a corresponding end of an adjacent finger line via an additional metal line, thus ensuring that the respective finger line has no open end.
- 10 2. The solar cell of claim 1, wherein the additional metal line is located near an edge of the solar cell, and wherein the additional metal line has a width that is larger than a width of the respective finger line.
- 15 3. The solar cell of claim 1, wherein an intersection between the additional metal line and the respective finger line is rounded or chamfered.
- 20 4. The solar cell of claim 1, wherein the metal grid further includes a metal adhesive layer situated between the electroplated metal layers and the photovoltaic structure, wherein the metal adhesive layer further comprises one or more of: Cu, Al, Co, W, Cr, Mo, Ni, Ti, Ta, titanium nitride (TiN_x), titanium tungsten (TiW_x), titanium silicide (TiSi_x), titanium silicon nitride (TiSiN), tantalum nitride (TaN_x), tantalum silicon nitride (TaSiN_x), nickel vanadium (NiV), tungsten nitride (WN_x), and their combinations.
- 25 5. The solar cell of claim 4, wherein the photovoltaic structure comprises a transparent conducting oxide (TCO) layer, and wherein the metal adhesive layer is in direct contact with the TCO layer.
6. The solar cell of claim 1, wherein the electroplated metal layers include one or more of:
 - a Cu layer;
 - an Ag layer; and
 - a Sn layer.

7. The solar cell of claim 1, wherein the metal grid further includes a metal seed layer situated between the electroplated metal layers and photovoltaic structure.

8. The solar cell of claim 7, wherein the metal seed layer is formed using a physical vapor deposition (PVD) technique, including one of: evaporation and sputtering deposition.

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9. The solar cell of claim 1, wherein a predetermined edge portion of the respective finger line has a width that is larger than a width of a center portion of the respective finger line.

10. The solar cell of claim 1, wherein the photovoltaic structure includes:
a base layer comprising Si; and

10 an emitter layer situated above the base layer, wherein the emitter layer includes at least one of:

regions diffused with dopants located within the base layer;
a poly Si layer diffused with dopants situated above the base layer;

and

15 a doped amorphous Si (a-Si) layer situated above the base layer.

11. The solar cell of claim 10, wherein the dopants include one of:
phosphorus; and
boron.

12. The solar cell of claim 1, further comprising a back-side metal grid situated below 20 the photovoltaic structure, wherein the back-side metal grid includes one or more electroplated metal layers, wherein the back-side metal grid includes one or more finger lines, and wherein each end of a respective finger line is coupled to a corresponding end of an adjacent finger line via an additional metal line, thus ensuring that the respective finger line has no open end.

13. A method for fabricating a solar cell, comprising:
25 depositing a transparent conducting oxide (TCO) layer on top of a semiconductor structure to form a photovoltaic structure;

forming a front-side metal grid on top the photovoltaic structure, wherein the front-side metal grid includes one or more electroplated metal layers, wherein the front-side metal grid

includes one or more finger lines, and wherein each end of a respective finger line is coupled to a corresponding end of an adjacent finger line via an additional metal line, thus ensuring that the respective finger line has no open end.

14. The method of claim 13, wherein the additional metal line is located near an edge 5 of the solar cell, and wherein the additional metal line has a width that is larger than a width of the respective finger line.

15. The method of claim 13, wherein an intersection between the additional metal line and the respective finger line is rounded or chamfered.

16. The method of claim 13, wherein forming the front-side metal grid involves 10 depositing a metal adhesive layer on top of the TCO layer using a physical vapor deposition (PVD) technique, wherein the metal adhesive layer comprises one or more of: Cu, Al, Co, W, Cr, Mo, Ni, Ti, Ta, titanium nitride (TiN_x), titanium tungsten (TiW_x), titanium silicide (TiSi_x), titanium silicon nitride (TiSiN), tantalum nitride (TaN_x), tantalum silicon nitride (TaSiN_x), nickel vanadium (NiV), tungsten nitride (WN_x), and their combinations.

15 17. The method of claim 13, wherein the electroplated metal layers include one or more of:

- a Cu layer;
- an Ag layer; and
- a Sn layer.

20 18. The method of claim 13, wherein forming the front-side metal grid involves depositing a metal seed layer using a physical vapor deposition (PVD) technique prior to forming the electroplated metal layers.

19. The method of claim 18, wherein forming the electroplated metal layers involves: 25 depositing a patterned masking layer on top of the metal seed layer, wherein openings of the masking layer correspond to positions of the front-side electrode grid, and wherein the masking layer is electrically insulating; electroplating one or more layers of metal on top of the patterned masking layer by submerging the solar cell in an electrolyte solution;

removing the patterned masking layer; and
performing an etching process to remove portions of the metal seed layer that are not covered by the electroplated metal layers.

20. The method of claim 13, wherein a predetermined edge portion of the respective finger line has a width that is larger than a width of a center portion of the respective finger line.

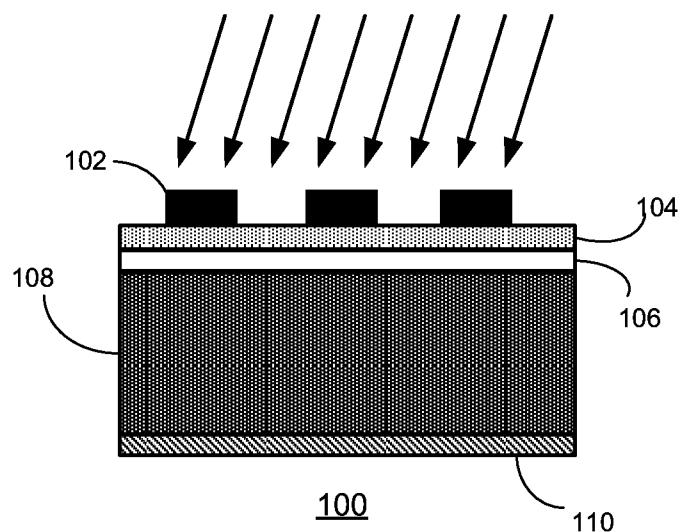
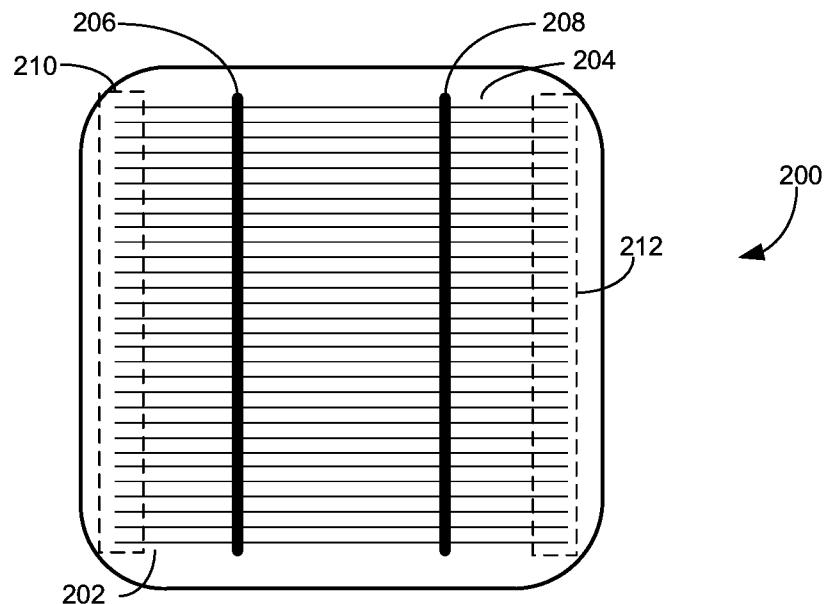
21. The method of claim 13, wherein forming the photovoltaic structure further comprises forming an emitter layer on top of a lightly doped base layer, and wherein forming the emitter layer involves at least one of:

10 diffusing dopants into the lightly doped base layer comprising Si;
diffusing dopants into a poly Si layer situated above the base layer; and
depositing a doped amorphous Si layer.

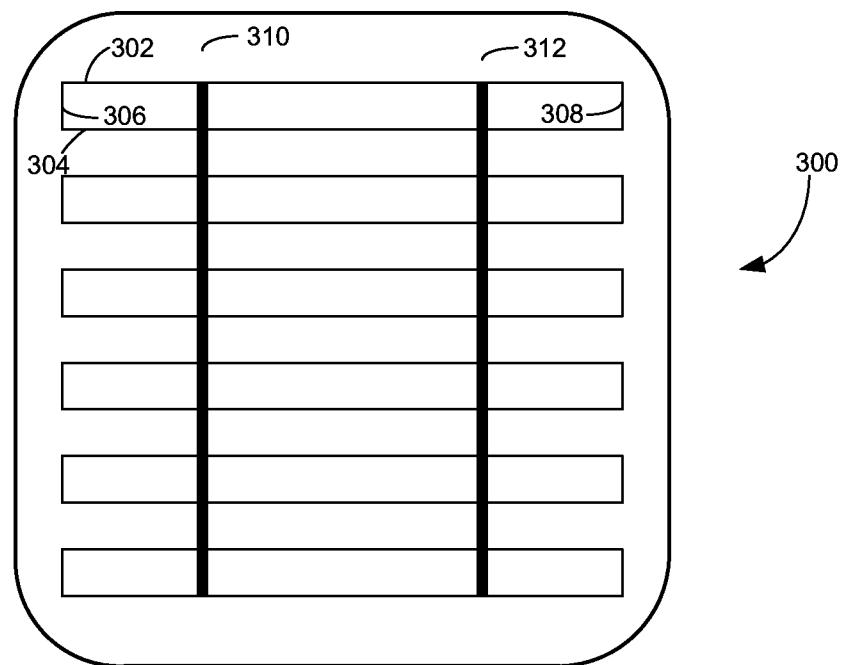
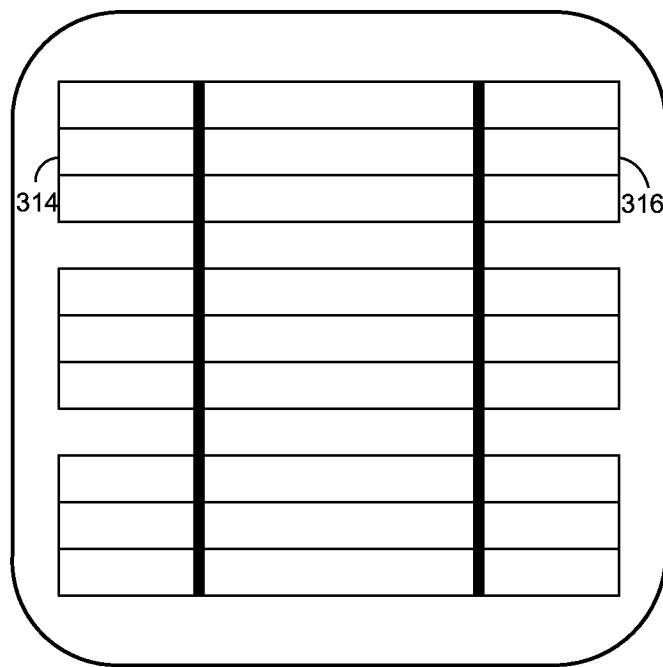
22. The method of claim 21, wherein the dopants include one of:
phosphorus; and
boron.

15 23. The method of claim 13, further comprising forming a back-side metal grid situated below the photovoltaic structure, wherein the back-side metal grid includes one or more electroplated metal layers, wherein the back-side metal grid includes one or more finger lines, and wherein each end of a respective finger line is coupled to a corresponding end of an adjacent finger line via an additional metal line, thus ensuring that the respective finger line has no open
20 end.

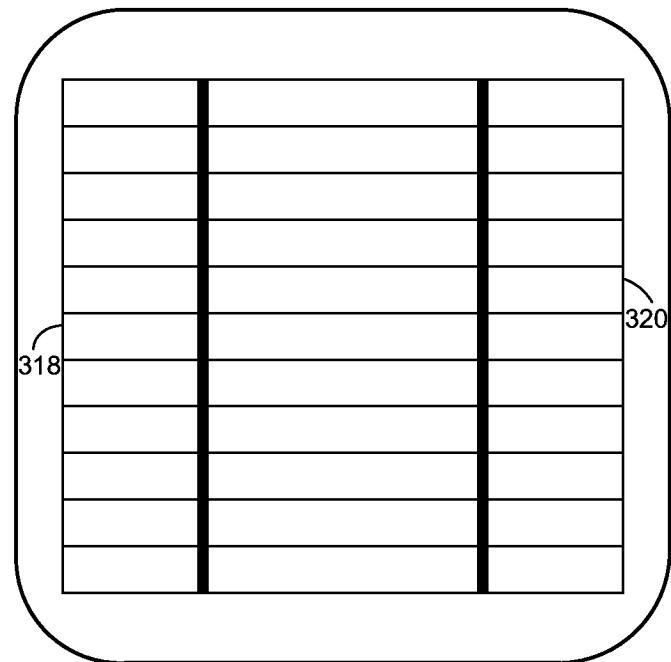
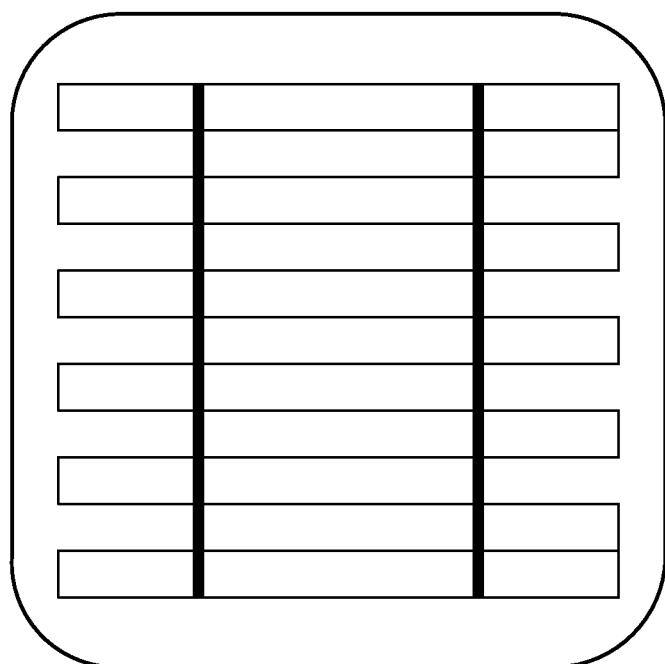
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**FIG. 1 (PRIOR ART)****FIG. 2 (PRIOR ART)**

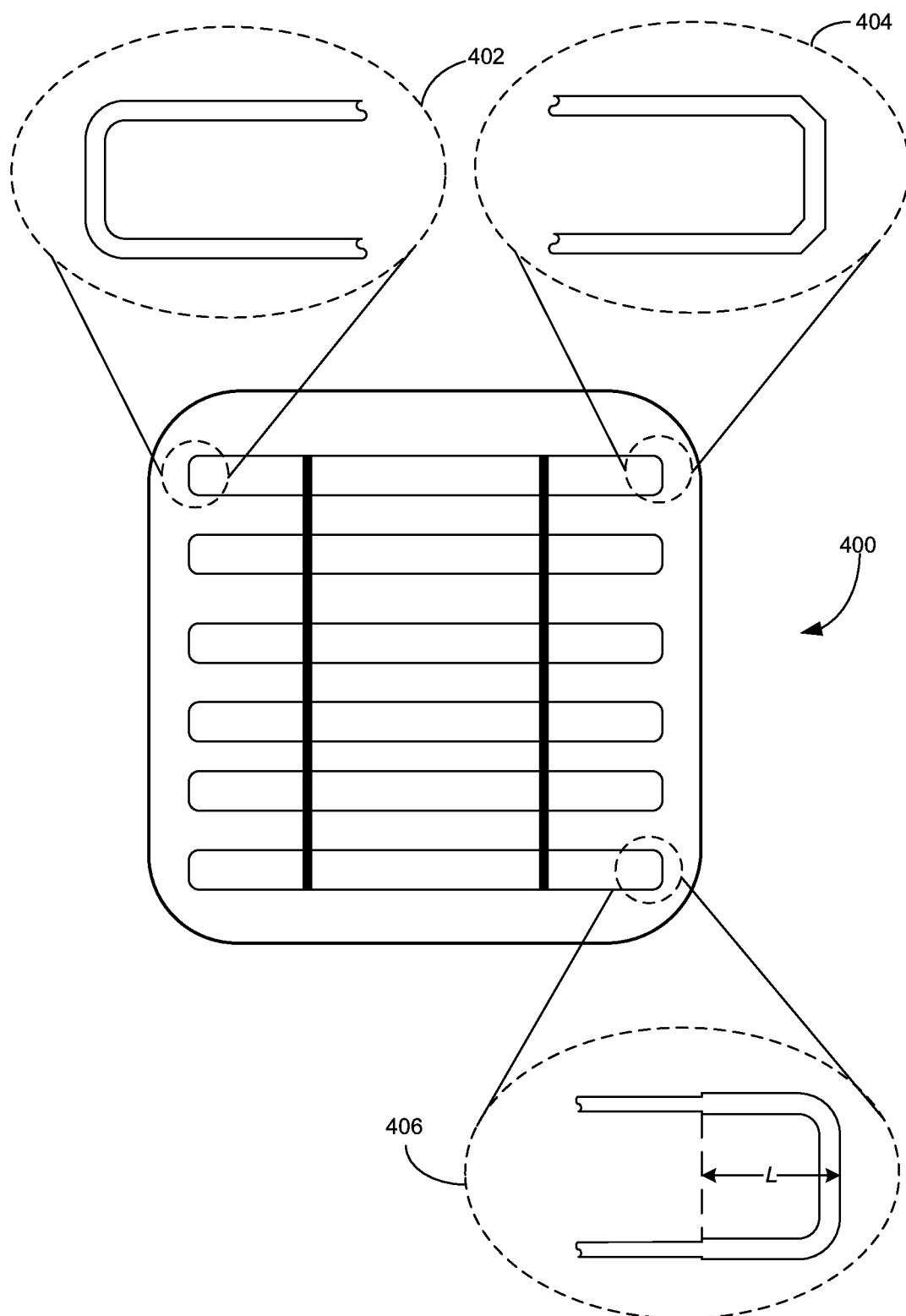
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**FIG. 3A****FIG. 3B**

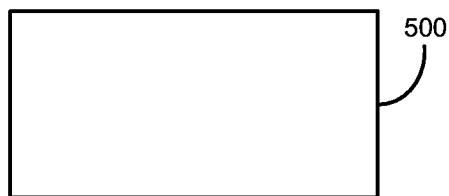
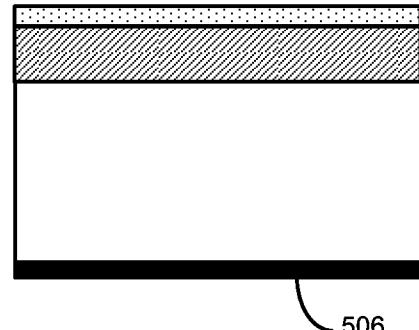
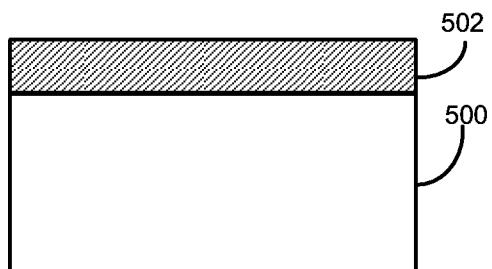
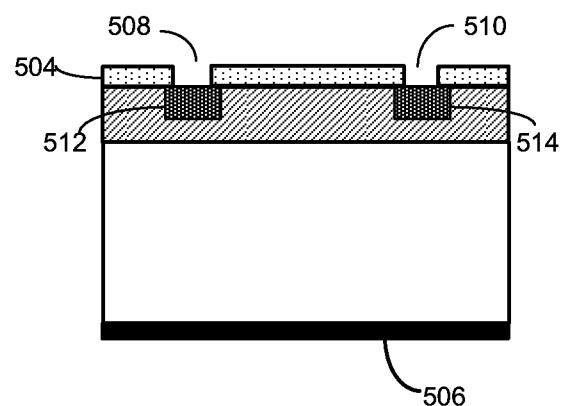
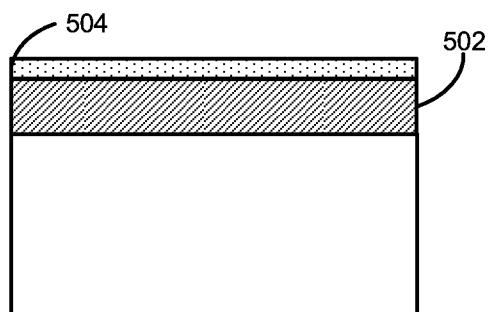
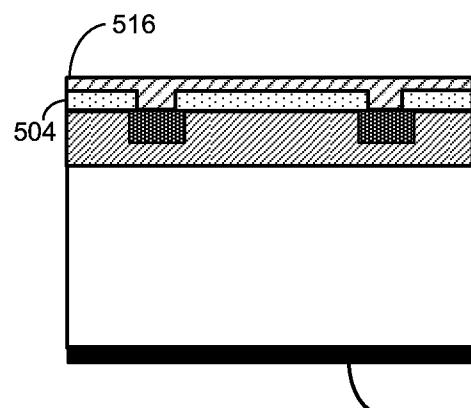
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**FIG. 3C****FIG. 3D**

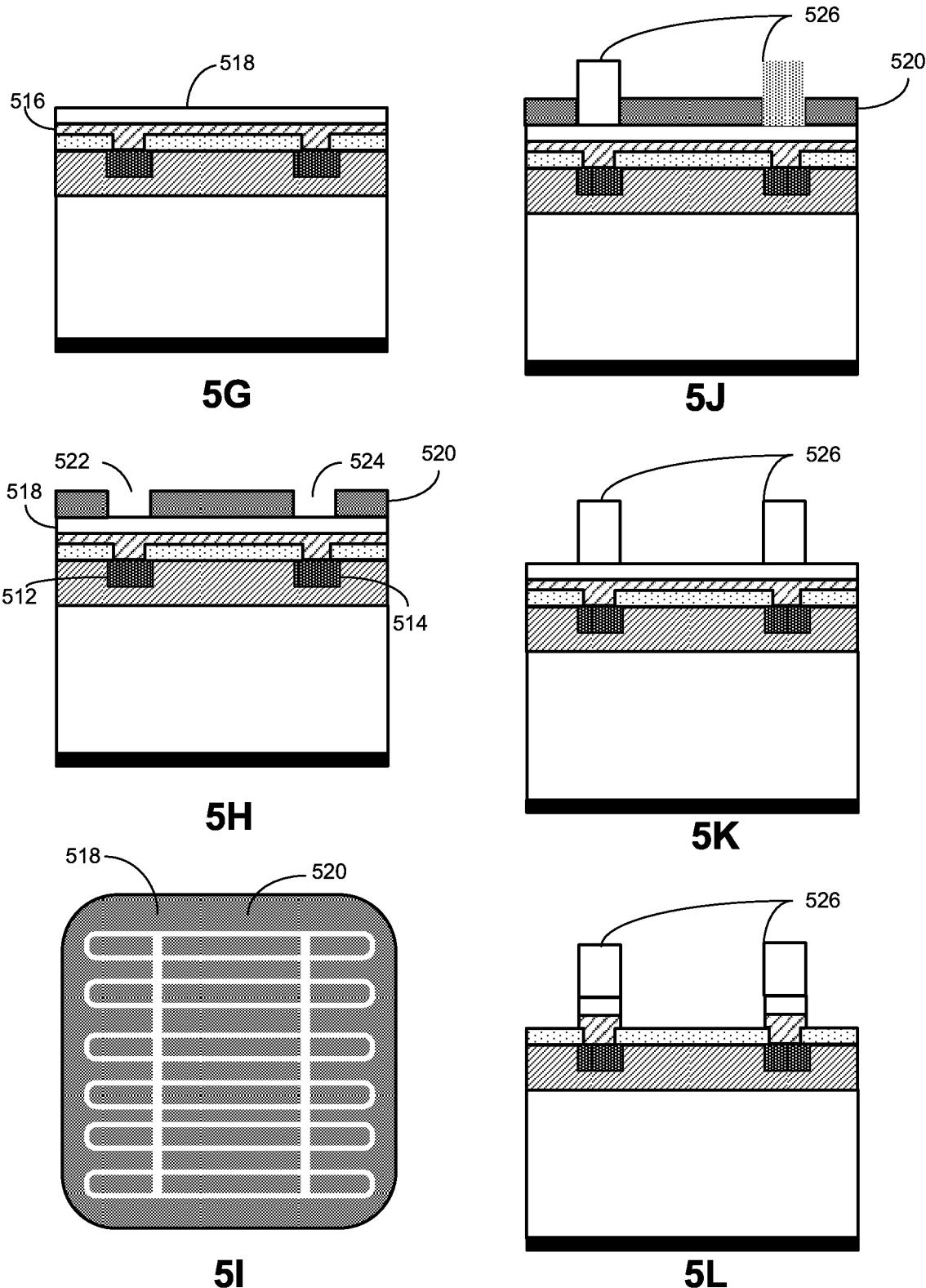
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**FIG. 4**

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**5A****5D****5B****5E****5C****5F****FIG. 5**

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**FIG. 5 (continued)**

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/063303

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L31/0224 H01L31/068 H01L31/0747
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/192932 A1 (WU MENG-HSIU [TW] ET AL) 2 August 2012 (2012-08-02)	1,2,6, 10,11
Y	paragraphs [0011] - [0014], [0023] paragraph [0037] - paragraph [0042]; figures 2a, 2b	4,5,7,8, 12-14, 16,17,
A	paragraph [0043] - paragraph [0044]; figures 3a,3b	21-23 9,18-20

X	US 2012/031480 A1 (TISLER ANTHONY C [US]) 9 February 2012 (2012-02-09)	1,3,6, 10,11
Y	paragraph [0011] - paragraph [0018]; figures 2-4	13,15

		-/-

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 December 2013	02/01/2014
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Hofmann, Kerrin

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/063303

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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E	-& EP 2 648 224 A1 (SANYO ELECTRIC CO [JP]) 9 October 2013 (2013-10-09) paragraph [0013] - paragraph [0030]; figures 1,2,5,6,7,8 -----	1-23
1		

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Information on patent family members

International application No
PCT/US2013/063303

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