(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 February 2002 (28.02.2002)

PCT

(10) International Publication Number
WO 02/17459 A1

(51) International Patent Classification[7]: H02H 7/085, 3/093

(21) International Application Number: PCT/IE01/00107

(22) International Filing Date: 23 August 2001 (23.08.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
S2000/0664 23 August 2000 (23.08.2000) IE

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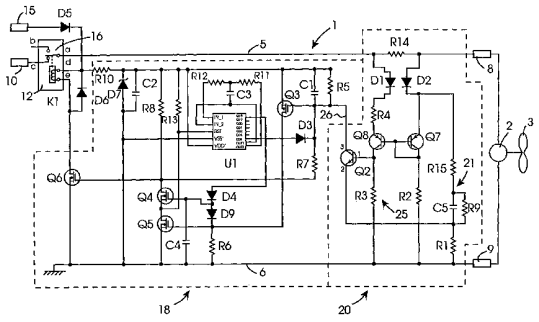
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) Title: A CONTROL CIRCUIT FOR CONTROLLING A POWER SUPPLY TO A MOTOR



(57) Abstract: A control circuit (1) for controlling a relay (12) for supplying power to a motor (2) and for switching off the relay (12) in the event of excessive power being drawn by the motor (2) comprises a reference circuit (21) which in turn comprises series connected first and second main reference resistors (R1, R15), the resistance of which is selected to be proportional to the resistance of the armature of the motor (2) and a secondary reference resistor (R9), the value of which is chosen so that the combined resistance of the first and second main reference resistors (R1, R15) and the secondary reference resistor (R9) is proportional to the normal steady-state running resistance of the motor (2) is connected in series with the main reference resistors (R1, R15) across the motor (2). A shunt resistor (R14) in a live rail (5) develops a voltage which is indicative of the current being drawn by the motor (2), and an amplifying circuit (25) amplifies the voltage across the shunt resistor (R14), and an amplified sample voltage is developed across a second scaling resistor (R3) in the amplifying circuit (25) which is proportional to the voltage developed across the shunt resistor (R14). A comparing transistor (Q2) compares the sample voltage across the resistor (R14). A comparing transistor (Q2) compares the sample voltage across the resistor (R1), and on the amplified sample voltage exceeding the reference voltage indicating excessive current being drawn by the motor (2) the comparing transistor (Q2) pulls a fourth MOSFET Q3 of a secondary switching circuit (18) which in turn switches off a first MOSFET (Q6) which in turn switches off the relay (12) for isolating the motor (2) from the power supply. A timer (U1) is provided in the secondary switching circuit (18) for timing a first time period during which the first MOSFET (Q6) is held switched on after the excessive current being drawn by the motor has been detected in case the excessive current was caused by a current spike.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

"A control circuit for controlling a power supply to a motor"

The present invention relates to a control circuit for controlling a power supply to an electrically powered motor, and in particular, to a control circuit for operating a main switch for controlling the power supply to the motor.

It is important that the power supply to an electrically powered motor should be controlled, and in many cases switched off in the event of excessive current being drawn by the motor. Otherwise, a motor may burn out, or the excessive current being drawn could cause fire or could result in other serious consequence. There are many reasons why an electrically powered motor may draw excessive power, for example, if the motor is overloaded, as a result of bearing wear in the motor or transmission which is being driven by the motor, and in more serious cases by the motor being stalled. This can be a particularly serious problem in the case of an electrically powered motor for driving a fan in a cooling system for a motor vehicle, for example, a motor which drives a fan for drawing cooling air across a heat exchanger for cooling the water of the vehicle engine cooling system. For various reasons, a fan may stall, thus causing excessive current to be drawn by the motor which would ultimately lead to burn out of the motor, or even more seriously could result in fire. Bearing wear in the fan or motor in general, also leads to excessive current being drawn by the motor. In general, electrical motors for driving a fan of a vehicle cooling system are DC brush motors which may be permanent magnet or field magnet motors. Such motors require a high start-up current which falls off exponentially to a steady-state running current. The start-up current can be as high as four times the normal steady-state running current. Additionally, the stall current can also be as high as four times the normal steady state running current.

It is therefore desirable that a control circuit for monitoring the current being drawn by an electrically powered motor should be provided. However, the provision of such a control circuit is difficult. Because of the relatively high start-up current which such motors draw by comparison to the normal steady-state current which is subsequently drawn, a control circuit set up to trip out a motor when the current being drawn

exceeds a normal steady-state current would trip out the motor on start-up, since the start-up current drawn by the motor would far exceed the normal steady-state current. On the other hand, a control circuit set to trip out the motor on the current being drawn exceeding the start-up current would allow the current being drawn by the motor during normal steady-state running of the motor to reach the start-up current before the motor would be tripped out. To allow a motor to run continuously for only a relatively short period of time drawing such a high start-up current, in general, would lead to burnout of the motor, and in many cases to more serious consequences, such as, fire in the circuitry supplying the motor. This is thus unacceptable. A further problem which such a control circuit would have to deal with is that in many cases wear in a motor, in general, is gradual, and thus, the steady-state current only increases as a result of wear over a relatively lengthy time period. In general, because of this it is difficult to detect excessive current draw resulting from gradual wear.

There is therefore a need for a control circuit which overcomes this problem.

The present invention is directed towards providing such a control circuit.

According to the invention there is provided a control circuit for operating a main switch means for controlling an electrical power supply to a motor, wherein the control circuit comprises a reference circuit powered through the main switch means for drawing a reference current proportional to the ideal current which would be drawn by the motor when operating unimpaired, and a comparing means for comparing a sample signal indicative of the actual current being drawn by the motor with a reference signal indicative of the reference current simultaneously being drawn by the reference circuit, and for outputting a trip signal for tripping out the main switch means in the event of the motor current being excessive.

In one embodiment of the invention the reference current drawn by the reference circuit is proportional to the ideal current which would be drawn by the motor when operating unimpaired during start-up of the motor and normal steady-state running

thereof.

In another embodiment of the invention the reference circuit comprises a main reference impedance means and a secondary reference impedance means, the impedance value of the main reference impedance means being selected to be proportional to the impedance of the armature of the motor, and the combined impedance values of the main and secondary reference impedance means being selected to be proportional to the steady-state impedance of the motor when operating unimpaired.

Preferably, the main and secondary reference impedance means are arranged so that the effect of the impedance of the secondary reference impedance means on the reference circuit is gradual when the reference circuit is initially powered up so that the reference current stimulates the ideal current drawn by the motor at start-up when unimpaired. Advantageously, a time constant inducing means is associated with the secondary reference impedance means for facilitating stimulation of the ideal start-up current of the motor.

In one embodiment of the invention the secondary impedance means comprises a secondary resistor, and the time constant inducing means comprises a capacitor connected in parallel with the secondary resistor for forming an RC timing circuit.

Preferably, the reference signal is derived from the main reference impedance means.

Advantageously, the main reference impedance means comprises respective first and second main reference impedance means connected in series.

Ideally, the reference signal is derived from the first main reference impedance means.

In one embodiment of the invention the first and second main reference impedance

means are provided by respective first and second main reference resistors.

In another embodiment of the invention the reference signal is a reference voltage signal developed across the first reference impedance means.

In a further embodiment of the invention the main and secondary reference impedance are connected in series across the motor.

In a further embodiment of the invention the sample signal is derived from a shunt impedance connected in the power supply to the motor. Preferably, the shunt impedance is connected in series with the motor. Advantageously, the sample signal is a sample voltage derived from a voltage signal developed across the shunt impedance.

In one embodiment of the invention an amplifying means is provided for amplifying the voltage signal developed across the shunt impedance for providing the sample signal. Preferably, the amplifying means comprises respective first and second scaling impedance means connected in series across the power supply to the motor and forming a potential divider. Advantageously, the first and second scaling impedance means are connected in series through a first bi-polar junction transistor, the first scaling impedance means being connected between the first transistor and the shunt impedance, and the second scaling means being connected between the first transistor and the motor.

In one embodiment of the invention a second bi-polar transistor connects a biasing impedance means across the power supply to the motor. Advantageously, the biasing impedance means is provided by a biasing resistor. Preferably, the biasing impedance means is connected between the second transistor and a terminal of the motor to which the second scaling impedance means is connected.

In one embodiment of the invention the bases of the respective first and second transistors are connected together, and the bases of the respective first and second

transistors are connected to the collector of the second transistor.

Advantageously, the sample signal is derived from the second scaling impedance means.

In one embodiment of the invention the first and second scaling impedance means are provided by respective first and second scaling resistors.

In a further embodiment of the invention the first scaling impedance means is of impedance values such that the voltage developed across the first scaling impedance means is substantially similar to the voltage developed across the shunt impedance.

In another embodiment of the invention the comparing means compares the sample signal developed across the second scaling impedance means with reference signal developed across the first main reference impedance means.

In one embodiment of the invention the comparing means comprises a comparing transistor, the base of the comparing transistor being connected to one of the power supply rails of the power supply to the motor through one of the first main reference impedance means and the second scaling impedance means, and the emitter or collector being connected to the rail of the power supply to which the base is connected, the said emitter or collector being connected to the said rail through the other of the first main reference impedance means and the second scaling impedance means, so that when the voltage of the sample signal is indicative of excessive current being drawn by the motor, the state of the comparing transistor changes from one of a conducting state and a non-conducting state to the other of the conducting state and the non-conducting state.

In another embodiment of the invention the base of the comparing transistor is connected to a ground rail of the power supply through the second scaling impedance means.

In a further embodiment of the invention the emitter of the comparing transistor is connected to the ground rail through the first main reference impedance means.

In a still further embodiment of the invention the comparing transistor is a bi-polar junction transistor.

Alternatively, the comparing means comprises a comparator for comparing the sample signal with the reference signal.

In another embodiment of the invention the comparator outputs a signal for tripping out the main switch means on the voltage of the sample signal crossing over the voltage of the reference signal.

In one embodiment of the invention the control circuit comprises an activating signal receiving terminal for receiving an activating signal for switching the main switch means for switching on the power supply to the motor, and a secondary switching circuit for switching the main switch means in response to the activating signal. Preferably, the secondary switching circuit is responsive to the comparing means detecting excessive current being drawn by the motor for switching the main switch means for switching off the power supply to the motor.

In one embodiment of the invention a timing means is provided for timing a first time period during which the secondary switching circuit holds the main switch means switched on for delivering the power supply to the motor during the first time period while the activating signal is present on the activating signal receiving terminal, the timing means being responsive to the comparing means detecting excessive current being drawn by the motor for commencing timing of the first time period. Advantageously, the secondary switching circuit is responsive to the timing means having timed out the first time period for switching the main switch means for switching off the power supply to the motor.

In one embodiment of the invention the first time period is in the range of 0.5 seconds to 3 seconds.

In another embodiment of the invention the first time period is in the range of 0.75 seconds to 2 seconds.

In a still further embodiment of the invention the first time period is approximately 1 second.

In one embodiment of the invention the timing means is responsive to the comparing means detecting excessive current being drawn by the motor for timing a second time period, the secondary switching circuit being responsive to the timing means for holding the main switch means off from the end of the first time period until the timing means has timed out the second time period in the event that the current being drawn by the motor at the end of the first time period is excessive.

In another embodiment of the invention the secondary switching circuit is responsive to the timing means having timed out the second time period for switching on the main switch means for supplying power to the motor in the event that the activating signal is still present on the activating signal receiving terminal.

In one embodiment of the invention the second time period lies in the range of 5 seconds to 300 seconds.

In another embodiment of the invention the second time period lies in the range of 10 seconds to 100 seconds.

In a further embodiment of the invention the second time period is approximately 30 seconds.

Preferably, the secondary switching circuit comprises a first secondary switch means through which a secondary power supply is fed to the main switch means for

switching the main switch means, the first secondary switch means being responsive to the presence of the activating signal on the activating signal receiving terminal for switching the secondary power supply to the main switch means, and the first secondary switch means being responsive to the comparing means detecting excessive current being drawn by the motor for switching off the secondary power supply to the main switch means. Advantageously, the first secondary switch means is responsive to the timing means.

In one embodiment of the invention the control circuit is adapted for controlling an electrical power supply to a DC brush motor.

The advantages of the invention are many. The main and most important advantage of the invention is that the motor is only tripped out when the current being drawn by the motor exceeds the ideal current which would be drawn if the motor were operating unimpaired irrespective of the operating state of the motor, in other words irrespective of whether the motor is operating at start-up or in steady-state. This is achieved by virtue of the fact that the reference circuit draws a current which at all times is proportional to an ideal current which would be drawn by the motor if the motor were operating unimpaired, even during the start-up period of the motor. The power supply to the motor is only isolated should the current being drawn by the motor exceed the ideal current which is proportional to the reference current. Thus, the control circuit according to the invention accommodates the relatively high start-up current which is initially drawn by the motor in the start-up period, and the steady-state current. Accordingly, there is no danger of the motor being tripped inadvertently during the start-up phase, as would otherwise happen if the control circuit were provided with a constant reference current. The fact that the reference current varies in proportion with the ideal current avoids this problem.

A further advantage of the invention is derived when the timing means is provided for timing the first time period during which the main switch means is held switched on for applying power to the motor. This, thus, accommodates momentary or temporary surges in the current being drawn by the motor such as current spikes as a result of

momentary or temporary glitches, which in general, would cause no damage to the motor or to the circuitry supplying power to the motor. However, if the excessive current being drawn by the motor is not the result of a momentary or temporary glitch, and the excessive current is still being drawn when the first time period has timed out, the main switch means is thus switched off, thus isolating the motor from the power supply. A further advantage of the invention is achieved by virtue of the fact that the timing means times the second time period during which the main switch means is held switched off and the motor is thus isolated from the power supply. The advantage of this is that at the end of the second time period the control circuit again operates normally, and if the activating signal is present, the control circuit again switches on the main switch means and in turn powers up the motor so that if the condition causing the excessive current being drawn by the motor has corrected itself, then the motor can operate normally. However, if the condition causing the excessive current to be drawn has not been corrected, then the control circuit operates as normal and thus commences to time the first time period, and at the end of the first time period switches off the main switch means, thus again powering down the motor.

A particularly important advantage of the invention is achieved by virtue of the fact that the reference circuit and the motor are both powered by the same power supply through the main switch means, and accordingly, the voltage applied to the reference circuit is always substantially similar to the voltage applied to the motor, and thus the current being drawn by the reference circuit should always be proportional to the ideal current which would be drawn by the motor if the motor were operating unimpaired.

The invention will be more clearly understood from the following description of some preferred embodiments thereof which are given by way of example only with reference to the accompanying drawings, in which:

Fig. 1 is a circuit diagram of a control circuit according to the invention for controlling an electrical power supply to a motor,

Fig. 2 is a curve illustrating the current being drawn by a reference circuit of the control circuit, and

Fig. 3 is a circuit diagram of a control circuit according to another embodiment of the invention for controlling an electrical power supply to a motor.

Referring to the drawings and initially to Figs. 1 and 2 there is illustrated a control circuit according to the invention indicated generally by the reference numeral 1 for controlling a power supply to an electrically powered motor 2 which drives a fan 3 of a motor vehicle cooling system (not shown). In this embodiment of the invention the motor is a DC brush motor having a high start-up current, which falls off exponentially to a substantially constant steady-state current. The start-up and stall currents of the motor 2 can typically be four times the normal steady-state running current. Such a motor vehicle cooling system typically comprises a heat exchanger, more commonly referred to as a radiator in which cooling water for the engine is cooled, and the fan 3 draws cooling air across the radiator (not shown) for cooling the cooling water. The power supply to the motor 2 is fed on a live rail 5 and a ground rail 6 through terminals 8 and 9, respectively. The power supply, which in this embodiment of the invention is a 12 volt power supply is applied to the live rail 5 on a main terminal 10 and through a main switch means, namely, a relay 12.

An activating signal receiving terminal 15 receives a high activating signal from, for example, a thermostat for switching the relay 12 for switching on the power supply to the motor 2 as will be described below. A relay coil K1 in the relay 12 operates a switch contact 16 for switching an output *a* of the relay 12 connected to the live rail 5 between inputs *b* and *c* of the relay 12. The input *c* is connected to the main terminal 10 so that when the switch contact 16 connects the output *a* to the input *c* power is supplied to the motor 2, while when the switch contact 16 connects the output *a* to the input *b* the motor 2 is isolated from the main terminal 10, and thus power to the motor 2 is switched off. The activating signal is applied through the activating signal receiving terminal 15 to one terminal, namely, the terminal *d* of the coil K1 of the

relay 12 through a diode D5. The other terminal *e* of the coil K1 is connected to the ground rail 6 through a first secondary switch means provided by a first N-channel MOSFET Q6 of a secondary switching circuit 18 of the control circuit 1. The secondary switching circuit 18 switches the first MOSFET Q6 for switching the relay 12 for switching off the power supply to the motor 2 in response to a detecting circuit 20 detecting an excessive current being drawn by the motor 2 when the activating signal is present on the terminal 15, as will be described below. A diode D6 discharges the coil K1 of the relay 12 when the first MOSFET Q6 is switched off for in turn switching off the relay 12, and in turn the power supply to the motor 2. Before describing the secondary switching circuit 18 in detail, the detecting circuit 20 will first be described.

The detecting circuit 20 comprises a shunt impedance means, namely, a shunt resistor R14 in the live rail 5 between the relay 12 and the terminal 8 of the motor 2. A voltage is developed across the shunt resistor R14 which is indicative of the current being drawn by the motor 2. The resistance value of the shunt resistor R14 is low, in this embodiment of the invention 0.002 ohms for minimising the voltage drop along the live rail 5.

An amplifying means provided by an amplifying circuit 25 for amplifying the voltage developed across the shunt resistor R14 comprises first and second scaling impedance means, namely, first and second scaling resistors R4 and R3, respectively, which are connected in series across the power supply to the motor 2 and the shunt resistor R14 through a first bi-polar junction transistor Q8. The first and second scaling resistors R4 and R3 act as a potential divider circuit which develops an amplified version of the voltage across the shunt resistor R14 across the second scaling resistor R3, which for convenience is referred to as the sample voltage signal. A biasing impedance means, namely, a biasing resistor R2 is connected across the power supply to the motor 2 through a second bi-polar junction transistor Q7 for maintaining the sample voltage developed across the second scaling resistor R3 proportional to the voltage developed across the shunt resistor R14. The respective bases of the first and second transistors Q8 and Q7,

respectively are connected together, and the base and collector of the second transistor Q7 are connected so that the second transistor Q7 effectively acts as a diode. The connection of the first and second transistors Q8 and Q7 causes the voltage which is developed across the first scaling resistor R4 to be similar to the sample voltage developed across the shunt resistor R14 plus any differences that might exist in the emitter-base voltages of the first and second transistors Q7 and Q8. By carefully selecting the value of the biasing resistor R2 the difference between the respective voltages developed across the first scaling resistor R4 and the shunt resistor R14 is minimised. In this way, the sample voltage developed across the second scaling resistor R3 is an accurate amplified representation of the voltage developed across the shunt resistor R14, and is proportional thereto, and is thus indicative of the current being drawn by the motor at any given time.

A reference circuit 21 which is powered by the power supply to the motor 2 is connected between the live rail 5 and the ground rail 6 across the motor 2 on the downstream side of the shunt resistor R14. The reference circuit 21 draws a current which is proportional to the ideal current which would be drawn by the motor 2 if the motor were operating unimpaired, in other words, if the motor were operating without any additional mechanical resistances, such as, for example, worn bearings in the motor or the fan transmission. In other words, the current drawn by the reference circuit 21 represents and is proportional to the ideal current which should be drawn by the motor 2 both during normal unimpaired start-up and normal unimpaired steady-state running. Curve A in Fig. 2 illustrates a plot of the reference current drawn by the reference circuit 21 plotted against time which flows through the reference circuit 21 immediately the relay 12 is switched on by an activating signal on the activating signal receiving terminal 15, and for so long as the relay 12 is held switched on by the activating signal on the activating signal receiving terminal 15. Initially, the current drawn by the reference circuit 21 is high at approximately 20 microamps, and falls off exponentially during the start-up period to reach a normal running steady-state value of approximately 6 microamps at the end of the start-up phase at approximately 0.8 seconds. In this way the current drawn by the reference circuit is proportional to and simulates the ideal current which would be drawn by the

motor 2.

The reference circuit 21 comprises a main reference impedance means, namely, first and second main reference resistors R1 and R15, respectively. The reference circuit 21 also comprises a secondary reference impedance means, namely, a secondary reference resistor R9. The first and second main reference resistors R1 and R15 are connected in series with the secondary reference resistor R9 between the live rail 5 and the ground rail 6 on the downstream side of the shunt resistor R14. The resistance values of the first and second main reference resistors R1 and R15, respectively, are selected so that the sum of the resistances of the resistors R1 and R2 is proportional to the armature resistance of the motor 2. The secondary reference resistor R9 is selected to have a resistance value which when summed with the resistance values of the first and second main reference resistors R1 and R15 is substantially proportional to the normal steady-state running resistance of the motor 2. A time constant inducing means, namely, a capacitor C5 is connected in parallel with the secondary reference resistor R9 to form with the resistor R9 an RC timing circuit, the time constant of which is similar to the normal start-up period of the motor. This, thus, causes the high start-up reference current to be drawn by the reference circuit 21 when powered up, and the reference current falls off exponentially to a normal steady-state reference current, thereby simulating the start-up and steady-state ideal current of the motor 2. The steady-state reference current I_{ref} drawn by the reference circuit is equal to:

$$I_{ref} = \frac{V}{R1 + R9 + R15}$$

where V is the voltage across the terminals 8 and 9. Thus, the reference current I_{ref} is proportional to the ideal steady-state current which would be drawn by the motor 2 if the motor 2 were operating unimpaired under normal steady-state conditions.

The values of the resistors R1, R9 and R15 and the capacitor C5 are selected to minimise the current drawn by the reference circuit 21, and although the current drawn through the reference circuit 21 is significantly less than the normal current

which is drawn by the motor 2, as discussed above the current drawn by the reference circuit 21 is proportional to the ideal current which would be drawn by the motor 2 if unimpaired, both during start-up and normal steady-state running.

In this embodiment of the invention the reference current drawn by the reference circuit 21 is monitored and detected by detecting the voltage developed across the first main reference resistor R1 which provides a reference voltage signal against which the sample voltage signal developed across the second scaling resistor R3 can be compared.

A comparing means which is provided by a comparing bi-polar junction transistor Q2 compares the sample voltage signal developed across the second scaling resistor R3 with the reference voltage signal developed across the first main reference resistor R1 for determining if the current drawn by the motor 2 is excessive. The sample voltage signal developed across the second scaling resistor R3 is applied to the base of the comparing transistor Q2, and the emitter of the comparing transistor Q2 is connected to ground through the first main reference resistor R1. Accordingly, when the current being drawn by the motor 2 becomes excessive at any time the sample voltage signal across the second scaling resistor R3 increases to a sufficient level to bias the comparing transistor Q2 into a conducting mode thereby pulling a line 26 from the collector of the comparing transistor Q2 low through the first reference resistor R1. The low on the line 26 acts as a trip signal for controlling the secondary switching circuit 18 for tripping the relay 12 as will be described below.

The reference circuit 21 and the amplifying circuit 25 are connected to the live rail 5 on respective opposite sides of the shunt resistor R14 through diodes D1 and D2, respectively. The diodes D1 and D2 act as a means to prevent damage to the control circuit in the event that a positive voltage is applied to the ground rail 6 relative to the chassis of the vehicle, in other words, in the event that the relay 12 is incorrectly wired. In which case, a path would exist back to the chassis via the low impedance winding of the motor 2 which would result in damage to the first and second transistors Q8 and Q7. Even in the case of correct wiring of the relay 12, the

diodes D1 and D2 still prevent damage to the first and second transistors Q8 and Q7. When the relay 12 is open the voltage at the resistor R1 relative to the chassis is negative due to the back EMF of the motor. This back EMF is of the same order as the battery voltage, and without the diodes D1 and D2 the maximum base emitter voltage of the first and second transistors Q8 and Q7, respectively, would be exceeded causing failure of the transistors Q8 and Q7.

Turning now to the secondary switching circuit 18, the activating signal from the terminal 15 is applied to the gate of the first MOSFET Q6 through resistors R10 and R8 for switching on the MOSFET Q6 for pulling the terminal *e* of the coil K1 of the relay 12 to ground for in turn switching the relay 12 for switching on the power supply to the motor 2. A pair of N-channel MOSFETS, namely, second and third MOSFETs Q4 and Q5 pull the gate of the first MOSFET Q6 to ground when switched on for switching off the first MOSFET Q6 for in turn switching the relay 12 for switching off the power supply to the motor 2 in the event of excessive current being detected by the detecting circuit 20. A fourth P-channel MOSFET Q3 the source of which is fed with the activating signal through the resistor R10, pulls the gate of the third MOSFET Q5 high for keeping the third MOSFET Q5 switched on. The gate of the third MOSFET Q5 is pulled low through a resistor R6. The gate of the second MOSFET Q4 is also pulled low through the resistor R6 and a diode D9.

A timing means comprising an integrated circuit counter U1 is powered by the activating signal through the resistor R10, and is provided for timing first and second time periods from the time an excessive current being drawn by the motor 2 is detected by the detecting circuit 20. During the first time period which is relatively short, in this embodiment of the invention one second approximately, the secondary switching circuit 18 is operated to hold the relay 12 switched on for so long as the activating signal is present on the terminal 15, in the event that the detected excessive current resulted from a current spike caused by a momentary glitch. During the second time period the secondary switching circuit 18 is operated to hold the relay switched off from the end of the first time period if at the end of the first time period the current being drawn by the motor is still excessive, irrespective of whether

the activating signal is present on the terminal 15 or not. In this embodiment of the invention the duration of the second time period is approximately 30 seconds. At the end of the second time period the secondary switching circuit 18 is again operated to switch on the relay 12 for powering the motor 2 if the activating signal is still on the terminal 15. A momentary glitch during the first time period could be caused, for example, by an unduly excessive current being drawn for a momentary period during the start-up, or as a result of a momentary stall of the fan during normal operation. Such momentary glitches would not in themselves lead to any problem with the motor or the circuitry, and thus could be accommodated. It is envisaged that excessive currents for longer periods of time could also be of a temporary nature, and thus, for this reason, at the end of the second time period the control circuit 1 is operated for again powering up the motor 2 in the event that the activating signal is still on the terminal 15 should the condition which caused the temporary excessive current have disappeared. It is, however, envisaged that the control circuit may be provided with further intelligence which if after a predetermined number of attempts to power up the motor at the end of respective second time periods the condition causing the excessive current still prevailed, that no further attempts would be made to power up the motor until the condition had been rectified.

The counter U1 remains inactive for so long as a reset pin RST of the counter U1 is held high. When the counter U1 is inactive an output pin Q18 is held low, thus holding the second MOSFET Q4 off and in turn the first MOSFET Q6 on. On a low being applied to the reset pin RST the counter U1 commences to count the first and second time periods. The activating signal on the terminal 15 is applied to the reset pin RST of the counter U1 through the resistor R10 and a resistor R13. The reset pin RST of the counter U1 is pulled to ground through the third MOSFET Q5 when the third MOSFET Q5 is switched on. The gate of the fourth MOSFET Q3 is pulled high by the activating signal on the terminal 15 through the resistor R10 and a resistor R5, and is pulled to ground, as discussed above, through the comparing transistor Q2 and the first main reference resistor R1 when the current drawn by the motor 2 is excessive. The value of the resistors R10 and R5 are appropriately selected so that when the comparing transistor Q2 is conducting due to excessive

current being drawn by the motor 2 the gate of the fourth MOSFET Q3 is pulled sufficiently low so that the fourth MOSFET Q3 conducts and applies the activating signal on the terminal 15 to the gate of the third MOSFET Q5 for switching on the third MOSFET Q5.

Accordingly, for so long as the third MOSFET Q5 remains switched off the reset pin RST of the counter U1 is pulled high by the activating signal on the terminal 15, and the counter remains inactive. However, on the gate of the fourth MOSFET Q3 being pulled low through the comparing transistor Q2 as a result of excessive current being drawn by the motor 2 the gate of the third MOSFET Q5 is pulled high through the fourth MOSFET Q3, thus switching on the third MOSFET Q5 and in turn pulling the reset pin RST of the counter U1 to ground. This causes the counter U1 to commence timing the first and second time periods. While the counter U1 is timing the first time period the output pin Q18 of the counter U1 is held low, thus allowing the gate of the second MOSFET Q4 to be pulled low through to diode D9 and the resistor R6. While the output pin Q18 remains low the second MOSFET Q4 is held off. Accordingly, for so long as the activating signal remains on the terminal 15 during the first time period the gate of the first MOSFET Q6 is held high and the first MOSFET Q6 remains on, thus holding the relay 12 on.

Additionally, during the first time period should the current drawn by the motor return to normal the comparing transistor Q2 is switched into the non-conducting state, and thus the gate of the fourth MOSFET Q3 is pulled high by the activating signal through the resistor R10 and the resistor R5. This, thus, switches off the fourth MOSFET Q3 which in turn switches off the third MOSFET Q5, thereby allowing the reset pin RST of the counter U1 to be pulled high by the activating signal through the resistors R10 and R13. This, thus, terminates the count of the first and second time periods and power continues to be supplied through the relay 12 for so long as the activating signal remains on the terminal 15 and the detecting circuit fails to detect an excessive current being drawn in the motor 2.

However, should the counter U1 time out the first time period the output pin Q18 of

the counter U1 goes high, thus pulling the gate of the second MOSFET Q4 high for in turn switching on the second MOSFET Q4. If the fourth MOSFET Q3 is still held on by the comparing transistor Q2 as a result of excessive current being drawn by the motor, the second and third MOSFETs Q4 and Q5 will thus be switched on, and the gate of the first MOSFET Q6 will be pulled to ground, thus switching off the first MOSFET Q6. This isolates the coil K1 of the relay 12 from ground thus switching the relay 12 for switching off the power supply to the motor 2. Once the power supply to the motor 2 is switched off the excessive current condition is no longer detected by the detecting circuit 20, and thus the comparing transistor Q2 goes into the non-conducting state. This would thereby allow the fourth MOSFET Q3 to switch off, which would in turn switch off the third MOSFET Q5, and the reset pin RST of the counter U1 would be pulled high by the activating signal, thus preventing the counter U1 from continuing to time the second time period. In order to retain the reset pin RST of the counter U1 low so that the counter U1 can continue to time the second time period, the gate of the fourth MOSFET Q3 is held low through a resistor R7 and the second and third MOSFETs Q4 and Q5. In this way the counter U1 is latched, and continues to count the second time period.

When the counter U1 has timed out the second time period an output pin Q24 of the counter Q1 goes high thereby pulling the gate of the fourth MOSFET Q3 high through a diode D3 which in turn switches off the fourth MOSFET Q3. With the fourth MOSFET Q3 switched off the gate of the third MOSFET Q5 is pulled low through the resistor R6 thereby switching off the third secondary MOSFET Q5. If the activating signal is still on the terminal 15 the reset pin RST of the counter U1 is thus pulled high again through the resistors R10 and R13, thus deactivating the counter U1, and allowing the output pin Q18 of the counter U1 to again go low, which in turn switches the second MOSFET Q4 off. Simultaneously, the gate of the first MOSFET Q6 is also pulled high by the activating signal on the terminal 15 through the resistors R10 and R8, and thus the first MOSFET Q6 is switched on thereby connecting the coil K1 of the relay 12 to ground. The coil K1 is thus powered by the activating signal for switching the relay 12 for switching the power on to the motor 2. The relay 12 remains in the on state for so long as the activating signal remains on the terminal

15 and the current drawn by the motor 2 remains normal.

The counter U1 is of the type whereby the output pin Q18 does not output a continuous high when it is high, rather it has a one second time period, and it cycles between a high and a low during each one second time period, remaining low for 0.5 seconds of each one second time period, and high for the remaining 0.5 seconds. A capacitor C4 between the gate of the second MOSFET Q4 and the ground rail 6 latches the gate of the second MOSFET Q4 high during each 0.5 second low transition of the output pin Q18. The diode D4 between the output pin Q18 and the gate of the second MOSFET Q4 prevents the gate of the second MOSFET Q4 being pulled low during the low transitions of the output pin Q18 during each one second time period. The resistor R6 and the diode D9 discharge the capacitor C4 on the output pin Q18 going continuously low.

Resistors R11 and R12 and a capacitor C3 are provided for setting the internal oscillator of the counter U1 to oscillate at a predetermined frequency for counting the first time period of one second and the second time period of thirty seconds.

A zener diode D7 latches the voltage applied to the counter U1, and a capacitor C2 smoothes the voltage against voltage fluctuations in the activating signal.

In use, on an activating signal being applied to the activating signal receiving terminal 15 the relay 12 is operated by the secondary switching circuit 18 to connect the output *a* to the input *c* for applying power from the terminal 10 to the live rail 5, and in turn to the motor 2, and the motor 2 is powered up. The current being drawn by the motor 2 develops a voltage across the shunt resistor R14 which is indicative of the current being drawn by the motor 2. The voltage across the shunt resistor R14 is amplified across the second scaling resistor R3 to form the sample voltage signal across the second scaling resistor R3. The sample voltage signal developed across the second scaling resistor R3 is compared with the reference voltage signal developed across the first main reference resistor R1 by the comparing transistor Q2, and for so long as the sample voltage signal developed across the second

scaling resistor R3 is below the reference voltage signal developed across the first main reference resistor R1 the comparing transistor Q2 remains switched off. In this state the gate of the fourth MOSFET Q3 is pulled high by the activating signal on the terminal 15 and the relay 12 is held switched on for powering the motor 2 for so long as the activating signal remains on the activating signal receiving terminal 15.

On the current being drawn by the motor 2 becoming excessive, in other words, when the sample voltage signal developed across the second scaling resistor R3 reaches a level to bias the base of the comparing transistor Q2 sufficiently for switching on the comparing transistor Q2, the comparing transistor Q2 commences to conduct, and thus the gate of the fourth MOSFET Q3 is pulled low through the line 26, the comparing transistor Q2 and the first main reference resistor R1. This, thus, causes the fourth MOSFET Q3 to conduct, thus applying a high derived from the activating signal on the terminal 15 to the third MOSFET Q5 which in turn pulls the reset pin RST of the counter U1 low, thus resetting the counter U1 to zero and commencing the counter U1 timing the first and second time periods. While the counter U1 is timing the first time period the output pin Q18 of the counter U1 is held low, thus holding the second MOSFET Q4 switched off, and the first MOSFET Q6 is held switched on by the activating signal on the terminal 15 through the resistors R10 and R8. On the counter U1 timing out the first time period, if the current being drawn by the motor 2 has returned to normal, the comparing transistor Q2 goes into a non-conducting state, thus allowing the gate of the fourth MOSFET Q3 to be pulled high by the activating signal, and the third MOSFET Q5 is thus switched off, allowing the reset pin RST of the counter U1 to be pulled high by the activating signal, and the counter U1 is deactivated and the control circuit 1 continues to hold the relay 12 switched on for powering the motor 2.

On the other hand, at the end of the first time period should the current being drawn by the motor 2 continue to be excessive, the sample voltage signal developed across the second scaling resistor R3 will still be sufficient for maintaining the comparing transistor Q2 switched on, thus holding the gate of the fourth MOSFET Q3 low and the fourth MOSFET Q3 conducting. In this state the third MOSFET Q5

continues to be held switched on, and the reset pin RST of the counter U1 is held low and timing. At the end of the first time period the output pin Q18 goes high, thus switching on the second MOSFET Q4 and pulling the gate of the first MOSFET Q6 to ground, and thus switching off the first MOSFET Q6, which in turn switches off the relay 12 and in turn the power supply to the motor 2 is switched off. At the end of the second time period the counter U1 outputs a high on the output pin Q24 which in turn switches off the fourth MOSFET Q3, and thus provided the activating signal 15 is still present on the activating signal receiving terminal 15 the control circuit 1 again switches on the relay 12 for powering up the motor 2, and so the operation of the control circuit 1 continues.

Referring now to Fig. 3 there is illustrated a control circuit according to another embodiment of the invention which is indicated generally by the reference numeral 30 for controlling a power supply to an electrically powered motor 2 which drives a fan 3, both of which are similar to the motor 2 and fan 3 of Fig. 1. The control circuit 30 is somewhat similar to the control circuit 1 and where relevant similar components are identified by the same reference numerals. In this embodiment of the invention the first MOSFET Q6 of the secondary switching circuit 18 is replaced by a first bi-polar junction transistor Q6. The secondary switching circuit 18 will be described in more detail below.

In this embodiment of the invention the reference circuit 21 comprises first and second main reference resistors R30 and R31, respectively, and a third main reference resistor R32. A secondary reference resistor R33 is provided in conjunction with a capacitor C30 which forms with the secondary resistor R33 the RC timing circuit. The first, second and third reference resistors R30, R31 and R32 are of resistance values such that the sum of their resistance values is proportional to the resistance value of the armature of the motor 2. The secondary reference resistor R33 is selected so that the combined resistance value of the first, second and third main reference resistors R31, R32 and R33 and the secondary reference resistor R33 is proportional to the steady-state resistance of the motor 2.

The detecting circuit 20 comprises the shunt resistor R14 which is located in the live rail 5. The amplifying circuit 25 in this embodiment of the invention comprises a first scaling resistor R36 and a second scaling resistor R37 which are connected in series across the motor 2 between the live and ground rails 5 and 6. A biasing resistor R35 connects the up-stream side of the shunt resistor R14 to the junction of the first and third main reference resistors R30 and R32. An amplifier U2B, one input pin 5 of which is connected between the biasing resistor R35 and the first main reference resistor R30, and the other input pin 6 of which is connected between the first and second scaling resistors R35 and R37 amplifies the sample voltage developed across the second scaling resistor R37. A resistor R38 connected between the input pin 6 and an output pin 7 of the amplifier U2B determines the gain of the amplifier U2B which in this embodiment of the invention is approximately ten. The resistance values of the first and second scaling resistors R36 and R37 are equal, and the resistance values of the biasing resistor R35 and the first main reference resistor R30 are equal so that the value of the sample voltage signal applied to the amplifier U2B is half the value of the voltage developed across the shunt resistor R14. Thus, the voltage appearing on the output pin 7 of the amplifier U2B is an amplified version of and directly proportional to the voltage developed across the shunt resistor R14, and is thus proportional to the current being drawn by the motor 2 at any given time.

The comparing means in this embodiment of the invention comprises a comparator U2A which compares the amplified sample voltage outputted on the output pin 7 of the amplifier U2B with the reference voltage, which in this embodiment of the invention is developed across the first and third main reference resistors R30 and R32. The amplified sample voltage is applied to an input pin 2 of the comparator U2A, while the reference voltage developed across the first and third main reference resistors R30 and R32 is applied to an input pin 3 of the comparator U2A. While the current drawn by the motor 2 remains normal the amplified sample voltage on the input pin 2 of the comparator U2A remains below the reference voltage on the input pin 3, and the output on an output pin 1 of the comparator U2A remains high. However, on the current being drawn by the motor 2 becoming excessive, the

amplified sample voltage on the input pin 2 of the comparator U2A exceeds the reference voltage on the input pin 3, and the output pin 1 of the comparator U2A goes low and remains low for so long as the amplified sample voltage exceeds the reference voltage.

A capacitor C6 between the input pin 3 of the comparator U2A and the ground rail 6 holds the reference voltage on the input pin 3 relatively steady against fluctuations in the power supply voltage.

Turning now to the secondary switching circuit 18, the secondary switching circuit 18 comprises three inverters U3A, U3B and U3D of a hex inverter U3. The inverters U3C, U3E and U3F of the hex inverter U3 are not required and thus not used in this embodiment of the invention. However, in order to prevent the outputs of the three unused inverters U3C, U3E and U3F wandering, the input pin 5 of the unused inverter U3C is connected to the output of the inverter U3B, while the input pins 11 and 13 of the unused inverters U3E and U3F are fed with the activating signal from the activating receiving terminal 15 through the resistor R10. The counter U1 is powered by the activating signal on the activating signal receiving terminal 15, and the voltage supplied to the counter U1 is clamped by the zener diode D7. Capacitors C39 and C40 smooth the voltage across the zener diode D7 against voltage fluctuations in the activating signal.

The first transistor Q6 is switched on when the signal applied to its base is high, and switched off when the signal applied to its base goes low. Input pins 1 and 3 of the inverters U3A and U3B are connected to the ground rail 6 through a capacitor C31 and a resistor R39. For so long as the capacitor C31 remains discharged the input pins 1 and 3 of the inverters U3A and U3B are held low, and thus, their respective output pins 2 and 4 are high. The high on the output pin 2 of the inverter U3A applies a high to the base of the first transistor Q6 through a resistor R40, thus maintaining the first transistor Q6 switched on. When switched on the first transistor Q6 holds the relay 12 switched on, thus supplying power to the motor 2. The high on the output pin 4 of the inverter U3B is applied to the reset pin RST of the counter

U1 through a resistor R41 which holds the counter U1 inactive.

The output pin 1 of the comparator U2A is connected to the reset pin RST of the counter U1 through a diode D30 and a resistor R42 so that on the output pin 1 of the comparator U2A going low as a result of excessive current being drawn by the motor 2, the reset pin RST of the timer U1 is pulled low, thus resetting the counter U1 to commence timing the first and second time periods. The output pin Q18 of the counter U1 is connected through a resistor R43 and a diode D31 to the input pins 1 and 3 of the respective inverters U3A and U3B. Thus, during the first time period while the output pin Q18 is held low the output pins 2 and 4 of the inverters U3A and U3B are held high, thus maintaining the first transistor Q6 switched on and the relay 12 also switched on and powering the motor 2. The values of the resistors R41 and R42 are chosen so that in this state the reset pin is held low by the comparator U2A. At the end of the first time period if the output of the comparator U2A is still low, the counter U1 continues to count into the second time period, and at the end of the first time period the output Q18 of the timer of the counter U1 goes high, thus applying a high to the inverters U3A and U3B, which in turn applies a low to the first transistor Q6 which switches off the first transistor Q6 and in turn the relay 12 for isolating the motor 2 from the power supply during the second time period. The function of the capacitor C31 and R39 is similar to that of the capacitor C4 and R6 in the control circuit 1 of Fig. 1 in that the capacitor C31 holds the input terminals 1 and 3 of the inverters U3A and U3B high during low transitions of the output pin Q18 during each one second period of the signal on the output pin Q18. The resistor R39 discharges the capacitor C31 on the signal on the output pin Q18 going continuously low. The diode D31 prevents the input pins 1 and 3 of the inverters U3A and U3B being pulled low during the low transitions of the output pin Q18 of the counter U1 while the output pin Q18 is in the high state.

The output pin Q24 of the counter U1 feeds an input pin 9 of the inverter U3D. An output pin 8 of the inverter U3D is connected to the input pins 1 and 3 of the inverters U3A and U3B through a diode D33. Thus, at the end of the second time period when the output pin Q24 of the counter U1 goes high, a high is applied to an

input pin 9 of the inverter U3D which pulls its output pin 8 low, thus pulling the input pins 1 and 3 of the inverters U3A and U3B low through the diode D33, which in turn apply a high to the first transistor Q6 and the reset pin RST of the counter U1, respectively. The high on the reset pin RST of the counter U1 deactivates the timer U1, and the high on the first transistor Q6 switches on the transistor Q6 and in turn the relay 12 for again powering up the motor 2, and the control circuit operates as already described holding the relay 12 switched on for so long as the activating signal remains on the activating signal receiving terminal until excessive current being drawn by the motor is detected.

If during the first time period the current being drawn by the motor 2 returns to normal, the output of the comparator U2A goes high, thus allowing the reset pin RST of the counter U1 to go high and deactivating the counter U1, and the counter U1 ceases to time the first and second time periods. The transistor Q6 remains switched on, thus holding the relay 12 switched on also.

During the second time period once the relay 12 has been switched off, the excessive power condition no longer remains on the motor 2, and thus the output pin 1 of the comparator U2A goes high. However, the output pin 4 of the inverter U3B is held low by the high output on the output pin Q18 of the counter U1 which in turn holds the reset pin RST of the counter U1 low to allow the counter U1 to continue to time the second time period.

As in the case of the control circuit 1, the resistors R11 and R12 and the capacitor C3 set the frequency of the internal clock generator of the counter U1. A zener diode D37 clamps the voltage on a power supply pin USS of the counter U1 and a capacitor C38 smoothes the voltage against fluctuations in the supply voltage.

A zener diode D39 protects the first transistor Q6 from the back emf produced by the relay coil K1 when the relay coil K1 is denergised, and also discharges the coil K1 when denergised. A metal oxide varistor 39 acts as a suppresser for suppressing transients from the activating signal 15, and protects the control circuit, and prevents

the relay coil from becoming energised through the zener diode D39 when high voltage transients are present in the activating signal on the terminal 15. These transients could also cause excessive dissipation in resistors R10 and R50, and diode D7 and would probably cause eventual failure of these components.

The resistors R35 and R36 in this embodiment of the invention also serve to prevent damage to the circuit in the event that a positive voltage is applied to the negative rail 6 of the control circuit 30 relative to the chassis. Incorrect wiring of the relay 12 could result in a positive voltage being produced on the ground rail 6, and a path would exist back to the chassis via the low impedance winding of the motor 2 resulting in damage to the amplifier U2B. The resistors R35 and R36 limit the current between the amplifier U2B, and this connection to provide protection for such a situation.

While the control circuits have been described for controlling a switch means provided by a relay, it will be appreciated that the control circuit may be provided for controlling any switch means, whether a relay, a solid state switch means or any other switch means.

While the first and second predetermined time periods have been described as being one second and thirty seconds, respectively, the first and second time periods may be of any suitable or desired value.

Additionally, it will be appreciated that while the control circuits have been described for switching a twelve volt power supply to a fan motor, it will be appreciated that the control circuit may be used for switching a power supply of any other voltage to any other type of motor.

While the control circuits has been described for controlling a power supply to a DC brush motor, it is envisaged that the control circuit may be used for controlling the power supply to other motors, and where the control circuit is used for controlling the power supply to a DC brush motor, the DC brush motor may be a permanent magnet

or a field magnet motor.

Claims

1. A control circuit for operating a main switch means (12) for controlling an electrical power supply to a motor (2), characterised in that the control circuit (1) comprises a reference circuit (21) powered through the main switch means (12) for drawing a reference current proportional to the ideal current which would be drawn by the motor (2) when operating unimpaired, and a comparing means (Q2,U2A) for comparing a sample signal indicative of the actual current being drawn by the motor (2) with a reference signal indicative of the reference current simultaneously being drawn by the reference circuit (21), and for outputting a trip signal for tripping out the main switch means (12) in the event of the motor current being excessive.

2. A control circuit as claimed in Claim 1 characterised in that the reference current drawn by the reference circuit (21) is proportional to the ideal current which would be drawn by the motor (2) when operating unimpaired during start-up of the motor and normal steady-state running thereof.

3. A control circuit as claimed in Claim 1 or 2 characterised in that the reference circuit (21) comprises a main reference impedance means (R1, R15, R30, R31, R32) and a secondary reference impedance means (R9, R33), the impedance value of the main reference impedance means (R1, R15, R30, R31, R32) being selected to be proportional to the impedance of the armature of the motor (2), and the combined impedance values of the main and secondary reference impedance means (R1, R15, R30, R31, R32, R9, R33) being selected to be proportional to the steady-state impedance of the motor (2) when operating unimpaired.

4. A control circuit as claimed in Claim 2 characterised in that the main and secondary reference impedance means (R1, R15, R30, R31, R32, R9, R33) are arranged so that the effect of the impedance of the secondary reference impedance means (R9, R33) on the reference circuit (21) is gradual when the reference circuit (21) is initially powered up so that the reference current simulates the ideal current drawn by the motor (2) at start-up when unimpaired.

5. A control circuit as claimed in Claim 3 or 4 characterised in that a time constant inducing means (C5, C30) is associated with the secondary reference impedance means (C5, C30) for facilitating simulation of the ideal start-up current of the motor (2).

6. A control circuit as claimed in Claim 5 characterised in that the secondary impedance means (R9, R33) comprises a secondary resistor (R9, R33), and the time constant inducing means (C5, C30) comprises a capacitor (C5, C30) connected in parallel with the secondary resistor (R9, R33) for forming an RC timing circuit.

7. A control circuit as claimed in any of Claims 3 to 6 characterised in that the reference signal is derived from the main reference impedance means (R1, R30, R32).

8. A control circuit as claimed in any of Claims 3 to 7 characterised in that the main reference impedance means (R1, R15, R30, R31, R32) comprises respective first and second main reference impedance means (R1, R15, R31, R32) connected in series.

9. A control circuit as claimed in Claim 8 characterised in that the reference signal is derived from the first main reference impedance means (R1, R30,32).

10. A control circuit as claimed in Claim 8 or 9 characterised in that the first and second main reference impedance means (R1, R15, R30, R32) are provided by respective first and second main reference resistors (R1, R15, R30, R32).

11. A control circuit as claimed in any of Claims 3 to 10 characterised in that the reference signal is a reference voltage signal developed across the first reference impedance means (R1, R30, R32).

12. A control circuit as claimed in any of Claims 3 to 11 characterised in that the main and secondary reference impedance (R1, R15, R30, R31, R32, R9, R33) are

connected in series across the motor (2).

13. A control circuit as claimed in any preceding claim characterised in that the sample signal is derived from a shunt impedance (R14) connected in the power supply to the motor (2).

14. A control circuit as claimed in Claim 13 characterised in that the shunt impedance (R14) is connected in series with the motor (2).

15. A control circuit as claimed in Claim 13 or 14 characterised in that the sample signal is a sample voltage derived from a voltage signal developed across the shunt impedance (R14).

16. A control circuit as claimed in Claim 15 characterised in that an amplifying means (R15) is provided for amplifying the voltage signal developed across the shunt impedance (R14) for providing the sample signal.

17. A control circuit as claimed in Claim 16 characterised in that the amplifying means (25) comprises respective first and second scaling impedance means (R4, R3, R36, R37) connected in series across the power supply to the motor (2) and forming a potential divider.

18. A control circuit as claimed in Claim 17 characterised in that the first and second scaling impedance means (R4, R3) are connected in series through a first bi-polar junction transistor (Q8), the first scaling impedance means (R4) being connected between the first transistor (Q8) and the shunt impedance (R4), and the second scaling means (R3) being connected between the first transistor (Q8) and the motor (2).

19. A control circuit as claimed in Claim 18 characterised in that a second bi-polar transistor (Q7) connects a biasing impedance means (R2) across the power supply to the motor (2).

20. A control circuit as claimed in Claim 19 characterised in that the biasing impedance means (R2) is provided by a biasing resistor (R2).

21. A control circuit as claimed in Claim 19 or 20 characterised in that the biasing impedance means (R2) is connected between the second transistor (Q7) and a terminal of the motor (2) to which the second scaling impedance means (R3) is connected.

22. A control circuit as claimed in any of Claims 19 to 21 characterised in that the bases of the respective first and second transistors (Q8, Q7) are connected together, and the bases of the respective first and second transistors (Q8, Q7) are connected to the collector of the second transistor (Q7).

23. A control circuit as claimed in any of Claims 17 to 22 characterised in that the sample signal is derived from the second scaling impedance means (R3, R37).

24. A control circuit as claimed in any of Claims 17 to 23 characterised in that the first and second scaling impedance means (R4, R3, R36, R37) are provided by respective first and second scaling resistors (R4, R3, R36, R37).

25. A control circuit as claimed in any of Claims 17 to 24 characterised in that the first scaling impedance means (R4, R36) is of impedance values such that the voltage developed across the first scaling impedance means (R4, R36) is substantially similar to the voltage developed across the shunt impedance (R14).

26. A control circuit as claimed in any of Claims 17 to 25 characterised in that the comparing means compares the sample signal developed across the second scaling impedance means (R3, R37) with reference signal developed across the first main reference impedance means (R1, R30, R32).

27. A control circuit as claimed in any of Claims 17 to 26 characterised in that the

comparing means (Q2, V2A) comprises a comparing transistor (Q2), the base of the comparing transistor being connected to one of the power supply rails (6) of the power supply to the motor (2) through one of the first main reference impedance means (R1) and the second scaling impedance means (R3), and the emitter or collector being connected to the rail (6) of the power supply to which the base is connected, the said emitter or collector being connected to the said rail (6) through the other of the first main reference impedance means (R1) and the second scaling impedance means (R3), so that when the voltage of the sample signal is indicative of excessive current being drawn by the motor (2), the state of the comparing transistor (Q2) changes from one of a conducting state and a non-conducting state to the other of the conducting state and the non-conducting state.

28. A control circuit as claimed in Claim 27 characterised in that the base of the comparing transistor (Q2) is connected to a ground rail (6) of the power supply through the second scaling impedance means (R3).

29. A control circuit as claimed in Claim 27 or 28 characterised in that the emitter of the comparing transistor (Q2) is connected to the ground rail (6) through the first main reference impedance means (R1).

30. A control circuit as claimed in any of Claims 27 to 29 characterised in that the comparing transistor (Q2) is a bi-polar junction transistor (Q2).

31. A control circuit as claimed in any of Claims 1 to 17 characterised in that the comparing means (Q2, U2A) comprises a comparator (U2A) for comparing the sample signal with the reference signal.

32. A control circuit as claimed in Claim 31 characterised in that the comparator (U2A) outputs a signal for tripping out the main switch means (12) on the voltage of the sample signal crossing over the voltage of the reference signal.

33. A control circuit as claimed in any preceding claim characterised in that the

control circuit (1) comprises an activating signal receiving terminal (15) for receiving an activating signal for switching the main switch means (12) for switching on the power supply to the motor (2), and a secondary switching circuit (18) for switching the main switch means (12) in response to the activating signal.

34. A control circuit as claimed in Claim 33 characterised in that the secondary switching circuit (18) is responsive to the comparing means detecting excessive current being drawn by the motor (2) for switching the main switch means (12) for switching off the power supply to the motor (2).

35. A control circuit as claimed in Claim 33 or 34 characterised in that a timing means (U1) is provided for timing a first time period during which the secondary switching circuit (18) holds the main switch means (12) switched on for delivering the power supply to the motor (2) during the first time period while the activating signal is present on the activating signal receiving terminal (15), the timing means being responsive to the comparing means (Q2, U2A) detecting excessive current being drawn by the motor (2) for commencing timing of the first time period.

36. A control circuit as claimed in Claim 35 characterised in that the secondary switching circuit (18) is responsive to the timing means (U1) having timed out the first time period for switching the main switch means (12) for switching off the power supply to the motor (2).

37. A control circuit as claimed in Claim 35 or 36 characterised in that the first time period is in the range of 0.5 seconds to 3 seconds.

38. A control circuit as claimed in any of Claims 35 to 37 characterised in that the first time period is in the range of 0.75 seconds to 2 seconds.

39. A control circuit as claimed in any of Claims 35 to 38 characterised in that the first time period is approximately 1 second.

40. A control circuit as claimed in any of Claims 35 to 39 characterised in that the timing means (U1) is responsive to the comparing means (Q2, U2A) detecting excessive current being drawn by the motor (2) for timing a second time period, the secondary switching circuit (18) being responsive to the timing means (U1) for holding the main switch means (12) off from the end of the first time period until the timing means (U1) has timed out the second time period in the event that the current being drawn by the motor (2) at the end of the first time period is excessive.

41. A control circuit as claimed in Claim 40 characterised in that the secondary switching circuit (18) is responsive to the timing means (U1) having timed out the second time period for switching on the main switch means (12) for supplying power to the motor (2) in the event that the activating signal is still present on the activating signal receiving terminal (15).

42. A control circuit as claimed in Claim 40 or 41 characterised in that the second time period lies in the range of 5 seconds to 300 seconds.

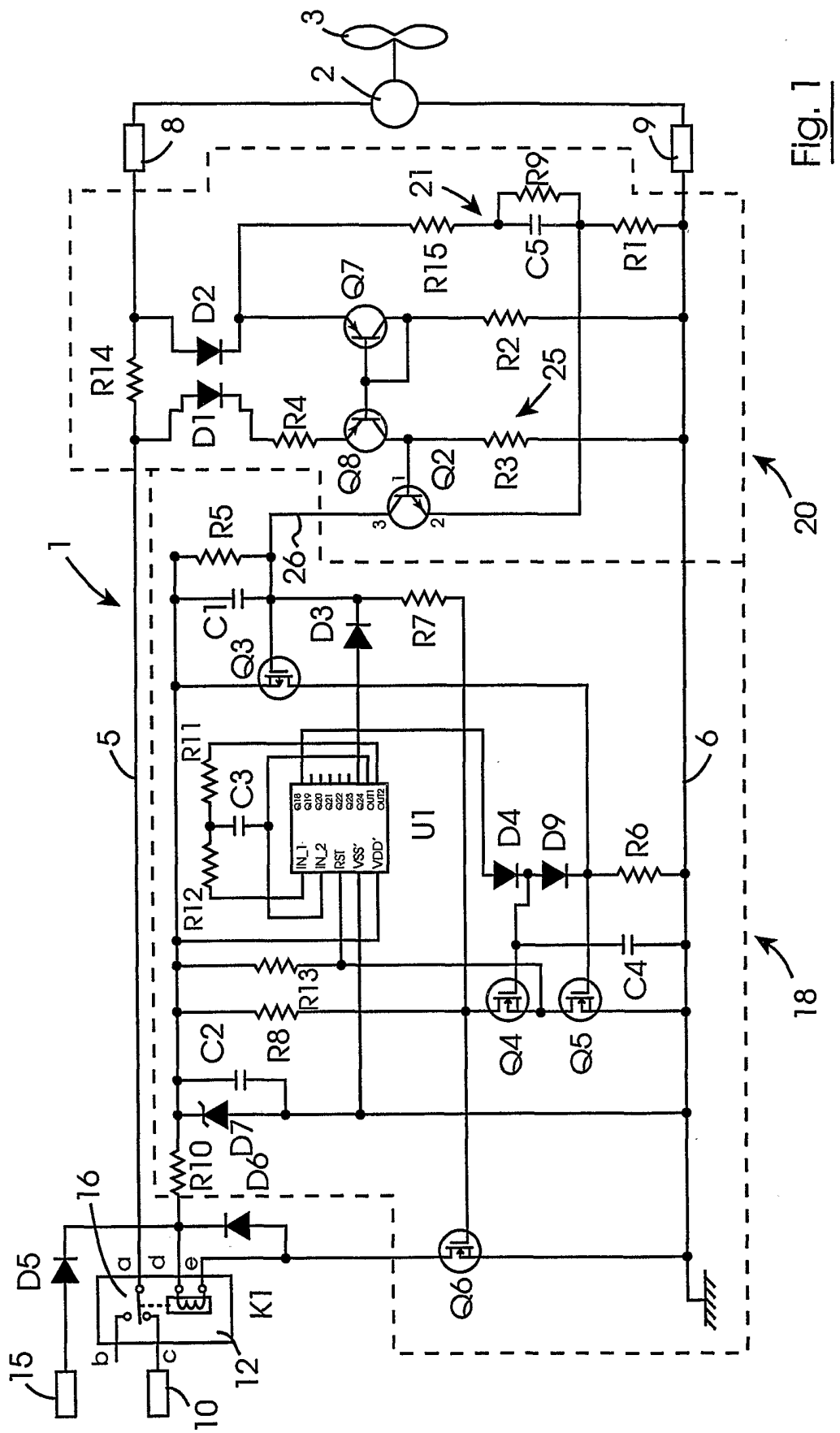
43. A control circuit as claimed in any of Claims 40 to 42 characterised in that the second time period lies in the range of 10 seconds to 100 seconds.

44. A control circuit as claimed in any of Claims 40 to 43 characterised in that the second time period is approximately 30 seconds.

45. A control circuit as claimed in any of Claims 35 to 44 characterised in that the secondary switching circuit (18) comprises a first secondary switch means (Q6) through which a secondary power supply is fed to the main switch means (12) for switching the main switch means (12), the first secondary switch means (Q6) being responsive to the presence of the activating signal on the activating signal receiving terminal (15) for switching the secondary power supply to the main switch means (12), and the first secondary switch means (Q6) being responsive to the comparing means (Q2, U2A) detecting excessive current being drawn by the motor (2) for switching off the secondary power supply to the main switch means (12).

46. A control circuit as claimed in any of Claims 35 to 45 characterised in that the first secondary switch means (Q6) is responsive to the timing means (U1).

47. A control circuit as claimed in any preceding claim characterised in that the control circuit (1) is adapted for controlling an electrical power supply to a SC brush motor (2).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R3
R5
26
C1
D3
R7
Q3
1
5
6
R11
C3
U1
D4
D9
R6
R12
C4
R13
Q4
Q5
C2
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Q6
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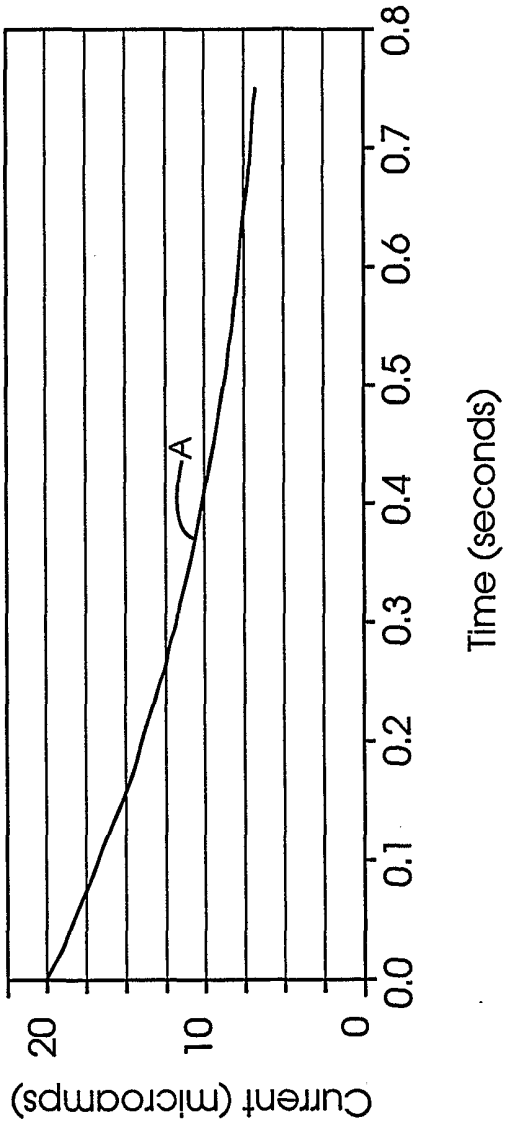
20
18

Fig. 1

Fig. 2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Time (seconds)
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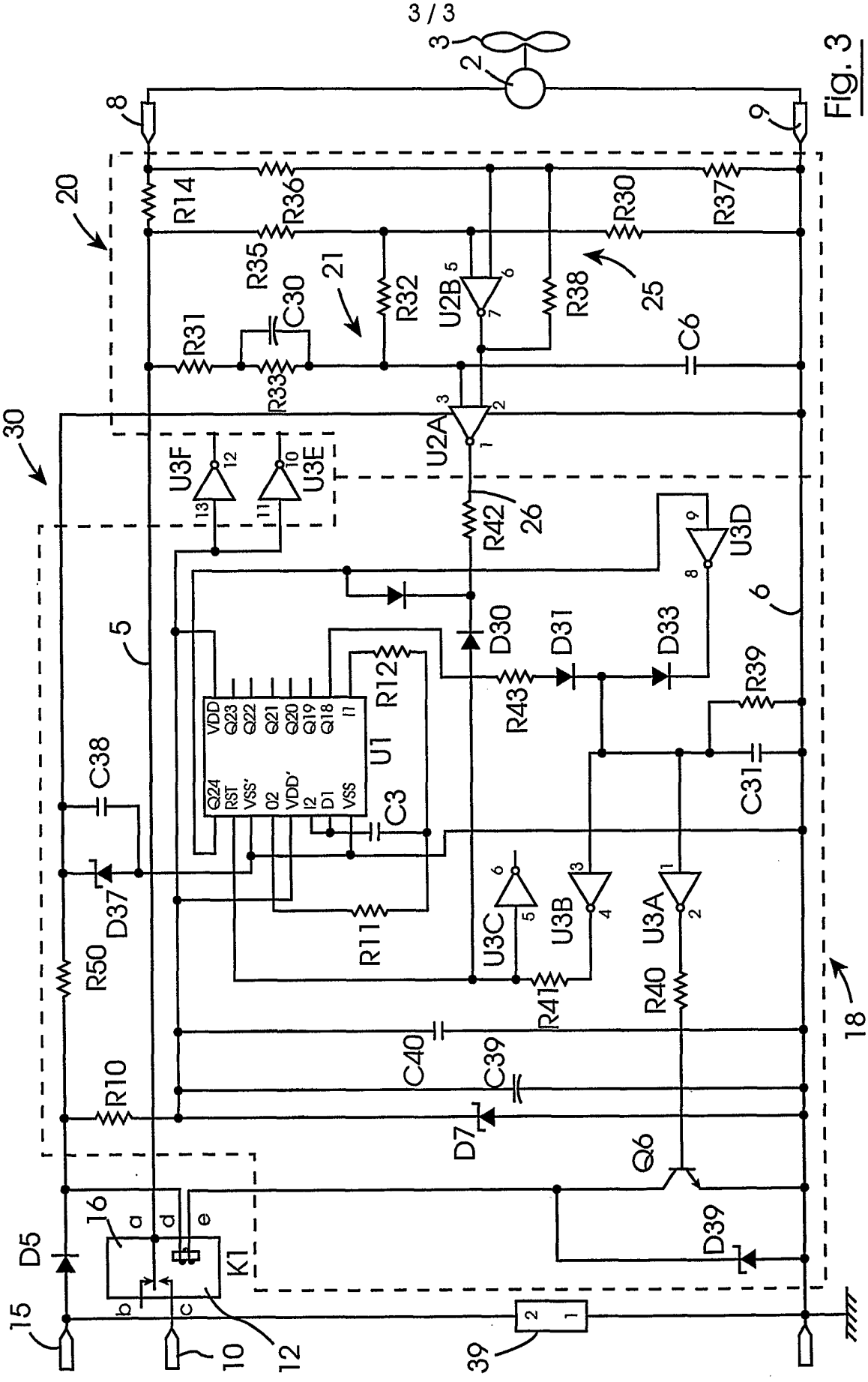
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R14
R36
R30
R37
R35
C30
21
R32
U2B
R38
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R31
C6
R33
U2A
30
U3F
U3E
R42
26
U3D
5
D30
D31
D33
6
R12
R43
R39
U1
C3
C38
C31
D37
R50
U3C
U3B
U3A
R11
R41
R40
18
C40
C39
R10
D7
Q6
D39
16
a
d
e
K1
D5
15
b
c
10
12
39

Fig. 3

INTERNATIONAL SEARCH REPORT

Int[illegible]nal Application No
PCT/IE 01/00107

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H02H7/085 H02H3/093

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H02H H02P

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 845 354 A (BOOTHMAN ET AL.) 29 October 1974 (1974-10-29)	1-6
A	column 2, line 27-40 column 3, line 4 -column 5, line 32; figures 1-3	31,32

X	US 3 609 461 A (ROBERT E. OBENHAUS) 28 September 1971 (1971-09-28) column 1, line 4-33	1-6
A	column 1, line 63 -column 2, line 20 column 2, line 51 -column 4, line 14; figures 1,2	31-36

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
23 November 2001	03/12/2001

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/IE 01/00107

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	page 1, line 55 -page 2, line 4 page 2, line 31 -page 3, line 40 page 3, line 95 -page 4, line 106; figures 1-3	4,5,31, 32
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INTERNATIONAL SEARCH REPORT

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