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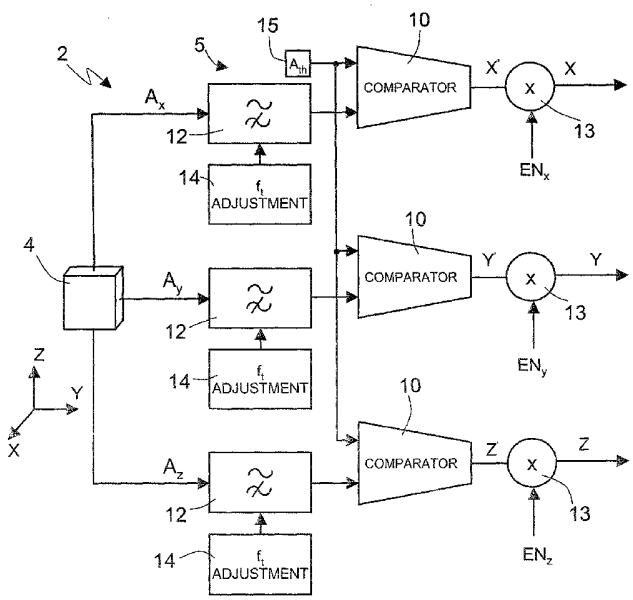
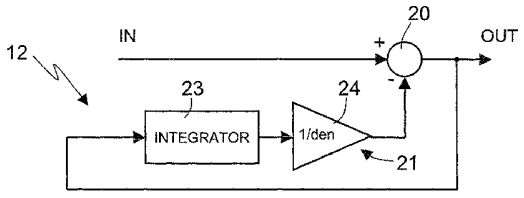
(54) Title: DIGITAL HIGH-PASS FILTER FOR A DISPLACEMENT DETECTION DEVICE OF A PORTABLE APPARATUS





(57) Abstract: A digital high-pass filter (12) has an input (IN), an output (OUT), and a subtractor stage (20), having a first input terminal, a second input terminal and an output terminal. The first input terminal of the subtractor stage (20) is connected to the input (IN) of the digital high-pass filter (12) and the output terminal is connected to the output (OUT) of the digital high-pass filter (12). A recursive circuit branch (21) is connected between the output (OUT) of the digital high-pass filter (12) and the second input terminal of the subtractor stage (20). Within the recursive circuit branch (21) are cascaded an accumulation stage (23), constituted by an integrator circuit, and a divider stage (24). The cutoff frequency (f_t) of the digital high-pass filter (12) is variable according to a dividing factor (den) of the divider stage (24).

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DIGITAL HIGH-PASS FILTER FOR A DISPLACEMENT DETECTION DEVICE OF A PORTABLE APPARATUS

TECHNICAL FIELD

The present invention relates to a digital high-pass filter, in particular for use in a displacement detection device for detecting displacements of a portable apparatus, to which the following description will make explicit reference, without this implying any loss of generality.

BACKGROUND ART

As is known, in the last few years, with the increasing use of portable apparatuses (such as laptops, PDAs - Personal Data Assistants, digital audio players, mobile phones, digital cameras, and the like), a need has grown for simplifying the use of said apparatuses and in particular their user interface. In this regard, of particular interest has proven the possibility of activating given functions or programs in the portable apparatuses with a simple movement made by the user. Consider, for example, navigation within a list of options or the phone book of a mobile phone by simply tilting it or moving it in the direction in which the list or the phone book is to be scrolled, or the possibility of adapting the display of an image on a PDA by simply modifying its inclination.

In some portable apparatuses, the introduction of displacement detection devices has thus been proposed which enable the activation of functions or programs following upon the detection of a movement imparted by the user.

The displacement detection devices of a known type generally comprise acceleration sensors, which detect the acceleration acting on the corresponding portable apparatus along one or more detection directions, and generate corresponding electrical signals. An appropriate processing circuit

connected to the acceleration sensors processes the acceleration signals thus generated, and in particular compares them with pre-set acceleration thresholds. In particular, exceeding of one of the acceleration thresholds indicates that the portable apparatus has undergone a displacement in a corresponding direction.

However, due to the acceleration of gravity, the acceleration sensors have a non-zero output also in the absence of an acceleration exerted on the portable apparatus by the user. Furthermore, the acceleration signals generated on account of the sole acceleration of gravity have different values according to the resting position of the portable apparatus, in so far as the components of the acceleration of gravity along the detection directions are each time different. Consequently, the exceeding of the acceleration thresholds by the acceleration signals, in the presence of an acceleration exerted on the portable apparatus, is dependent upon the initial position (and in particular upon the orientation) of the portable apparatus. This leads to disparity of operation according to the initial resting position of the portable apparatus chosen by the user, a position that varies, for example, between right-handed users and left-handed users, and in any case according to the preference of the various users.

To solve the above problem, in the Italian patent application No. TO2004A000847, filed in the name of the present applicant on December 1, 2004, the use of a high-pass filter was proposed, said high-pass filter being arranged between the acceleration sensors and the corresponding processing circuit. The high-pass filter eliminates the continuous component of the acceleration signals linked to the acceleration of gravity so as to render the displacement detection independent of the initial position of the portable apparatus.

As is known, numerical high-pass filters are generally made

with FIR (Finite Impulse Response) or IIR (Infinite Impulse Response) structures. In order to effectively reduce the continuous component of the acceleration signals, without, however, altering the frequency components indicative of the displacements to be detected (frequency components that can be low-frequency ones in the case of slow movements or high-frequency ones in the case of fast movements), the high-pass filters must have a long time constant, for example longer than 100 ms, and a high order. Since the FIR or IIR filters envisage the repetition of one and the same circuit structure a number of times equal to the order of the filter, and the storage of a number of constants once again equal to the order of the filter, these characteristics lead to a considerable circuit complexity and consequently a high use of resources. In particular, in the case of hardware implementation via an ASIC (Application Specific Integrated Circuit) the silicon area occupation and the memory occupation can be excessive beyond a certain order of the filter (mainly in the case of portable applications). Instead, in case of software implementation via a firmware, stored for example in a microcontroller or in a DSP (Digital Signal Processor), it is necessary to choose very costly components and to use all or a large part of the resources of the system just for the filter implementation.

In addition, in numerical filters of a conventional type it is not easy to vary the cutoff frequency, a possibility that is, instead, extremely useful in the described application for the detection of displacements of portable apparatuses. In fact, to detect slow movements made by the user, it is preferable to select a cutoff frequency that is sufficiently low, such that the low-frequency components of the corresponding acceleration signals will have an amplitude sufficient to be detected. Instead, it is preferable to select a higher cutoff frequency if the movements of the user are faster so as to cut off the low-frequency components and in any case to accurately detect

the signal components linked to the movements made by the user.

DISCLOSURE OF INVENTION

The aim of the present invention is consequently to provide a digital high-pass filter that will enable the problems and the disadvantages referred to above to be overcome, and in particular will have high time constants, will be readily configurable, and at the same time will lead to a reduced use of resources.

According to the present invention, a digital high-pass filter is provided, as defined in Claim 1.

According to the present invention a displacement detection device is moreover provided, as defined in Claim 10.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, preferred embodiments thereof are now described, purely by way of non-limiting examples and with reference to the attached drawings, wherein:

- Figure 1 shows a block diagram of a portable apparatus incorporating a displacement detection device according to one embodiment of the present invention;
- Figure 2 shows a circuit block diagram of a processing circuit of the displacement detection device of Figure 1;
- Figure 3 shows a possible circuit embodiment of a digital high-pass filter in the processing circuit of Figure 2;
- Figure 4 shows the time response of the digital high-pass filter in the presence of a square-wave input signal;
- Figure 5 shows a possible circuit embodiment of an integrator block of the digital high-pass filter of Figure 3;
- Figure 6 shows an alternative circuit embodiment of the integrator block of the digital high-pass filter of Figure 3;
- Figures 7a-7b and 8a-8b show diagrams of the magnitude and

phase response of the digital high-pass filter, for two different values of a variable dividing factor; and

- Figure 9 shows a block diagram of a portable apparatus incorporating a displacement detection device, according to a further embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Figure 1 is a schematic illustration of a portable apparatus 1 equipped with a displacement detection device 2 and a microprocessor 3, connected to the displacement detection device 2 and configured to control the general operation of the portable apparatus 1. The displacement detection device 2 comprises an accelerometer 4 of a linear type, and a processing circuit 5, connected to the accelerometer 4. In particular, the processing circuit 5 is made in an ASIC and is integrated together with the accelerometer 4 within a single chip 6 of semiconductor material, preferably silicon.

The accelerometer 4 is of a known type, in particular is constituted by a MEMS (Micro-Electro-Mechanical System) device made using semiconductor technology, has three detection axes x, y and z, and generates three acceleration signals A_x, A_y, A_z (see also Figure 2), each correlated to the acceleration detected along a respective detection axis. For example, the accelerometer 4 can be made as described in "3-axis Digital Output Accelerometer for Future Automotive Applications", B. Vigna et al., AMAA 2004.

In brief, the processing circuit 5 receives at input the acceleration signals A_x, A_y, A_z, carries out appropriate processing operations, and supplies at output logic signals corresponding to the displacements of the portable apparatus from a reference position. The microprocessor 3 receives said logic signals and reconstructs therefrom the displacement direction of the portable apparatus 1 so as to activate corresponding functions or programs in the portable apparatus

1.

In detail, Figure 2, the processing circuit 5 comprises, for each of the acceleration signals A_x, A_y, A_z, a threshold comparator 10, a digital high-pass filter 12 (which will be described in detail hereinafter) receiving at input a respective acceleration signal A_x, A_y, A_z from the accelerometer 4, an enabling stage 13, and an adjustment stage 14. The processing circuit 5 further comprises a first register 15, which stores an acceleration threshold A_{th}, which can be set from outside by a user.

The threshold comparator 10 has a first input connected to the first register 15, a second input connected to the output of the digital high-pass filter 12, and an output connected to the enabling stage 13. The enabling stage 13, preferably made with logic gates, has a first input connected to the output of the threshold comparator 10, a second input receiving an enabling signal EN_x, EN_y, EN_z of a logic type, and an output connected to the microprocessor 3 of the portable apparatus 1 (see Figure 1). In addition, the adjustment stage 14 is connected to the digital high-pass filter 12 for varying its cutoff frequency f_t on the basis of a selection by the user.

The operation of the displacement detection device 2 is the following.

The acceleration signals A_x, A_y, A_z generated by the accelerometer 4 are filtered in the respective digital high-pass filters 12 and supplied to the respective threshold comparators 10, which first calculate their magnitudes, and then compare them with the acceleration threshold A_{th}, generating at output a logic signal (designated by X', Y', Z'). The logic signal X', Y', Z' has, for example, a high value, if the magnitude of the respective acceleration signal A_x, A_y, A_z is greater than the acceleration threshold A_{th} (a

situation corresponding to the detection of an acceleration greater than the threshold set along the respective detection axis x, y, z). When the enabling signal EN_x, EN_y, EN_z assumes a pre-set logic value, for example high, the enabling stage 13 supplies at output a respective displacement detection signal X, Y, Z corresponding to the logic signal X', Y', Z' received from the respective threshold comparator 10. Otherwise, the enabling stage 13 supplies at output a pre-set logic signal, for example low, so disabling displacement detection along the respective axis x, y, z. Said function is useful for disabling one or more of the detection axes and thus simplifying processing by the microprocessor 3 when it is known which will be the displacement direction of the portable apparatus 1. In any case, the displacement detection signals X, Y, Z are sent to the microprocessor 3, which processes them (in a per-se known manner which is not described in detail herein) to determine the displacement direction of the portable apparatus 1.

In particular, the digital high-pass filter 12 eliminates (or in any case reduces) the continuous component of the respective acceleration signal A_x, A_y, A_z received at input, which is related to the acceleration of gravity, so that the displacement detection is independent of the initial position of the portable apparatus 1. Furthermore, the adjustment stage 14 enables variation of the cutoff frequency f_t of the digital high-pass filter 12, so as to adapt operation of the processing circuit 5 to the type of application/function that it is desired to obtain. For example, if it is desired to detect slow movements by the user, it is preferable to select a cutoff frequency f_t that is sufficiently low so that the low-frequency components of the corresponding acceleration signals will have an amplitude sufficient to be detected. It is, instead, preferable to select a higher cutoff frequency f_t if the movements by the user are faster.

According to an aspect of the present invention, Figure 3, the digital high-pass filter 12 has a recursive structure and has an input IN connected to the accelerometer 4 and receiving the respective acceleration signal A_x, A_y, A_z, and an output OUT connected to the respective threshold comparator 10. The digital high-pass filter 12 comprises a subtractor stage 20 and a recursive branch 21. The subtractor stage 20 has a positive input terminal connected to the input IN, a negative input terminal connected to the recursive branch 21, and an output terminal connected to the output OUT of the digital high-pass filter 12. The recursive branch 21 connects the output OUT to the negative input terminal of the subtractor stage 20, and comprises an integrator stage 23 and a divider stage 24, cascaded to one another. In particular, the integrator stage 23 is connected at input to the output OUT of the digital high-pass filter 12, and the divider stage 24 has an output connected to the negative input terminal of the subtractor stage 20.

The integrator stage 23 performs an accumulation function in so far as it carries out a summation, possibly weighted (according to the specific circuit configuration), of the samples that it receives at input. The divider stage 24 carries out a division by a dividing factor den, having a value greater than 1.

In detail, when the input IN of the digital high-pass filter 12 is constant at a given value α (for example, on account of a constant acceleration signal due to the sole acceleration of gravity), the recursive branch 21, and in particular the accumulation function of the integrator stage 23, causes the output of the integrator stage 23 to change, in particular to increase, until it assumes a value of α*den. When this condition arises, the negative terminal of the subtractor stage 20 is equal to α, matching the value of the input signal, and the output OUT of the digital high-pass filter 12

goes to zero.

When the input IN varies rapidly (for example, on account of an acceleration signal originated by a movement on the portable apparatus 1), the output OUT of the digital high-pass filter 12 substantially follows the input IN in so far as the recursive branch 21 is not sufficiently fast to follow the variations of the input IN. In this way, the information related to the movement issued by the user to the portable apparatus 1 is brought substantially unaltered to the output OUT of the digital high-pass filter 12. Next, when the input IN reaches again a stable or slowly variable value, the recursive branch 21 brings back to zero the output OUT of the digital high-pass filter 12, with a time that is related to its time constant.

Input signals having low frequencies (for example due to slow movements made by the user of the portable apparatus 1) are instead more or less attenuated, according to whether they are more or less close to the cutoff frequency f_t of the digital high-pass filter 12.

In particular, the cutoff frequency f_t of the digital high-pass filter 12 results from the speed of the recursive branch 21 in annulling the output OUT of the digital high-pass filter 12, i.e., from the speed of the integrator stage 23 in following the variations of the input IN. Said speed is a function of the sampling period of the integrator stage 23, and of the dividing factor den. Given the same sampling period, the higher the dividing factor den, the longer the digital high-pass filter 12 takes to reach a steady state (output OUT zero); i.e., the greater is its time constant. The cutoff frequency f_t of the digital high-pass filter 12 can hence be modified in a simple and fast way by the adjustment stage 14, by simply varying the dividing factor den of the divider stage 24.

Figure 4 illustrates the waveform of the signal at the output OUT of the digital high-pass filter 12 (represented with a solid line) in the presence of a square-wave signal (represented with a dashed line) at the input IN, simulating impulsive application of positive and negative displacements to the portable apparatus 1 by the user. The ordinate gives a normalized numerical value, whilst the abscissa gives the generated number of samples, normalized with respect to the sampling frequency. As may be noted, the output OUT of the digital high-pass filter 12 follows the impulsive variations of the input IN, and goes to zero, in a time related to its time constant, when the signal at the input IN is stable.

Two possible embodiments of the integrator stage 23 are now described.

In detail, according to a first embodiment, shown in Figure 5, the integrator stage 23 comprises an adder block 26, and a delay block 28. The adder block 26 has a first positive input terminal connected to the output OUT of the digital high-pass filter 12, a second positive input terminal connected to the output of the delay block 28, and an output terminal connected to the divider stage 24. The delay block 28 has an input connected to the output terminal of the adder block 26, and an output connected to the second positive input of the adder block 26.

With simple mathematical steps, it is found that the Z-transform, designated by H(z), of the digital high-pass filter 12 transfer function is the following:

$$H(z)=\frac{1-z^{-1}}{(1+\frac{1}{den})-z^{-1}}$$

which has a zero for $z=1$ and a pole for $z=1/(1+1/den)$.

In a second embodiment of the present invention, shown in Figure 6, the integrator stage 23 has a different circuit configuration. In particular, the delay block 28 is connected at input to the output terminal of the adder block 26 and at output to the divider stage 24. The adder block 26 has, instead, a first positive input terminal connected to the output OUT of the digital high-pass filter 12, a second positive input terminal connected to the divider stage 24, and an output terminal connected to the input of the delay block 28.

In a similar way, also in this case it is possible to obtain with simple mathematical steps the Z-transform of the digital high-pass filter 12 transfer function:

$$H(z) = \frac{1 - z^{-1}}{1 + (\frac{1}{den} - 1) \cdot z^{-1}}$$

which has a zero for $z = 1$ and a pole for $z = 1/(1 - 1/den)$.

In particular, it should be noted how both of the embodiments of the integrator stage 23 share the common feature of comprising a recursive accumulation structure.

As regards the second embodiment, Figures 7a and 7b show the magnitude and phase response against frequency, respectively, of the digital high-pass filter 12 for a first value of the dividing factor den, equal to 32. Likewise, Figures 8a and 8b show the magnitude and phase response, respectively, of the digital high-pass filter 12 for a second value of the dividing factor den, equal to 256. In particular, the cutoff frequency f_t of the digital high-pass filter 12 moves towards lower frequencies as the dividing factor den increases.

The advantages of the digital high-pass filter are clear from

the foregoing description.

It is, however, emphasized that the structure of the digital high-pass filter is extremely simple, is readily configurable, and calls for a minimum use of resources. In particular, it is sufficient to vary the dividing factor den of the divider stage 24 in order to vary the cutoff frequency f_t. In addition, if the values of the dividing factor den are chosen as powers of two, the operation of the divider stage 24 reduces to a simple shift of a digital word, thus further simplifying operation of the digital high-pass filter 12.

Furthermore, the overall displacement detection device can be integrated in a single chip, with obvious advantages in terms of area occupation.

Finally, it is clear that modifications and variations may be made to what has been described and illustrated herein, without thereby departing from the scope of the present invention, as defined in the attached claims.

In particular, in the embodiment of Figure 9, the processing circuit 5 is obtained entirely via software. In this case, the displacement detection device 2 comprises a microprocessor circuit 30 (for example, a microcontroller or a DSP), on which a firmware is stored that provides the processing circuit 5. In particular, the digital high-pass filter 12 of the processing circuit 5 can be made via software with three simple blocks, namely, an adder block, a subtractor block, and a divider block. Also in this case, the displacement detection device 2 can advantageously be integrated within a single chip 6.

The microprocessor circuit 30 can be equipped with appropriate logic circuits designed to deduce the displacement direction of the portable apparatus 1 and to transmit said information

directly to the main microprocessor 3 of the portable apparatus 1 so as to further simplify the management software of the portable apparatus 1.

In addition, the order of cascaded connection between the integrator stage 23 and the divider stage 24 within the recursive branch 21 can be reversed. In this case, the input of the divider stage 24 is connected to the output OUT of the digital high-pass filter 12, and the integrator stage 23 has an output connected to the negative input terminal of the subtractor block 20.

In addition, it is evident to the person skilled in the art that the integrator stage 23 can be made with other circuit configurations with the characteristic recursive accumulation structure.

Furthermore, in addition to being used for simplifying the man-machine interface, the displacement detection device can be used for re-activating a portable apparatus from a stand-by condition (the so-called wake-up function). In this case, the detection of an acceleration greater than the pre-set threshold causes re-activation of functions of the portable apparatus that had previously been de-activated in order to save energy. Finally, the displacement detection device can also be used in systems for control and compensation of vibrations, for example within electrical household appliances. In this case, in fact, it is not necessary to know the continuous acceleration to which the apparatus is subject, but rather the displacement with respect to a resting position.

CLAIMS

1. A digital high-pass filter (12) comprising:
an input (IN);
an output (OUT);
a subtractor stage (20), having a first input terminal and a second input terminal and an output terminal, said first input terminal being connected to said input (IN) of said digital high-pass filter (12) and said output terminal being connected to said output (OUT) of said digital high-pass filter (12); and
a recursive circuit branch (21) connected between said output (OUT) of said digital high-pass filter (12) and said second input terminal of said subtractor stage (20),
characterized in that said recursive circuit branch (21) comprises an accumulation stage (23) and a divider stage (24) cascaded to one another.

2. The digital high-pass filter according to claim 1, wherein said divider stage (24) performs a division by a variable dividing factor (den), having a value greater than 1; a cutoff frequency of said digital high-pass filter (12) being variable according to said variable dividing factor (den).

3. The digital high-pass filter according to claim 2, wherein said dividing factor (den) is a power of 2.

4. The digital high-pass filter according to any one of the preceding claims, wherein said accumulation stage comprises an integrator circuit (23).

5. The digital high-pass filter according to claim 4, wherein said integrator circuit (23) has a recursive accumulation structure having an own input terminal and an own output terminal, and comprising at least one adder block (26) connected to said own input terminal, and at least one delay

block (28) connected to said adder block (26) and to said own output terminal.

6. The digital high-pass filter according to claim 5, wherein said adder block (26) has a first positive input and a second positive input and an output, said first positive input of said adder block (26) being connected to said input terminal of said integrator stage (23), and said output of said adder block (26) being connected to said output terminal of said integrator stage (23); said delay block (28) having an input connected to said output terminal of said integrator stage (23) and an output connected to said second positive input of said adder block (26).

7. The digital high-pass filter according to claim 5, wherein said adder block (26) has a first positive input and a second positive input and an output, said first positive input of said adder block (26) being connected to said input terminal of said integrator stage (23), said second positive input of said adder block (26) being connected to said output terminal of said integrator stage (23); said delay block (28) having an input connected to said output of said adder block (26) and an output connected to said output terminal of said integrator stage (23).

8. The digital high-pass filter according to any one of the preceding claims, implemented via hardware using an application specific integrated circuit - ASIC.

9. The digital high-pass filter according to any one of claims 1-7, implemented via software using a firmware stored in a microprocessor.

10. A displacement detection device (2) for a portable apparatus (1), comprising:
- an acceleration sensor (4) generating a first acceleration

signal (A_x) corresponding to a first detection axis (x); and
- a displacement detection circuit (5) connected to said acceleration sensor (4) and generating a first displacement-detection signal (X), said displacement detection circuit (5) comprising first high-pass filtering means (12) configured to reduce a continuous component of said first acceleration signal (A_x);
characterized in that said first high-pass filtering means comprise a digital high-pass filter (12), made according to any one of the preceding claims.

11. The displacement detection device (2) according to claim 10, wherein said displacement detection circuit (5) comprises a first comparator stage (10) receiving said first acceleration signal (A_x) and a first acceleration threshold (A_{th}), and generating said first displacement-detection signal (X); said digital high-pass filter (12) being arranged between said acceleration sensor (4) and said first comparator stage (10).

12. The device according to claim 10 or claim 11, wherein said displacement detection circuit (5) further comprises cutoff frequency modifying means (14) connected to said digital high-pass filter (12), for adjusting the cutoff frequency of said digital high-pass filter (12); said cutoff frequency modifying means (14) varying a dividing factor (den) of a divider stage (24) of said digital high-pass filter (12).

13. The device according to any one of claims 10-12, wherein said displacement detection circuit (5) is implemented as an ASIC and is integrated with said acceleration sensor (4) within a single chip (6); said acceleration sensor (4) being implemented as a microelectromechanical system - MEMS.

14. The device according to any one of claims 10-12, further comprising a microprocessor circuit (30) connected to said

acceleration sensor (4) and wherein said displacement detection circuit (5) is implemented in a firmware stored in said microprocessor (30), and said microprocessor (30) and said acceleration sensor (4) are integrated in a single chip (6); said acceleration sensor (4) being implemented as a MEMS.

15. The device according to any one of claims 10-14, wherein said acceleration sensor (4) is a linear accelerometer with three detection axes (x, y, z) further generating a second acceleration signal (A_y) and a third acceleration signal (A_z), said first, second and third acceleration signals (A_x, A_y, A_z) being correlated to a component of the acceleration along a respective detection axis (x, y, z); and wherein said displacement detection circuit (5) further comprises: a second comparator stage (10) and a third comparator stage (10), for comparing, respectively, said second acceleration signal (A_y) and said third acceleration signal (A_z) with said first acceleration threshold (A_{th}) and generating a second displacement-detection signal (Y') and a third displacement-detection signal (Z'); and second and third filtering means (12) arranged, respectively, between said acceleration sensor (4) and said second comparator stage (10) and third comparator stage (10), and configured to reduce a continuous component, respectively, of said second and of said third acceleration signal (A_y, A_z); said second and third filtering means (12) comprising a digital high-pass filter made according to any one of claims 1-9.

16. A portable apparatus (1), characterized in that it comprises a displacement detection device (2) made according to any one of claims 10-15, said portable apparatus (1) being chosen in the group comprising laptops, PDAs, audio players, mobile phones, cameras, and videocameras.

17. The portable apparatus according to claim 16, further comprising a microprocessor (3), said microprocessor (3) being

connected to an output of said displacement detection device (2) for determining the displacement direction of said portable apparatus (1).

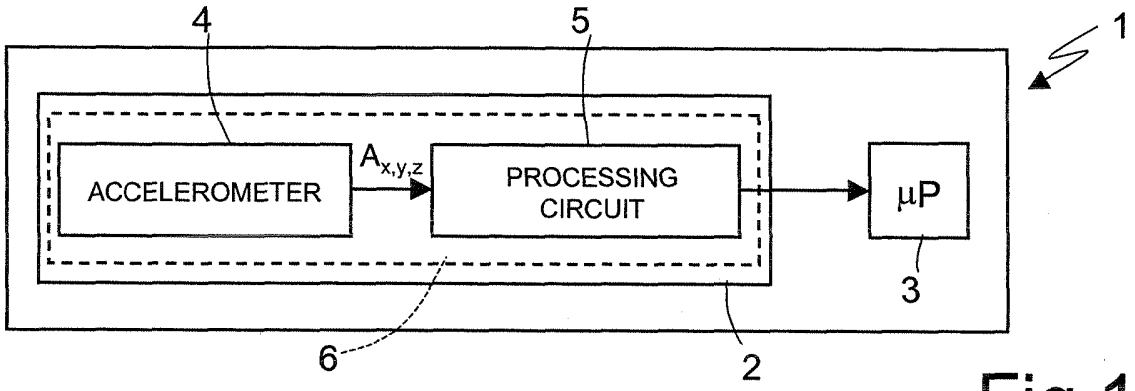
4
5
1
ACCELEROMETER
$A_{x,y,z}$
PROCESSING CIRCUIT
µP
3
6
2

Fig.1

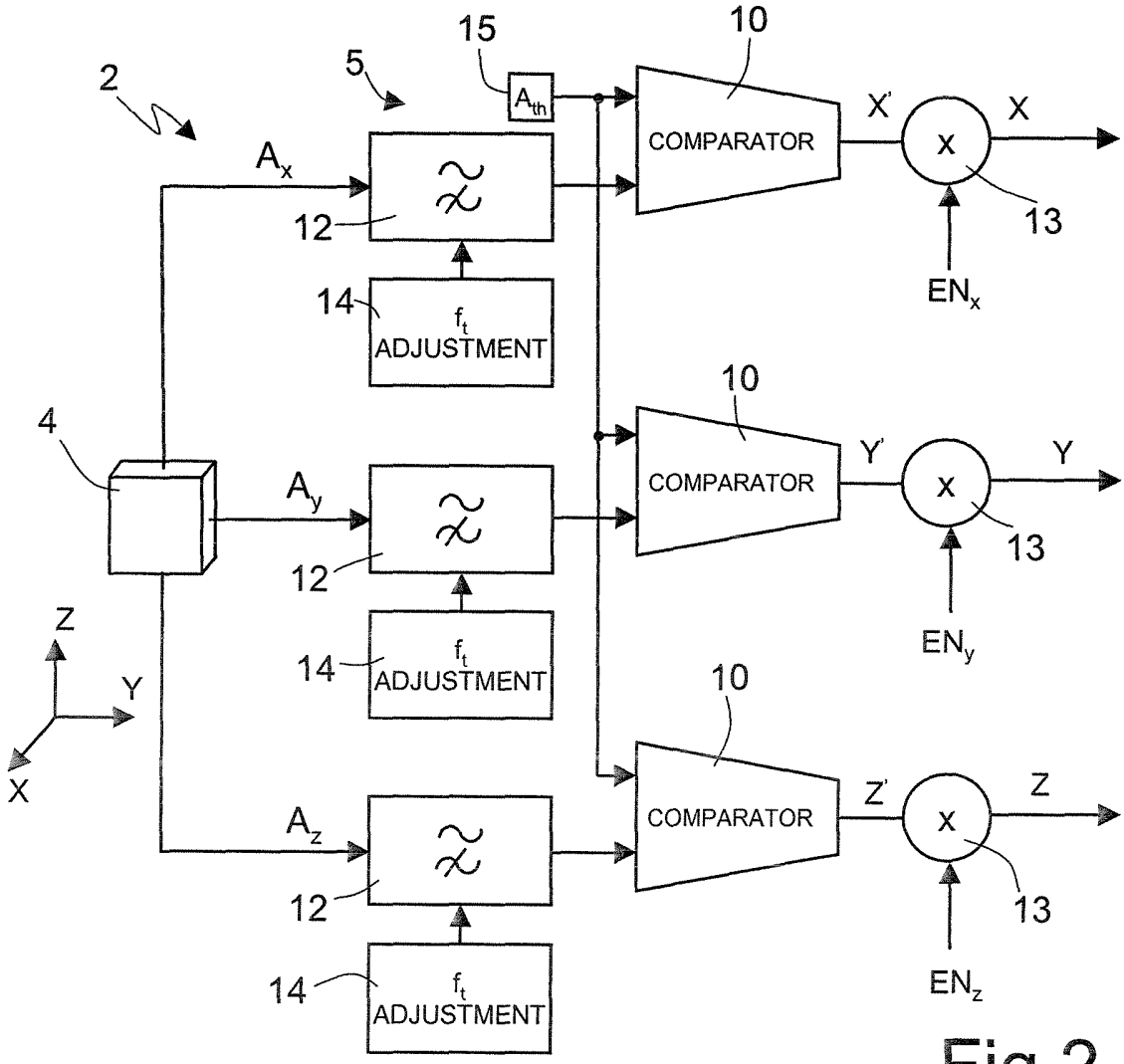
2
5
15
A_{th}
10
COMPARATOR
X'
X
x
13
EN_x
A_x
12
14
f_t ADJUSTMENT
4
A_y
Y'
Y
EN_y
Z
Y
X
A_z
Z'
Z
EN_z

Fig.2

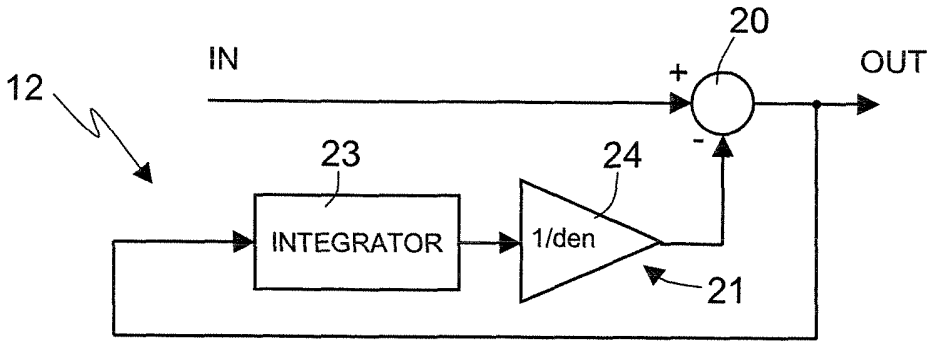

Fig.3

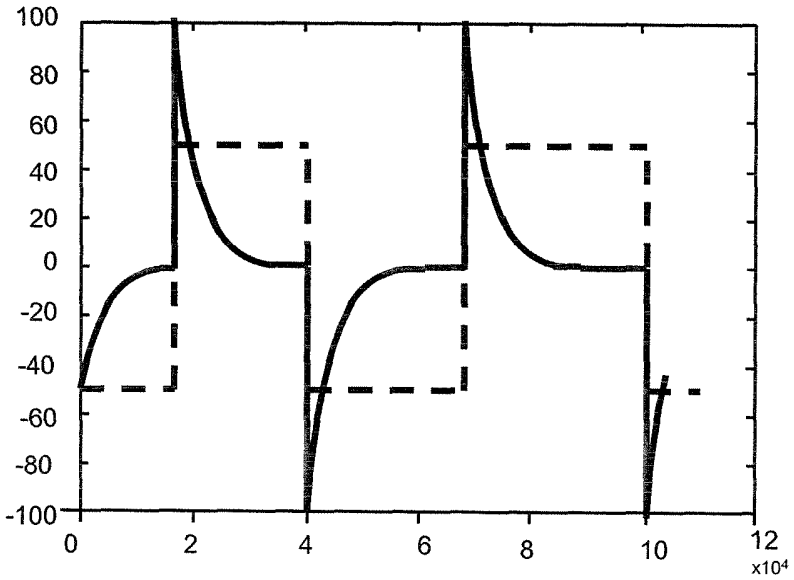

Fig.4

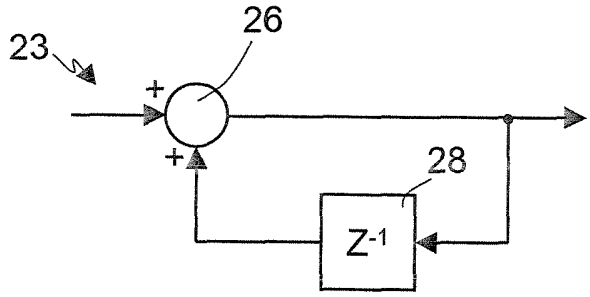

Fig.5

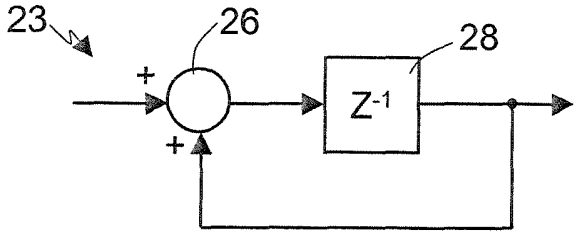

Fig.6

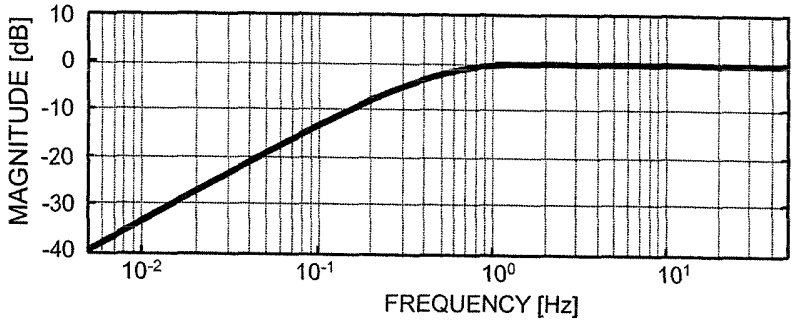

Fig.7a

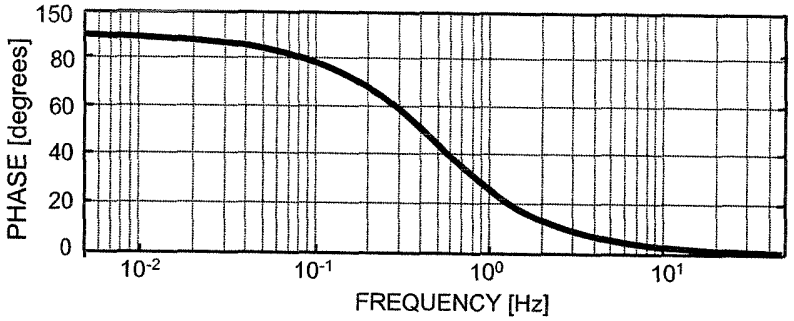

Fig.7b

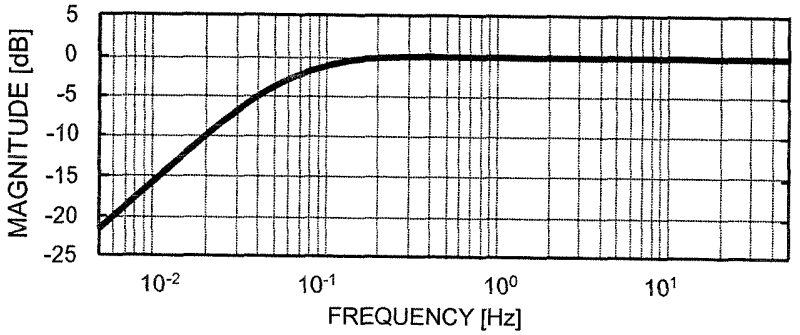

Fig.8a

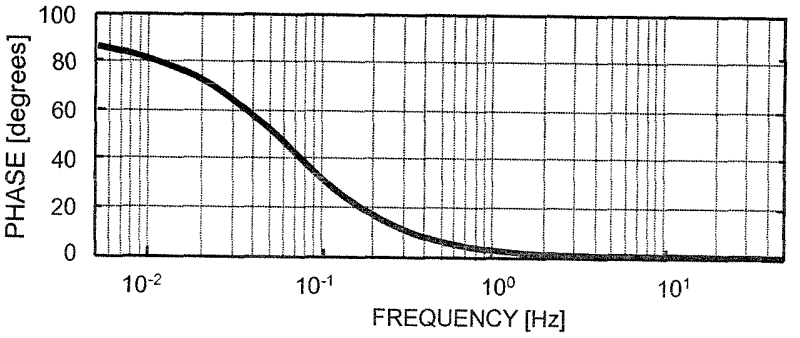

Fig.8b

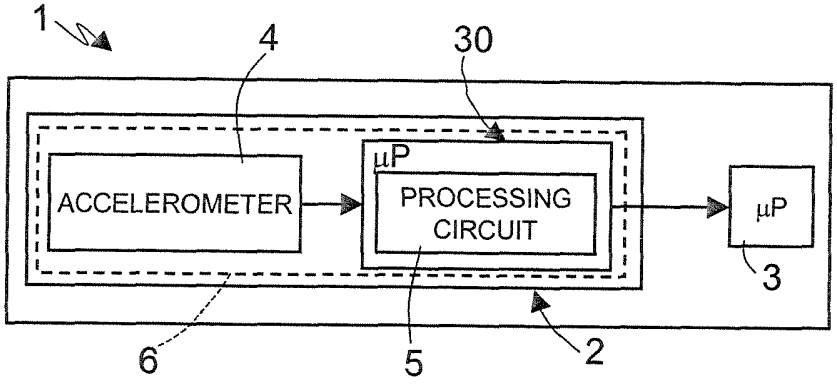

Fig.9

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/061116

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03H17/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 777 909 A (LEUNG ET AL) 7 July 1998 (1998-07-07) abstract column 2, line 26 - column 3, line 37; figure 1	1-9
Y		10,16
A		11-15,17

Y	US 5 155 520 A (NAGASAKI ET AL) 13 October 1992 (1992-10-13) abstract column 10, line 49 - column 11, line 2; figures 9,10	10,16
A		11-15

	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 June 2006	29/06/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Trafidlo, R

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2006/061116

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 128 442 A (ENOMOTO ET AL) 3 October 2000 (2000-10-03) abstract column 3, line 35 - column 4, line 23; figure 2 column 6, line 5 - line 40; figure 6 column 7, line 1 - column 8, line 15; figure 8	1,4-7, 10,16,17
A		2,3,8,9, 11-15

X	US 5 590 065 A (LIN ET AL) 31 December 1996 (1996-12-31) column 8, line 36 - column 9, line 7; figures 9(a),9(b)	1,4,5, 7-9
A		2,3,6, 10-17

X	RICHARD G. LYONS: "Understanding Digital Signal Processing" 2004, PRENTICE HALL , U.S.A. , XP002342103 page 553 - page 555; figures 13-62(c)	1,4,5, 7-9
A		2,3,6, 10-17

X	C. DICK; F. HARRIS: "FPGA Signal Processing Using Sigma-Delta Modulation" IEEE SIGNAL PROCESSING MAGAZINE, vol. 17, no. 1, January 2000 (2000-01), pages 20-35, XP002342101 U.S.A. page 32, right-hand column; figure 24	1,4,5, 7-9
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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US 5590065 A	31-12-1996	NONE	