

Oct. 11, 1966

A. SHOH

3,278,770

EXTREMAL-CENTERING METHOD AND SYSTEM

Filed Aug. 2, 1962

5 Sheets-Sheet 1

FIG. 1

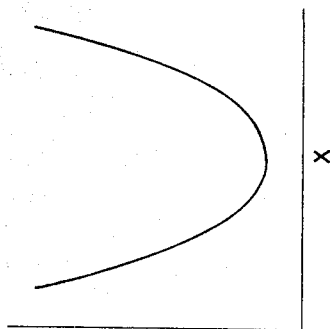
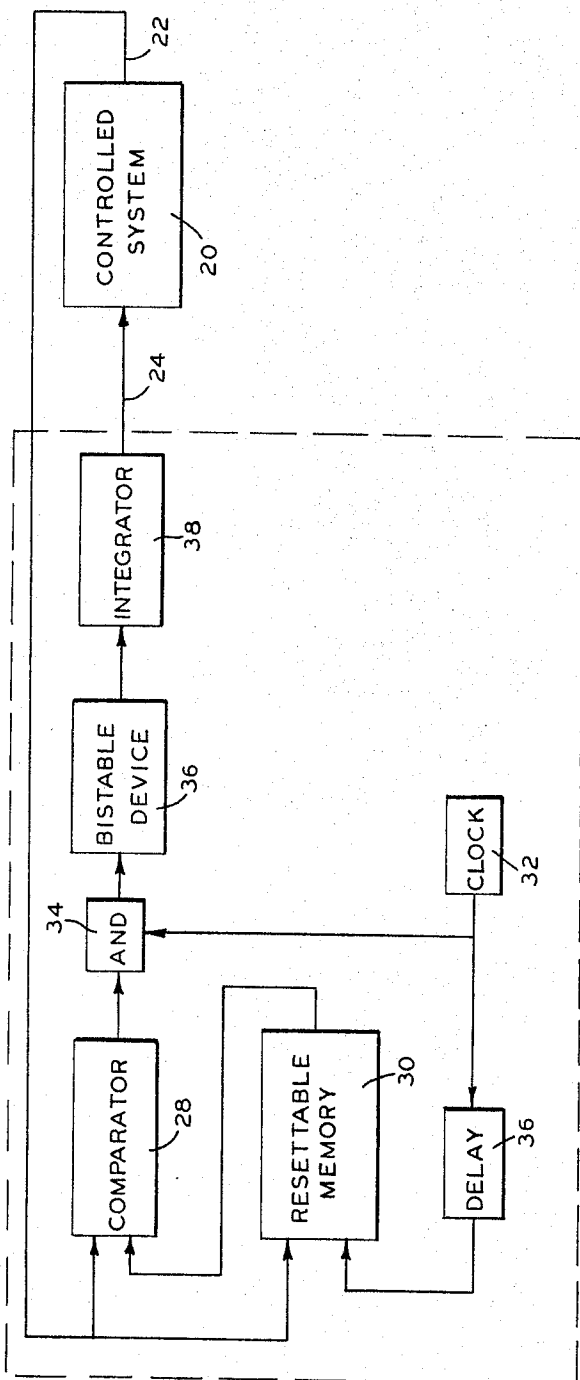


FIG. 3

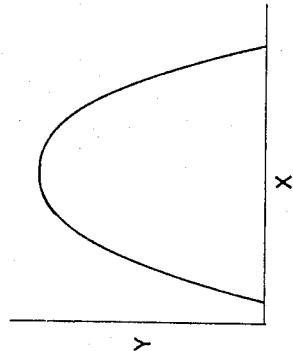


FIG. 2

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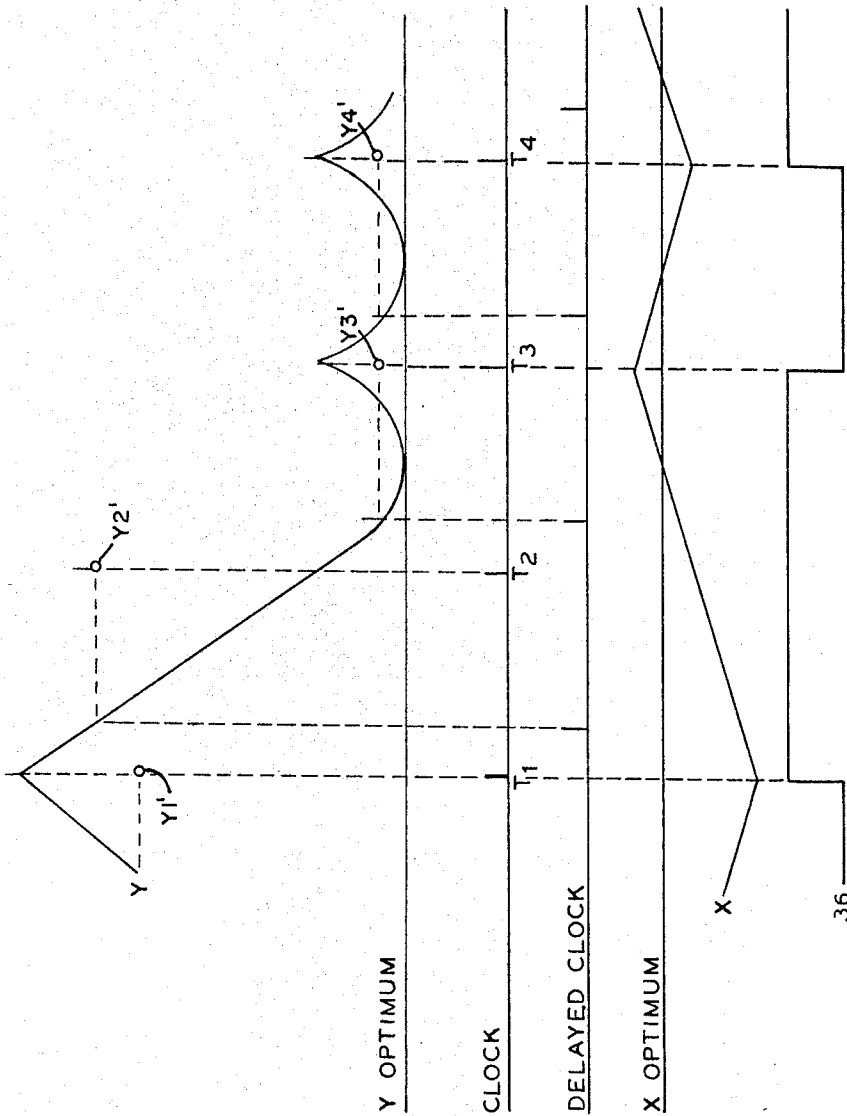
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FIG. 4



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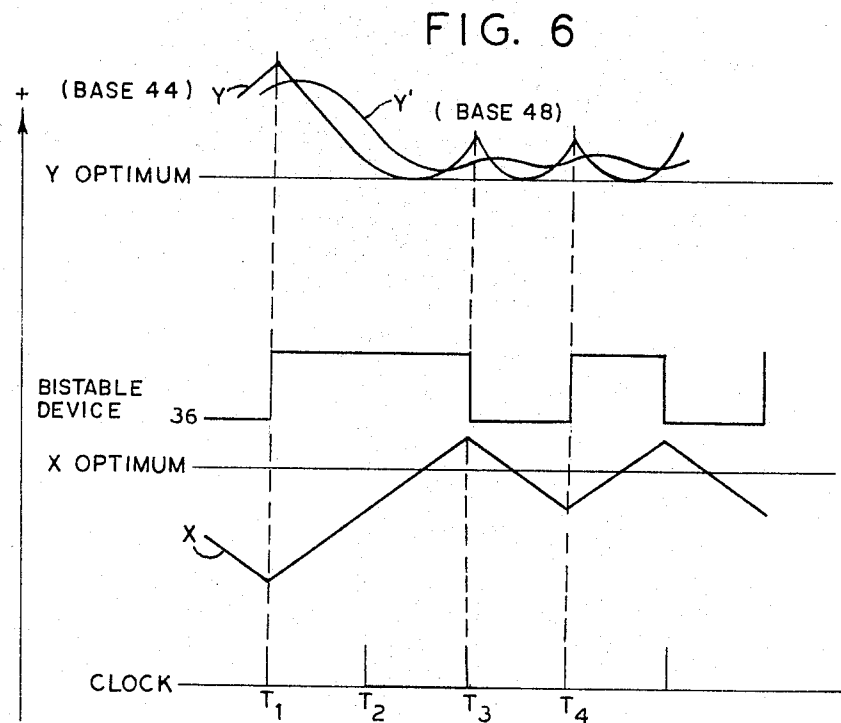
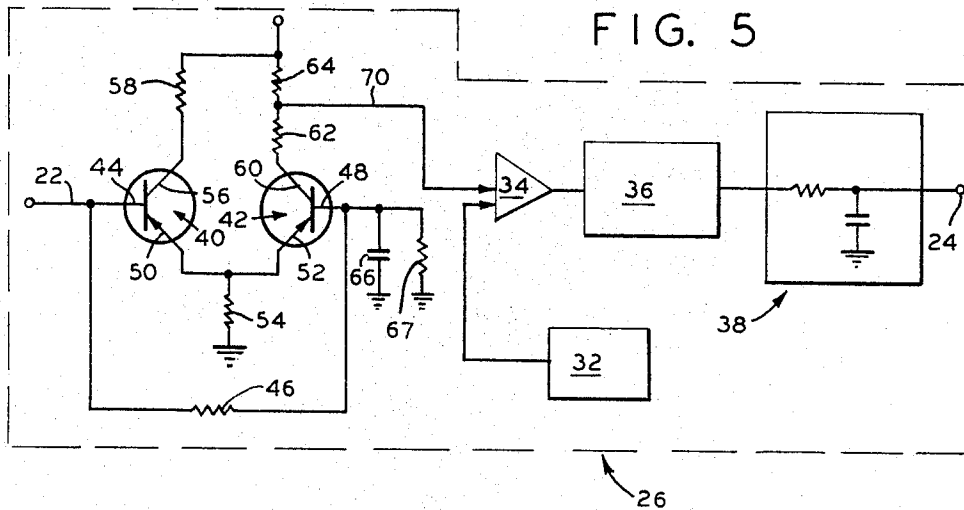
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EXTREMAL-CENTERING METHOD AND SYSTEM

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EXTREMAL-CENTERING METHOD AND SYSTEM

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FIG. 8

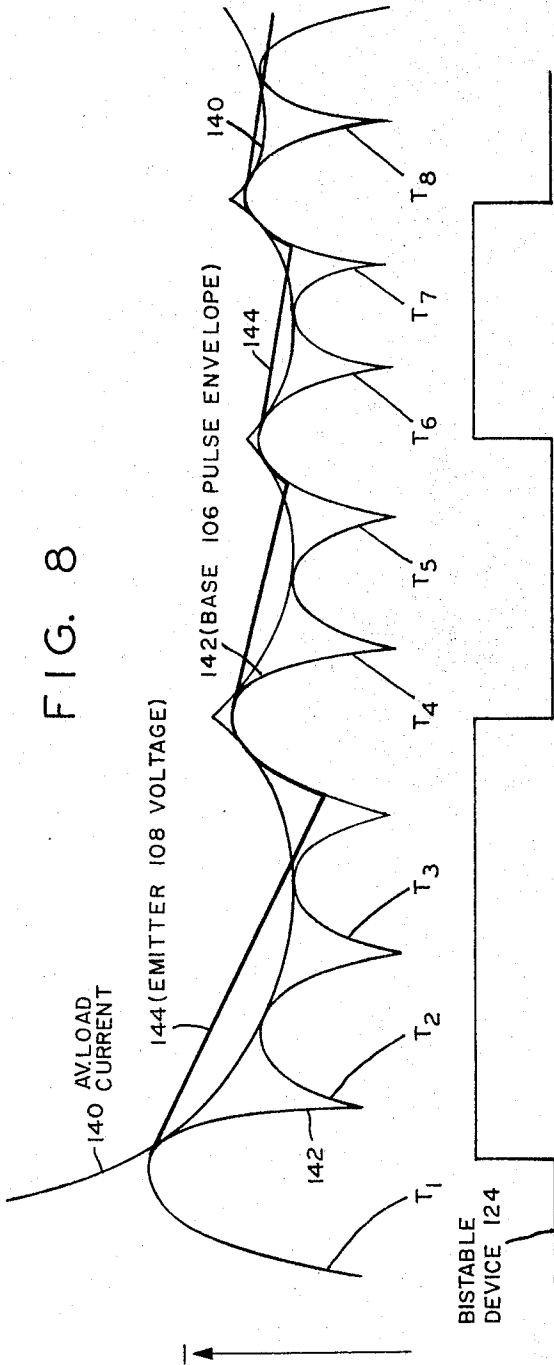


FIG. 10

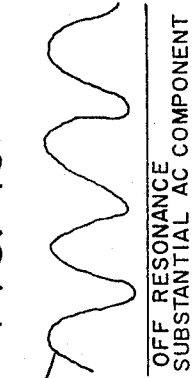
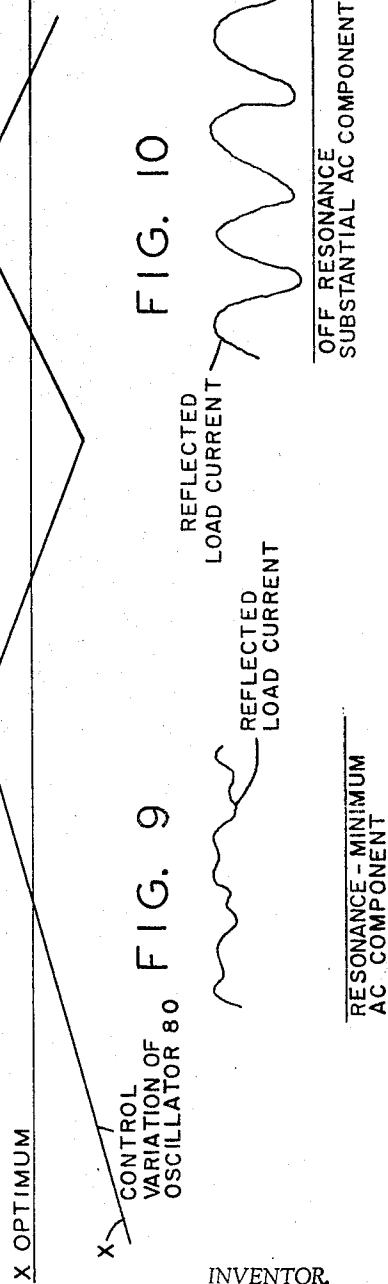


FIG. 9



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EXTREMAL-CENTERING METHOD AND SYSTEM
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 Filed Aug. 2, 1962, Ser. No. 214,255
 8 Claims. (Cl. 310-8.1)

The present invention concerns a method and system for maintaining a given first parameter at an extremal value. This is generally accomplished by continually varying a control or second parameter in one direction until the first parameter is noted to be departing from the extremal value, then reversing the direction of variation of the control parameter until the first parameter is again observed to be departing from the extremal value.

Many systems have an optimum operating point for a first parameter which is located at an extremal value of the first parameter as a function of a second or control parameter. Frequently it is inconvenient or impossible to determine directly the value of the control parameter corresponding to the extremal value of the first parameter, while the first parameter is relatively easy to measure. In such a system, when the second parameter drifts from the value required to maintain the first parameter at the extremal point, the question arises as to whether the second parameter should be increased or decreased. Typical prior art systems provided only manual correction.

Accordingly, it is an object of the invention to provide a method for automatically maintaining a parameter at an extremal value.

A further object is to provide a method of the above character which is generally applicable in a wide variety of systems.

A further object is to provide control systems to perform the above method.

A more specific object is to provide a system for maintaining the output frequency of a voltage controlled oscillator matched to a resonant load.

Other objects of the invention will in part be obvious and will in part appear hereinafter.

The invention accordingly comprises the several steps and the relation of one or more of such steps with respect to each of the others, and the apparatus embodying features of construction, combinations of elements and arrangement of parts which are adapted to effect such steps, all as exemplified in the following detailed disclosure, and the scope of the invention will be indicated in the claims.

For a more complete understanding of the nature and objects of the invention, reference should be had to the following detailed description taken in connection with the accompanying drawings, in which:

FIGURE 1 is a schematic block diagram illustrating generally the method and apparatus of the present invention.

FIGURES 2 and 3 are illustrative characteristics curves showing certain parameters of the system of FIGURE 1.

FIGURE 4 is a diagram showing certain parameters of the system of FIGURE 1 as a function of time.

FIGURE 5 is a schematic circuit diagram of a simplified form of control system.

FIGURE 6 is a diagram of certain parameters of the circuit shown in FIGURE 6, plotted as a function of time.

FIGURE 7 is a schematic circuit diagram of a specific system for maintaining the output voltage of an oscillator at a particular frequency.

FIGURES 8 through 10 are diagrams of various parameters of the system shown in FIGURE 7.

Referring now to FIGURES 1-3, a controlled system 20 is shown which has an output parameter Y at 22 which varies as a function of an input parameter X at 24. When

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the relationship between Y and X is of the type illustrated in FIGURE 2 or 3, there is a particular value of X which determines that the value of Y is at an extremal point on the characteristic curve. The extremal point may be at a maximum as illustrated in FIGURE 2, or at a minimum as illustrated in FIGURE 3.

As noted above, it is frequently more convenient to determine the value of Y than the particular value of X. In such a system, if the value of Y departs from its extremal value and X is not being sensed, there is no indication as to whether X should be increased or decreased in order to return Y to its extremal value. According to the present invention, a control system 26 is constructed and arranged to provide an input control signal X at 24 which alternatively either continuously increases or continuously decreases. The instantaneous output Y of system 20 at 22 is compared with a previous value, Y'. So long as the instantaneous value of Y is closer to the extremal value than the previous value Y' when comparison occurs, the control system 26 continues to vary the value of X in a first direction. When Y' is closer to the extremal value than the instantaneous value of Y, the direction of change of X at 24 is reversed until Y' is again closer to the extremal value than Y. This process is continually repeated, and accordingly results in the operating point of Y "scanning" across the extremal values of the characteristic curve.

As shown in FIGURE 1, the signal at 22 corresponding to the parameter Y is supplied to a comparator 28 and to a resettable memory 30. A clock source 32 supplies periodic pulses to one input of an AND gate 34, and through a delay network 36 to the resettable memory 30. The output of comparator 28 supplies the other input of AND gate 34. The output of AND gate 34 controls a bistable device, such as flip-flop 36, the output of which is integrated by network 38. This integrated signal is supplied by conductor 24 to provide a control input for system 20.

Referring now to FIGURE 4, the signals present in the various parts of the FIGURE 1 circuit are shown as a function of time. As shown therein, the actual value of Y is compared with the optimum value of Y. Just before the time interval T1, Y may be seen to be decreasing from the maximum value under the control of the decreasing value of X. When time T1 occurs, the instantaneous value of Y is compared by comparator 28 with a first value Y1', which is a previous value of Y that has been stored in resettable memory 30 (FIGURE 1). If, as illustrated at time T1 in FIGURE 4, the instantaneous value of Y is more positive than the first stored value Y1', gate 34 is enabled by comparator 28 to pass a clock pulse signal from clock source 32. The clock pulse signal is applied to the input of bistable device 36, which switches to its other stable state. The output of bistable device 36 is integrated and applied to conductor 24. This change in state of bistable device 36, when integrated, reverses the direction in which the control signal at 24 is varying, causing the value of X to increase until bistable device 36 is again actuated.

At a time interval after T1 fixed by the delay of delay network 36, the delayed pulse from clock source 32 discharges the first stored signal Y1' in memory 30 and stores therein a second signal Y2' corresponding to the value of Y existing at that time. At time interval T2, the instantaneous value of Y is more negative than the second stored value Y2', and accordingly gate 34 is not enabled at the occurrence of the clock pulse from source 32, and bistable device 36 is unaffected. The value of X continues to increase.

As before, a fixed time after the occurrence of the clock pulse at T2, a pulse is supplied through delay net-

work 36, discharging the second stored value of Y2' and storing therein a third value Y3' corresponding to the instantaneous value of Y prevailing at that time.

Just before time T3, Y reaches the extremal value and starts going positive relative thereto. At the time T3 when the next comparison occurs, the instantaneous value of Y is more positive than the stored value Y3', and accordingly the clock pulse occurring at time T3 is passed by gate 34. This actuates bistable device 36, which changes to its other condition and reverses the direction in which its integrated output 24 is changing. This reverses the direction of change of parameter Y. Memory 30 is again reset as before, to provide a fourth stored value Y4'.

At time interval T4, the value of Y is again more positive than the stored value Y4', and the clock signal is passed by gate 34, actuating bistable device 36 and reversing the direction in which X and Y are varying. The above steps are continuously repeated, and result in a continuous scanning of Y across its extremal value.

In the embodiment shown in FIGURE 5, the extremal value of Y is represented by a maximum negative voltage on conductor 22. A pair of transistors 40 and 42 are connected to provide a combined comparator and resettable memory. The signal Y at 22 is applied directly to base 44 of transistor 40, and through resistor 46 to base 48 of transistor 42. The emitters 50 and 52 of transistors 40 and 42, respectively, are connected directly together and to ground through resistor 54. Collector 56 is connected to a direct current power supply by resistor 58, while collector 60 is connected to the power supply by a pair of series resistors 62 and 64. A capacitor 66 connects base 48 to ground. A resistor 67 is preferably connected in parallel with capacitor 66, in order to aid in starting the system. Resistor 67 preferably has a value several times larger than resistor 46, and thus does not substantially affect the normal operation of the circuit. The junction between resistor 62 and 64 is connected to AND gate 34, the output of which controls the operation of a bistable device 36, which may be a flip-flop. The output of bistable device 36 is integrated in network 38 to provide a control signal X.

Resistor 46 and capacitor 66 provide a time constant network for applying a delayed signal Y' to base 48 a fixed period of time after it is applied to base 44. Since transistors 40 and 42 are PNP transistors, so long as base 44 is maintained more negative than base 48, which can only occur if conductor 22 continues to increase the negative direction, there will be no output at terminal 70, since the voltage developed across emitter coupling resistor 54 will maintain emitter 52 negative with respect to base 48. However, when the voltage on base 48 becomes more negative than the voltage on base 44, transistor 42 conducts. This provides a positive signal on conductor 70, enabling AND gate 34.

Referring to FIGURE 6, at time T1 base 44 (curve Y), is less negative than base 48 (curve Y'), and accordingly transistor 42 is conducting as noted above, enabling gate 34. Thus when the trigger pulse, from clock 32 occurs at time T1, the pulse is passed through AND gate 34 to transfer bistable device 36 to its other stable state. This reverses the direction in which the integrated X output is varying, and accordingly reverses the direction in which the signal at 22 (curve Y) is varying. The voltage at 22 begins to increase in the negative direction. As shown in FIGURE 6, the voltage at base 48 (curve Y') follows the changing voltage at conductor 22, and begins to increase negatively. After a short period of time, the voltage on conductor 22 is more negative than the voltage at conductor 48, and during such condition, transistor 44 is conducting and AND gate 34 disabled if a clock pulse should occur during this condition, as illustrated at time T2.

Shortly after time T2, as the control output voltage X passes its optimum value, the signal Y at conductor 22

begins to decrease from its extremal value again. The signal at base 48 follows the changing direction of the signal at 22, but because of the time constant produced by resistor 46 and capacitor 66, by time T3 the voltage at 22 is again more positive than the voltage at 48, enabling AND gate 34. The clock pulse at time T3 accordingly reverses the state of bistable device 36, which reverses the direction in which control signal X is varying.

The value of Y then decreases and passes its extremal value, driven by the constantly decreasing value of X until time T4, at which time the value of Y has again decreased to a less negative value than the signal at 48. The clock pulse at T4 again reverses the condition of bistable device 36, and reverses the direction in which control signal X is varying. This process is then repeated continually, causing the operating point of parameter Y to "scan" the extremal point on its characteristic curve.

Referring now to FIGURES 7-9, there is shown an illustrative system wherein a voltage controlled oscillator 80 is required to provide an output signal having a frequency matched to drive a parallel-resonant load 82 at its resonant frequency. The sine-wave output of oscillator 80 is supplied through a push-pull transformer primary winding 84 to a secondary winding 86, across which load 82 is connected. Oscillator 80 is supplied with power by an unfiltered full-wave power supply 88 through the primary winding 90 of a small current transformer to the center tap of winding 84. As an example, the output frequency of oscillator 80 may be approximately 25 kc., while the repetition rate of the unidirectional ripple pulses supplied by power supply 88 may be 120 per second. The output signal amplitude of oscillator 80 thus increases from zero to a maximum and decreases back to zero 120 cycles per second.

The control circuitry of FIGURE 7 takes advantage of the presence of the unfiltered ripple in power supply 88 by eliminating the external clock source, and utilizing such ripple to provide clock signals.

At the resonant frequency F1, load 82 exhibits a maximum impedance and the current therethrough is at a minimum. Accordingly, the high-frequency current in primary winding 84 is at a minimum when the output of oscillator 80 is at frequency F1. Winding 90, connected in series between the center tap of primary 85 and power supply 88, couples to its secondary winding 92 a signal corresponding to the current in winding 84. The signal at 92 is supplied to an amplitude modulation detector 94, comprising diode 96 having resistor 98 connected between its cathode and ground, with capacitor 100 shunted across resistor 98. The signal at the cathode of diode 96 is accordingly a series of pulses at the repetition rate of the pulses supplied by power supply 88, with an amplitude corresponding to the envelope of the high frequency current signal in transformer winding 90. The amplitude of pulses at the anode of diode 96 is thus inversely proportional to the impedance presented by load 82 to the high frequency signal in primary winding 84.

The amplitude of each of these envelope pulses is compared with the amplitude of the preceding envelope pulse by peak detector 102. Peak detector 102 comprises an NPN transistor 104 connected in the common emitter configuration, with its base 106 connected to the cathode of diode 96, its emitter 108 connected to ground by emitter resistor 110, and its collector 112 connected to a source of constant positive potential by series resistors 114 and 116. A capacitor 118 is shunted across resistor 110.

The values of resistor 110 and capacitor 118 are selected to provide signal-biased class "C" operation for transistor 104. As illustrative values for the frequencies under consideration, resistor R2 may have a value of 50 kilohms, while capacitor C2 may have a value of 2 microfarads.

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The time constant of resistor 110 and capacitor 118 is so adjusted that the positive polarity signal produced at emitter 108 upon the occurrence of an envelope pulse decreases only a slight amount before the occurrence of the next envelope pulse. Resistor 110 and capacitor 118 therefore store a signal which is proportional to the preceding envelope pulse. So long as each envelope pulse on base 106 is larger than the preceding pulse which is stored at emitter 108, the base-emitter junction of transistor 104 will be forwardly biased by the pulse at 106, giving a pulse output at collector 112. However, when the incoming pulse at base 106 is smaller than the stored signal at emitter 108, the base-emitter junction of transistor 104 remains reversely biased, and transistor 104 provides no output signal.

When an output pulse is produced at collector 112, a portion thereof is supplied to the input of a further amplifier stage 120. Preferably, a capacitor 122 is shunted across the input of transistor 120 to eliminate the effects of individual high frequency pulses. Transistor 120 has its output connected to operate a bistable device 124, which may be a conventional flip-flop, the output of which is integrated by resistor 126 and capacitor 128 and applied as the input control signal on conductor 130 to regulate the output frequency provided by oscillator 80.

When the output of oscillator 80 is substantially sinusoidal, it is possible to eliminate components 96, 98, and 100, since transistor 104 itself will rectify the signal from winding 92. In this case, the output of transistor 104 should be filtered, as by capacitor 122, to insure that bistable device 124 is actuated only by the 120-cycle envelope and not by individual high frequency pulses.

As shown in FIGURE 8, it is desired to minimize the average current through the load 82. Curve 140 represents the average current through load 82 as a function of time, curve 142 represents the envelope pulse signal at base 106, while curve 144 represents the signal at emitter 108. It is assumed that the output of oscillator 80 is below F_1 and increasing. At the occurrence of pulse T1 of the pulse envelope curve 142, the average current in load 82 is found to be decreasing. The amplitude of the second pulse T2 applied to base 106 is less than the signal stored at emitter 108, and transistor 104 remains nonconductive. Similarly, at pulse T3, although the voltage at emitter 108 continues to decrease according to the time constant provided by resistor 110 and capacitor 118, the pulse amplitude is still smaller than the signal at emitter 108 and accordingly transistor 104 remains non-conducting.

However, when pulse T4 occurs, the signal frequency output of oscillator 80 is just past the optimum resonant frequency of load 82, and accordingly the signal current (curve 140) has increased. The amplitude of pulse T4 is greater than the signal at emitter 108, and causes conduction of transistor 104. This produces an output signal which is supplied to amplifier 120 and applied to reverse the state of bistable device or flip-flop 124. As shown in curve 144, flip-flop 124 reverses its output, which results in the integrated output at 130 beginning to decrease. This decrease in the potential at 130 causes the output frequency of oscillator 80 to decrease. Since the output frequency is now again approaching the resonant frequency of load 82, the average current there-through decreases.

During the conduction of transistor 104 in period T4, the potential at emitter 108 increased to very nearly the amplitude of the signal impressed on base 106. As shown, the voltage of emitter 108 slowly decreases thereafter, and at the occurrence of pulse T5, is still greater than the amplitude of the signal at base 106.

As the output frequency of oscillator 80 continues to decrease, it passes the resonant frequency of load 82 and the average current (curve 140) through load 82 increases. Accordingly, pulse T6 is larger than pulse T5, and is also larger than the stored signal remaining at

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emitter 108. Therefore upon the occurrence of pulse T6, the transistor 104 is rendered conducting and provides an output signal which reverses the state of flip-flop 124. The integrated output 130 of flip-flop 124 begins to increase, causing the output frequency of oscillator 80 to increase toward the resonant frequency of load 82.

The above comparison of each new envelope pulse with a previous stored envelope pulse, and reversal of the direction in which the output frequency of oscillator 80 is changing when the new pulse is larger than the stored pulse, is repeated continuously. This automatically maintains a match between the output of oscillator 80 and the resonant frequency of load 82.

In a particular ultrasonic cleaning application where the resonant load 82 in the FIGURE 7 system was a loaded piezoelectric transducer radiating into a tank containing cleaning liquid and having a parallel power factor correction coil, the control system is equally effective if the output of oscillator 80 is in the switching mode, supplying essentially square waves to a loaded crystal 82. When the crystal is resonant the load reflected into the primary winding 84 will be primarily resistive and the current therein will have a relatively small A.C. component, as shown by FIGURE 9. However when the repetition rate of the square wave output of oscillator 80 is either above or below the resonant frequency of crystal 82, the alternating component in primary winding 90 will be substantially increased, as shown in FIGURE 10. This increased alternating component may be used to control the repetition rate of oscillator 80 exactly as in the case wherein oscillator 80 has a sinusoidal output as above described. However, when the output of oscillator 80 is essentially square wave, it is usually more desirable to utilize a separate amplitude modulation detector 94 than when oscillator 80 output is sinusoidal.

It will thus be seen that the objects set forth above, among those made apparent from the preceding description, are efficiently attained and, since certain changes may be made in carrying out the above method and in the constructions set forth without departing from the scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

It is also to be understood that the following claims are intended to cover all of the generic and specific features of the invention which, as a matter of language, might be said to fall therebetween.

Having described my invention, what I claim as new and desire to secure by Letters Patent is:

1. In a system having a first parameter controllable as a function of a second parameter, said first parameter having an optimum point at an extremal value of said function, the combination comprising,

(a) means for providing a derived signal corresponding to said first parameter on a first conductor,
(b) a resettable storage device for storing a sample of said derived signal,

(c) a comparator means for periodically comparing the instantaneous value of said derived signal with said stored sample, said comparator means having

(1) one input connected to said storage device and another input connected to said first conductor

(2) and further having an output connected to an input terminal of an AND gate

(d) clock means connected to the other input of said AND gate and connected through delay means to said resettable storage means,

(e) a bistable element having its input connected to the output of said gate,

(f) an integrator having its input connected to the output of said bistable element

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(g) and control means for said system for controlling said second parameter proportionally to the integrated output of said integrator.

2. A system for driving a resonant load at its resonant frequency comprising:

(a) a voltage-controlled oscillator having an input terminal and an output stage driving an output transformer,

(1) said transformer having a center-tapped primary winding and

(2) a secondary winding connected to said resonant load,

(b) a low frequency pulsating direct current power supply for said output stage connected to said center tap by a series impedance for deriving a signal representative of the total current in said output stage,

(c) means for rectifying and filtering said derived signal to provide a second signal pulsating at said low frequency rate and representative of the amplitude of high frequency components in said output transformer,

(d) a peak detector having its input connected to the output of said filter means,

(e) a flip-flop having its input connected to the output of said peak detector,

(f) and an integrating network connected between the output of said flip-flop and said input terminal.

3. A system for driving a resonant load at its resonant frequency comprising:

(a) a voltage controlled oscillator having an input terminal and a signal output terminal connected to said resonant load,

(b) a low frequency pulsating direct current power supply for said oscillator,

(c) means for deriving a signal representative of the current through said resonant load,

(d) means for rectifying and filtering said derived signal to provide a second signal pulsating at said low frequency rate and representative of the amplitude of high frequency components in said resonant load,

(e) comparator means for comparing the instantaneous amplitudes of said second signal pulses with previous stored second signal pulses and for providing an output signal whenever a pulse is greater in amplitude than a preceding stored pulse,

(f) bistable means having its control input connected

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to the output of said comparator means and having its output connected to an integration network,

(g) the input terminal of said oscillator being connected to the output of said integration network.

4. The combination of claim 3, wherein said resonant load is an electromechanical transducer.

5. The combination of claim 4, wherein said transducer is a piezoelectric transducer.

6. The combination of claim 4, wherein said transducer is mounted to couple mechanical vibrations into a liquid.

7. The combination of claim 3, wherein said comparator comprises,

(a) a differential amplifier having a first input terminal, a second input terminal and an output terminal,

(b) means for applying a signal to said first input terminal,

(c) and signal delay means connecting said first and said second input terminals.

8. The combination of claim 3, wherein said comparator comprises,

(a) first and second transistors, each having an emitter, a base, and a collector electrode,

(b) said emitters being connected together and through a common impedance to a point of reference potential,

(c) means connecting a direct current power supply between said collectors and said point of reference potential, including a load impedance connected between said second collector and said power supply,

(d) means for applying an input signal to said first base,

(e) and signal delay means connected to apply said signal at said first base to said second base.

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