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(54) Title: SILICON NANOWIRE AND COMPOSITE FORMATION AND HIGHLY PURE AND UNIFORM LENGTH SILICON NANOWIRES

(57) Abstract: The invention provides a method for forming silicon nanowires and composites in polymers. In a preferred method of the invention, a device quality silicon layer that is on a silicon on oxide substrate is etched with an HF/silver nitrate etching solution to form silicon nanowires attached to an oxide layer of the silicon on oxide substrate. A silver film that forms during the etching is easily removed. The nanowires are released from the surface of the oxide via a brief HF acid treatment and gentle agitation. Uniform length nanowires form having a length that is equal to the thickness of the device quality silicon layer. The nanowires that form have pure crystalline silicon structure with no bulk contamination, and any residual silver on the surface of the nanowires after fabrication can be easily removed by selective etching.

SILICON NANOWIRE AND COMPOSITE FORMATION AND HIGHLY PURE AND UNIFORM LENGTH SILICON NANOWIRES

FIELD

A field of the invention is silicon nanowires and composites.

BACKGROUND

Significant interest exists in the possible use of silicon nanowires as basic charge carriers for electronic components. Silicon nanowires offer the promise of operational speeds that far exceed present state of the art solid state electronic devices. Silicon nanowires have the advantage of being compatible with existing process technology in the integrated circuit industry.

When fabrication issues are solved, silicon nanowires will be used to form many electronic devices, such as field effect transistors (FETs), diodes, and logic gates. Such devices will incorporate silicon nanowires as charge carriers that will operate under physics laws of quantum mechanics. The potential exists for silicon nanowires to be powerful building blocks for nanoelectronics devices if the nanowires can be fabricated with single-crystal structures, diameters as small as several nanometers and controllable hole and electron doping. Silicon nanowire based devices should eventually form an important alternative to conventional planar technology. A silicon nanowire based FET, for example, will provide improved electrostatic control of the channel via the gate voltage and better suppression of short channel effects than conventional planar technology.

Additional promising applications for silicon nanowires are as biosensors for the real-time detection of biological molecules (i.e. DNA, RNA, proteins). Such sensors are based on the fact that changes in conduction occur when a charged object is brought in close proximity to the silicon nanowire surface.

Efforts to fabricate silicon nanowires that have been used in the art include chemical vapor deposition (CVD), pulsed laser vaporization (PLV), and thermal evaporation (TE). CVD and vapor-liquid-solid PLV require catalysts, while oxide-assisted thermal evaporation is catalyst free. A catalyst free technique provides a likely important advantage in terms of purity control, especially for avoiding trace metals.

Silicon nanowires fabricated by CVD are now grown on surfaces catalyzed by metal nanoparticles, such as gold nanoparticles. With this technique, there is marginal control over the length, direction and straightness or curvature of the silicon nanowires that form. The cross section is governed generally by the diameter of the metal nanoparticle. In principle, the length increases with monotonically proportional to the growth time but is also statistical with length distribution. The wires are expected to be epitaxial but tend to have metal in its bulk.

Previous researchers have used etching in ionic silver/HF solution to produce columns /wires on a regular silicon wafer. These columns /wires are firmly connected to the substrate and not readily detached or dispersed as wires.

SUMMARY OF THE INVENTION

The invention provides a method for forming silicon nanowires and nanowire composites. The invention also provides a dispersed material consisting of highly pure silicon nanowires of substantially identical lengths, referred to as uniform dispersed material silicon nanowires. In a preferred method of the invention, a device quality silicon layer that is on a silicon on oxide substrate is etched with an HF/silver nitrate etching solution to form silicon nanowires attached to an oxide layer of the silicon on oxide substrate. A silver film that forms during the etching is easily removed. The nanowires are released from the surface of the oxide via gentle agitation. Uniform length nanowires form having a length that is equal to the thickness of the device quality silicon layer. The nanowires that form have pure crystalline silicon

structure with no bulk contamination, and any residual silver on the surface of the nanowires after fabrication can be easily removed by selective etching.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a flowchart illustrating steps in a preferred embodiment silicon nanowire formation method of the invention;

FIG. 2 is a flowchart illustrating steps in a preferred embodiment method for functionalizing silicon nanowires;

FIG. 3 illustrates a preferred embodiment method for forming a silicon nanowire composite; and

FIG. 4 is an SEM image of silicon nanowires formed in an experiment conducted in accordance with the method of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the invention is a method for forming silicon nanowires. Methods of the invention form dispersions of free standing silicon nanowires that are straight and identical. Formation methods of the invention produce pure crystalline silicon nanowires with no bulk contamination. Dispersed material of the invention consists of quantities of such highly pure silicon nanowires of substantially identical lengths. Silicon nanowires formed by the invention exhibit the doping of the starting device quality silicon used in formation methods of the invention. In additional, the silicon nanowires can be doped using ion implantation or diffusive doping at higher temperatures after formation. Additionally, composites of the invention can be formed with silicon nanowires dispersed in a matrix, such as an RTV, polymer or epoxy matrix.

A preferred embodiment formation method of the invention conducts electroless etching with ionic silver HF acid of a Si on oxide (SOI) substrate to allow making free-standing nanowires by detachment at the oxide interface, and enables easy recovery of dispersions of nearly identical wires for

subsequent controlled delivery as dispersed material or for incorporation in a matrix material.

Preferred embodiments of the invention will now be discussed with respect to the drawings. The drawings may include schematic representations, which will be understood by artisans in view of the general knowledge in the art and the description that follows. Features may be exaggerated in the drawings for emphasis, and features may not be to scale.

Referring now to FIG. 1, a preferred method of fabrication is illustrated. In the method, a silicon on insulator (SOI) wafer is provided 10. The SOI wafer has a device quality silicon layer with a predetermined thickness. The thickness is selected to achieve a desired length of silicon nanowire, as the thickness of the layer and length of the silicon nanowire produced are the same. The lengths of pure silicon nanowires that are produced are formed by the method a substantially identically, namely the uniformity in length is entirely consistent with the uniformity in the thickness of the device quality silicon layer of the silicon on insulator (SOI) wafer. A suitable SOI layer is, for example, a commercially available boron-doped (p-type) silicon (100) SOI wafer. N-type device quality silicon SOI wafers can also be used. The wafer is cleaned 12, for example with acetone, to remove organic contaminants. The surface of the device quality silicon layer is then etched with an HF/silver nitrate solution 14. The wafer is then dried 16, gently, such as by gentle blow drying or with a drying solvent. A silver film that forms around the wafer is removed 18, by simple mechanical detaching or wet etching. Silicon nanowires are harvested 20 from the wafer by gentle agitation, which can be achieved via sonication. The nanowires themselves are pure crystalline silicon, but will have some residual silver on their surface. The residual silver can be removed 22 by selective etching, such as etching in nitric acid. The method produces a material consisting of a dispersion of highly pure silicon nanowires having substantially identical lengths.

The silicon nanowires produced are not necessarily luminescent, but the nanowires can be functionalized to be luminescent or for other

purposes. Silicon nanowires produced by the FIG. 1 process (or another process) can be, for example, functionalized for optoelectronics and sensing applications, as in a preferred method illustrated in FIG. 2. A process for plating nanoparitcles that are fluorescent onto the nanowires can be adopted from PCT Publication WO 2007/018959. The process involves treating a treating a silicon substrate with hexachloroplatinic acid (HCPA) and etching the silicon substrate with HF/H_2O_2 to form silicon nanoparticles. The process can also treat silicon nanowires to form silicon nanoparitcles on their surface, as is described with respect to FIG. 2. First, silicon nanowires are harvested 24 in a dispersion solvent, such as methanol. A plating solution is then added 26 to the nanowire dispersion solution. A plating mixture is, for example, HCPA/HF. The combined solution is stirred gently 28 for a time sufficient to permit plating of the nanowires. This can be a relatively short time period, e.g., 15min. The solvent is then decanted (meaning drained) and the wires are hence removed 30 from the plating solution and rinsed 32, e.g., with de-ionized water to remove residual plating solution. HF/H_2O_2 is then added to the wires 34, which can typically be completed in about 30-45 seconds. The nanowires are then removed and rinsed 36, e.g., with de-ionized water. The nanowires are then dried 38, such as by air drying or adding a drying solvent.

Once the nanowires are recovered and collected, a composite can be formed with the nanowires. FIG. 3 illustrates a preferred embodiment method for forming a silicon nanowire composite by embedding the nanowires in a matrix. In step 40, recovered silicon nanowires are mixed with matrix precursors. Example precursors include precursors for RTV, polyurethane or any other polymer material, or any epoxy material. The mix is then sonicated in step 42, and the matrix is cured in step 44. The result is a nanowire-composite, which can be an RTV, polymer, epoxy, etc. composite. Nanowires embedded in the matrix can consist of a dispersion of highly pure silicon nanowires having substantially identical lengths.

The matrix material can be selected to be electrically non-conducting or electrically conducting depending on the application. The matrix

can also be a good or poor thermal conductor. In one example application, devices have been fabricated in experiments by sputtering metal contacts on the two faces of the composites. One face is contacted with a heat source such as a current driven thermal coil of nicrom wire. The electrical potential across the composite was measured, and compared to the response of a control device that had no wires embedded. The measurements reveal some enhanced thermoelectric response.

Experiments

Experiments have been conducted to demonstrate the formation method of the invention, and example silicon nanowires 10 μm long and 50 - 100 nm thick were produced and observed by scanning electron microscopy. The wires are readily dispersed and are pure crystalline silicon. The experiments also demonstrated that the length of the wires can be controlled in methods of the invention, as the length of nanowires is governed by the thickness of the silicon layer.

In the experiments, a commercial boron-doped silicon (100) (4–8Ωcm) silicon on insulator wafer (SOI) was used. The wafer consists of three layers, a handle, an oxide layer, and a device quality silicon layer. The handle is a thick silicon layer typically of the order of half a millimeter on the backside of the wafer. The oxide layer is a few hundred nanometers thick silicon oxide layer. A thin device quality silicon layer is on top of the oxide. Various thicknesses of device quality silicon layers are available in commercial SOI wafers. The available thicknesses are typically in the range of about the range of 100 nm to tens of micrometers.

As preparation for the fabrication, the SOI wafer is first cleaned by acetone, followed by etching in diluted aqueous HF solution. An HF and silver nitrate solution was prepared as 5.0mol/L HF / 0.02mol/L silver nitrate. The SOI wafer is immersed in the 5.0mol/L HF solution containing 0.02mol/L silver nitrate at 50°C. After the etching process, the SOI wafer is removed and

rinsed with de-ionized water and blown dry in air very gently. In the process, a thick silver film wrapping the silicon wafer forms, which can be simply mechanically detached or wet etched. The wafer is then sonicated in a solvent to harvest the wires. A simple selective chemical etching treatment in nitric acid permits removal of residual silver.

The length of the nanowires is controlled by the thickness of the device quality silicon layer. The uniformity of the length is controlled by the uniformity of the layer. This was established by numerous experiments. The commercial SOI wafer used in the experiments is rated at $10 \pm 0.5\mu$. The cross section of the wire size achieved in the experiments was 50-90 nm. Adjustment of the etchant composition and a more uniform silicon layer is expected to achieve tighter control of the size and shape of the wire cross section.

FIG. 4 shows a scanning electron microscopy (SEM) of the wafer after etching but prior to separation of the nanowires from the wafer by sonication. The silicon nanowires appear as piles as well as individual dispersed nanowires on both faces of the wafer. Those observed individually show that they of the same length and thickness. The etched depth (i.e. the lengths of silicon nanowires) of the Si wafer is approximately 10μm, which is the thickness of the device quality silicon layer of the SOI wafer used to form the silicon nanowires. The diameters of nanowires are in the range of 30–200nm. Chemical analysis using the electron spectroscopy shows very little silver remaining.

The wires are weakly attached to the oxide layer. They may also detach during the process A brief acid treatment in HF or gentle sonication in a liquid of choice releases the wires into the liquid. Harsh or continued sonication may shatter or break the wires. Experiments also showed that the sonicated nanowires can be deposited on a fresh silicon wafer or mixed in polymers to produce composites..

The experiments showed that the wires produced by methods of the invention lack the metal contamination that is difficult to avoid with

techniques that use nanoparticles as catalysts for the formation of nanowires. The silver used in the method of the invention stays on the outer surface of the wire if at all, and the small amount that may be present on the surface of the wire can easily be removed by with selective wet etching, such as by etching in nitric acid. Also, nanowires produced by the invention are readily processes, since can be harvested as dispersions in any suitable liquid of choice. This permits the nanowires to be functionalized on their surface, such as by plating.

While specific embodiments of the present invention have been shown and described, it should be understood that other modifications, substitutions and alternatives are apparent to one of ordinary skill in the art. Such modifications, substitutions and alternatives can be made without departing from the spirit and scope of the invention, which should be determined from the appended claims.

Various features of the invention are set forth in the appended claims.

CLAIMS

1. A method for forming silicon nanowires, the method comprising steps of:

etching a device quality silicon layer that is on a silicon on oxide substrate with an HF/silver nitrate etching solution to form silicon nanowires attached to an oxide layer of the silicon on oxide substrate; and

removing a silver film that forms during said etching.

2. The method of claim 1, further comprising a step of cleaning the silicon on oxide substrate prior to said step of etching.

3. The method of claim 1, further comprising a step of drying the silicon nanowires prior to said step of removing the silver film.

4. The method of claim 3, wherein said step of drying comprises gentle blow drying.

5. The method of claim 1, further comprising a step of removing any residual silver from the silicon nanowires.

6. The method of claim 5, wherein said step of removing any residual silver comprises

wherein said step of removing comprises selective etching.

7. The method of claim 6, wherein said selective etching etches with nitric acid.

8. The method of claim 1, further comprising a step of harvesting the silicon nanowires by gentle agitation.

9. The method of claim 8, wherein said gentle agitation comprises sonication.

10. The method of claim 1, further comprising a step of functionalizing the nanowires.

11. The method of claim 10, wherein said step of functionalizing comprises plating the nanowires with fluorescent nanoparticles.

12. The method of claim 1, wherein said device quality silicon layer comprises a doped silicon layer.

13. The method of claim 1, further comprising a step of forming a composite matrix including the nanowires.

14. The method of claim 13, wherein said step of forming a composite matrix comprises:

mixing the nanowires in precursors for matrix material; and

curing the matrix material.

15. Material consisting of a dispersion of a quantity of pure silicon nanowires having substantially identical lengths.

16. The material of claim 15, wherein the dispersion is contained within a matrix material.

17. The material of claim 16, wherein the matrix material comprises one of a polymer and an epoxy.

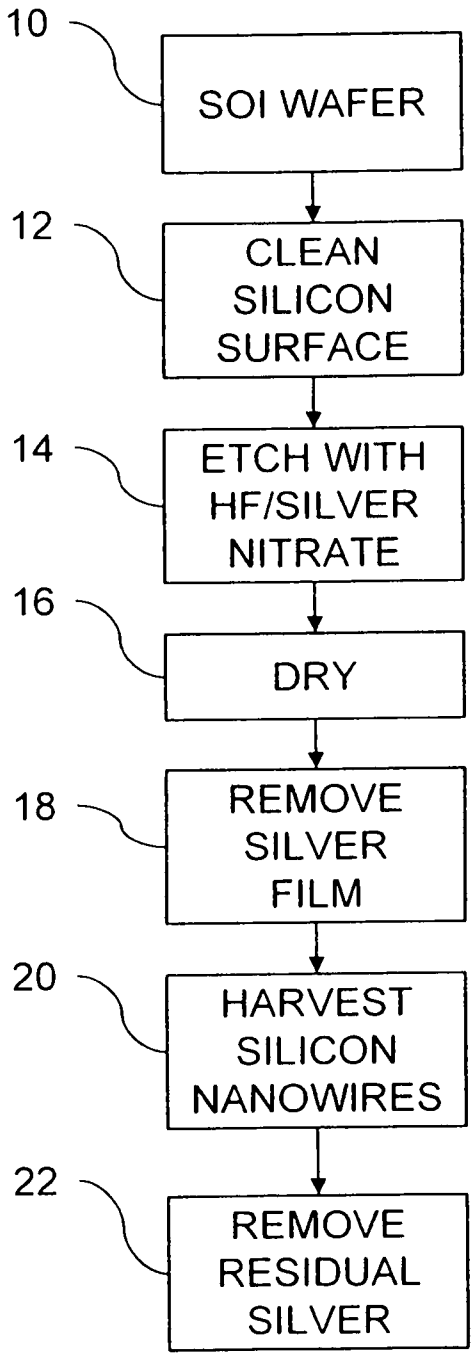
10
SOI WAFER
12
CLEAN SILICON SURFACE
14
ETCH WITH HF/SILVER NITRATE
16
DRY
18
REMOVE SILVER FILM
20
HARVEST SILICON NANOWIRES
22
REMOVE RESIDUAL SILVER

FIG. 1

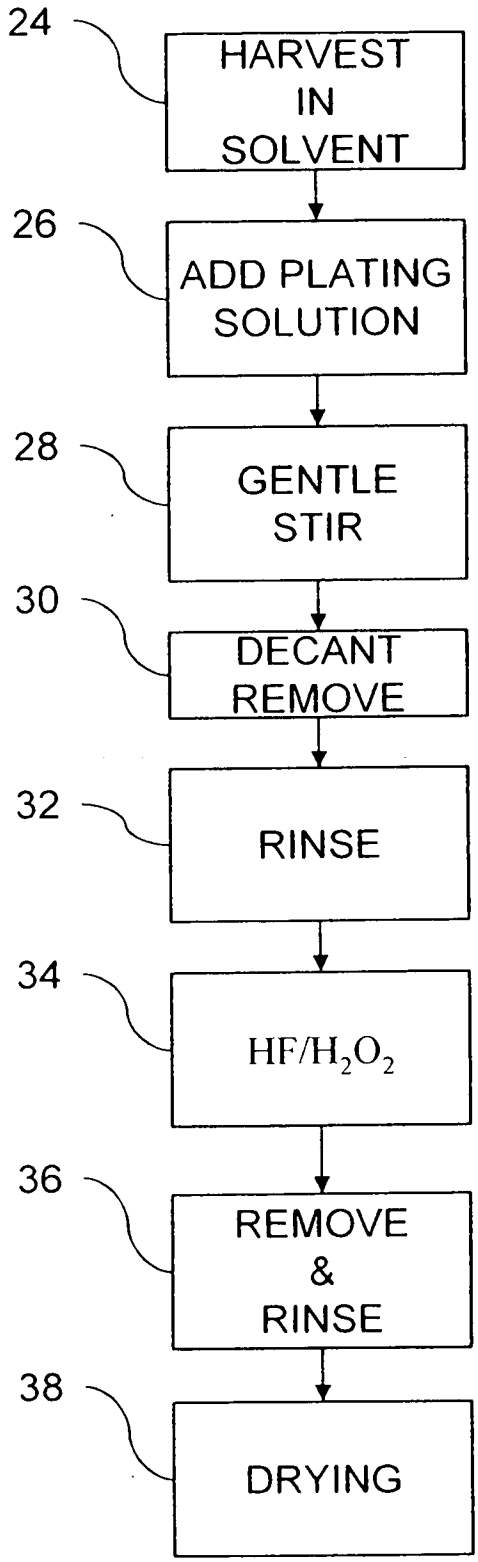
24
HARVEST IN SOLVENT
26
ADD PLATING SOLUTION
28
GENTLE STIR
30
DECANT REMOVE
32
RINSE
34
HF/H_2O_2
36
REMOVE & RINSE
38
DRYING

FIG. 2

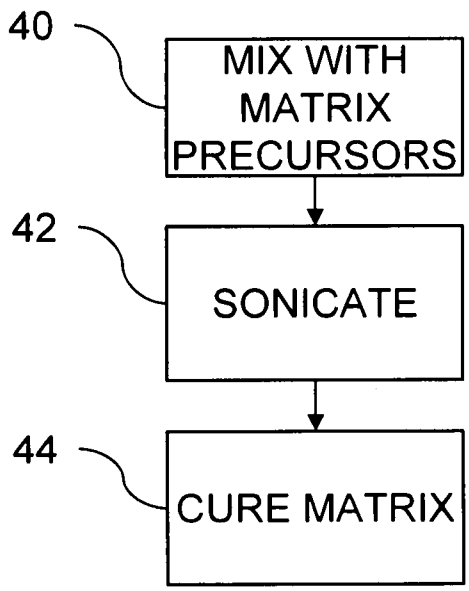

FIG. 3

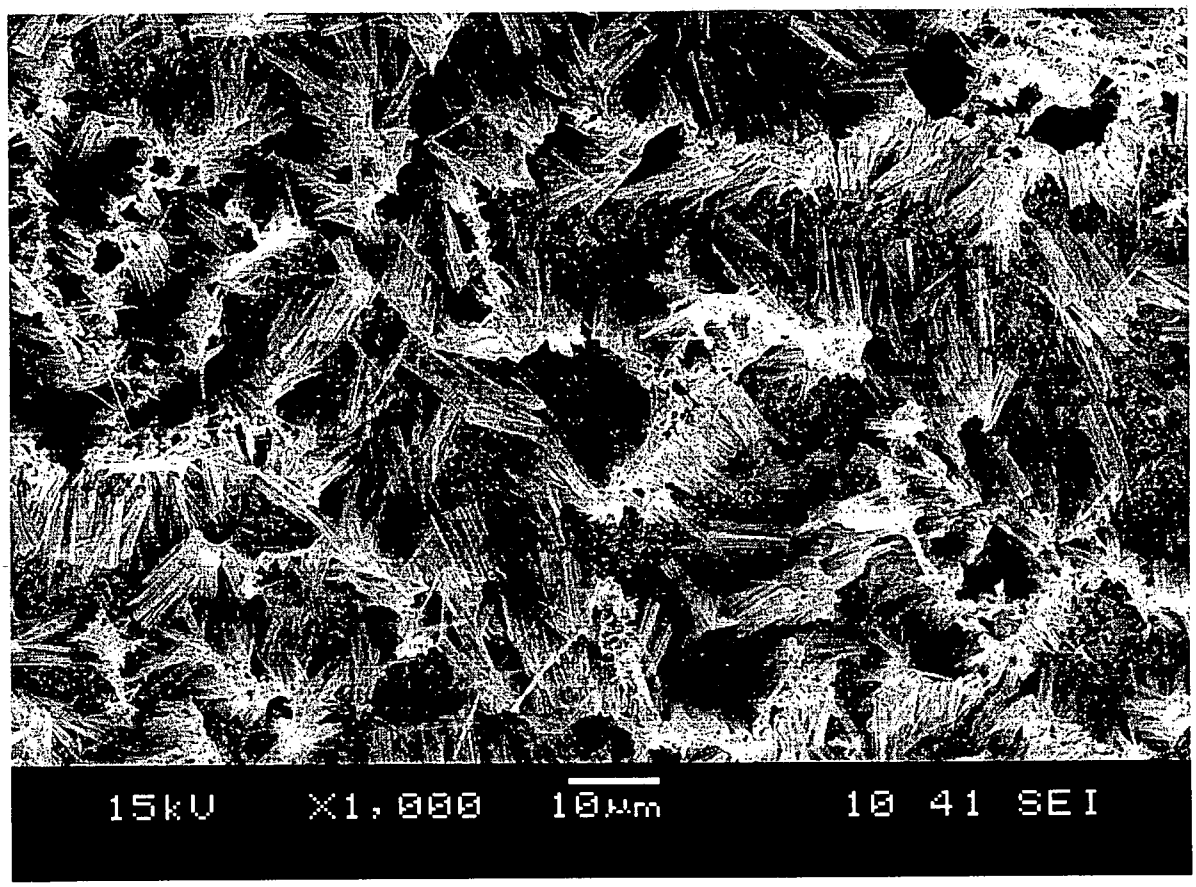

FIG.4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 08/04983

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/8234 (2008.04)
USPC - 438/197; 257/E21.616
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8)- H01L 21/8234 (2008.04)
USPC- 438/197; 257/E21.616

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC- 257/401, 257/E29.345; 438/480;
Patents and NPL

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWest (US Patent, PgPub, OCR: classification), DialogClassic (Derwent, Claims, fulltexts US, EPO, WIPO: keyword), GoogleScholar; search terms: silicon?, nanowire?, etch?, silver?, nitrate?, on oxide?, insulator?, soi, matri?, polymer?, epox?, identical?, same?, length, sonicat?, nitric? acid?, blow? dry?

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2006/0207647 A1 (TSAKALAKOS et al.) 21 September 2006 (21.09.2006), para [0069], [0071], [0076], [0079], [0081], [0082], [0093], [0102], [0107],	1-3, 5, 6, 10-12 ---------- 4, 7-9, 13, 14
X -- Y	US 2006/0019472 A1 (PAN et al.) 26 January 2006 (26.01.2006), para [0020], [0123], [0125], [0147], [0148]	15-17 -------- 13, 14
Y	US 2003/0180472 A1 (ZHOU et al.) 25 September 2003 (25.09.2003), para [0042], [0045]	7-9
Y	US 2005/0038498 A1 (DUBROW et al.) 17 February 2005 (17.02.2005), para [0273]	4
A	US 2006/0255481 A1 (PAN et al.) 16 November 2006 (16.11.2006), entire document	1-17
A	US 2003/0089899 A1 (LIEBER et al.) 15 May 2003 (15.05.2003), entire document	1-17

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 December 2008 (23.12.2008)	08 JAN 2009
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774