



(51) International Patent Classification:
H01L 21/60 (2006.01) *H01L 23/485* (2006.01)

(21) International Application Number:
PCT/EP2009/064260

(22) International Filing Date:
29 October 2009 (29.10.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/344,802 29 December 2008 (29.12.2008) US

(71) Applicant (for all designated States except US): **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, New York 10504 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **GAMBINO, Jeffrey** [US/US]; IBM Corporation, MD 975A, 1000 River Street, Essex Junction, Vermont 05452-4299 (US). **DAUBENSPECK, Timothy, Harrison** [US/US]; IBM Corporation, MD 975E, 1000 River Street, Essex Junction, Vermont 05452-4299 (US). **MUZZY, Christopher, David** [US/US]; IBM Corporation, MD 972C, 1000 River Street, Essex Junction, Vermont 05452-4299 (US). **SAUTER, Wolfgang** [DE/US]; IBM Corporation, MD 9651D, 1000 River Street, Essex Junction, Vermont 05452-4299 (US). **SULLIVAN, Timothy, Dooling** [US/

US]; IBM Corporation, MD 967A, 1000 River Street, Essex Junction, Vermont 05452-4299 (US).

(74) Agent: **WILLIAMS, Julian, David**; IBM United Kingdom Limited, Intellectual Property Law, Hursley Park, Winchester Hampshire SO21 2JN (GB).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: STRUCTURES AND METHODS FOR IMPROVING SOLDER BUMP CONNECTIONS IN SEMICONDUCTOR DEVICES

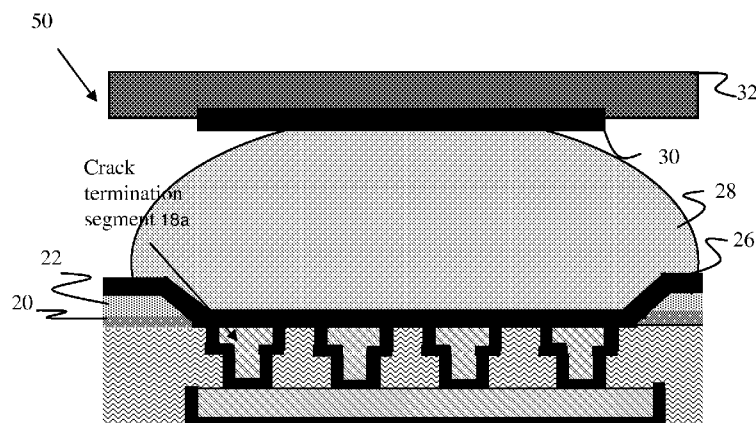


FIG. 8

(57) Abstract: Structures with improved solder bump connections and methods of fabricating such structures are provided herein. The method includes forming a plurality of trenches in a dielectric layer extending to an underlying metal layer. The method further includes depositing metal in the plurality of trenches to form discrete metal line islands in contact with the underlying metal layer. The method also includes forming a solder bump in electrical connection to the plurality of metal line islands.

STRUCTURES AND METHODS FOR IMPROVING SOLDER BUMP CONNECTIONS IN SEMICONDUCTOR DEVICES

CROSS REFERENCE TO RELATED APPLICATIONS

5

The present application is related to co-pending U.S. Application Serial No. _____ (Docket No. BUR920080217US1), filed on the same day herewith and incorporated by reference in its entirety herein.

10

FIELD OF THE INVENTION

The invention relates to integrated circuits, and more particularly, to structures with improved solder bump connections and methods of fabricating such structures.

15

BACKGROUND

20

Traditionally, high temperature C4 (Controlled Collapse Chip Connection) bumps have been used to bond a chip to a substrate with the most common and widely utilized package being an organic laminate. Conventionally, the C4 bumps (solder bumps) are made from leaded solder, as it has superior properties. For example, lead is known to mitigate thermal coefficient (TCE) mismatch between the chip and the substrate (i.e., organic laminate). Accordingly, stresses imposed during the cooling cycle are mitigated by the C4 bumps, thus preventing delaminations or other damage from occurring to the chip or the substrate.

25

Lead-free requirements are now being imposed by many countries forcing manufacturers to implement new ways to produce chip to substrate joints. For example, solder interconnects consisting of tin/copper, tin/silver (with high concentrations of silver) and tin/gold in combination with SAC alloys are being used as a replacement for the leaded solder interconnects. With lead-free requirements, though, concerns about defects in C4 interconnections have surfaced, e.g., cracks in chip metallurgy under C4 bumps (named “white bumps” due to their appearance in CSAM inspection processes) which lead to failure of the device. More specifically, white bumps are C4's that do not make good electrical

30

contact to the Cu last metal pad, resulting in either failing chips at functional test or in the field. This may be attributable, at least in part, due to chip designs using high stress Pb-free C4 (solder bumps) which exacerbate C4/AlCu bump to Cu wire adhesion problems.

5 As one illustrative example, during the chip joining reflow, the chip and its substrate are heated to an elevated temperature (about 250°C) in order to form the solder interconnection joints. The initial portion of the cool down leads to little stress build up; however, as the joints solidify (around 180°C for small lead-free joints), increased stress is observed on the package. In particular, as the package (laminate, solder and chip) begins to cool, the solder
10 begins to solidify (e.g., at about 180° C) and the laminate begins to shrink as the chip remains substantially the same size. The difference in thermal expansion between the chip and the substrate is accommodated by out-of-plane deformation of the device and the substrate, and by the shear deformation of the solder joints. The peak stresses on the device occur during the cool down portion of the reflow.

15 As the solder is robust and exceeds the strength of the chip, tensile stresses begin to delaminate structures on the chip. The high shear stresses caused by the TCE mismatch between the chip (3.5ppm) and the laminate (16ppm) results in an interfacial failure (i.e., a separation between the BEOL copper and the dielectric (e.g., FSG) under the C4). This
20 interfacial failure embodies itself as cracks in the chip metallurgy under C4 bumps. Additionally, there is also a tendency for Sn to diffuse down from the Pb-free solder bump through the BLM/capture pad structure and into the last-metal copper layer, due to inadequate barrier integrity in these overlying films. When this happens, the copper in the last metal level undergoes volume expansion in reaction with the Sn, and creates a crack.

25 Accordingly, there exists a need in the art to overcome the deficiencies and limitations described hereinabove.

SUMMARY

30 In a first aspect of the invention, a method of manufacturing a semiconductor structure comprises forming a plurality of trenches in a dielectric layer extending to an underlying

metal layer. The method further comprises depositing metal in the plurality of trenches to form discrete metal line islands in contact with the underlying metal layer. The method also comprises forming a solder bump in electrical connection to the plurality of metal line islands.

5

In a second aspect of the invention, a method of manufacturing a package comprises: forming a plurality of discrete trenches in a dielectric layer extending to an underlying metal layer; depositing a metal liner in the plurality of discrete trenches; depositing a metal material over the metal liner to form discrete metal line islands in contact with the underlying metal layer; depositing a lead free solder bump in electrical connection to the plurality of discrete metal line islands; and bonding a laminate structure to the lead free solder bump.

10

15

In a third aspect of the invention, a solder bump structure comprises a dielectric layer having a plurality of discrete trenches filled with a conductive material in contact with an underlying metal layer in the dielectric layer. A metal layer is formed in electrical contact with the plurality of discrete trenches filled with the conductive material. A solder bump is in electrical connection with the metal layer.

20

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The present invention is described in the detailed description which follows, in reference to the noted plurality of drawings by way of non-limiting examples of exemplary embodiments of the present invention.

25

FIGS. 1-8 show structures and respective processing steps in accordance with an aspect of the invention.

30

DETAILED DESCRIPTION

The invention relates to integrated circuits and, more particularly, to structures with improved solder bump connections and methods of fabricating such structures. More

specifically, the present invention provides structures and methods of manufacturing such structures which stops fatigue cracks or delamination from occurring in underlying BEOL (back end of line) vias and related metal interconnects and/or pads and/or wires. For example, in implementation, the present invention prevents C4 stresses from being translated to an entire wiring level where it can result in a catastrophic wiring failure. Also, the segmentation of the last-metal copper into islands per will limit any catastrophic propagation of that crack, in the event the copper in the last metal level undergoes volume expansion in reaction with the Sn, and creates a crack. This can be accomplished by providing discrete metal islands or segments of a wiring layer, which prevent stresses imposed during a cooling period from delaminating an entire wiring layer, rendering the device inoperable.

The present invention is applicable to all C4 processes, including plating, screening, and physical placement methods such as, for example, C4NP (Controlled Collapse Chip Connection New Process). C4NP, pioneered by International Business Machines Corp., provides flip chip technology combining the advantages of 100 percent lead-free, high reliability, fine pitch, lower material cost, as well as the flexibility to use virtually all types of solder compositions. The processes and structures herein can be used for known and upcoming generations, and is especially applicable to 300mm wafer technology using C4NP. Accordingly, the processes of the present invention will provide benefits for future copper wiring generations.

In particular, FIG. 1 shows a beginning structure comprising a lower metal layer 12 formed in a dielectric material 10. The lower metal layer 12 may be, for example, a copper material lined with a diffusion barrier layer of tantalum nitride, for example. Those of skill in the art will recognize that the metal layer 12 is not limited to copper lined with tantalum nitride, but may be, for example, any conductive metal lined titanium nitride or other diffusion barrier layers. The dielectric material 10 may be, for example, SiO₂.

A plurality of trenches 14 is formed in the dielectric material 10, extending to the underlying metal layer 12, e.g., wire. The trenches 14 form isolated, discrete segments, which are designed to prevent cracks from affecting an entire metal layer (which would otherwise result in device failure). The trenches 14 can be formed using any conventional lithographic

and etching processes. For example, the formation of the trenches 14 can be processed using conventional photolithography using a masking layer exposed to light to form openings, and a subsequent etching (e.g., reactive ion etching (RIE)) technique to form the trenches 14 in the dielectric material 10. This may be a two step etching process in that the trenches
5 include two different cross sectional shapes. As these are conventional processes, further explanation is not required for a person of ordinary skill in the art to practice the invention.

The trenches 14 can range from 1 micron to 10 microns across and can be several different shapes and sizes (e.g., smaller and larger openings). The trenches 14 can include radial or
10 arc-shaped offset segments surrounding several sized openings. In embodiments, the trenches 14 can include patterns of one or more openings or shapes such as a grid pattern, checkerboard pattern, segmented lines, overlapping lines, offset lines, perpendicular lines, arc segments or any combination discussed herein.

FIG. 2 shows a metal liner 16, e.g., diffusion barrier layer, deposited in the trenches 14. The metal liner 16 may be, for example, a tantalum nitride material. The metal liner 16 is deposited using a conventional deposition method such as, for example, physical vapor deposition (PVD); although other deposition techniques can also be used with the present invention, e.g., chemical vapor deposition (CVD). A chemical mechanical polishing (CMP)
15 can be performed to planarize the surface of the structure of FIG. 2.

In FIG. 3, a metal material 18 is deposited in the trenches 14. The metal material 18 may be used to form an upper wiring level. More specifically, the metal material 18 may be BEOL wiring structures formed in trenches of the dielectric layer 10. The copper wirings 18 are
25 formed as islands (due to the arrangement of the trenches) such that stresses imposed on the structure will only delaminate an outer island, and will not affect the entire metal layer. This will prevent device failure from occurring when stresses are imposed on the structure. A chemical mechanical polishing (CMP) can also be performed to planarize the surface of the structure of FIG. 3.

In FIG. 4, dielectric layers 20, 22 are deposited on the planarized surface of the structure of FIG. 3. The dielectric layer 20 may be, for example, SiN. Alternatively, the dielectric layer
30

20 may be a layered structure of SiN, SiO₂ and SiN. The dielectric layer 22 may be a photosensitive polyimide or other type of insulative material deposited on the dielectric layer 20. The dielectric layers 20, 22 can be deposited using a conventional deposition technique such as, for example, CVD. In embodiments, the dielectric layers 20, 22 can range in thickness from about 5 to 10 microns in height; although other dimensions are also contemplated by the invention. In the case of photosensitive polyimide, the dielectric layer 22 can be about 5 microns in thickness.

Referring to FIG. 5, the dielectric layers 20, 22 are subject to a patterning step in order to form a via 23. In embodiments, in the case of a photosensitive polyimide, the photosensitive polyimide can be exposed and developed, without the need for a conventional etching process (e.g., RIE). In embodiments using other insulative materials, a conventional lithography and etching process can be used to form the via 23.

A ball limiting metallurgy (BLM) 26 is deposited in the via 23 and over portions of the layer 22. The BLM 26 makes contact with the underlying islands 18. The BLM 26 can be a UBM/BLM pad or capture pad structure 26. The ball limiting metallurgy (BLM) or under bump metallurgy (UBM) can be, for example, made of several layers such as, for example, a nickel material sandwiched between an upper gold layer and a bottom barrier layer. The barrier layer may be a TiW barrier layer with a thickness of typically about 1000 Å to 2000 Å; although other dimensions are contemplated by the invention. The gold layer may be typically about 500 -1000 Å; although other dimensions are also contemplated by the invention. The nickel layer may be typically about few microns in thickness; although other dimensions are also contemplated by the invention. In other embodiments, the capture pad 26 may be CrCu/Cu. A capture pad area may range from about 1 micron to 500 microns, with a preferred spacing (width) of about 50 microns. The UBM/BLM pad or capture pad structure 26 can also be comprised of other materials such as, for example, a refractory metal base layer (e.g., TiW), a conductive metal interlayer (e.g. Cu or CrCu), and a diffusion barrier top-layer (e.g., Ni), for example.

In FIG. 7, a solder bump is deposited on the capture pad area. More specifically, a lead-free solder bump 28 such as, for example, tin/copper, tin/silver and tin/gold in combination with SAC alloys, is deposited on the capture pad 26.

5 FIG. 8 shows a packaged chip generally designated as reference numeral 50. The packaged chip 50 shows the solder bump 28 connected to a bonding pad 30 of a laminate 32. The laminate 32 can be an organic or ceramic laminate. FIG. 8 also graphically shows fatigue crack termination in BLM segment (capture pad 30).

10 As should be understood by those of skill in the art, the present invention provides a metal wiring island pattern designed to prevent delamination of an entire wiring layer. With the island pattern, a crack or delamination of a single copper island 18a will not result in device failure. That is, an island 18a at a periphery of the C4/BLM structure will cause an interruption of the stresses which, in turn, acts as a termination point for the propagation of
15 the crack. In this way, any initiated crack or delamination will stop at a single wiring section and hence not propagate along the entire interface between the intermetallic (IMC) compound in the BLM and the solder material. This structure is applicable to any two parts being joined with a C4 solder bump, particularly for lead free C4s, and including any chip stacking or "3D" application.

20 Those of skill in the art should now understand that the present invention adds an additional segmentation pattern designed to prevent delamination of an entire wiring layer. With the additional segmentation pattern, stresses will be interrupted at a periphery of the wiring layer which, in turn, acts as a termination point for the propagation of any crack. That is, the outer
25 peripheral segment of the TaN/TiW layer 36a (in addition to the segment 18a) will cause an interruption of the stresses which, in turn, acts as termination points for the propagation of the crack. In this way, the C4 fatigue crack will stop at a single interconnect and hence not propagate along the entire interface between the intermetallic (IMC) compound in the BLM and the solder material. This structure is applicable to any two parts being joined with a C4
30 solder bump, particularly for lead free C4s, and including any chip stacking or "3D" application.

The methods as described above are used in the fabrication of integrated circuit chips. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

The corresponding structures, materials, acts, and equivalents of all means or step plus function elements, if any, in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope of the invention. The embodiments were chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated.

CLAIMS

1. A method of manufacturing a semiconductor structure, comprising:
forming a plurality of discrete trenches in a dielectric layer extending to an
underlying metal layer;
depositing metal in the plurality of discrete trenches to form discrete metal line
islands in contact with the underlying metal layer; and
forming a solder bump in electrical connection to the plurality of discrete metal line
islands.
2. The method of claim 1, further comprising forming intermediate metal layers
between the solder bump and the discrete metal line islands.
3. The method of claim 2, wherein the intermediate metal layers include a capture pad
and a conductive pad.
4. The method of claim 3, wherein the capture pad is deposited over the conductive pad.
5. The method of claim 3, wherein the capture pad includes a nickel material
sandwiched between an upper gold layer and a bottom barrier layer.
6. The method of claim 3, wherein the capture pad is an under bump metallurgy or a
ball limiting metallurgy.
7. The method claim 6, wherein the under bump metallurgy or ball limiting metallurgy
includes a refractory metal base layer, a conductive metal interlayer and a diffusion barrier
top-layer.
8. The method of claim 1, wherein the solder bump is a lead free solder bump.
9. The method of claim 1, wherein the forming a plurality of discrete trenches includes
openings of various sizes and shapes in the dielectric layer.

10. A method of manufacturing a structure as claimed in claim 8, wherein the depositing metal comprises depositing a metal liner in the plurality of discrete trenches, and depositing a metal material over the metal liner to form discrete metal line islands in contact with the underlying metal layer; the method further comprising bonding a laminate structure to the lead free solder bump.

11. The method of claim 10, wherein the forming a plurality of trenches includes openings of various sizes and shapes in the dielectric layer.

12. A solder bump structure, comprising:
a dielectric layer having a plurality of discrete metal line islands composed of a conductive material in contact with underlying metal layer in the dielectric layer; and
a solder bump in electrical connection with the metal layer.

13. The structure of claim 12, further comprising a laminate bonded to the solder bump.

14. The structure of claim 12, wherein the solder bump is a lead free solder bump.

15. The structure of claim 12, wherein the conductive material is copper.

16. The structure of claim 15, wherein the copper is lined with a barrier layer.

17. The structure of claim 12, wherein the plurality of discrete metal line islands are of various sizes and shapes.

18. The structure of claim 12, further comprising a capture pad in electrical contact with the solder bump.

19. The structure of claim 13, further comprising an under bump metallurgy or ball limiting metallurgy between the solder bump and the discrete metal line islands, wherein the under bump metallurgy or ball limiting metallurgy includes a refractory metal base layer, a conductive metal interlayer and a diffusion barrier top-layer.

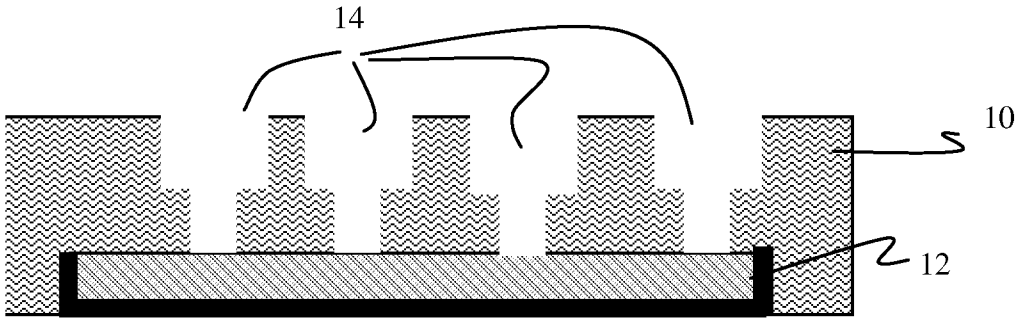


FIG. 1

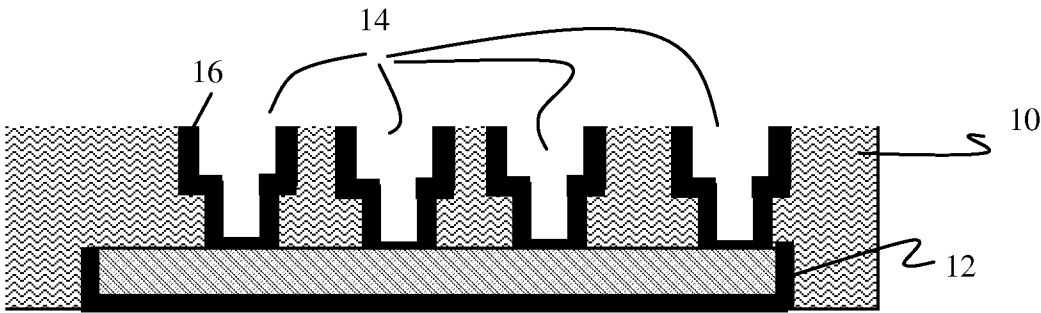


FIG. 2

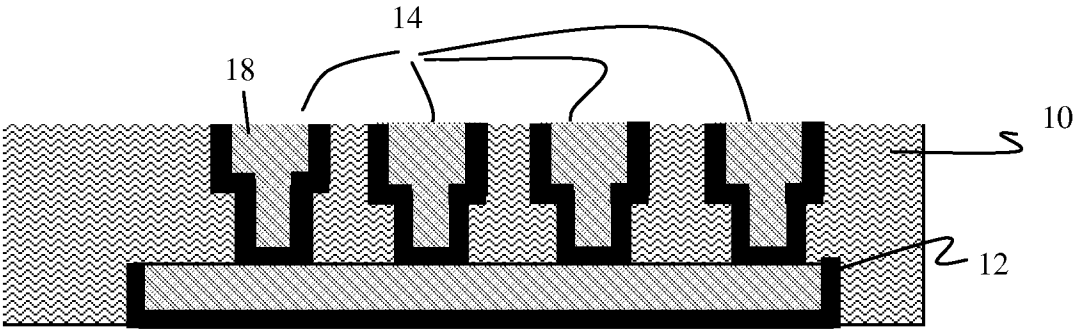


FIG. 3

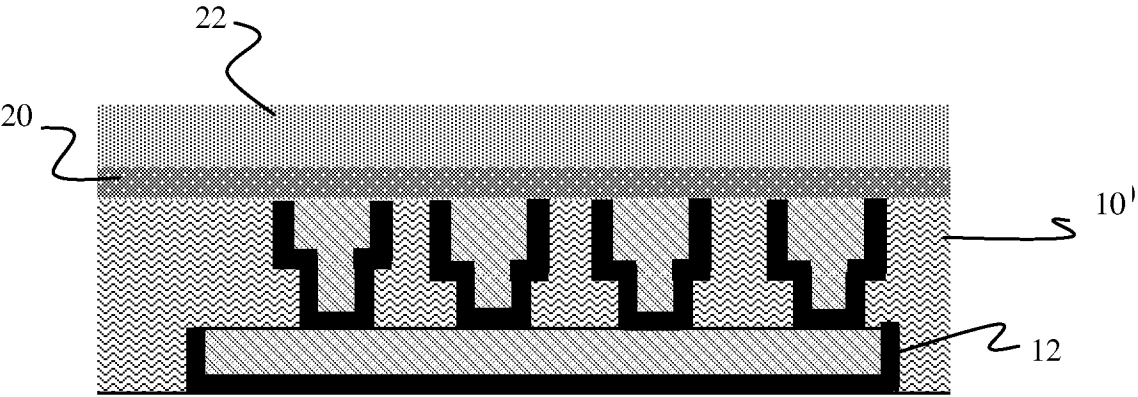


FIG. 4

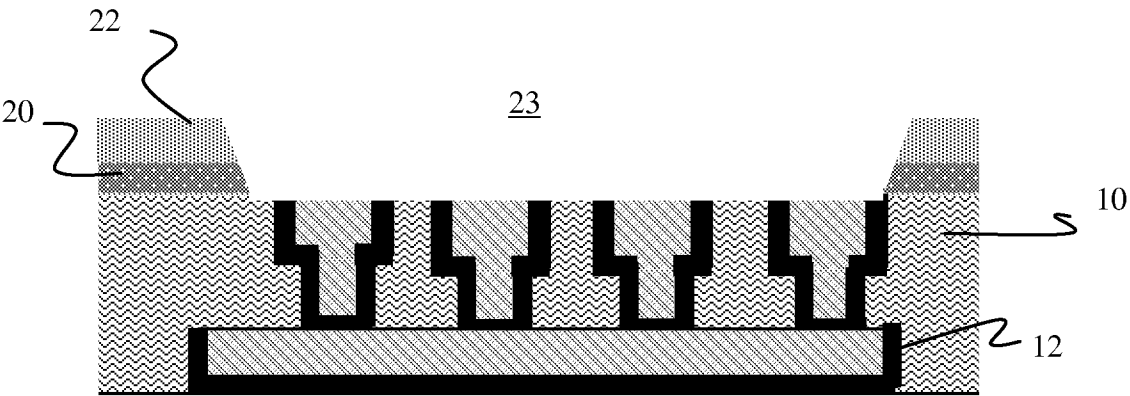


FIG. 5

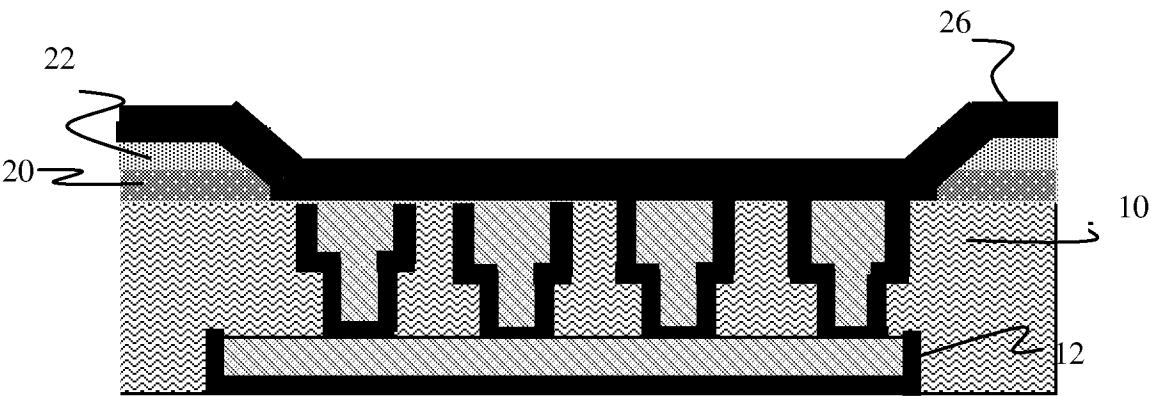


FIG. 6

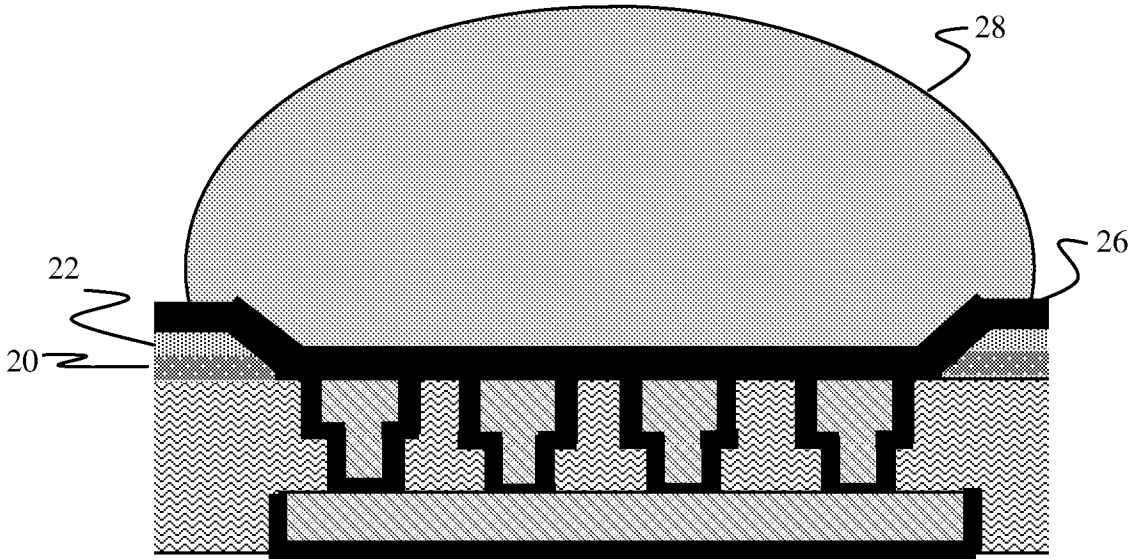


FIG. 7

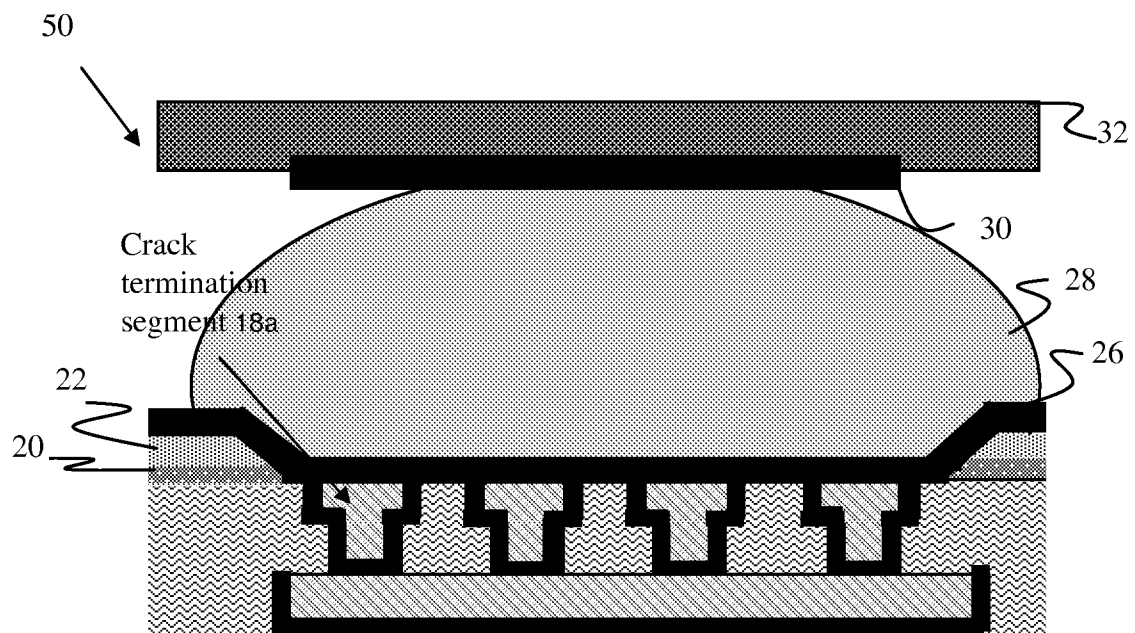


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/064260

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/60 H01L23/485

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EP0-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2007/127816 A2 (IBM [US]; FAROOQ MUKTA G [US]; DAUBENSPECK TIMOTHY H [US]; SAUTER WOLF) 8 November 2007 (2007-11-08)	1-4,6-19
Y	figure 13 paragraphs [0001], [0 38] claim 1	5
Y	----- US 2008/079461 A1 (LIN MOU-SHIUNG [TW] ET AL) 3 April 2008 (2008-04-03) figure 15L paragraph [0384]	5
A	----- US 2006/244156 A1 (CHENG TAO [TW] ET AL) 2 November 2006 (2006-11-02) figures 3-5 paragraph [0019] - paragraph [0024] ----- -/--	9,11,17

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *&* document member of the same patent family

Date of the actual completion of the international search

27 January 2010

Date of mailing of the international search report

02/02/2010

Name and mailing address of the ISA/
European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Crampin, Nicola

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/064260

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>US 2006/125118 A1 (YAMAZAKI YASUSHI [JP]) 15 June 2006 (2006-06-15) figure 3 paragraph [0040] - paragraph [0043] -----</p>	9,11,17

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2009/064260

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2007127816 A2	08-11-2007	EP 2020023 A2 US 2007252274 A1	04-02-2009 01-11-2007
US 2008079461 A1	03-04-2008	US 2008080111 A1 US 2008080112 A1 US 2008111242 A1 US 2008081458 A1 US 2008080113 A1 US 2008081457 A1	03-04-2008 03-04-2008 15-05-2008 03-04-2008 03-04-2008 03-04-2008
US 2006244156 A1	02-11-2006	CN 1855468 A	01-11-2006
US 2006125118 A1	15-06-2006	JP 2006165419 A	22-06-2006