



(51) International Patent Classification:

H01L 25/075 (2006.01) H01L 25/18 (2006.01)
H01L 27/15 (2006.01)

(21) International Application Number:

PCT/US2017/038087

(22) International Filing Date:

19 June 2017 (19.06.2017)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

15/190,813 23 June 2016 (23.06.2016) US

(71) Applicant: SHARP KABUSHIKI KAISHA [—/JP]; 1 Takumi-cho, Sakai-ku, Sakai City, Osaka 590-8522 (JP).

(72) Inventors: SCHUELE, Paul, John; C/o Sharp Laboratories Of America, Inc., 5750 Nw Pacific Rim Blvd., Camas, WA 98607 (US). HEINE, David, Robert; C/o Sharp Laboratories Of America, Inc., 5750 Nw Pacific Rim Blvd., Camas, WA 98607 (US). CROWDER, Mark Albert; C/o Sharp Laboratories Of America, Inc., 5750 Nw Pacific Rim Blvd., Camas, WA 98607 (US). GARNER, Sean, Mathew; C/o Sharp Laboratories Of America, Inc., 5750 Nw Pacific Rim Blvd., Camas, WA 98607 (US). ZHAN, Changqing; C/o Sharp Laboratories Of America, Inc., 5750 Nw Pacific

ic Rim Blvd., Camas, WA 98607 (US). SHINDE, Avinash Tukaram; C/o Sharp Laboratories Of America, Inc., 5750 Nw Pacific Rim Blvd., Camas, WA 98607 (US). SASAKI, Kenji Alexander; C/o Sharp Laboratories Of America, Inc., 5750 Nw Pacific Rim Blvd., Camas, WA 98607 (US). ULMER, Kurt, Michael; C/o Sharp Laboratories Of America, Inc., 5750 Nw Pacific Rim Blvd., Camas, WA 98607 (US).

(74) Agent: HAMILTON, Douglas M.; Hamilton DeSanctis and Cha, Financial Plaza at Union Square, 225 Union Boulevard, Suite 150, Lakewood, CO 80228 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,

(54) Title: DIODES OFFERING ASYMMETRIC STABILITY DURING FLUIDIC ASSEMBLY

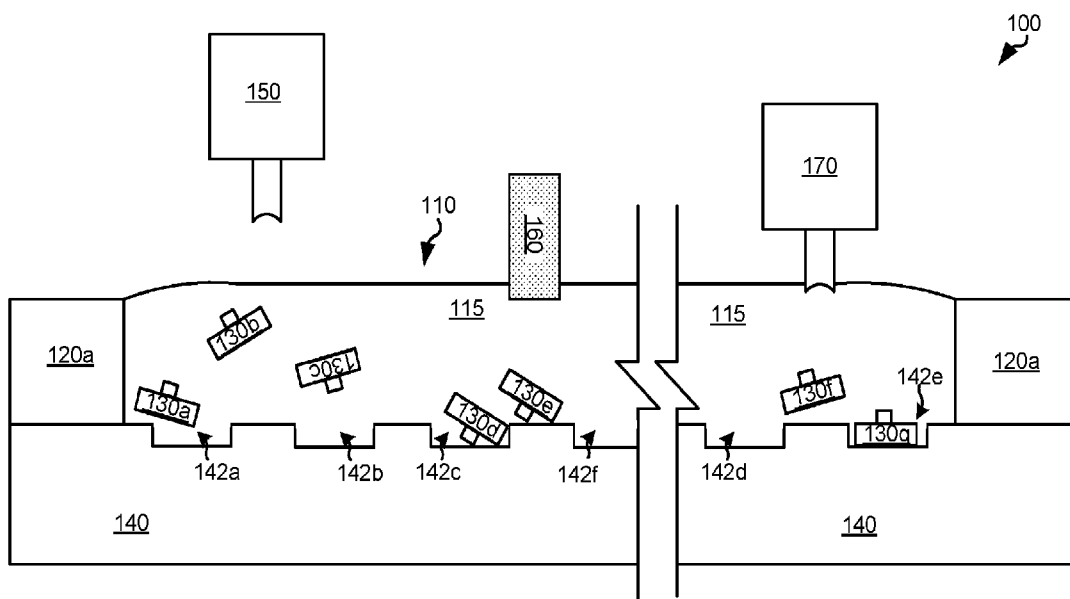


Fig. 1

(57) Abstract: Embodiments are related to systems and methods for fluidic assembly, and more particularly to systems and methods for assuring deposition of elements in relation to a substrate.

WO 2017/222960 A1

TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

Diodes Offering Asymmetric Stability During Fluidic Assembly

FIELD OF THE INVENTION

[0001] Embodiments are related to systems and methods for fluidic assembly, and more particularly to systems and methods for assuring deposition of elements in relation to a substrate.

BACKGROUND

[0002] LED displays, LED display components, and arrayed LED devices include a large number of diodes formed or placed at defined locations across the surface of the display or device. Forming or placing such a large number of diodes often results in low throughput or in a number of defects which reduce the yield of a display or device manufacturing process. Some approaches to increasing throughput and yield include adding additional diodes per pixel to provide enough redundancy to ensure that at least a sufficient number of diodes per pixel are properly formed. This type of approach offers enhanced yield, but without adding a large number of redundant diodes per pixel, display yields are often still lower than desired. Any yield less than one hundred percent within a display is costly both in an impact on profits and an impact on manufacturing throughput.

[0003] Hence, for at least the aforementioned reasons, there exists a need in the art for advanced systems and methods for manufacturing LED displays, LED display components, and LED devices.

SUMMARY

[0004] Embodiments are related to systems and methods for fluidic assembly, and more particularly to systems and methods for assuring deposition of elements in relation to a substrate.

[0005] This summary provides only a general outline of some embodiments of the invention. The phrases “in one embodiment,” “according to one embodiment,” “in various embodiments”, “in one or more embodiments”, “in particular embodiments” and the like generally mean the particular feature, structure, or characteristic following the phrase is included in at least one embodiment of the present invention, and may be included in more than one embodiment of the present invention. Importantly, such phrases do not necessarily refer to the same embodiment. Many other embodiments of the invention will become more fully apparent from the following detailed description, the appended claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE FIGURES

[0006] A further understanding of the various embodiments of the present invention may be realized by reference to the figures which are described in remaining portions of the specification. In the figures, like reference numerals are used throughout several figures to refer to similar components. In some instances, a sub-label consisting of a lower case letter is associated with a reference numeral to denote one of multiple similar components. When reference is made to a reference numeral without specification to an existing sub-label, it is intended to refer to all such multiple similar components.

[0007] Fig. 1 depicts a fluidic assembly system capable of moving a suspension composed of a carrier liquid and a plurality of post enhanced diodes relative to the surface of a substrate in accordance with one or more embodiments of the present inventions;

[0008] Figs. 2a-2e show a portion of a display including a substrate having a number of wells each filled with a respective post enhanced diode in accordance with embodiments of the present inventions;

[0009] Figs. 3a-3d show a portion of a display including a well into which a post enhanced diode can be deposited in accordance with some embodiments of the present inventions;

[0010] Figs. 4a-4d show a portion of a display including a through hole via well into which a post enhanced diode can be deposited in accordance with other embodiments of the present inventions;

[0011] Figs. 5a-5d show a portion of a display including a concentric grooved well into which a post enhanced diode can be deposited in accordance with one or more embodiments of the present inventions;

[0012] Figs. 6a-6b are top views of alternate groove patterns in accordance with other embodiments of the present inventions;

[0013] Fig. 7 is a flow diagram depicting a method for forming a post enhanced diode in accordance with some embodiments of the present inventions; and

[0014] Figs. 8-9 are flow diagrams showing methods for depositing or placing post enhanced diodes into substrate wells in accordance with various embodiments of the present inventions.

DETAILED DESCRIPTION OF SOME EMBODIMENTS

[0015] Embodiments are related to systems and methods for fluidic assembly, and more particularly to systems and methods for assuring deposition of elements in relation to a substrate.

[0016] Various embodiments of the present inventions provide fluidic assembly systems that include: a substrate and a suspension. The substrate includes a plurality of wells, and the suspension includes a carrier liquid and a plurality of post enhanced diodes each including a post extending from a top surface of a diode structure. In some instances of the aforementioned embodiments, the systems further include a suspension movement device operable to move the suspension over the substrate such that a portion of the plurality of post enhanced diodes deposit in respective ones of the plurality of wells.

[0017] In various instances of the aforementioned embodiments, the diode structure of the post enhanced diodes includes: the top surface formed at least in part of a first electrically conductive material; a planar bottom surface formed at least in part of a second electrically conductive

material; a first electrical contact configured to conduct charge to the first electrically conductive material; and a second electrical contact configured to conduct charge to the second electrically conductive material. In one or more instances of the aforementioned embodiments, each of the plurality of wells includes a through hole via extending through the substrate from the bottom of the respective well. In some such cases, a width of a surface of the post substantially parallel to the top surface of the diode structure is greater than a width of the through hole via. In other such cases, the through hole via is off center from a substantially circular shaped bottom of the respective well.

[0018] In some instances of the aforementioned embodiments, a maximum width of the bottom surface is less than a maximum width of each of the plurality of wells. In various instances of the aforementioned embodiments, an electrical contact is formed on an interior surface of each of the plurality of wells. In some instances of the aforementioned embodiments, an orientation of each of the plurality of post enhanced diodes where the post extends away from the substrate is a non-inverted orientation, wherein an orientation of each of the plurality of post enhanced diodes where the post extends toward the substrate is an inverted orientation, and wherein one of the plurality of post enhanced diodes deposited in a respective well is more mechanically stable in the non-inverted orientation than in the inverted orientation. In one or more instances of the aforementioned embodiments, an orientation of each of the plurality of post enhanced diodes where the post extends away from the substrate is a non-inverted orientation, an orientation of each of the plurality of post enhanced diodes where the post extends toward the substrate is an inverted orientation, and an orientation of one of the plurality of post enhanced diodes in contact with a surface of the substrate is more mechanically stable in the non-inverted orientation than in the inverted orientation.

[0019] In various instances of the aforementioned embodiments, an orientation of each of the plurality of post enhanced diodes where the post extends away from the substrate is a non-inverted orientation, an orientation of each of the plurality of post enhanced diodes where the post extends toward the substrate is an inverted orientation, and the substrate further includes at least one groove configured such that an orientation of one of the plurality of post enhanced diodes traversing the groove is more mechanically stable in the non-inverted orientation than in the inverted orientation. In some such instances, the groove extends into the substrate with a

leading edge exhibiting a slope greater than a trailing edge, and whereupon moving the suspension over the substrate one of the post enhanced diodes crosses the trailing edge before crossing the leading edge. In various such instances, a depth of the groove into the substrate is less than a distance from an edge of the top surface of the diode structure to an edge of the post. In one or more such instances, a width of the groove at a surface of the substrate is less than a distance from an edge of the top surface of the diode structure to an edge of the post.

[0020] Other embodiments of the present inventions provide post enhanced diodes. Such post enhanced diodes include: a planar top surface formed at least in part of a first electrically conductive material; a planar bottom surface formed at least in part of a second electrically conductive material; a post extending from the top surface; a first electrical contact configured to conduct charge to the first electrically conductive material; and a second electrical contact configured to conduct charge to the second electrically conductive material.

[0021] In some instances of the aforementioned embodiments, the top surface exhibits a first maximum width, a surface of the post that is substantially parallel to the top surface exhibits a second maximum width, and the first maximum width is at least two times the second maximum width. In various instances of the aforementioned embodiments, the height of the post is measured from the top surface to the surface of the post that is substantially parallel to the top surface and the thickness of the diode structure is measured from the top surface and the bottom surface. In some cases, the thickness-to-height ratio is in a range of 1:0.6 to 1:4. In one or more instances of the aforementioned embodiments, the top surface exhibits a maximum width and the thickness of the diode structure is measured from the top surface and the bottom surface. In some cases, the maximum width-to-thickness aspect ratio is in a range of 5:1 to 50:1.

[0022] In some instances of the aforementioned embodiments, the post is the first electrical contact. In various instances of the aforementioned embodiments, the post is formed of an insulator material. In some cases, the top surface is circular in shape, while in other instances the top surface is polygonal in shape. In particular cases, the top surface is hexagonal in shape with a width of each facet of the hexagon sufficiently small to allow the top surface to fit within a given well. In various instances of the aforementioned embodiments, a surface of the post that is substantially parallel to the top surface has a shape circular in shape, while in other instances it is polygonal in shape. In one or more instances of the aforementioned embodiments, the post is

formed of a third conductive material which, in some cases, is the same as the first conductive material. In some cases, the first conductive material is a p-doped semiconductor material, and the second conductive material is an n-doped semiconductor material. In some cases the post can have a rounded top surface or surface with complex curvature, and in other cases it can have a substantially flat top surface. In other cases, multiple posts may exist on the diode top surface. The posts can be center on the diode surface or they can be off-set.

[0023] Yet other embodiments provide substrates for fluidic assembly. Such substrates include: a plurality of wells extending from a top surface of the substrate, where each of the plurality of wells is configured to accept a post enhanced diode; and at least one groove extending into the top surface of the substrate and configured such that an orientation of the post enhanced diodes traversing the groove is more mechanically stable in a non-inverted orientation than in an inverted orientation. The post enhanced diode includes a post extending from a top surface of a diode structure. When the post enhanced diode is in a non-inverted orientation, the post extends away from the top surface of the substrate. When the post enhanced diode is in an inverted orientation, the post extends toward the top surface of the substrate. In some instances of the aforementioned embodiments, a depth of the groove into the substrate is less than a distance from an edge of the top surface of the diode structure to an edge of the post. In various instances of the aforementioned embodiments, a width of the groove at a surface of the substrate is less than a distance from an edge of the top surface of the diode structure to an edge of the post.

[0024] Turning to Fig. 1, a fluidic assembly system 100 capable of moving a suspension 110 composed of a carrier liquid 115 and a plurality of post enhanced diodes 130 relative to the surface of a substrate 140 is shown in accordance with one or more embodiments of the present inventions. In some embodiments, substrate 140 is formed of a polymer material laminated to the surface of a glass substrate. In particular embodiments, wells 142 are etched or otherwise formed in the laminate layer. As used herein, the term "well" is used in its broadest sense to mean any surface feature into which a post enhanced diode may be deposited. In other embodiments, the substrate is made of glass with wells 142 directly formed into the glass. Wells 142 may have flat and vertical surfaces as shown, or they may have bottoms and sides with complex curvatures. Based upon the disclosure provided herein, one of ordinary skill in the art

will recognize a variety of materials, processes, and/or structures that may be used to form substrate 140. For example, substrate 140 can be formed of any material or composition compatible with fluidic device processing. This can include, but is not limited to, glass, glass ceramic, ceramic, polymer, metal, or other organic or inorganic materials. As examples, wells 142 can be defined in a single material forming a surface feature layer when applied to the surface of a base glass sheet. It is also possible for patterned conductor layers to exist between wells 142 formed in such a surface feature layer and the base glass layer. Substrate 140 can also be made of multiple layers or combinations of these materials. Substrate 140 may be a flat, curved, rigid, or flexible structure. In some cases, substrate 140 may end up being the final device substrate or it may only serve as an assembly substrate to position post enhanced diodes 130. In the case of an assembly substrate, post enhanced diodes 130 would then be transferred to the final device substrate in subsequent steps.

[0025] In some embodiments, carrier liquid 115 is isopropanol. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of liquids, gasses, and/or liquid and gas combinations that may be used as the carrier liquid. It should be noted that various analysis provided herein is based upon flow in a single, continuous direction or in other cases a relatively simple back-forth motion, but that the flow may be more complex where both the direction and magnitude of fluid velocity can vary over time.

[0026] As shown in Fig. 1, post enhanced diodes 130 each include a relatively large diode structure and a smaller post extending from a top surface of the diode structure, and wells 142 in substrate 140 are each capable of receiving a given post enhanced diode 130 in a non-inverted orientation. As used herein, the phrase "post enhanced diode" is used broadly to mean any device with a post extending from a surface of either an anode or cathode of a diode structure such that at least a portion of an outer edge of the post is set back from an edge of the diode structure. As used herein the phrase "non-inverted orientation" is used in its broadest sense to mean any orientation of a post enhanced diode 130 with the post extending generally away from the top surface of substrate 140 (i.e., away from the bottom of wells 142); and as used herein the phrase "inverted orientation" is used in its broadest sense to mean any orientation of a post enhanced diode 130 with the post extending generally toward the top surface of substrate 140 (i.e., toward from the bottom of wells 142). Using these definitions, post enhanced diodes 130a,

130b, 130f, and 130g are each in a non-inverted orientation; and post enhanced diodes 130c, 130d, and 130e are each in an inverted orientation. The diode structure and post of post enhanced diodes 130 are discussed in greater detail below in relation to Figs. 2a-2e. It should be noted that in some cases the diode structure including an anode on one side and a cathode on the other can be referred to as asymmetric due to the different materials on each side of the diode structure, however, the use of the term "asymmetric" in relation to a diode herein refers to any asymmetry of forces generated by liquid movement around a post enhanced diode between an inverted orientation and a non-inverted orientation due to a post extending from the diode structure. In some cases, the depth of wells 142 is substantially equal to the height of the diode structure of each of the post enhanced diodes 130, and the inlet opening of wells 142 is greater than the width of the diode structure of each of the post enhanced diodes 130 such that only one post enhanced diode 130 deposits into any given well 142. It should be noted that while embodiments discuss post enhanced diodes that include a single post extending from a diode structure, that various embodiments provide post enhanced diodes that each include two or more posts each extending from the same diode structure.

[0027] A depositing device 150 deposits suspension 110 over the surface of substrate 140 with suspension 110 held on top of substrate 140 by sides 120 of a dam structure. In some embodiments, depositing device 150 is a pump with access to a reservoir of suspension 110. A suspension movement device 160 agitates suspension 110 deposited on substrate 140 such that post enhanced diodes 130 move relative to the surface of substrate 140. As post enhanced diodes 130 move relative to the surface of substrate 140 they deposit into wells 142 in either a non-inverted orientation or an inverted orientation. In some embodiments, suspension movement device 160 is a brush that moves in three dimensions. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of devices that may be used to perform the function of suspension movement device 160 including, but not limited to, a pump.

[0028] When deposited in the inverted orientation (e.g., post enhanced diode 130d), the movement generated by suspension movement device 160 generates force likely to dislocate an inverted post enhanced diode 130 from a given well 142. In contrast, when deposited in the non-inverted orientation (e.g., post enhanced diode 130g), the force on the deposited, non-inverted post enhanced diode 130 caused by suspension movement device 160 is unlikely to dislocate the

post enhanced diode from a given well 142. In some embodiments, the likelihood of dislocating an inverted post enhanced diode 130 from a well 142 is much greater than the likelihood of dislocating a non-inverted post enhanced diode 130 from a well 142. In some embodiments the moment of force required to dislocate an inverted post enhanced diode 130 from a well 142 is between 0.01×10^{-14} N-m and 1.0×10^{-14} N-m depending upon the width to height ratio of the post and the diameter of the diode structure (where a positive value of the moment of force indicates the diode structure of a post enhanced diode 130 is being forced to rotate about a point of rotation); and the moment of force required to dislocate a non-inverted post enhanced diode 130 from a well 142 is a negative value (where a negative value of the moment of force indicates the diode structure of a post enhanced diode 130 is being pushed down on the surface of substrate 140) for the same width to height ratio of the post and thickness of the diode structure making any displacement unlikely. As used herein, a post enhanced diode is considered "likely to dislocate" where the moment of force is a positive value, and is considered "unlikely to dislocate" where the moment of force is a negative value.

[0029] Similarly, when moving across the surface of substrate 140 in the inverted orientation (e.g., post enhanced diode 130e), the movement generated by suspension movement device 160 generates a force likely to flip an inverted post enhanced diode 130. In contrast, when moving across the surface of substrate 140 in the non-inverted orientation (e.g., post enhanced diode 130f), the force on the non-inverted post enhanced diode 130 caused by suspension movement device 160 is less likely to flip the post enhanced diode. In some embodiments, the likelihood of flipping an inverted post enhanced diode 130 moving near the surface of substrate 140 is greater than the likelihood of flipping a non-inverted post enhanced diode 130 moving similarly near the surface of substrate 140 as the moment of force for the inverted post enhanced diode 130 is greater than the moment of force for the non-inverted post enhanced diode 130.

[0030] A capture device 170 includes an inlet extending into suspension 110 and capable of recovering a portion of suspension 110 including a portion of carrier liquid 115 and non-deposited post enhanced diodes 130, and returning the recovered material for reuse. In some embodiments, capture device 170 is a pump. More detail regarding the interaction of post enhanced diodes 130 with substrate 140 and wells 142 is provided in relation to Figs. 3-5 below.

[0031] Turning to Fig. 2a, a top view 200 of a substrate portion 230 is shown including a number of wells 205 into which post enhanced diodes 210 have been successfully deposited. Each of post enhanced diodes 210 of Fig. 2a are represented in a top view 235 of Fig. 2b, a cross sectional view 250 of Fig. 2c, and a circuit symbol 280 of a post enhanced diode 210 operating as an LED. Post enhanced diodes 210 include one or more features that enable the relative flow of a carrier liquid about post enhanced diodes 210 to create a net moment of force for increasing a likelihood of flipping post enhanced diodes 210 from a first orientation to a second orientation, with a dissimilar (i.e., asymmetric) likelihood of flipping post enhanced diodes 210 from the second orientation to the first orientation. These features may include sidewall angles, surface structures such as posts, or the general shape of the post enhanced diodes 210. Notably, the aforementioned structures and shapes of the post enhanced diodes 210 that encourage asymmetric re-orientation may or may not be present in a final display incorporating post enhanced diodes 210.

[0032] As shown in Figs. 2b-2c, post enhanced diode 210 includes a planar top surface 245 of an electrically conductive material 260 (shown as an un-patterned region). As used herein, the term "planar" is used in its broadest sense to mean two dimensional with exception of defects or process related variance standard in semiconductor manufacturing processes. In some embodiments, electrically conductive material 260 is p-doped Gallium Nitride (GaN). A post 255 (shown as a hatched pattern region) extending from top surface 245 is also shown. A top surface 240 of post 255 is also shown. In some embodiments, post 255 is formed of electrically conductive material 260 (i.e., a homogeneous post). In other embodiments, post 255 is formed of a material other than electrically conductive material 260 (i.e., a heterogeneous post). In some cases, a heterogeneous post is formed at least in part of an insulating layer such as SiO₂, and in other cases a heterogeneous post is formed of a conductive material such as a metal compatible with deposition on electrically conductive material 260. It should be noted that while post 255 is shown as substantially centered on top surface 245, in other embodiments post 255 may be offset from a center position at any location from a center point of top surface 245 to a radial distance from the center point such that a portion, but not all of the edges, of post 255 is coextensive with an edge of a diode structure 285. In some cases the post can have a rounded top surface or surface with complex curvature, and in other cases it can have a substantially flat top surface. In other cases, multiple posts may exist on the diode top surface.

[0033] Various approaches may be used for forming post 255 on diode structure 285. For example, fabricating a homogeneous post may include etching the top surface of a thick layer of electrically conductive material 260 to yield the combination of both post 255 and the layer of electrically conductive material 260 shown in cross sectional view 250; or by forming the layer of electrically conductive material 260 followed by selective epitaxial growth using the same material to form post 255. As other examples, fabricating a heterogeneous post may include etching the post from a film that is deposited onto top surface 245 of diode structure 285, or by forming a post with a different material through plating or a templated growth process on top of top surface 245 of diode structure 285. This latter approach permits the use of any material for the post (e.g., dielectrics, metals, etc.). In some cases, photolithography of a photo resist may be used in relation to the aforementioned plating or template growth.

[0034] Top surface 245 includes one or more electrical contacts 282, 286 that conduct charge from a signal source (not shown) to electrically conductive material 260. In some embodiments, electrical contacts 282, 286 are formed of a metal deposited onto the layer of electrically conductive material 260. In other embodiments, electrical contacts 282, 286 are an exposed area of top surface 245 to which a signal source (not shown) can contact electrically conductive material 260. In some embodiments where post 255 is formed of a conductive material it operates as a post. In one particular embodiment where post 255 is formed of electrically conductive material 260, an exposed area of top surface 240 to which a signal source (not shown) can contact electrically conductive material 260 operates as an electrical contact.

[0035] The layer of electrically conductive material 260 is disposed on top of a multiple quantum well (MQW) 265 (shown as a hatched pattern region), which in turn is disposed on top of a layer of an electrically conductive material 270 (shown as an un-patterned region). In some embodiments, electrically conductive material 270 is n-doped Gallium Nitride (GaN). MQW 265 may be formed of any material compatible with both electrically conductive material 260 and electrically conductive material 270, and which when sandwiched between electrically conductive material 260 and electrically conductive material 270 is capable of operating as a light emitting diode (LED). Together, the layer of electrically conductive material 260, MQW 265, and the layer of electrically conductive material 270 form a diode structure of post enhanced diodes 210. Based upon the disclosure provided herein, one of ordinary skill in the art will

recognize a variety of materials and material combinations that may be used in forming diode structure 285 of a given post enhanced diode 210. As different post enhanced diodes 210 are intended to emit light of different wavelengths (e.g., red, green, blue), the construction and/or materials for different instances of post enhanced diodes 210 will vary to achieve a desired color distribution.

[0036] The layer of electrically conductive material 270 includes a planar bottom surface 275. Bottom surface 275 includes one or more electrical contacts 284, 288 that conduct charge from a signal source (not shown) to electrically conductive material 270. In some embodiments, electrical contacts 284, 284 are formed of a metal deposited onto the layer of electrically conductive material 270. In other embodiments, electrical contacts 284, 288 are an exposed area of bottom surface 275 to which a signal source (not shown) can contact electrically conductive material 270. In particular cases, electrical contacts 284, 288 are two sides of the same contact extending as a concentric circle of exposed electrically conductive material 270 around the perimeter of bottom surface 275.

[0037] Post 255 has a width (W_p) and a height (H_p), and diode structure 285 has a width (W_d) and a height (H_d). As more fully discussed below in relation to Fig. 2e, the sides of post 255 and diode structure 285 in some cases are not perfectly vertical and may vary. In such a case, the aforementioned width and height characteristics of post 255 and diode structure 285 are considered to be: the maximum width where the width varies as a function of height, and the maximum height where the height varies as a function of width. In some embodiments, the width:height ratio of diode structure 285 (i.e., $W_d:H_d$) is between 5:1 and 50:1. In some particular embodiments, the width:height ratio of diode structure 285 (i.e., $W_d:H_d$) is between 5:1 and 30:1. In some embodiments, the width:height ratio of post 255 (i.e., $W_p:H_p$) is between 2:1 and 5:1. In various embodiments, the height of diode structure 285 (i.e., H_d) is between $4\mu\text{m}$ and $7\mu\text{m}$, and the height of post 255 (i.e., H_p) is between $2\mu\text{m}$ and $7\mu\text{m}$, in part depending upon the desired ratio of H_d to H_p .

[0038] The dimensions of post 255 can affect the stability of an inverted post enhanced diode 210. In particular, if the post is too small, post enhanced diode 210 will not be as likely to flip into a non-inverted orientation. Numerical modeling of the fluidic process shows that, for a $50\text{-}\mu\text{m}$ -diameter (W_d) diode structure that is $5\text{ }\mu\text{m}$ thick (H_d) exposed to a flow velocity of a carrier

liquid of 4.6mm/s, a post with dimensions of $10\ \mu\text{m} \times 5\ \mu\text{m}$ ($W_p \times H_p$) will flip the disk to the non-inverted orientation. Models with varying post dimensions on a 50- μm -diameter (W_d) disk diode structure that are captured in a 3 μm deep well have shown that small posts (e.g., with a height (H_p) less than or equal to 4 μm) exposed to a similar flow velocity as above, have little influence on the orientation, but a 5- μm high (H_p) post is sufficient to cause an inverted post enhanced diode 210 to flip while a non-inverted post enhanced diode 210 will remain in a non-inverted orientation. Experimental data has demonstrated that the modeling revealing the aforementioned dimensions is reliable, and that a post with dimensions of $12\mu\text{m} \times 3\mu\text{m}$ ($W_p \times H_p$) is able to influence the orientation of fluidically-aligned disks, with a yield of over 99.7% of disks (out of 150 disks) having a desired non-inverted orientation. The following table shows additional modeling data for the net moment of force for inverted post enhanced diodes 210 having different diode structure widths (W_d) and ratios of post height to width ($H_p \times W_p$):

	$W_p \times H_p = 10 \times 5$	$W_p \times H_p = 15 \times 5$	$W_p \times H_p = 20 \times 5$	$W_p \times H_p = 20 \times 7$
$W_d = 40 \mu\text{m}$	$+0.29 \times 10^{-14} \text{N-m}$	--	--	--
$W_d = 50 \mu\text{m}$	$+0.52 \times 10^{-14} \text{N-m}$	--	--	--
$W_d = 70 \mu\text{m}$	$-0.29 \times 10^{-14} \text{N-m}$	$-0.11 \times 10^{-14} \text{N-m}$	$+0.07 \times 10^{-14} \text{N-m}$	--
$W_d = 90 \mu\text{m}$	$-1.57 \times 10^{-14} \text{N-m}$	$-1.33 \times 10^{-14} \text{N-m}$	$-1.13 \times 10^{-14} \text{N-m}$	$+0.09 \times 10^{-14} \text{N-m}$

[0039] Turning to Fig. 2e, a cross sectional view 290 of another embodiment of a post enhanced diode 210 where side walls 291, 292 of post 255 and sidewalls 295, 296 of diode structure 285 each exhibit a tapered slope compared with the vertical slope shown in cross sectional view 250 of Fig. 2c. As discussed above, where the sidewalls are tapered (i.e., vary as a function of height), the width of the post (W_p) is the maximum width thereof, and the width of diode structure 285 (W_d) is the maximum width thereof as shown in cross sectional view 290. The taper exhibited by the sidewalls will vary dependent upon the processes and materials used for constructing post enhanced diodes 130 as is known in the art. Similar tapering may occur on the sides of wells 205. It should be noted that addition of the post to diode structure 285 results an asymmetry of forces generated by liquid movement around a plate diode between an inverted orientation and a non-inverted orientation. As such, the post need not be a perfectly vertical structure, but rather may be any structure sufficient to result in a net positive moment of force when post enhanced diode 210 is in an inverted orientation, and a substantially lower moment of force when post enhanced diode 210 is in a non-inverted orientation such that post enhanced diodes 210 will prefer a non-inverted orientation. In some cases, the depth of wells 205 is substantially equal to the height of diode structure 285 of each of the post enhanced diodes 210, and the inlet opening of wells 205 is greater than the width of diode structure 285 of each of the post enhanced diodes 210 such that only one post enhanced diode 210 deposits into any given well 205.

[0040] Once post enhanced diodes 210 are deposited in wells 205 with post 255 extending away from substrate portion 230, one or more electrical contacts in wells 205 are connected to

one or more electrical contacts on bottom surface 275 of post enhanced diodes 210, and one or more processing steps are performed to electrically connect one or more electrical contacts on top surface 245 of post enhanced diodes 210 to controllable signals. Upon completion of such processing, post enhanced diodes 210 can be individually controlled causing a display including substrate portion 230 and post enhanced diodes 210 to display a desired image. Post enhanced diodes 210 as discussed herein may be used, among other things, to fabricate both direct emission displays and locally-addressed backlight units.

[0041] Turning to Figs. 3a-3b, a top view 300 and a cross sectional view 301 of a portion of a display including a well 312 into which a post enhanced diode 210 can be deposited is depicted in accordance with some embodiments of the present inventions. As shown, the display includes a substrate 390 composed of a polymer material 315 laminated to the surface of a glass substrate 305. It should be noted that materials other than glass may be used in place of glass substrate. Additionally, other conductive or non-conductive layers may exist between materials 315 and 305. Further, it should be noted that in some cases polymer material 315 may be replaced by glass or another suitable material. In some embodiments, substrate 315 is made by forming an electric contact layer on the surface of glass substrate 305, and etching the electric contact layer to yield an electrical contact 335 at a location corresponding to a future well. It should be noted that while electrical contact 335 is shown as a donut shape, that it may be a solid circle shape as there is not a through hole via or another suitable shape for forming an electrical contact in the bottom of a well. Polymer material 315 is then laminated over glass substrate 305 and electrical contact 335, followed by an etch of polymer material 315 to open well 312 defined by a sidewall 314 and expose a portion of electrical contact 335. Electrical contact 335 may be formed of any material capable of forming an electrical junction with bottom surface 275 of a post enhanced diode 210. In some cases, electrical contact 335 is formed of a metal that when annealed with a post enhanced diode 210 disposed within well 312 forms an electrically conductive location between a signal connected to electrical contact 335 and electrically conductive material 270 of a post enhanced diode 210. In some embodiments, the depth of well 312 is substantially equal to the height of the diode portion (H_d) of a post enhanced diode 210 such that only one post enhanced diode 210 deposits in well 312.

[0042] During fluidic assembly a liquid flow (indicated by arrows 360) results in drag forces on post enhanced diodes 210 traversing the surface of substrate 390. Because post enhanced diodes 210 include a post 255 extending from the diode structure, the drag forces have an asymmetric impact on the orientation of the plate diodes. In particular, the drag forces result in a positive moment of force about a fixed point of rotation (e.g., an edge of the diode structure in contact with the surface of substrate 390) that will flip an inverted post enhanced diode 210 into a non-inverted orientation. In contrast, the drag forces on a non-inverted post enhanced diode 210 due to the liquid flow are primarily due to perturbations around post 255, and the forces exerted on the diode structure of a post enhanced diode 210 lead to a negative net moment of force. This negative net moment of force the leading edge (i.e., the edge leading in the direction of arrows 360) of the diode structure down and stabilizes the post enhanced diode 210 in the non-inverted orientation.

[0043] A similar asymmetric impact of the drag forces occurs between a post enhanced diode 210 deposited in a non-inverted orientation in well 312 (shown in a cross sectional view 302 of Fig. 3c), and a post enhanced diode 210 deposited in an inverted orientation in well 312 (shown in a cross sectional view 303 of Fig. 3d). As shown in Fig. 3c, any moment of force around the lower right corner of post enhanced diode 210 caused by the liquid flow is offset by forces exerted on top surface 245 of post enhanced diode 210 resulting in a negative net moment of force tending to maintain post enhanced diode 210 deposited in well 210. As shown in Fig. 3d, when post enhanced diode 210 is inverted in well 312 top surface 245 acts a hydrofoil generating a lifting force from the liquid flow such that a net positive moment of force results around the right side of post enhanced diode 210 contacting side 314 of well 312. This net positive moment of force tends to cause post enhanced diode 210 to flip in a direction indicated by an arrow 370 such that post enhanced diode 210 is forced out of well 312 and possibly into a non-inverted orientation as the liquid flow moves post enhanced diode 210 toward another downstream well where it may re-deposit.

[0044] Turning to Figs. 4a-4b, a top view 400 and a cross sectional view 401 of a portion of a display including a through hole via well 412 into which a post enhanced diode 210 can be deposited is depicted in accordance with some embodiments of the present inventions. As shown, the display includes a substrate 490 composed of a polymer material 415 laminated to the

surface of a glass substrate 405. Additionally, other conductive or non-conductive layers may exist between materials 415 and 405. It should be noted that materials other than glass may be used in place of glass substrate. Further, it should be noted that in some cases polymer material 415 may be replaced by glass or another suitable material. In some embodiments, substrate 415 is made by forming an electric contact layer on the surface of glass substrate 405, and etching the electric contact layer to yield an electrical contact 435 at a location corresponding to a future well. Polymer material 415 is then laminated over glass substrate 405 and electrical contact 435, followed by an etch of polymer material 415 to open well 412 and expose a portion of electrical contact 435. Electrical contact 435 may be formed of any material capable of forming an electrical junction with bottom surface 275 of a post enhanced diode 210. In some cases, electrical contact 435 is formed of a metal that when annealed with a post enhanced diode 210 disposed within well 412 forms an electrically conductive location between a signal connected to electrical contact 435 and electrically conductive material 270 of a post enhanced diode 210. In some embodiments, the depth of well 412 is substantially equal to the height of the diode portion (Hd) of a post enhanced diode 210 such that only one post enhanced diode 210 deposits in well 412.

[0045] An additional process is performed to form a through hole via 425 extending through glass substrate 405. In some cases, the width of through hole via 425 (Wv) is less than a minimum width of post 255 to assure that post 255 does not insert into through hole via 425 when post enhanced diode 210 is inverted in well 412 as such insertion would limit the ability for post enhanced diode 210 to flip out of well 412. In other cases, through hole via 425 is substantially centered in well 512 and post 255 is considerably off-center on top surface 425 of the diode structure, or through hole via 425 is considerably off-center in the base of well 512 and post 255 is substantially centered on top surface 425 of the diode structure such that when a post enhanced diode 210 deposits in well 512 in an inverted orientation post 255 does not align with through hole via 425.

[0046] During fluidic assembly a liquid flow (indicated by arrows 460) results in drag forces on post enhanced diodes 210 traversing the surface of substrate 490. Because post enhanced diodes 210 include a post 255 extending from the diode structure, the drag forces have an asymmetric impact on the orientation of the plate diodes. In particular, the drag forces result in a

positive moment of force about a fixed point of rotation (e.g., an edge of the diode structure in contact with the surface of substrate 490) that will flip an inverted post enhanced diode 210 into a non-inverted orientation. In contrast, the drag forces on a non-inverted post enhanced diode 210 due to the liquid flow are primarily due to perturbations around post 255, and the forces exerted on the diode structure of a post enhanced diode 210 lead to a negative net moment of force. This negative net moment of force the leading edge (i.e., the edge leading in the direction of arrows 460) of the diode structure down and stabilizes the post enhanced diode 210 in the non-inverted orientation.

[0047] A similar asymmetric impact of the drag forces occurs between a post enhanced diode 210 deposited in a non-inverted orientation in well 412 (shown in a cross sectional view 402 of Fig. 4c), and a post enhanced diode 210 deposited in an inverted orientation in well 412 (shown in a cross sectional view 403 of Fig. 4d). As shown in Fig. 4c, any moment of force around the lower right corner of post enhanced diode 210 caused by the liquid flow is offset by forces exerted on top surface 245 of post enhanced diode 210 resulting in a negative net moment of force tending to maintain post enhanced diode 210 deposited in well 210. As shown in Fig. 4d, when post enhanced diode 210 is inverted in well 412 top surface 245 acts a hydrofoil generating a lifting force from the liquid flow such that a net positive moment of force results around the right side of post enhanced diode 210 contacting a side of well 412. This net positive moment of force tends to cause post enhanced diode 210 to flip in a direction indicated by an arrow 470 such that post enhanced diode 210 is forced out of well 412 and possibly into a non-inverted orientation as the liquid flow moves post enhanced diode 210 toward another downstream well where it may re-deposit.

[0048] Additionally, a suction may be applied to the bottom side of substrate 490. When post enhanced diode 210 deposits in well 412 in a non-inverted orientation such as that shown in cross sectional view 402, the applied suction force further stabilizes post enhanced diode 210 in well 412. It should be noted that the applied suction also provides some stabilization of a post enhanced diode 210 deposited in well 412 in an inverted orientation, but the stabilization due to the suction on a non-inverted post enhanced diode 210 is substantially greater than that on an inverted post enhanced diode 210. Such suction allows for increased assembly speed. Additionally, at the end of fluidic assembly after depositing or placing post enhanced diodes in a

number of wells, a clean up process is performed to remove any excess post enhanced diodes. The addition of the suction force allows for a more aggressive clean up operation including, for example, flowing a cleaning fluid over the surface of substrate 490 at a much higher rate than that used during the deposition process without disturbing the deposited post enhanced diodes 210 held in place in part by the added suction force.

[0049] Turning to Figs. 5a-5b, a top view 500 and a cross sectional view 501 of a portion of a display including a through hole via well 512 into which a post enhanced diode 210 can be deposited is depicted in accordance with some embodiments of the present inventions. As shown, the display includes a substrate 590 composed of a polymer material 515 laminated to the surface of a glass substrate 505. It should be noted that materials other than glass may be used in place of glass substrate. Additionally, other conductive or non-conductive layers may exist between materials 515 and 505. Further, it should be noted that in some cases polymer material 515 may be replaced by glass or another suitable material. In some embodiments, substrate 515 is made by forming an electric contact layer on the surface of glass substrate 505, and etching the electric contact layer to yield an electrical contact 535 at a location corresponding to a future well. Polymer material 515 is then laminated over glass substrate 505 and electrical contact 535, followed by an etch of polymer material 515 to open well 512 and expose a portion of electrical contact 535. Electrical contact 535 may be formed of any material capable of forming an electrical junction with bottom surface 275 of a post enhanced diode 210. In some cases, electrical contact 535 is formed of a metal that when annealed with a post enhanced diode 210 disposed within well 512 forms an electrically conductive location between a signal connected to electrical contact 535 and electrically conductive material 270 of a post enhanced diode 210. In some embodiments, the depth of well 512 is substantially equal to the height of the diode portion (Hd) of a post enhanced diode 210 such that only one post enhanced diode 210 deposits in well 512.

[0050] An additional process is performed to form a through hole via 525 extending through glass substrate 505. In some cases, the width of through hole via 525 (Wv) is less than a minimum width of post 255 to assure that post 255 does not insert into through hole via 525 when post enhanced diode 210 is inverted in well 512 as such insertion would limit the ability for post enhanced diode 210 to flip out of well 512. In other cases, through hole via 525 is

substantially centered in well 512 and post 255 is considerably off-center on top surface 525 of the diode structure, or through hole via 525 is considerably off-center in the base of well 512 and post 255 is substantially centered on top surface 525 of the diode structure such that when a post enhanced diode 210 deposits in well 512 in an inverted orientation post 255 does not align with through hole via 525.

[0051] Further, substrate 590 is etched to form a groove 510 concentrically around well 512. As shown, in some embodiments groove 510 exhibits one substantially vertical side wall and one highly tapered side wall. The tapered side wall is less likely to catch a leading edge of post enhanced diode 210 traversing the surface of substrate 590 in either a non-inverted orientation (shown in a cross sectional view 502 of Fig. 5c) or an inverted orientation (shown in a cross sectional view 503 of Fig. 5c) in a direction indicated by an arrow 570. As the edge catches, a moment of force develops around the edge inducing post enhanced diode 210 to flip. In contrast, a more vertical side wall on groove 510 is more likely to catch a leading edge of post enhanced diode 210 traversing the surface of substrate 590 in an inverted orientation (shown in cross sectional view 503 of Fig. 5c), but unlikely to catch the leading edge of post enhanced diode 210 traversing in a non-inverted orientation (shown in cross sectional view 502 of Fig. 5c). To limit the ability for groove 510 to catch the leading edge of post enhanced diode 210 traversing in a non-inverted orientation (shown in cross sectional view 502 of Fig. 5c), the width of groove 510 is relatively small. In some embodiments, the width of groove is less than twenty-five percent of the width of the diode structure (W_d). Groove 510 should be designed such that it is large enough to catch a leading edge of an inverted post enhanced diode 210, but small enough to let a non-inverted post enhanced diode 210 pass without catching a leading edge. As further guidance to avoiding catching a leading edge of a non-inverted post enhanced diode 210, groove 510 should be flush with the surface of substrate 590.

[0052] It should be noted that other shapes for groove 510 are possible in accordance with other embodiments of the present invention. For example, groove 510 may include two substantially vertical walls with each wall about equal in catching a leading edge of a post enhanced diode 210 traversing the surface of substrate 590 in an inverted orientation. Thus, regardless of the direction that a post enhanced diode 210 is traversing the surface of substrate 590, it is equally likely to catch and flip. In such cases, it may be desirable to make the width of

groove 510 less than the width of post 255 to avoid the possibility of post 255 inserting into groove 510 and becoming trapped.

[0053] During fluidic assembly a liquid flow (indicated by arrows 560) results in drag forces on post enhanced diodes 210 traversing the surface of substrate 590. Because post enhanced diodes 210 include a post 255 extending from the diode structure, the drag forces have an asymmetric impact on the orientation of the plate diodes. In particular, the drag forces result in a positive moment of force about a fixed point of rotation (e.g., an edge of the diode structure in contact with the surface of substrate 590) that will flip an inverted post enhanced diode 210 into a non-inverted orientation. In contrast, the drag forces on a non-inverted post enhanced diode 210 due to the liquid flow are primarily due to perturbations around post 255, and the forces exerted on the diode structure of a post enhanced diode 210 lead to a negative net moment of force. This negative net moment of force about the leading edge (i.e., the edge leading in the direction of arrows 560) of the diode structure holds the diode structure down and stabilizes the post enhanced diode 210 in the non-inverted orientation.

[0054] In some cases, the drag forces on an inverted post enhanced diode 210 traversing the surface of substrate 590 are insufficient to cause a change in orientation. This may be in part due to the difference between the rate at which the carrier fluid is flowing and the rate at which the inverted post enhanced diode 210 is moving is insufficient. However, when a leading edge of an inverted post enhanced diode 210 catches in groove 510, the relative rate at which the carrier fluid is flowing and the rate at which the inverted post enhanced diode 210 is moving increases. This increase in the relative velocity results in a corresponding increase in drag forces and likelihood of flipping. As groove 510 is less likely to catch a leading edge of a non-inverted post enhanced diode 210, the impact of the groove on non-inverted post enhanced diodes 210 is insubstantial.

[0055] While the preceding embodiment disclosed a groove concentric around a well, other locations and geometries for a groove may be used in accordance with different embodiments. For example, Fig. 6a shows a top view 600 of a substrate portion 605 including a number of wells 610 into which post enhanced diodes 210 may be deposited. In addition, a number of parallel grooves 620 are formed in the surface of substrate portion 605 such that the direction of flow (shown by an arrow 601) is generally perpendicular to grooves 620. In this configuration,

grooves 620 perturb the orientation of inverted post enhanced diodes 210 traversing substrate portion 605 similar to that discussed above in relation to Fig. 5. As another example, Fig. 6b shows a top view 650 of a substrate portion 655 including a number of wells 660 into which post enhanced diodes 210 may be deposited. In addition, a number of parallel grooves 670 are formed in the surface of substrate portion 655 such that the direction of flow (shown by an arrow 651) is generally perpendicular to grooves 670. In this configuration, grooves 670 perturb the orientation of inverted post enhanced diodes 210 traversing substrate portion 655 similar to that discussed above in relation to Fig. 5.

[0056] Turning to Fig. 7, a flow diagram 700 depicts a method for forming a post enhanced diode in accordance with some embodiments of the present inventions. Following flow diagram 700, a first doped layer is formed (block 705). The first doped layer is formed by doping a semiconductor material with a first dopant type which is either a p-type dopant or an n-type dopant. Any process known in the art for forming a doped material may be used. In some embodiments, the first doped layer is an n-doped GaN layer.

[0057] An MQW layer is formed on the first doped layer (block 710). Any process known in the art for forming an MQW layer may be used. A second doped layer is formed on top of the MQW layer (block 715). The second doped layer is formed by doping a semiconductor material with a second dopant type which is the opposite doping of the first dopant type. Any process known in the art for forming a doped material may be used. In some embodiments where the first doped layer is an n-doped GaN layer, the second doped layer is a p-doped GaN layer.

[0058] A post is formed on the second doped layer (block 720). Various approaches may be used for forming a post extending from the second doped layer. For example, fabricating a homogeneous post may be done as part of the second doped layer where a semiconductor material is formed on the MQW layer, and then etched back leaving a thick post structure and a thinner layer of the semiconductor extending from the edges of the post to the edges of the MQW layer. In this case, the second doped layer may be doped after the post is formed. As another example, the post may be formed on the second doped layer after the second doped layer has been doped through selective epitaxial growth using the same material to as the second doped layer. As other examples, forming a heterogeneous post may include etching the post from a film that is deposited onto the second doped layer, or by forming a post with a different

material through plating or a templated growth process on top the second doped layer. This latter approach permits the use of any material for the post (e.g., dielectrics, metals, etc.). In some cases, photolithography of a photo resist may be used in relation to the aforementioned plating or template growth. While not shown in flow diagram 700, individual post enhanced diodes can then be cut by etching through the combination of the second doped material, the MQW layer, and the first doped material to yield individual post enhanced diodes similar to those discussed above in relation to Figs. 2b-2e.

[0059] Turning to Fig. 8, a flow diagram 800 shows a method for depositing or placing post enhanced diodes into substrate wells in accordance with various embodiments of the present inventions. Following flow diagram 800, a substrate is formed including a plurality of wells each capable of accepting a post enhanced diode (block 810). The substrate may be formed similar to that discussed above in relation to any of Figs. 3-5. In addition, a suspension is formed by adding a plurality of post enhanced diodes to a carrier liquid (block 805). In some cases, the carrier liquid is isopropanol, but may be another liquid or gas capable of moving post enhanced diodes across the surface of a substrate.

[0060] The suspension is deposited on a surface of the substrate that includes the wells (block 815). This deposit may be done by any suitable method including, but not limited to, pumping the suspension or draining the suspension onto the surface. The suspension is then agitated on the substrate such that the plurality of post enhanced diodes in the suspension move relative to the surface of the substrate and deposit into respective ones of the plurality of wells (block 820). Because of the asymmetry of force due to the post extending from a top surface of a diode structure, the post enhanced diodes tend to assume a non-inverted orientation when exposed to movement of the carrier liquid. The suspension including non-deposited post enhanced diodes and the carrier liquid is removed from the surface of the substrate in a clean-up process (block 825).

[0061] Turning to Fig. 9, a flow diagram 900 shows another method for depositing or placing post enhanced diodes into substrate wells in accordance with various embodiments of the present inventions. Following flow diagram 900, a substrate is formed including a plurality of wells each capable of accepting a post enhanced diode and at least one groove capable of catching a leading edge of an inverted post enhanced diode traversing the surface of the substrate (block

810). The substrate may be formed similar to that discussed above in relation to any of Figs. 3-5, and include a groove pattern similar to that discussed above in relation to Figs. 5-6. In addition, a suspension is formed by adding a plurality of post enhanced diodes to a carrier liquid (block 805). In some cases, the carrier liquid is isopropanol, but may be another liquid or gas capable of moving post enhanced diodes across the surface of a substrate.

[0062] The suspension is deposited on a surface of the substrate that includes the wells (block 915). This deposit may be done by any suitable method including, but not limited to, pumping the suspension or draining the suspension onto the surface. The suspension is then agitated on the substrate such that the plurality of post enhanced diodes in the suspension move relative to the surface of the substrate and deposit into respective ones of the plurality of wells (block 920). Because of the asymmetry of force due to the post extending from a top surface of a diode structure, the post enhanced diodes tend to assume a non-inverted orientation when exposed to movement of the carrier liquid. Further, because of the possibility of inverted post enhanced diodes catching a leading edge in the groove on the surface of the substrate as they move across the substrate, the tendency of the post enhanced diodes to assume a non-inverted orientation when exposed to movement of the carrier liquid is increased. The suspension including non-deposited post enhanced diodes and the carrier liquid is removed from the surface of the substrate in a clean-up process (block 925).

[0063] One of ordinary skill in the art will recognize various advantages achievable through use of different embodiments of the inventions. As just some of many advantages, lower display costs are possible as a significant cost of manufacturing a microLED display is the material cost of the microLEDs themselves. As some embodiments of the present inventions allow for reducing redundancy otherwise necessary to assure an operable display, the overall number of microLEDs may be reduced resulting in a corresponding reduction in costs. Various embodiments of the present inventions do not require lock-n-key type interaction between post enhanced diodes and wells which allow diodes to deposit in only a single orientation. As such, manufacturing tolerances may be reduced leading to greater yields and/or lower costs. Based upon the disclosure provided herein, one of ordinary skill in the art will recognize a variety of other advantages achievable through use of one or more embodiments of the present inventions.

[0064] In conclusion, the invention provides novel systems, devices, methods and arrangements for fluidic assembly. While detailed descriptions of one or more embodiments of the invention have been given above, various alternatives, modifications, and equivalents will be apparent to those skilled in the art without varying from the spirit of the invention. For examples, while some embodiments are discussed in relation to displays, it is noted that the embodiments find applicability to devices other than displays. Therefore, the above description should not be taken as limiting the scope of the invention, which is defined by the appended claims.

WHAT IS CLAIMED IS:

1 1. A fluidic assembly system, the system comprising:
2 a substrate including a plurality of wells; and
3 a suspension including a carrier liquid and a plurality of post enhanced diodes
4 each including a post extending from a top surface of a diode structure.

1 2. The fluidic assembly system of claim 1, the system further comprising:
2 a suspension movement device operable to move the suspension over the
3 substrate such that a portion of the plurality of post enhanced diodes deposit in respective ones of
4 the plurality of wells.

1 3. The fluidic assembly system of claim 1, wherein the diode structure of the
2 post enhanced diodes includes:
3 the top surface formed at least in part of a first electrically conductive material;
4 a planar bottom surface formed at least in part of a second electrically conductive
5 material;
6 a first electrical contact configured to conduct charge to the first electrically
7 conductive material; and
8 a second electrical contact configured to conduct charge to the second electrically
9 conductive material.

1 4. The fluidic assembly system of claim 1, wherein each of the plurality of
2 wells includes a through hole via extending through the substrate from the bottom of the
3 respective well, and wherein a width of a surface of the post substantially parallel to the top
4 surface of the diode structure is greater than a width of the through hole via.

1 5. The fluidic assembly system of claim 1, wherein each of the plurality of
2 wells includes a through hole via extending through the substrate from the bottom of the

3 respective well, and wherein the through hole via is off center from a circular shaped bottom of
4 the respective well.

1 6. The fluidic assembly system of claim 1, wherein the diode structure
2 includes a bottom surface, and wherein a maximum width of the bottom surface is less than a
3 maximum width of each of the plurality of wells.

1 7. The fluidic assembly system of claim 1, wherein an electrical contact is
2 formed on an interior surface of each of the plurality of wells.

1 8. The fluidic assembly system of claim 1, wherein an orientation of each of
2 the plurality of post enhanced diodes where the post extends away from the substrate is a non-
3 inverted orientation, wherein an orientation of each of the plurality of post enhanced diodes
4 where the post extends toward the substrate is an inverted orientation, and wherein one of the
5 plurality of post enhanced diodes deposited in a respective well is more mechanically stable in
6 the non-inverted orientation than in the inverted orientation.

1 9. The fluidic assembly system of claim 1, wherein an orientation of each of
2 the plurality of post enhanced diodes where the post extends away from the substrate is a non-
3 inverted orientation, wherein an orientation of each of the plurality of post enhanced diodes
4 where the post extends toward the substrate is an inverted orientation, and wherein an orientation
5 of one of the plurality of post enhanced diodes in contact with a surface of the substrate is more
6 mechanically stable in the non-inverted orientation than in the inverted orientation.

1 10. The fluidic assembly system of claim 1, wherein an orientation of each of
2 the plurality of post enhanced diodes where the post extends away from the substrate is a non-
3 inverted orientation, wherein an orientation of each of the plurality of post enhanced diodes
4 where the post extends toward the substrate is an inverted orientation, and wherein the substrate
5 further includes:

6 at least one groove configured such that an orientation of one of the plurality of
7 post enhanced diodes traversing the groove is more mechanically stable in the non-inverted
8 orientation than in the inverted orientation.

1 11. The fluidic assembly system of claim 10, wherein the groove extends into
2 the substrate with a leading edge exhibiting a slope greater than a trailing edge, and wherein
3 upon moving the suspension over the substrate one of the post enhanced diodes crosses the
4 trailing edge before crossing the leading edge.

1 12. The fluidic assembly system of claim 10, wherein a depth of the groove
2 into the substrate is less than a distance from an edge of the top surface of the diode structure to
3 an edge of the post.

1 13. The fluidic assembly system of claim 10, wherein a width of the groove at
2 a surface of the substrate is less than a distance from an edge of the top surface of the diode
3 structure to an edge of the post.

1 14. A post enhanced diode comprising:
2 a planar top surface formed at least in part of a first electrically conductive
3 material;
4 a planar bottom surface formed at least in part of a second electrically conductive
5 material;
6 a post extending from the top surface;
7 a first electrical contact configured to conduct charge to the first electrically
8 conductive material; and
9 a second electrical contact configured to conduct charge to the second electrically
10 conductive material.

1 15. The post enhanced diode of claim 14, wherein the top surface exhibits a
2 first maximum width, wherein a surface of the post that is substantially parallel to the top surface
3 exhibits a second maximum width, and wherein the first maximum width is at least two times the
4 second maximum width.

1 16. The post enhanced diode of claim 14, wherein the post exhibits a height
2 extending from the top surface to the surface of the post that is substantially parallel to the top
3 surface, wherein a distance between the top surface and the bottom surface is a thickness, and
4 wherein the thickness-to-height ratio is in a range of 1:0.6 to 1:4.

1 17. The post enhanced diode of claim 14, wherein the top surface exhibits a
2 maximum width, wherein a distance between the top surface and the bottom surface is a
3 thickness, and wherein the maximum width-to-thickness aspect ratio is in a range of 5:1 to 50:1.

1 18. The post enhanced diode of claim 14, wherein the post is the first
2 electrical contact.

1 19. The post enhanced diode of claim 14, wherein the post is formed of an
2 insulator material.

1 20. The post enhanced diode of claim 14, wherein the top surface has a shape
2 selected from a group consisting of: a circle, a polygon, and an ellipse.

1 21. The post enhanced diode of claim 14, wherein the top surface has a
2 hexagonal shape.

1 22. The post enhanced diode of claim 14, wherein a surface of the post that is
2 substantially parallel to the top surface has a shape selected from a group consisting of: a circle, a
3 polygon, and an ellipse.

1 23. The post enhanced diode of claim 14, wherein the post is formed of a third
2 conductive material.

1 24. The post enhanced diode of claim 23, wherein the third conductive
2 material is the same as the first conductive material.

1 25. The post enhanced diode of claim 24, wherein the first conductive material
2 is a p-doped semiconductor material, and wherein the second conductive material is an n-doped
3 semiconductor material.

1 26. The post enhanced diode of claim 24, wherein the first conductive material
2 is an n-doped semiconductor material, and wherein the second conductive material is a p-doped
3 semiconductor material.

1 27. A substrate for fluidic assembly, the substrate comprising:

2 a plurality of wells extending from a top surface of the substrate, wherein each of
3 the plurality of wells is configured to accept a post enhanced diode, wherein the post enhanced
4 diode includes a post extending from a top surface of a diode structure;

5 at least one groove extending into the top surface of the substrate and configured
6 such that an orientation of the post enhanced diodes traversing the groove is more mechanically
7 stable in a non-inverted orientation than in an inverted orientation, wherein in the non-inverted
8 orientation the post extends away from the top surface of the substrate, and wherein in the
9 inverted orientation the post extends toward the substrate.

1 28. The fluidic assembly system of claim 27, wherein a depth of the groove
2 into the substrate is less than a distance from an edge of the top surface of the diode structure to
3 an edge of the post.

1 29. The fluidic assembly system of claim 27, wherein a width of the groove at
2 a surface of the substrate is less than a distance from an edge of the top surface of the diode
3 structure to an edge of the post.

1

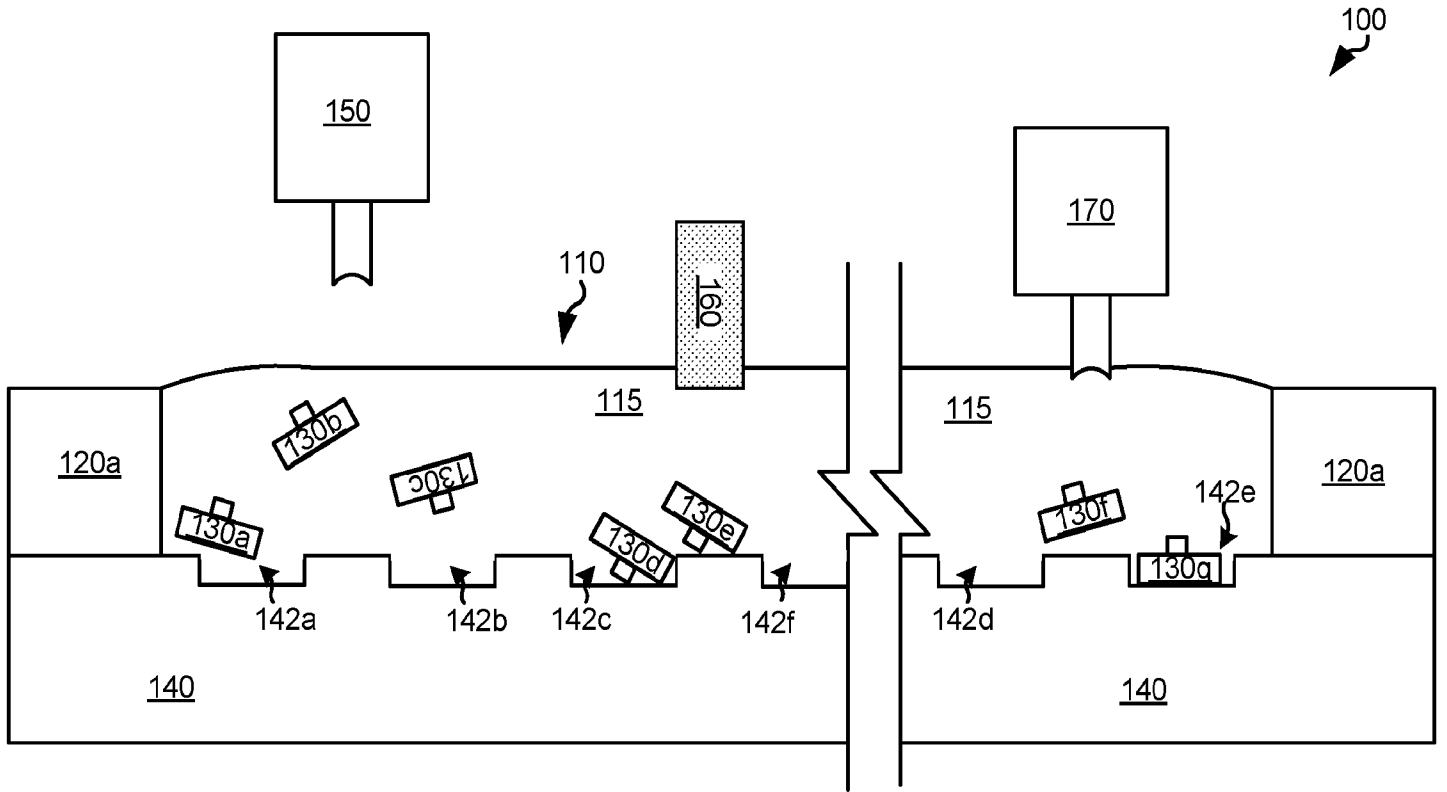


Fig. 1

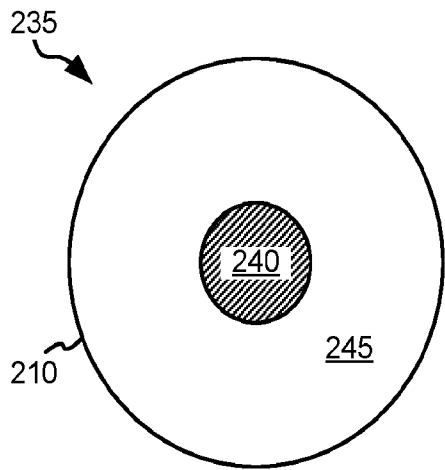


Fig. 2b

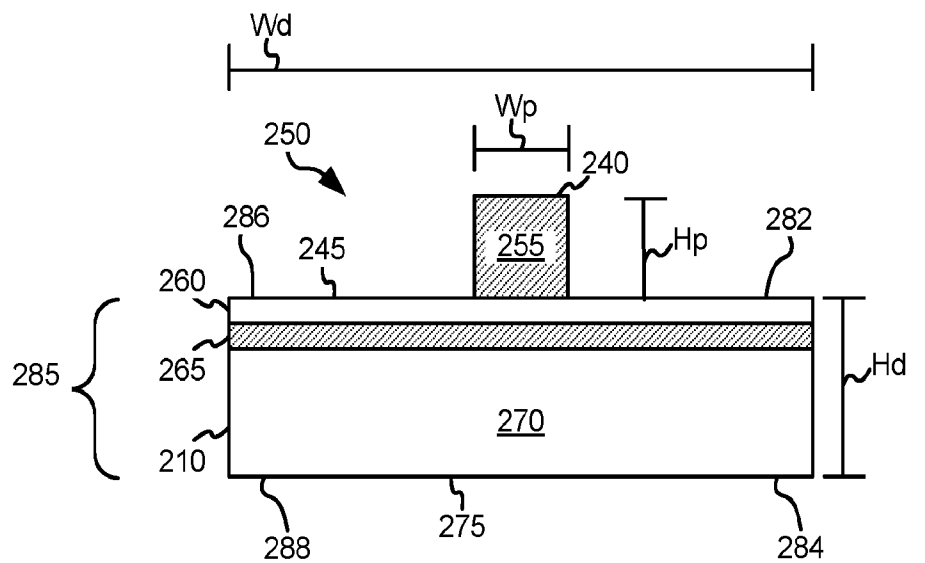


Fig. 2c

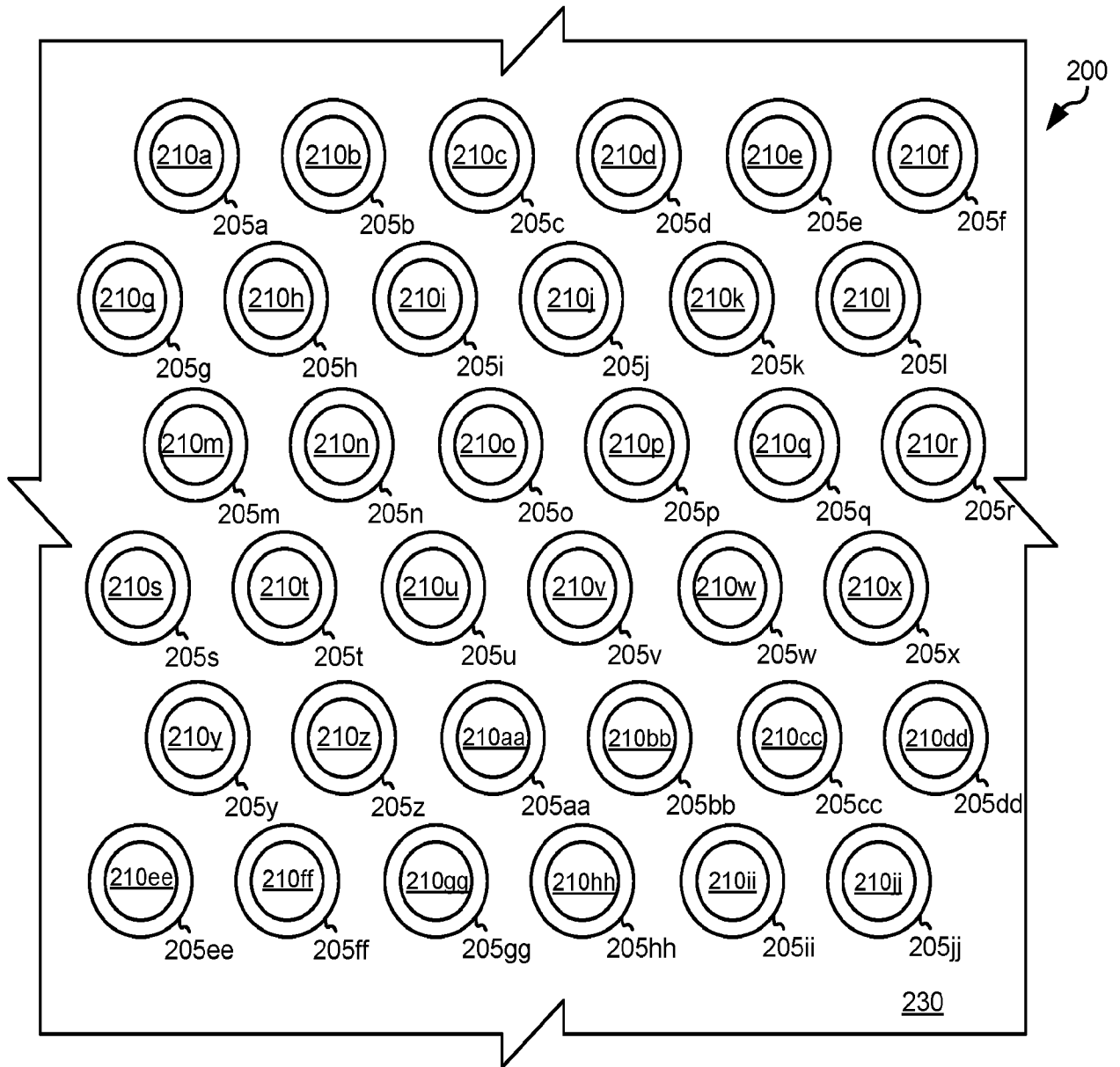


Fig. 2a

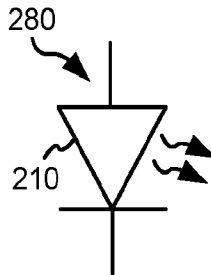


Fig. 2d

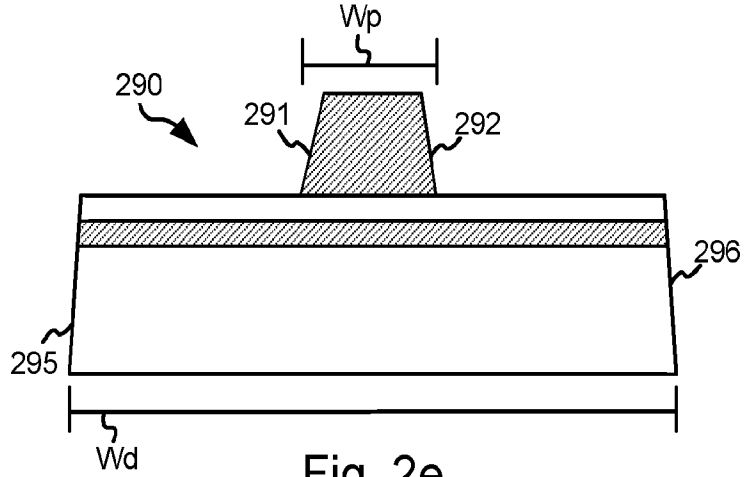


Fig. 2e

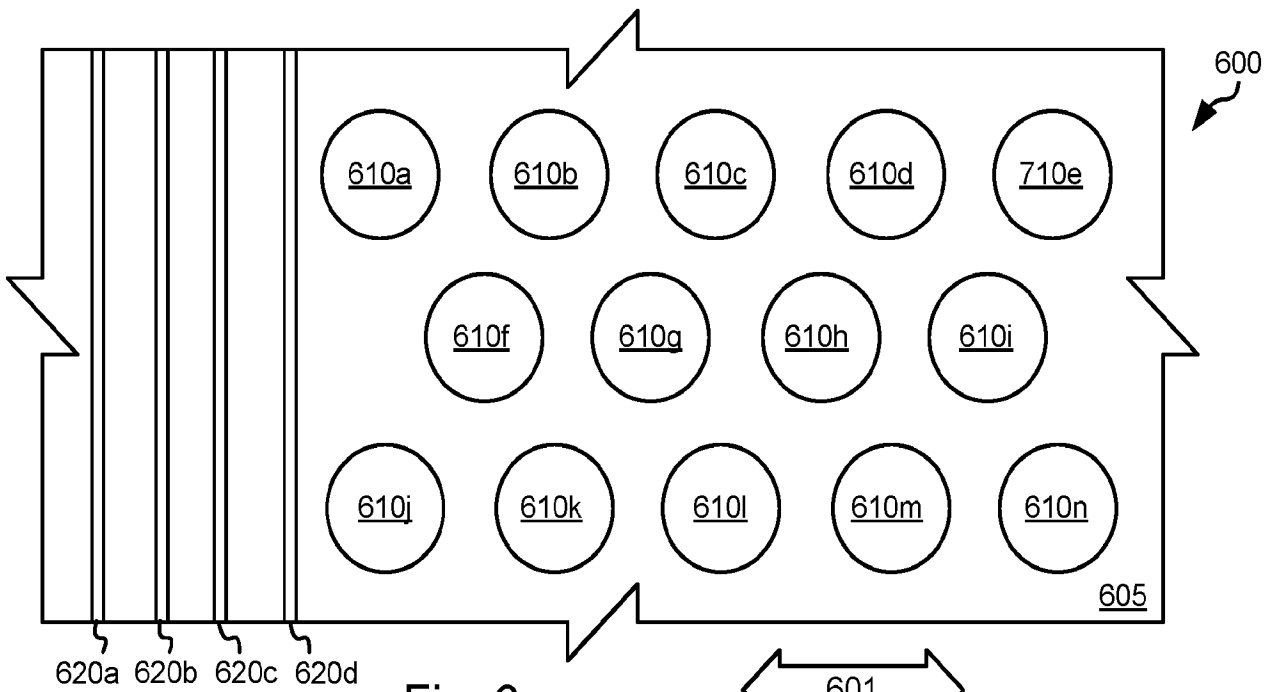


Fig. 6a

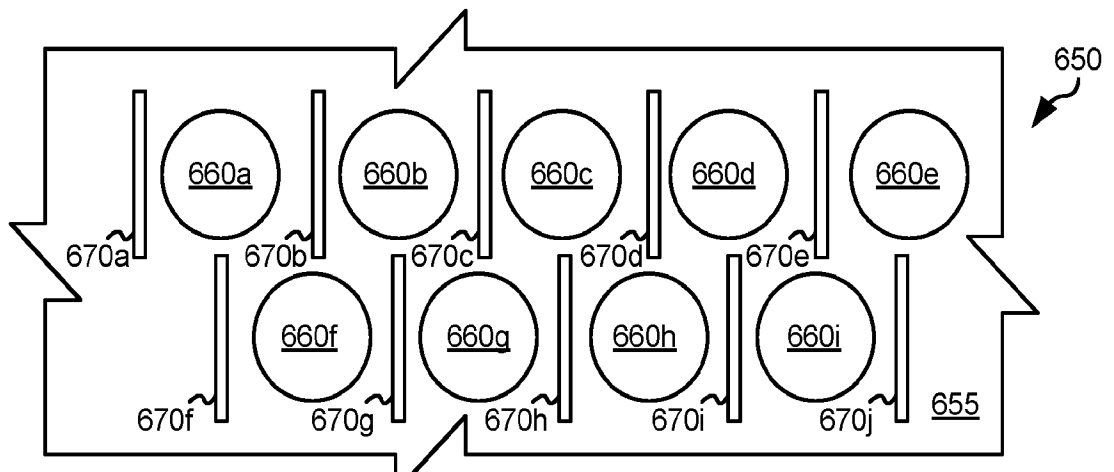


Fig. 6b

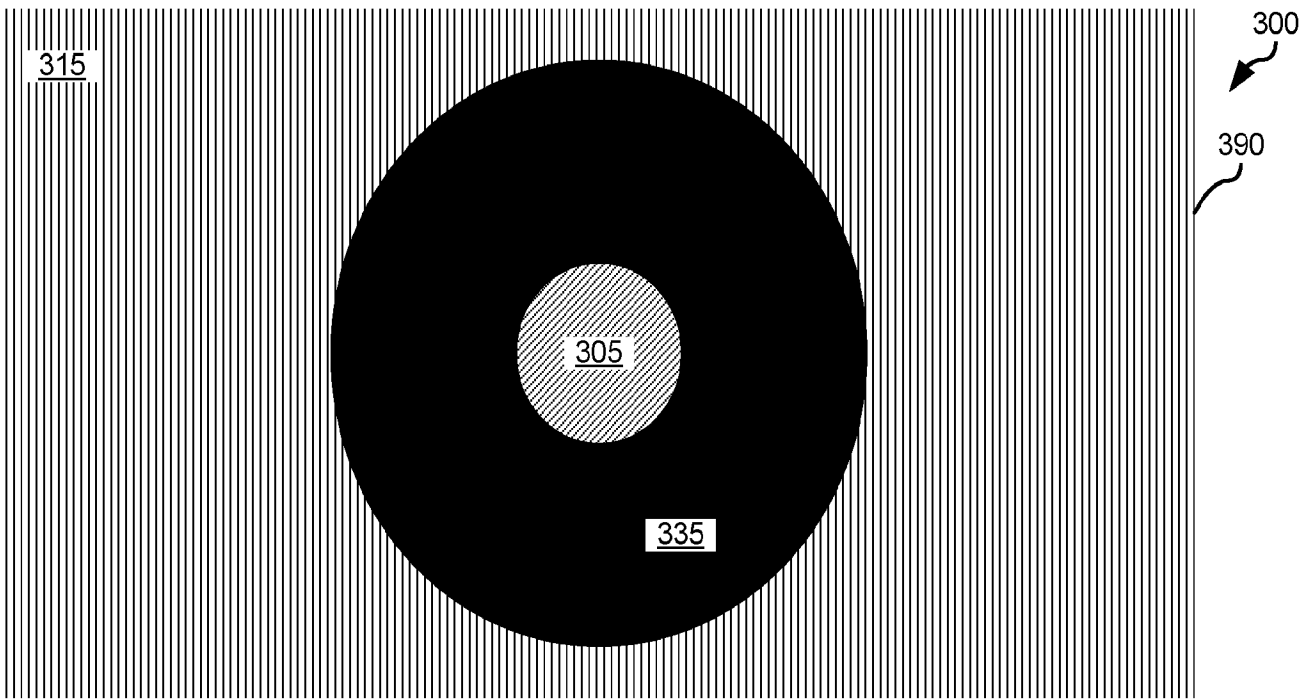


Fig. 3a

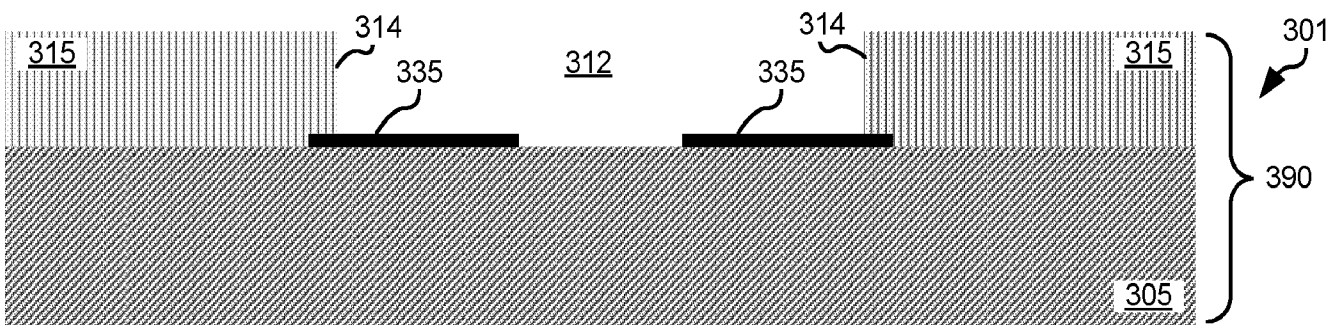


Fig. 3b

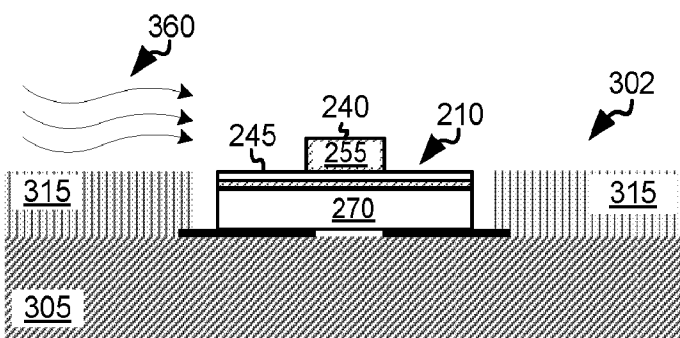


Fig. 3c

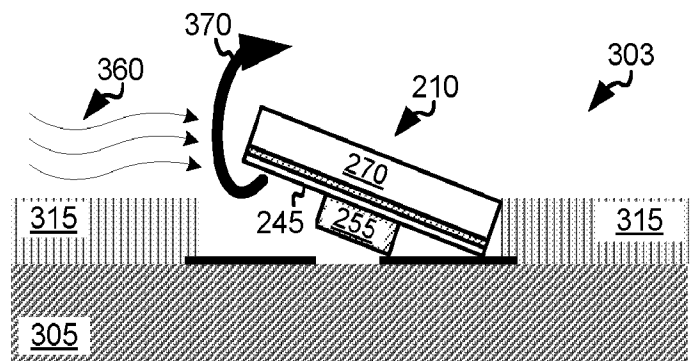


Fig. 3d

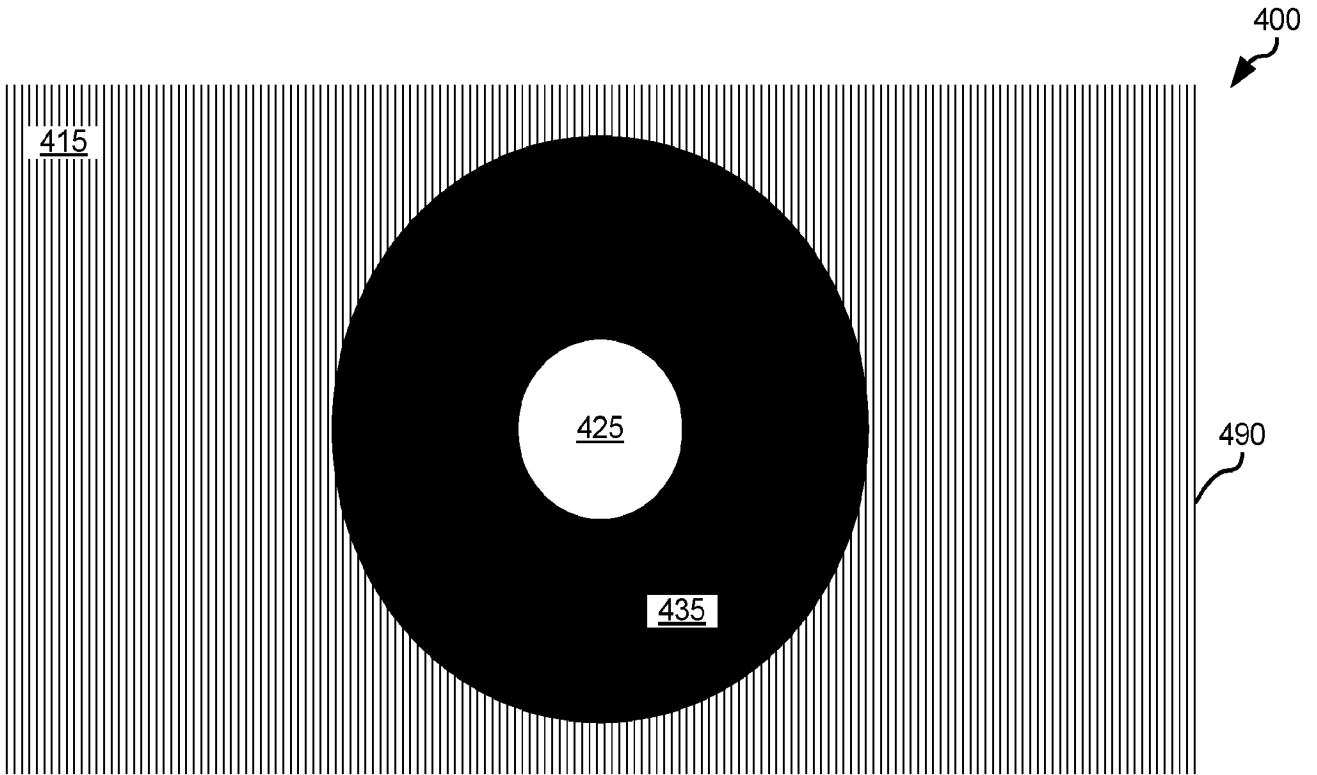


Fig. 4a

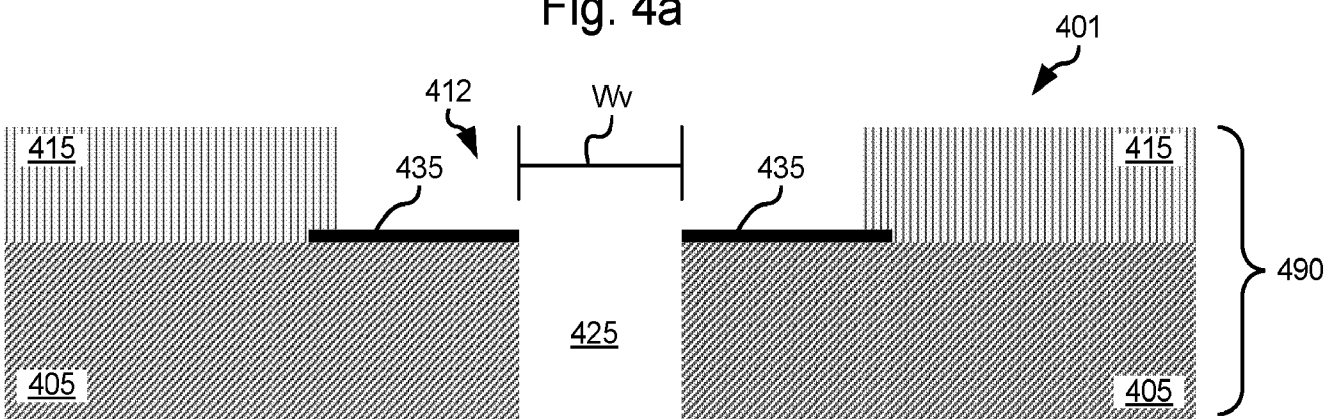


Fig. 4b

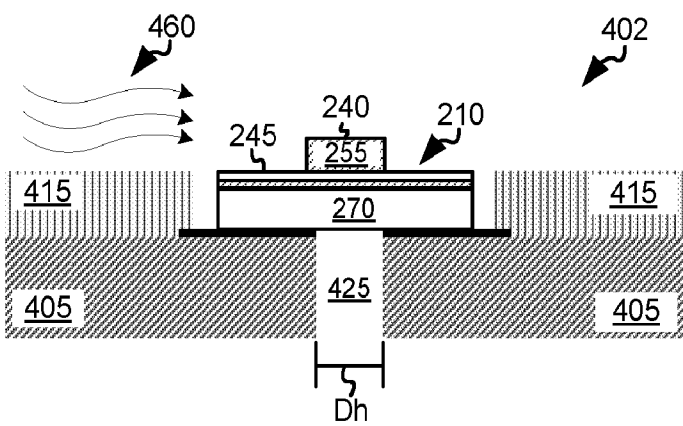


Fig. 4c

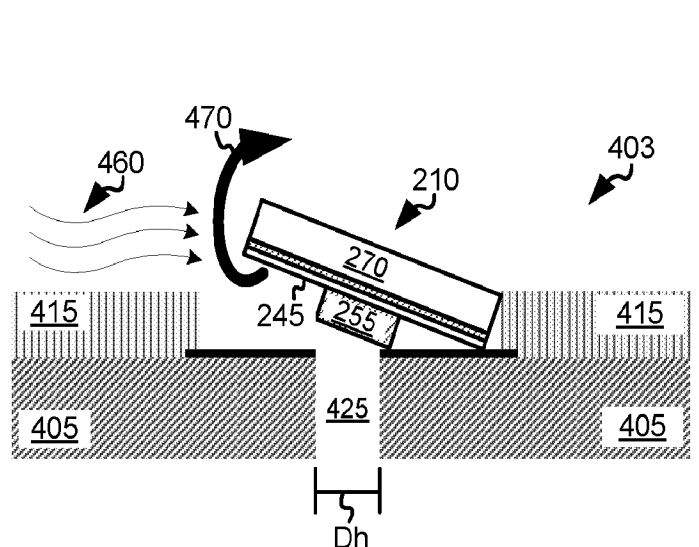


Fig. 4d

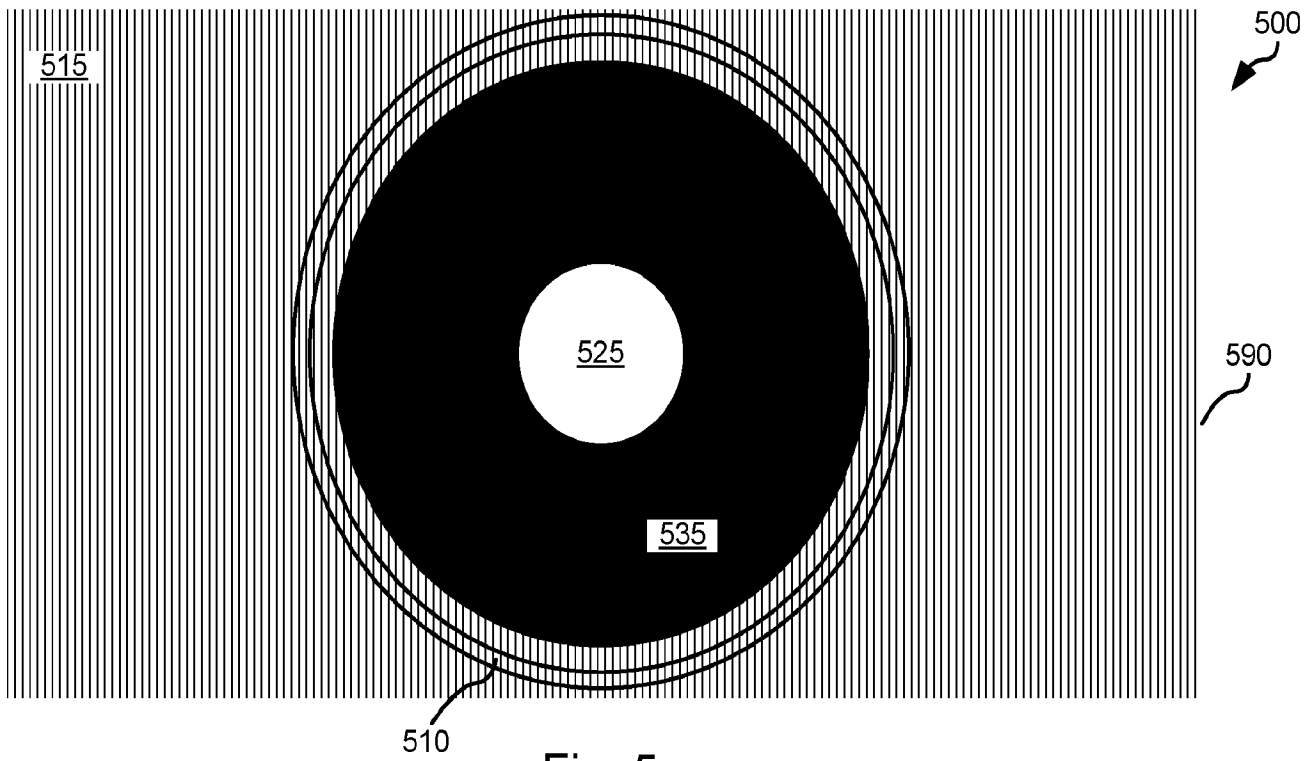


Fig. 5a

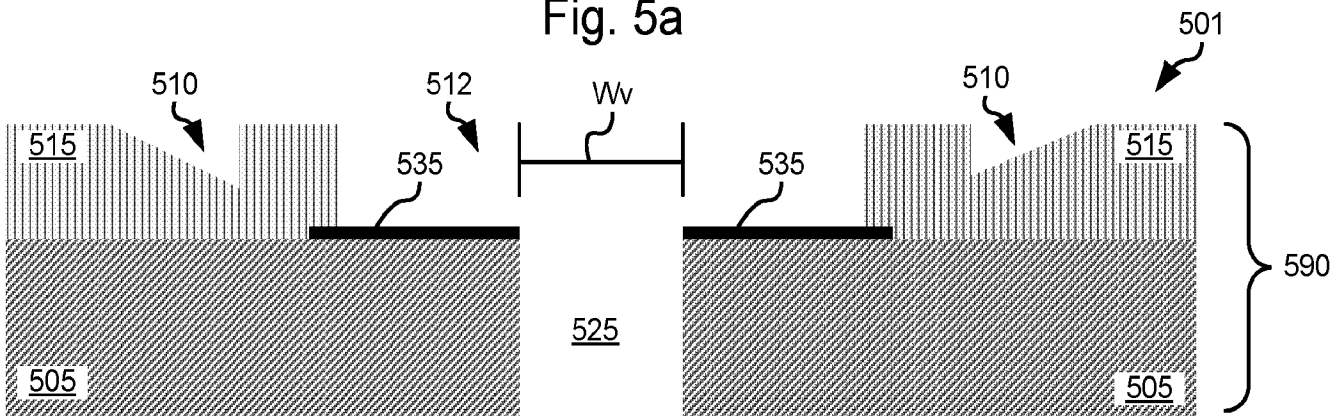


Fig. 5b

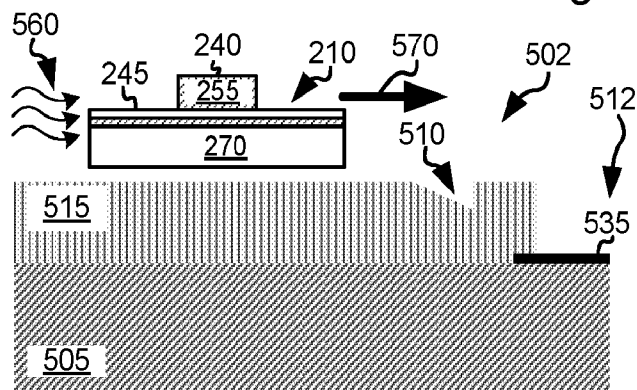


Fig. 5c

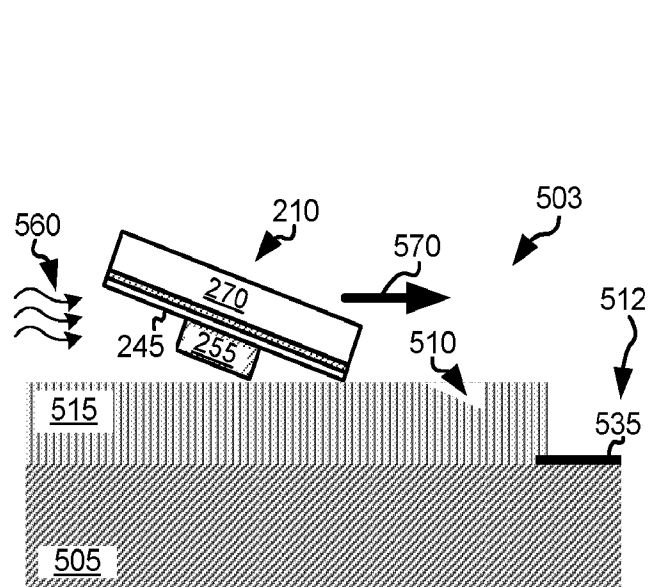


Fig. 5d

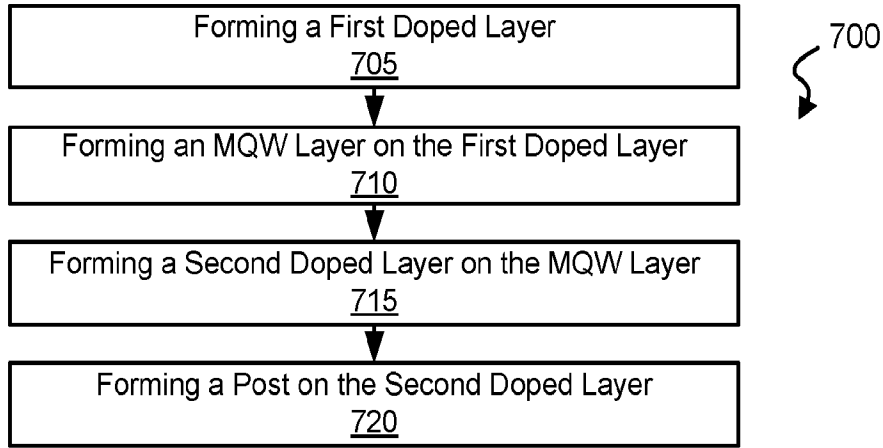


Fig. 7

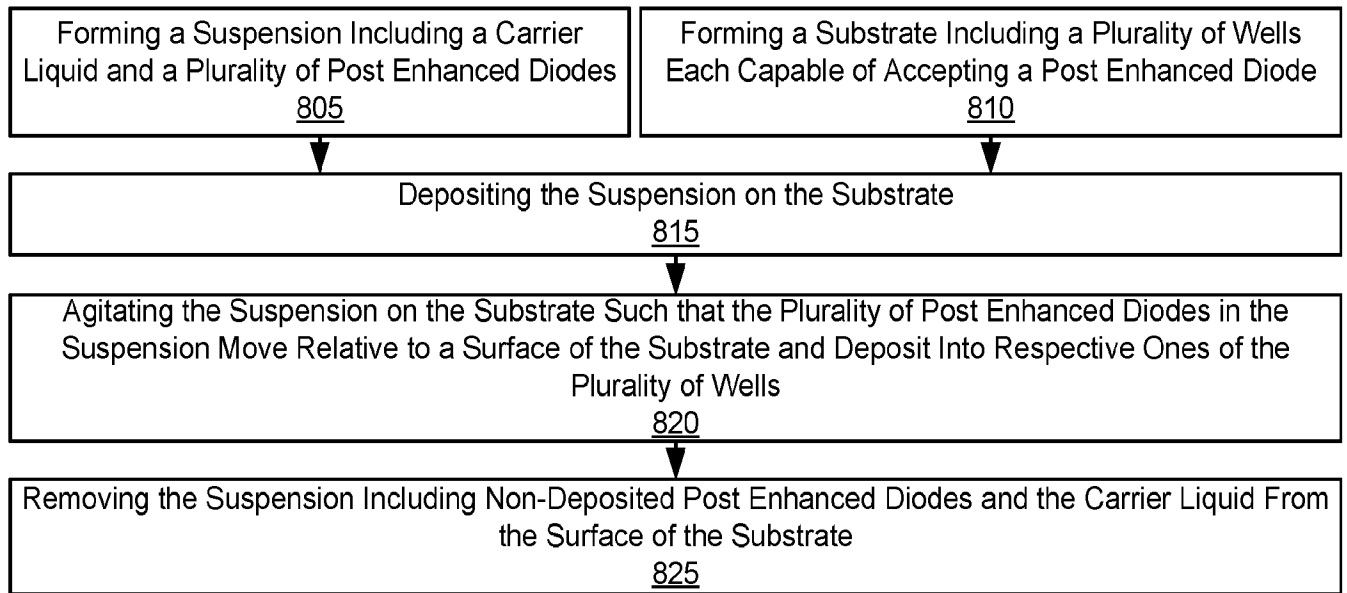


Fig. 8

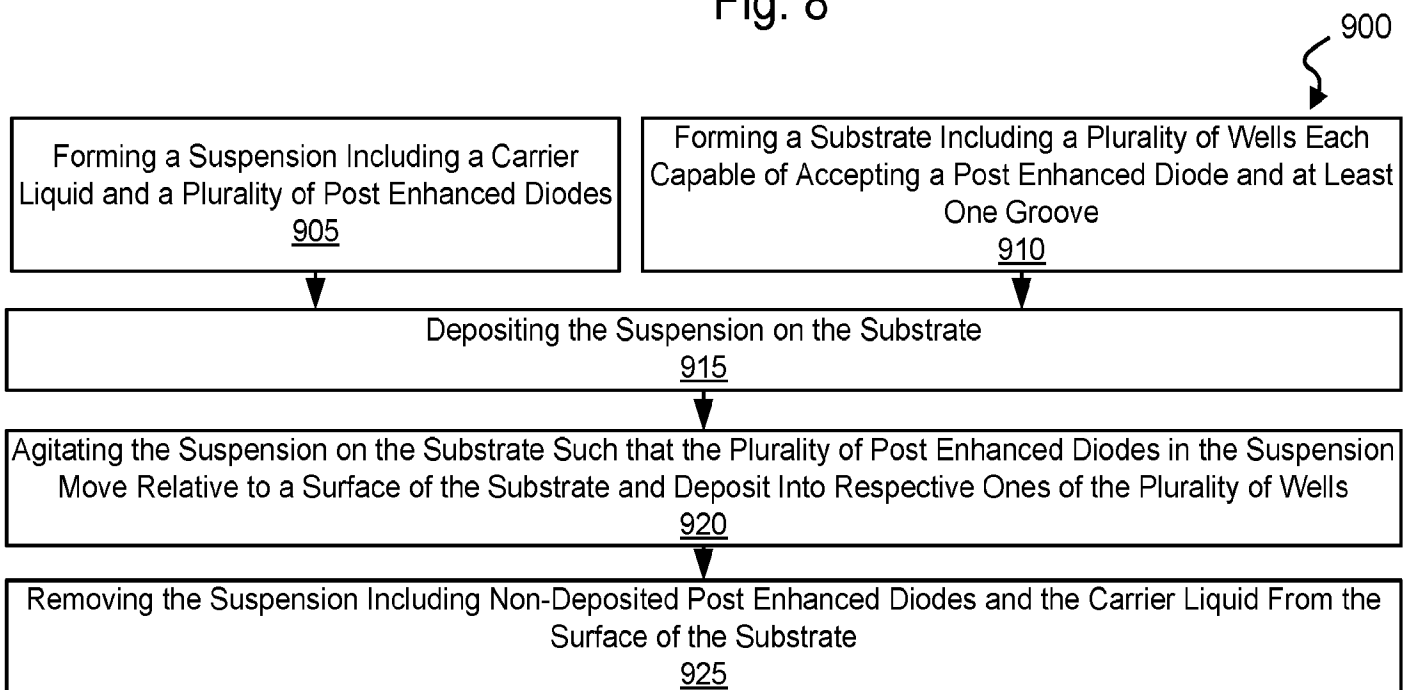


Fig. 9

A. CLASSIFICATION OF SUBJECT MATTER**H01L 25/075(2006.01)i, H01L 27/15(2006.01)i, H01L 25/18(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 25/075; H01L 21/20; G09F 9/33; H01L 33/00; H01L 33/06; B05C 11/10; B05B 1/00; H01L 31/0232; G06F 3/041; H01L 27/15; H01L 25/18

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: diode, display, fluid, light, liquid, stability, carrier

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015-0187740 A1 (LUXVUE TECHNOLOGY CORPORATION) 02 July 2015 See paragraphs [0047]-[0069] and figures 2, 10-11A.	14-26
Y		1-7
A		8-13, 27-29
Y	US 2012-0032220 A1 (NATHANIEL O. CANNON et al.) 09 February 2012 See paragraphs [0046]-[0058] and figures 3A-3B.	1-7
A	US 2012-0178195 A1 (WILLIAM JOHNSTONE RAY et al.) 12 July 2012 See paragraphs [0108]-[0134] and figures 1-12.	1-29
A	KR 10-2012-0124660 A (FALCON SYSTEM CO., LTD.) 14 November 2012 See paragraphs [0025]-[0052] and figures 3a-6.	1-29
A	KR 10-2007-0096212 A (SAMSUNG SDI CO., LTD.) 02 October 2007 See paragraphs [0025]-[0031] and figures 1-8.	1-29

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

29 September 2017 (29.09.2017)

Date of mailing of the international search report

29 September 2017 (29.09.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

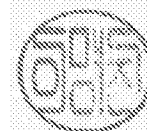
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

LEE, Myung Jin

Telephone No. +82-42-481-8474



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/038087

Patent document cited in search report	Publication date	Patent family member(s)	Publication date		
US 2015-0187740 A1	02/07/2015	AU 2014-370328 A1	02/07/2015		
		AU 2014-370328 B2	13/04/2017		
		CN 105814698 A	27/07/2016		
		EP 3087617 A1	02/11/2016		
		JP 2017-500757 A	05/01/2017		
		JP 6186516 B2	23/08/2017		
		KR 10-2016-0083035 A	11/07/2016		
		TW 201705521 A	01/02/2017		
		TW 1560904 B	01/12/2016		
		US 2015-0187991 A1	02/07/2015		
		US 2016-0336484 A1	17/11/2016		
		US 9450147 B2	20/09/2016		
		US 9583466 B2	28/02/2017		
		WO 2015-099944 A1	02/07/2015		
		US 2012-0032220 A1	09/02/2012	CN 102859648 A	02/01/2013
				EP 2543060 A1	09/01/2013
				JP 2013-521652 A	10/06/2013
KR 10-2013-0028905 A	20/03/2013				
US 2009-0179213 A1	16/07/2009				
US 2010-0155763 A1	24/06/2010				
US 8058088 B2	15/11/2011				
US 8618569 B2	31/12/2013				
US 8940561 B2	27/01/2015				
WO 2011-109192 A1	09/09/2011				
US 2012-0178195 A1	12/07/2012			AU 2008-259989 A1	11/12/2008
		AU 2010-295691 A1	24/03/2011		
		AU 2010-295691 B2	17/10/2013		
		CA 2688409 A1	11/12/2008		
		CA 2772919 A1	24/03/2011		
		CA 2795487 A1	13/10/2011		
		CN 101711405 A	19/05/2010		
		CN 101711405 B	30/10/2013		
		CN 101715592 A	26/05/2010		
		CN 101715592 B	30/10/2013		
		CN 102695914 A	26/09/2012		
		CN 102695914 B	09/12/2015		
		CN 103228980 A	31/07/2013		
		CN 103228980 B	09/11/2016		
		CN 103582962 A	12/02/2014		
		CN 103582962 B	22/03/2017		
		CN 103594460 A	19/02/2014		
		CN 103594460 B	05/10/2016		
		CN 103594461 A	19/02/2014		
		CN 103594461 B	05/10/2016		
		CN 103633222 A	12/03/2014		
		CN 103633222 B	11/08/2017		
		EP 2160730 A2	10/03/2010		

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/038087

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		EP 2160730 B1	12/06/2013
		EP 2478290 A1	25/07/2012
		EP 2556326 A1	13/02/2013
		EP 2612067 A2	10/07/2013
		EP 2612067 B1	23/08/2017
		EP 2612380 A2	10/07/2013
		EP 2617781 A2	24/07/2013
		EP 2617781 A3	19/03/2014
		EP 2618369 A2	24/07/2013
		EP 2618369 A3	12/03/2014
		EP 2618389 A2	24/07/2013
		EP 2618389 A3	19/03/2014
		EP 2618389 B1	16/08/2017
		IL 202380 A	30/06/2010
		IL 218610 A	31/05/2012
		IL 218610 B	30/04/2014
		IL 218611 A	31/05/2012
		IL 218611 B	30/04/2015
		JP 2010-529599 A	26/08/2010
		JP 2013-504861 A	07/02/2013
		KR 10-1429036 B1	12/08/2014
		KR 10-2010-0023897 A	04/03/2010
		KR 10-2012-0093880 A	23/08/2012
		KR 10-2013-0108575 A	04/10/2013
		KR 10-2013-0117766 A	28/10/2013
		KR 10-2013-0130079 A	29/11/2013
		KR 10-2013-0133886 A	09/12/2013
		TW 200901113 A	01/01/2009
		TW 200912854 A	16/03/2009
		TW 200950147 A	01/12/2009
		TW 201133959 A	01/10/2011
		TW 201226479 A	01/07/2012
		TW I431804 B	21/03/2014
		TW I534211 B	21/05/2016
		TW I539631 B	21/06/2016
		TW I550896 B	21/09/2016
		TW I555172 B	21/10/2016
		TW I566302 B	11/01/2017
		TW I566369 B	11/01/2017
		US 2008-0297071 A1	04/12/2008
		US 2008-0297453 A1	04/12/2008
		US 2010-0065862 A1	18/03/2010
		US 2010-0065863 A1	18/03/2010
		US 2010-0068838 A1	18/03/2010
		US 2010-0068839 A1	18/03/2010
		US 2010-0167441 A1	01/07/2010
		US 2010-0244056 A1	30/09/2010
		US 2010-0252173 A1	07/10/2010
		US 2011-0248448 A1	13/10/2011
		US 2012-0063136 A1	15/03/2012

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/038087

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 2012-0161112 A1	28/06/2012
		US 2012-0161113 A1	28/06/2012
		US 2012-0161195 A1	28/06/2012
		US 2012-0161196 A1	28/06/2012
		US 2012-0161338 A1	28/06/2012
		US 2012-0164796 A1	28/06/2012
		US 2012-0164797 A1	28/06/2012
		US 2012-0178194 A1	12/07/2012
		US 2012-0227008 A1	06/09/2012
		US 2013-0134438 A1	30/05/2013
		US 2013-0146905 A1	13/06/2013
		US 2013-0168658 A1	04/07/2013
		US 2014-0138666 A1	22/05/2014
		US 2014-0291644 A1	02/10/2014
		US 2014-0312332 A1	23/10/2014
		US 2014-0363908 A1	11/12/2014
		US 2014-0370629 A1	18/12/2014
		US 2015-0069429 A1	12/03/2015
		US 2015-0167949 A1	18/06/2015
		US 2015-0219284 A1	06/08/2015
		US 2015-0226383 A1	13/08/2015
		US 2015-0276194 A1	01/10/2015
		US 2015-0300575 A1	22/10/2015
		US 2015-0349206 A1	03/12/2015
		US 2015-0380608 A1	31/12/2015
		US 2016-0076750 A1	17/03/2016
		US 2016-0126417 A1	05/05/2016
		US 7972031 B2	05/07/2011
		US 8133768 B2	13/03/2012
		US 8384630 B2	26/02/2013
		US 8395568 B2	12/03/2013
		US 8415879 B2	09/04/2013
		US 8456392 B2	04/06/2013
		US 8456393 B2	04/06/2013
		US 8674593 B2	18/03/2014
		US 8723408 B2	13/05/2014
		US 8753946 B2	17/06/2014
		US 8753947 B2	17/06/2014
		US 8809126 B2	19/08/2014
		US 8846457 B2	30/09/2014
		US 8852467 B2	07/10/2014
		US 8877101 B2	04/11/2014
		US 8889216 B2	18/11/2014
		US 9018833 B2	28/04/2015
		US 9105812 B2	11/08/2015
		US 9130124 B2	08/09/2015
		US 9200758 B2	01/12/2015
		US 9236527 B2	12/01/2016
		US 9236528 B2	12/01/2016
		US 9316362 B2	19/04/2016

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/038087

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 9343593 B2	17/05/2016
		US 9349928 B2	24/05/2016
		US 9362348 B2	07/06/2016
		US 9400086 B2	26/07/2016
		US 9410684 B2	09/08/2016
		US 9419179 B2	16/08/2016
		US 9425357 B2	23/08/2016
		US 9534772 B2	03/01/2017
		WO 2008-150960 A1	11/12/2008
		WO 2008-150965 A2	11/12/2008
		WO 2008-150965 A3	29/01/2009
		WO 2011-034908 A1	24/03/2011
		WO 2011-126496 A1	13/10/2011
		WO 2012-031092 A2	08/03/2012
		WO 2012-031092 A3	10/05/2012
		WO 2012-031096 A2	08/03/2012
		WO 2012-031096 A3	20/03/2014
KR 10-2012-0124660 A	14/11/2012	KR 10-1063928 B1	08/09/2011
		KR 10-1240919 B1	11/03/2013
		WO 2012-064148 A1	18/05/2012
KR 10-2007-0096212 A	02/10/2007	KR 10-0763894 B1	05/10/2007
		US 2007-0224713 A1	27/09/2007
		US 7727788 B2	01/06/2010