



(51) International Patent Classification:
H01L 21/336 (2006.01) *H01L 29/78* (2006.01)

(21) International Application Number:
PCT/US2009/067151

(22) International Filing Date:
8 December 2009 (08.12.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/339,215 19 December 2008 (19.12.2008) US

(71) Applicant (for all designated States except US):
FAIRCHILD SEMICONDUCTOR CORPORATION
[US/US]; 82 Running Hill Road, South Portland, ME
04106 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **GREBS, Thomas, E.** [US/US]; 28 Woodbrook Way, Mountain Top, PA 18707 (US). **DOLNY, Gary, M.** [US/US]; 633 South Main Road, Mountain Top, PA 18707 (US). **KINZER,**

Daniel, M. [US/US]; 760 Center Street, El Segundo, CA 90245 (US).

(74) Agent: **FITZGERALD, Thomas, R.**; Hiscock & Barclay, LLP, 100 Chestnut Street, Rochester, NY 14604-2404 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,

[Continued on next page]

(54) Title: LATERAL MOSFET WITH SUBSTRATE DRAIN CONNECTION

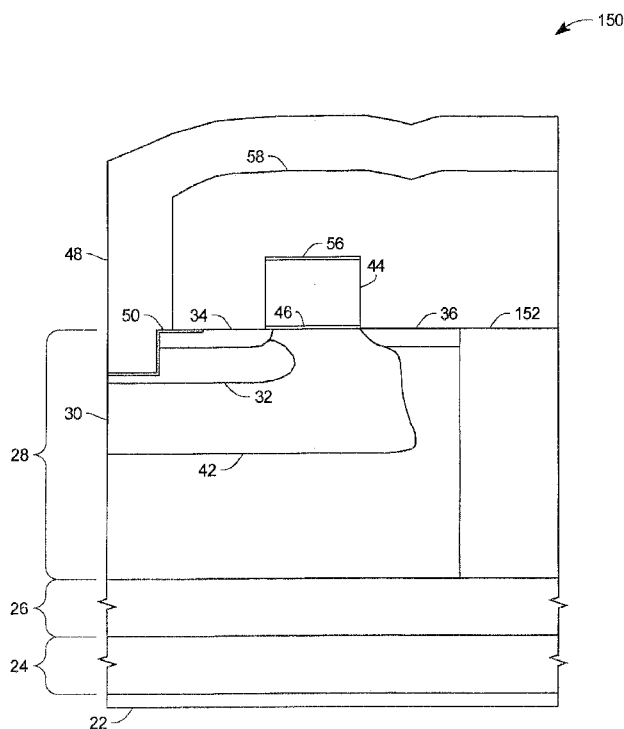


FIG. 8

(57) Abstract: In one form a lateral MOSFET includes an active gate positioned laterally between a source region and a drain region, the drain region extending from an upper surface of a monocrystalline semiconductor body to a bottom surface of the monocrystalline semiconductor body, and a non-active gate positioned above the drain region. In another form the lateral MOSFET includes a gate positioned laterally between a source region and a drain region, the drain region extending from an upper surface of a monocrystalline semiconductor body to a bottom surface of the monocrystalline semiconductor body, the source region and the drain region being of a first conductivity type, a heavy body region of a second conductivity type in contact with and below the source region, and the drain region comprising a lightly doped drain (LDD) region proximate an edge of the gate and a sinker extending from the upper surface of the monocrystalline body to the bottom surface of the monocrystalline semiconductor body.



MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, **Published:**

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,

ML, MR, NE, SN, TD, TG).

— *without international search report and to be republished
upon receipt of that report (Rule 48.2(g))*

LATERAL MOSFET WITH SUBSTRATE DRAIN CONNECTION

CROSS REFERENCE TO A RELATED APPLICATION

[0001] This application is based on U. S. Patent Application No. 12/339,215 filed December 19, 2008. Reference is also made to a related application entitled "Lateral Drain MOSFET With Improved Clamping Voltage Control" which has attorney docket number 3033356 and which is incorporated herein in its entirety by reference.

FIELD OF THE INVENTION

[0002] This invention relates to lateral MOSFETs with a substrate drain connection, and more particularly to lateral MOSFETs with a substrate drain connection wherein the drain has a lateral segment and a vertical segment.

BACKGROUND OF THE INVENTION

[0003] There exists a number of U.S. patents directed to lateral MOSFETs with a substrate drain connection including United States Patent Number 6,600,182 issued to Rumennik on July 29, 2003, and United States Patent Number 7,282,765 issued to Xu et al. on October 16, 2007, both of which make reference to additional patents related to lateral MOSFETs with a substrate drain connection. Also, Ng, Jacky C. W., A Novel Planar Power MOSFET With Laterally Uniform Body and Ion-Implanted JFET Region, IEEE Electron Device Letters, Vol. 29, No. 4, April 2008, pp. 375-377, describes a lateral MOSFET with a substrate drain connection. For these devices which are designed for use in high frequency power applications, a number of transistor characteristics, such as gate-to-drain capacitance and R_{dson} , are important and therefore affect the sales of such devices.

SUMMARY OF THE INVENTION

[0004] The invention comprises, in one form thereof, a lateral MOSFET comprising a heavily doped substrate of a first conductivity type with a first epitaxial layer of the first conductivity type laying over the substrate. The lateral MOSFET includes a diffused tub of a second conductivity type opposite to the first conductivity type formed in the first

epitaxial layer, an active gate electrode on a gate dielectric which is on a major surface of the first epitaxial layer, and a source region of the first conductivity type in the first epitaxial layer extending to the major surface of the first epitaxial layer and self aligned with a first edge of the active gate electrode. Also included is a lightly doped drain of the first conductivity type in the first epitaxial layer extending to the major surface of the first epitaxial layer and self aligned with a second edge of the active gate electrode on an opposite side of the active gate electrode from the first edge, and a sinker region of the first conductivity type on the same side of the active gate electrode as the lightly doped drain and spaced apart from the active gate electrode, the sinker region extending from the major surface of the first epitaxial layer to a depth substantially equal to the depth of the first epitaxial layer.

[0005] In a further aspect of the present invention the lateral MOSFET comprises a second epitaxial layer of the first conductivity type between the substrate and the first epitaxial layer.

[0006] In a still further aspect of the present invention the lateral MOSFET comprises a non-active gate attached to the major surface of the first epitaxial layer, the non-active gate on the same side of the active gate electrode as the lightly doped diffusion and spaced apart from the active gate electrode, and substantially between the lightly doped diffusion and the portion of the sinker in the major surface of the first epitaxial layer.

[0007] In yet another aspect of the present invention the diffused tub has a dopant profile of a diffused region such that the dopant profile of the diffused tub decreases from the major surface of the first epitaxial layer downward.

[0008] In an additional aspect of the present invention the diffused tub has a dopant profile of a region formed by multiple implants such that the vertical dopant profile of the diffused tub is substantially uniform.

[0009] In still another aspect of the present invention the lateral MOSFET includes a heavily doped region of the second conductivity type laying substantially below the source region.

[0010] In yet another aspect of the present invention the sinker has a vertical dopant profile which decreases from the major surface of the first epitaxial layer downward.

[0011] In an alternative aspect of the present invention the sinker has a vertical dopant profile which is substantially uniform.

[0012] In still another alternative aspect of the present invention the sinker has a vertical dopant profile which increases from the major surface of the first epitaxial layer downward.

[0013] The invention comprises, in one form thereof, a lateral MOSFET comprising an active gate positioned laterally between a source region and a drain region, the drain region extending from an upper surface of a monocrystalline semiconductor body to a bottom surface of the monocrystalline semiconductor body, and a non-active gate positioned above the drain region.

[0014] The invention comprises, in another form thereof, a lateral MOSFET comprising a gate positioned laterally between a source region and a drain region, the drain region extending from an upper surface of a monocrystalline semiconductor body to a bottom surface of the monocrystalline semiconductor body, the source region and the drain region being of a first conductivity type, a heavy body region of a second conductivity type in contact with and below the source region, metallization extending below the upper surface of the monocrystalline body in contact with the source region and the heavy body along a lateral surface and a side surface of each of the source region and the heavy body, and the drain region comprising a lightly doped drain (LDD) region proximate an edge of the gate and a sinker extending from the upper surface of the monocrystalline body to the bottom surface of the monocrystalline semiconductor body.

[0015] In yet another form, the invention includes a method for forming a lateral MOSFET with a substrate drain connection. The method comprises the steps of forming a source region and a drain region in an upper surface of a monolithic semiconductor body, and an active gate positioned above the monocrystalline semiconductor body between the source region and the drain region, the drain region extending from an upper surface of the monocrystalline semiconductor body to a bottom surface of the monocrystalline semiconductor body, and forming a non-active gate positioned above the drain region.

[0016] In still another form, the invention includes a method for forming a lateral MOSFET with a substrate drain connection. The method comprises the steps of forming

a source region and a drain region in an upper surface of a monolithic semiconductor body, and a gate positioned above the monocrystalline semiconductor body between the source region and the drain region, the drain region extending from an upper surface of the monocrystalline semiconductor body to a bottom surface of the monocrystalline semiconductor body, and forming a heavy body region of a second conductivity type in contact with and below the source region, wherein the step of forming the drain region includes the step of forming a lightly doped drain (LDD) region proximate an edge of the gate, and a sinker extending from the upper surface of the monocrystalline body to the bottom surface of the monocrystalline semiconductor body.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The aforementioned and other features, characteristics, advantages, and the invention in general will be better understood from the following more detailed description taken in conjunction with the accompanying drawings, in which:

[0018] FIG. 1A is a side diagrammatical view of an embodiment of a lateral MOSFET with a substrate drain connection according to the present invention;

[0019] FIG. 1B is a side diagrammatical view of another embodiment of a lateral MOSFET with a substrate drain connection according to the present invention;

[0020] FIGs. 2A, 2B, 2C, 2D, 2E, 2F, and 2G are side diagrammatical views of the lateral MOSFET shown in FIG. 1A at selected processing stages in forming the lateral MOSFET of FIG. 1A;

[0021] FIGs. 2H, 2I, and 2J show alternative embodiments of the heavy body shown in FIG. 1 at the process stage shown in FIG. 2E;

[0022] FIG. 3A is a side diagrammatical view of two other embodiments of a lateral MOSFET with a substrate drain connection according to the present invention;

[0023] FIG. 3B is a partial diagrammatical end view of one of the embodiments of the lateral MOSFET shown in FIG. 3A;

[0024] FIG. 3C is a perspective diagrammatical view of another of the embodiments of the lateral MOSFET shown in FIG. 3A;

[0025] FIG. 4 is a side diagrammatical view of the lateral MOSFET shown in FIG. 1A showing selected simulated characteristics of the lateral MOSFET of FIG. 1A;

[0026] FIG. 5 is a side diagrammatical view of three of the lateral MOSFETs shown in FIG. 1A embodied on a common substrate.

[0027] FIGs. 6A and 6B show alternative embodiments of the metallization shown in FIG. 1;

[0028] FIG. 7 shows an alternative embodiment of a gate dielectric structure shown in FIG. 1; and

[0029] FIG. 8 is another embodiment of a lateral MOSFET with a substrate drain connection according to the present invention.

[0030] It will be appreciated that for purposes of clarity and where deemed appropriate, reference numerals have been repeated in the figures to indicate corresponding features. Also, the relative size of various objects in the drawings has in some cases been distorted to more clearly show the invention.

DETAILED DESCRIPTION

[0031] Turning now to the drawings, FIG. 1A is a side diagrammatical view of an embodiment of a lateral MOSFET 20 according to the present invention. The lateral MOSFET 20 includes a substrate drain connection 22, which may be a metallization, a heavily doped substrate 24 of a first conductivity type which has grown thereon an optional heavily doped first epitaxial layer 26 of the first conductivity type, and a second epitaxial layer 28 having a top or major surface 29. The substrate 24 and the second epitaxial layer 28 with or without the optional heavily doped first epitaxial layer 26 form a monocrystalline semiconductor body. Although the first conductivity type can be N type or P type, for ease of discussion the first conductivity type will hereinafter be referred to as N type, and a second conductivity type, opposite to the first conductivity type, will therefore be referred to hereinafter as P type. As described in more detail below, the second epitaxial layer 28 is initially N type that is more lightly doped than the substrate 24 or the optional first epitaxial layer 26, and contains a P well 30, a heavy P body 32, a heavily doped N-type source region 34 which extends to the upper surface of the second epitaxial layer 28, an LDD region 36, a sinker 38, and an optional heavily doped N region 40 formed in the sinker 38 which extends to the upper surface of the

second epitaxial layer 28. The line 42 indicates the PN junction between the P well 30 and the N-type second epitaxial layer 28 and the LDD region 36.

[0032] An active gate electrode 44 is above the second epitaxial layer 28 and is separated from the second epitaxial layer 28 by a gate oxide 46. The gate oxide can be thermally grown, deposited or be of another dielectric material which can have a high dielectric constant (K) or a low dielectric constant, or a combination of dielectrics. FIG. 7 shows the active gate 44 with two dielectric layers 47 and 49 in place of the gate oxide 46, where dielectric layer 47 may be nitride and dielectric layer 49 may be a grown oxide. A portion of the P well 30 forms the channel region of the active gate electrode 44 with the source region 34 and the LDD region 36 extending for a short distance under the active gate electrode 44. The heavy P body 32 lies under the source region 34 and extends laterally further under the active gate electrode 44 in the embodiment shown in FIG. 1A. The P well 30 extends down from the gate oxide 46 and under the heavy P body 32.

[0033] Metallization 48 extends down into, and contacts, the heavy P body 32 and the source region 34 through a silicide layer 50.

[0034] A second non-active gate electrode 52 lies over the sinker 38 with a gate oxide 54 lying between the top of the second epitaxial layer 28 and the non-active gate electrode 52. Both the active gate electrode 44 and the non-active gate electrode 52 may be polysilicon with silicide layers 56 on the top surfaces of the two gate electrodes 44, 52. An interlevel dielectric 58 separates the metallization 48 from the gate electrodes 44, 52 and the top surface of the second epitaxial layer 28.

[0035] The lateral extent of the sinker 38 with respect to the active gate electrode 44 affects the $R_{ds(on)}$ and the breakdown voltage of the MOSFET 20. Although a lateral MOSFET according to the present invention does not have to have the non-active gate 52 as shown in FIG. 1B, the non-active gate electrode 52, which is formed with the same mask layer as the active gate electrode 44, provides more precise positioning of the sinker 38 with respect to the active gate electrode 44 than without the non-active gate electrode 52. The non-active gate electrode 52 is used as a portion of the mask for the sinker 36 implant, and thus the distance from the edge of the exposed region of the major surface 29 which will be implanted to form the sinker 38 to the edge of the active gate electrode

44 is set by a single mask. Without the non-active gate electrode 52, the distance from the exposed region of the major surface 29, which will be implanted to form the sinker 38, to the active gate electrode 44 is subject to the variation in alignment of two separate masks, and the width of the lateral MOSFET 60 shown in FIG. 1B may be wider than the width of the lateral MOSFET 20 shown in FIG. 1A to compensate for the mask alignment tolerance. For example, the width of the lateral MOSFET 20 of FIG. 1A may be 4 μm while the width of the lateral MOSFET 60 of FIG. 1B may be 5 μm .

[0036] Those skilled in the art will understand that the non-active gate electrode 52, while formed with the same etch mask used to form the active gate electrode 44, only has to be wide enough to compensate for the mask variations in the photoresist mask used to pattern the photoresist shown in FIG. 2D. Thus it may be possible that the non-active gate electrode 52 may be of a different material than the active gate electrode 44, and may have a shape different from the active gate electrode 44.

[0037] FIGS. 2A-2G are side diagrammatical views of the lateral MOSFET 20 at selected processing stages in one embodiment for forming the lateral MOSFET 20. In FIG. 2A, the substrate 24 is N⁺ and may be arsenic or phosphorous, and if phosphorous, may be red phosphorous with a conductivity, ρ , in the range of 0.5 to 2.5 $\text{m}\Omega\cdot\text{cm}$. If the substrate is phosphorous, the optional first epitaxial layer 26 may be arsenic doped to provide a buffer region between the heavily doped phosphorous substrate 24 into the second epitaxial layer 28 to isolate the diffusion from the heavily doped phosphorous substrate 24 and the second epitaxial layer 28. If an arsenic substrate 24 is used, the first arsenic epitaxial layer 26 may not be used. The arsenic first epitaxial layer 26 may have a ρ of about 8 $\text{m}\Omega\cdot\text{cm}$ to provide an adequate conductivity path from the second epitaxial layer 28 to the substrate 24 and may have a thickness range of 0 to 4 μm depending on the extent of the diffusion from the substrate 24 which, in turn, depends on the thermal cycles during manufacture of the lateral MOSFET 20. Thus the first epitaxial layer 26 is used to maintain the desired dopant concentration in the second epitaxial layer 28 which affects the breakdown voltage of the lateral MOSFET 20.

[0038] The second epitaxial layer 28 may be a N-type layer with phosphorous doping, preferably with a ρ of about 2 $\Omega\cdot\text{cm}$.

[0039] Formed in the upper portion of the second epitaxial layer 28 is a P well 30 which may be formed by gaseous diffusion, by a single implant, or by multiple implants. A typical CMOS tub may be created if the P well 30 is formed by gaseous diffusion. A single implantation, as indicated by arrows 64, may be a boron implant at a nominal dose of 7×10^{13} @ 60 KeV. Multiple implants, as indicated by arrows 64 and 66, may include retrograde implants which may be at about 40 KeV and about 120 KeV, respectively.

[0040] The single and multiple implantations used to form the P well 30 have the advantage over gaseous diffusion of forming a more uniform vertical doping profile which may provide more consistency in the threshold voltages, R_{ds} on, and Q_{gs} of multiple wafers of the lateral MOSFETs 20. If such consistency is present, the R_{ds} on likely can be reduced while maintaining an acceptable Q_{gs} compared to a diffused P well 30. The P well 30 is not formed in LOCOS regions or in termination regions of the semiconductor die.

[0041] FIG. 2B includes a threshold voltage, V_{th} , adjustment implant process which may or may not be necessary depending on the doping concentration at an upper region 70 of the P well 30. Shown in FIG. 2B is a sacrificial oxide layer 72 formed on the second epitaxial layer 28 prior to the threshold voltage adjust implantation, indicated by the arrows 74, to adjust the threshold voltage of the lateral MOSFET 20. Also shown in FIG. 2B is another possible implantation 75 of germanium to form a SiGe strained silicon channel region to improve hole and electron mobility. Other techniques which are known to those skilled in the art can be used to form the strained channel region.

[0042] FIG. 2C shows the structure shown in FIG. 2A after a gate oxide 80, which may be about 125 Å thick, depending on the desired electrical characteristics of the device, and may have a range of 50 to 400 Å, has been formed on the second epitaxial layer 28, and polysilicon has been deposited and patterned to form the active gate electrode 44 and the non-active gate electrode 52. The active gate electrode 44 may alternatively be a refractory metal. Seal oxides 82, which may be a little thicker than the gate oxide 80, have been formed around the gate electrodes 44, 52. The seal oxides 82 are optional and, if used, the thickness is dependent upon subsequent implantation energies. Implantation of the N type dopants, indicated by arrows 84, form LDD regions 86. The LDD regions 86 may be arsenic doped with an implantation dose selected from the range of 1×10^{11} to

1e12 based at least in part on the subsequent thermal cycles that the lateral MOSFET device 20 is subjected to and also by a tradeoff between the R_{dson} and Q_{gd} of the lateral MOSFET device 20. Although the LDD regions are formed everywhere in the active regions not masked by the gate electrodes 44, 52 and the seal oxides 82, only the LDD region 36 (shown in FIG. 1) does not receive heavier concentrations of dopants in later processing.

[0043] FIG. 2D shows a photoresist layer 90 used to form the sinker 38. The sinker 38 may be formed using up to three implants as indicated by the three sets of arrows 92, 94, and 96 in one or more embodiments of the present invention. For example a single implant of phosphorous at a dose of about $5 \times 10^{15} @ 160 \text{ KeV}$ may be used, two implants, one of arsenic at about $2 \times 10^{15} @ 40 \text{ KeV}$ and a second of phosphorous at about $3 \times 10^{16} @ 160 \text{ KeV}$ may be used, or three or more implants may be used with dopants, dosages, and implant voltages selected for a desired vertical dopant profile by those skilled in the art. The use of the non-active gate 52, the seal oxide 82 and the photoresist 90 allows relatively high implantation energies to form a uniform drain sinker 38 which has a relatively lower drain resistance than a drain sinker 38 with a vertical dopant gradient such as formed by gaseous diffusion. With multiple implants the vertical dopant profile of the sinker 38 may also increase from the major surface 29 to the lower region of the second epitaxial layer 28. Multiple implants allow the drain sinker 38 to be deeper with less lateral width compared to a single implant and subsequent diffusion since pushing a single implant deeper causes more lateral spread of the final sinker 38 and an increase in the resistivity of the sinker 38.

[0044] FIG. 2E shows process steps which may be used for forming the heavy P body 32, the source region 34, and the optional heavily doped N region 40. A photoresist layer 100 fills the gap between the gate electrodes 44, 52. The heavy P body 32, the N type source region 34, and the optional heavily doped N region 40 may be formed by the implantation of P-type dopants indicated by the arrows 102, and N-type dopants indicated by the arrows 104. If the optional heavily doped N region 40 is not desired, the photoresist layer 100 would be extended to the right edge of the second epitaxial layer 28.

[0045] The heavy P body 32 may be implanted with boron at a dose of about $2.5 \times 10^{14} @ 60 \text{ KeV}$. The concentration of the heavy P body 32 is determined by several

factors, including the desired unclamped inductive switching (UIS) capability, the impact on the threshold voltage, the breakdown voltage, the $R_{ds(on)}$, and the metallization used as Ti will leach boron out of the heavy P body 32. The source region 43 may be implanted with arsenic at a dose of about $5 \times 10^{15} @ 160 \text{ KeV}$. With the photoresist mask 100 the sinker 35 will also receive the boron implant, but the heavier concentration of sinker N type dopants will dominate the boron implanted dopants. Alternatively, the region at the surface of the second epitaxial layer 28 can be masked during the boron implant. After subsequent thermal treatment of the device shown in FIG. 2E, the source region may have a depth of $0.25 \mu\text{m}$ or less.

[0046] FIG. 2F shows a stage in the process of forming the lateral MOSFET 20 which may be used to form silicide on the gates 44, 52, on a side and a portion of the top surface of the source region 34, and on a side and a lateral surface of the heavy P body 32. An etched dimple 110 is formed on the left edge of the source region 34 and in an upper left portion of the heavy P body 32. The gate oxide 80 is stripped from the upper surface of the second epitaxial layer 28 except the portions 46, 54 under the gates 44, 52, respectively, and a dielectric 112, which may be borophosphosilicate glass (BPSG), is formed on the upper surface of the epitaxial layer 28 except in the dimple 110 and a portion on the top surface of source region 34 next to the dimple 110. The vertical height of the BPSG is the same as the height of the active gate 44 to allow formation of a silicide layer 114 on the top of the active gate 44 in one process embodiment.

Alternatively, the silicides for the source region 34 and the heavy P body 32 may be formed in a process step separate from the process step used to form the silicide of the gate electrode 44. In the process stage shown in FIG. 2F, the non-active gate 52 is also silicided to form a top silicide layer 116. Another silicide layer 118 is formed in the cutout region 110 and the exposed top portion of the source region 34. The silicide layers may consist of Ti, Co, Pt, TiW, W, and other refractory metals or combinations thereof. The silicide layer 114 on the top of the active gate 44 results in faster switching of the lateral MOSFET 20 as is well known by those skilled in the art.

[0047] FIG. 2G shows the dielectric layer 58, such as a BPSG layer, formed on the upper surfaces of the second epitaxial layer 28, the silicides 114, 116, and on a right portion of the silicide 118 on the top surface of the source region 34. Metallization is

then formed on the top and bottom of the structure shown in FIG. 2G to complete the lateral MOSFET 20 shown in FIG. 1A.

[0048] Chemical and mechanical polishing (CMP) can be used to provide planarity to improve photolithography capability and to facilitate forming salicides on the gate electrode 44.

[0049] FIGs. 2H, 2I, and 2J show alternative embodiments of the heavy body shown in FIG. 1 at the process stage shown in FIG. 2E. In FIG. 2H the heavy P body 32 extends downward to slightly above or below the bottom edge of the PN junction 42 shown in FIG. 2E. FIG. 2I shows the shape of the heavy P body 32 of FIG. 2E when the dimple 110 is formed before the heavy P body 32 is formed, and FIG. 2J is FIG. 2I with the dimple 110 formed before the heavy P body is formed.

[0050] FIGs. 3A 3B, and 3C show alternative methods of making contact to the heavy P body 32 by masking a portion of the source region 34 when it is formed so that a portion 124 of the heavy P body 32 lies at the top surface of the second epitaxial layer 28. The dimple 110 is not formed, and the metallization 48 lies on a silicide layer 126 which covers the top of portion 124 of the heavy P body 32 and the left top portion of source region 34. In FIG. 3C the metallization 48 and the dielectric layer 58 are not shown in order to avoid cluttering the drawing.

[0051] FIG. 4 is FIG. 1A showing simulated current paths 130 through the lateral MOSFET 20 together with simulated N-type dopant concentration contours 132, 134, and 136 shown in the second epitaxial layer 28 which shows two of several dopant contours which are not shown in FIG. 4 to avoid cluttering the figure. Contour lines 134 and 136 show the same dopant concentration which is a higher dopant concentration than the dopant concentration represented by the contour line 132. In one simulation, contour lines 134 and 136 represent an N-type dopant concentration of $1\text{e}18\text{ cm}^{-3}$, and contour line 132 represents an N-type dopant concentration of $1\text{e}17.5\text{ cm}^{-3}$.

[0052] In the simulation represented in FIG. 4, the vertical gradient is a simulation based on a single phosphorous implant at $5\text{e}15@160\text{ KeV}$. As stated above, multiple implantations may provide a narrower and more uniform vertical dopant profile.

[0053] The current density is greatest along the top surface of the second epitaxial layer 28 in the source region 34, the channel portion of the P well 30, and the LDD region 36.

Since the LDD region 36 is lightly doped compared to the source region 34, the LDD region 36 has a large effect on the R_{dson} of the lateral MOSFET 20. Also, since the LDD region 36 is the portion of the drain closest to the active gate 44, it has a large effect on the Q_{gd} of the lateral MOSFET 20.

[0054] FIG. 5 is a diagrammatical view of the physical relationship of three lateral MOSFETs 20 formed on a single substrate with metal plugs 140 that extend from the dimples 110 to the upper metal layer 48. The extension of the metallization 48 below the top surface of the second epitaxial layer 28 allows contact on side portions of the source region 34 and the heavy P body 32, thus allowing a shorter separation between adjacent source regions 34, and consequently a narrower width lateral MOSFET 20 than would generally be the case in which the metallization 48 did not extend along a side portion of the source region 34 and the heavy P body 32.

[0055] FIGs. 6A and 6B show alternative embodiments of the metallization 48 shown in FIG. 1. In FIG. 6A the aluminum top metallization 48 is covered by a barrier layer 142 with another metal layer 144, such as copper or other solderable metal such as silver, on top of the barrier layer 142 which has a lower resistivity than aluminum. The barrier layer 142 may be Ta, TaN, Ti, TiN or other barrier metals known in the industry. In FIG. 6B the barrier layer 142 and the low resistivity metal layer 144 replace the top aluminum layer 48 shown in FIG. 1A such that the barrier layer 142 is in direct contact with the silicide layer 50 and the dielectric layer 58.

[0056] FIG. 8 is another embodiment of a lateral MOSFET 150 with a substrate drain connection according to the present invention. Instead of the sinker 38 in the lateral MOSFET 20, the lateral MOSFET 150 has a trench 152 filled with a conductive material, such as polysilicon, which can be deposited without a dopant and later doped by ion implantation, or filled with a metal such as Ti, TiW, Co, Ta, TaN, Alum, Cu, etc., or a combination of such metal.

[0057] While the invention has been described with reference to particular embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from

the scope of the invention. For example, the lateral MOSFETs of the present invention can be formed as silicon-on-nothing MOSFETs.

[0058] Therefore, it is intended that the invention not be limited to the particular embodiments disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope and spirit of the appended claims.

Claims:

1. A lateral MOSFET comprising:
 - a) a heavily doped substrate of a first conductivity type;
 - b) a first epitaxial layer of said first conductivity type laying over said substrate;
 - c) a diffused tub of a second conductivity type opposite to said first conductivity type formed in said first epitaxial layer;
 - d) an active gate electrode on a gate dielectric which is on a major surface of said first epitaxial layer;
 - e) a source region of said first conductivity type in said first epitaxial layer extending to said major surface of said first epitaxial layer and self aligned with a first edge of said active gate electrode;
 - f) a lightly doped drain of said first conductivity type in said first epitaxial layer extending to said major surface of said first epitaxial layer and self aligned with a second edge of said active gate electrode on an opposite side of said active gate electrode from said first edge;
 - g) a sinker region of said first conductivity type on the same side of said active gate electrode as said lightly doped drain and spaced apart from said active gate electrode, said sinker region extending from said major surface of said first epitaxial layer to a depth substantially equal to the depth of said first epitaxial layer.
2. The lateral MOSFET of claim 1 further comprising a second epitaxial layer of said first conductivity type between said substrate and said first epitaxial layer.
3. The lateral MOSFET of claim 1 further comprising a non-active gate electrode attached to said major surface of said first epitaxial layer, said non-active gate electrode on the same side of said active gate electrode as said lightly doped diffusion and spaced apart from said active gate electrode, and substantially between said lightly doped diffusion and said portion of said sinker in said major surface of said first epitaxial layer.

4. The lateral MOSFET of claim 1 wherein said diffused tub has a dopant profile of a diffused region such that the dopant profile of the diffused tub decreases from the major surface of the first epitaxial layer downward.

5. The lateral MOSFET of claim 1 wherein said diffused tub has a dopant profile of a region formed by multiple implants such that the vertical dopant profile of the diffused tub is substantially uniform.

6. The lateral MOSFET of claim 1 further including a heavily doped region of said second conductivity type laying substantially below said source region.

7. The lateral MOSFET of claim 1 wherein said sinker has a vertical dopant profile which decreases from the major surface of the first epitaxial layer downward.

8. The lateral MOSFET of claim 1 wherein said sinker has a vertical dopant profile which is substantially uniform.

9. The lateral MOSFET of claim 1 wherein said sinker has a vertical dopant profile which increases from the major surface of the first epitaxial layer downward.

10. A lateral MOSFET comprising:

a) an active gate positioned laterally between a source region and a drain region, said drain region extending from an upper surface of a monocrystalline semiconductor body to a bottom surface of said monocrystalline semiconductor body; and

b) a non-active gate on a gate dielectric which is on a major surface of said lateral MOSFET and above said drain region.

11. A method for forming a lateral MOSFET with a substrate drain connection comprising the steps of:

- a) forming a source region and a drain region in an upper surface of a monolithic semiconductor body, and an active gate positioned above said monocrystalline semiconductor body between said source region and said drain region, said drain region extending from an upper surface of said monocrystalline semiconductor body to a bottom surface of said monocrystalline semiconductor body; and
- b) forming a non-active gate positioned above said drain region.

12. The method of claim 11 wherein said monocrystalline semiconductor body comprises an epitaxial layer formed on a substrate, said epitaxial layer and said substrate being of a first conductivity type.

13. The method of claim 11 wherein said monocrystalline semiconductor body comprises a substrate with a first epitaxial layer formed on said substrate, and a second epitaxial layer formed on said first epitaxial layer, said substrate, said first epitaxial layer, and said second epitaxial layer being of a first conductivity type.

14. The method of claim 13 further including the step of forming a counter doped region of a second conductivity type opposite to said first conductivity type in an upper portion of said second epitaxial layer.

15. The method of claim 14 wherein said counter doped region is formed by gaseous diffusion.

16. The method of claim 14 wherein said counter doped region is formed by a single ion implantation.

17. The method of claim 14 wherein said counter doped region is formed by multiple ion implantations.

18. The method of claim 14 further including the step of performing a threshold voltage implant in an upper surface region of said second epitaxial layer.

19. The method of claim 18 further including forming a sinker in said second epitaxial layer by performing an implant that is self aligned with the edged of the non-active gate which is farthest from said active gate.

20. The method of claim 19 wherein said sinker is formed by a single ion implantation.

21. The method of claim 19 wherein said sinker is formed by multiple ion implantations.

22. The method of claim 19 further including the steps of forming a heavy body of said second conductivity type and a source of said first conductivity type, both of which are self aligned with an edge of said active gate farthest from said sinker, said heavy body extending below said source region and having a lower dopant concentration than said source region.

23. The method of claim 22 further including forming a region of said first conductivity type that is self aligned with the edged of the non-active gate which is farthest from said active gate and is formed at the same time that said source region is formed.

24. The method of claim 22 further including forming a metal contact to said heavy body and source region, said metal contact extending below a top surface of said monocrystalline semiconductor body.

1/18

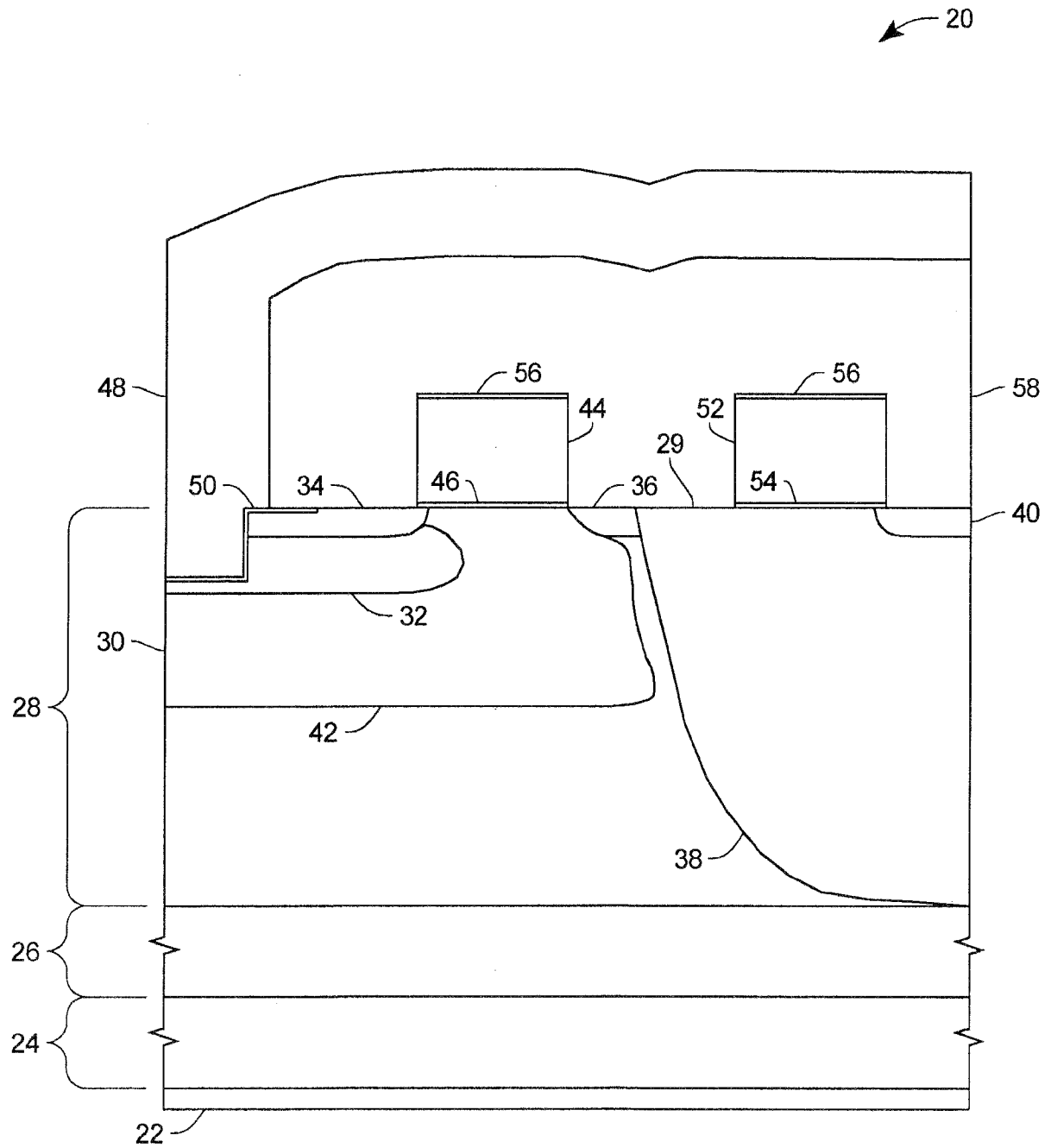


FIG. 1A

2/18

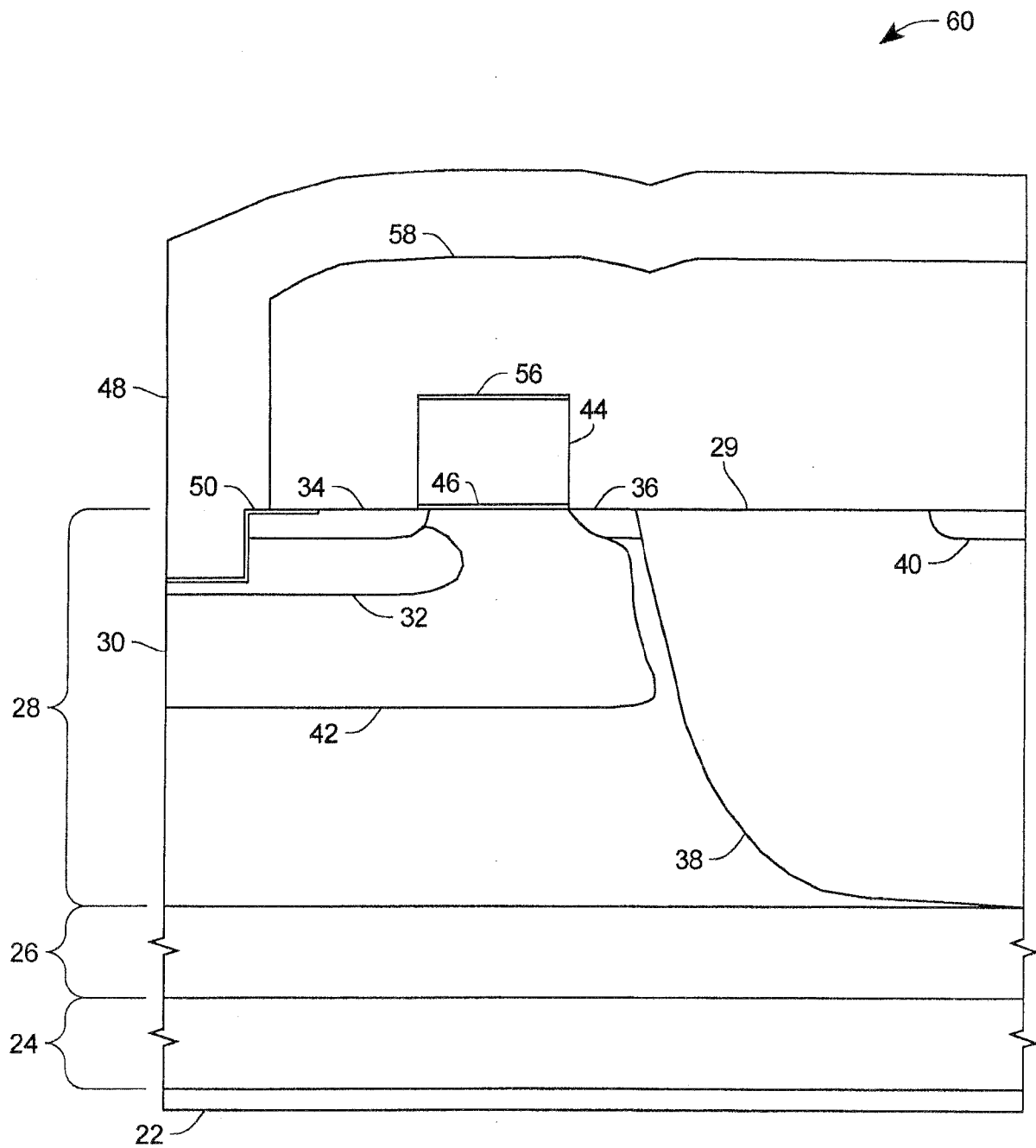


FIG. 1B

3/18

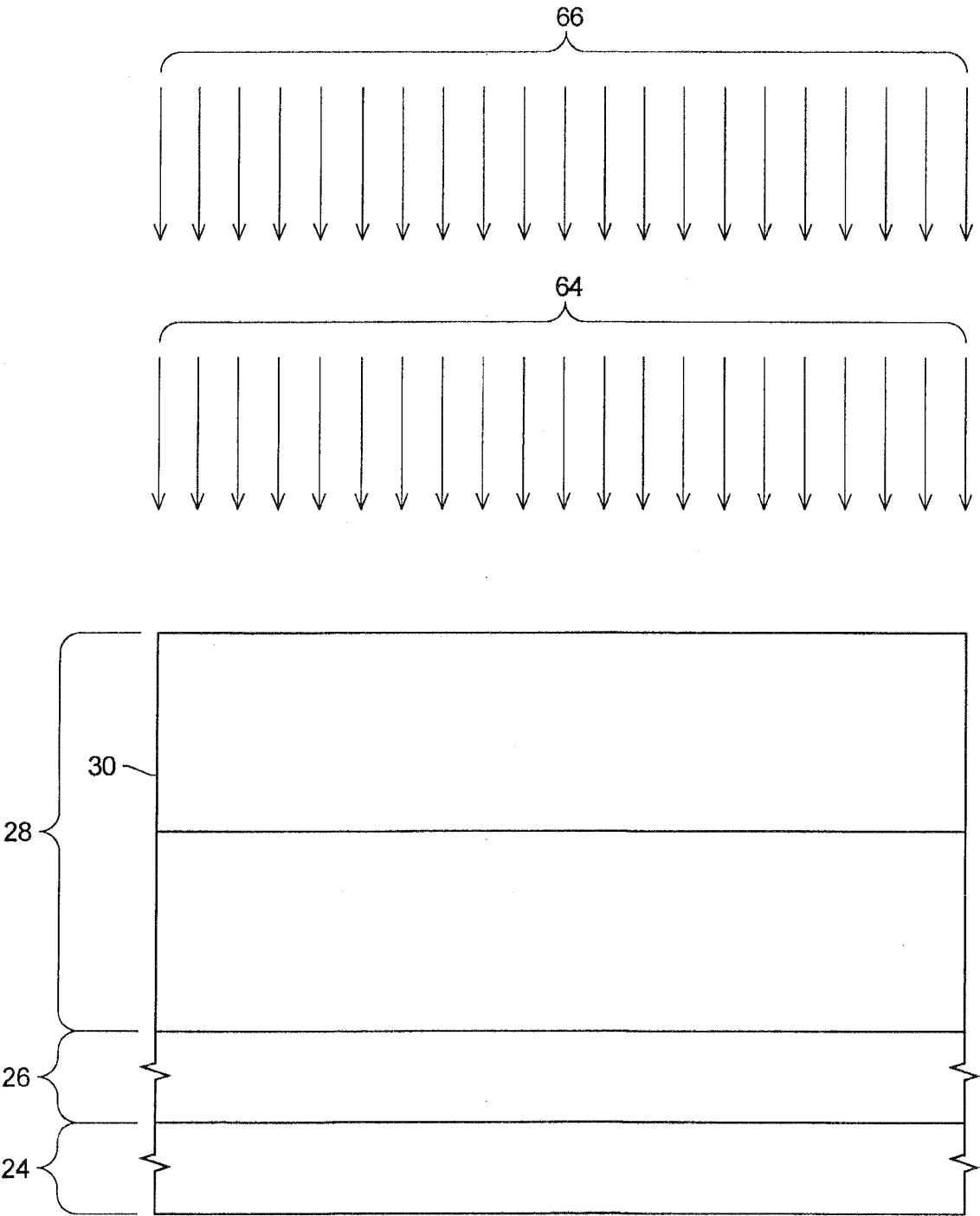


FIG. 2A

4/18

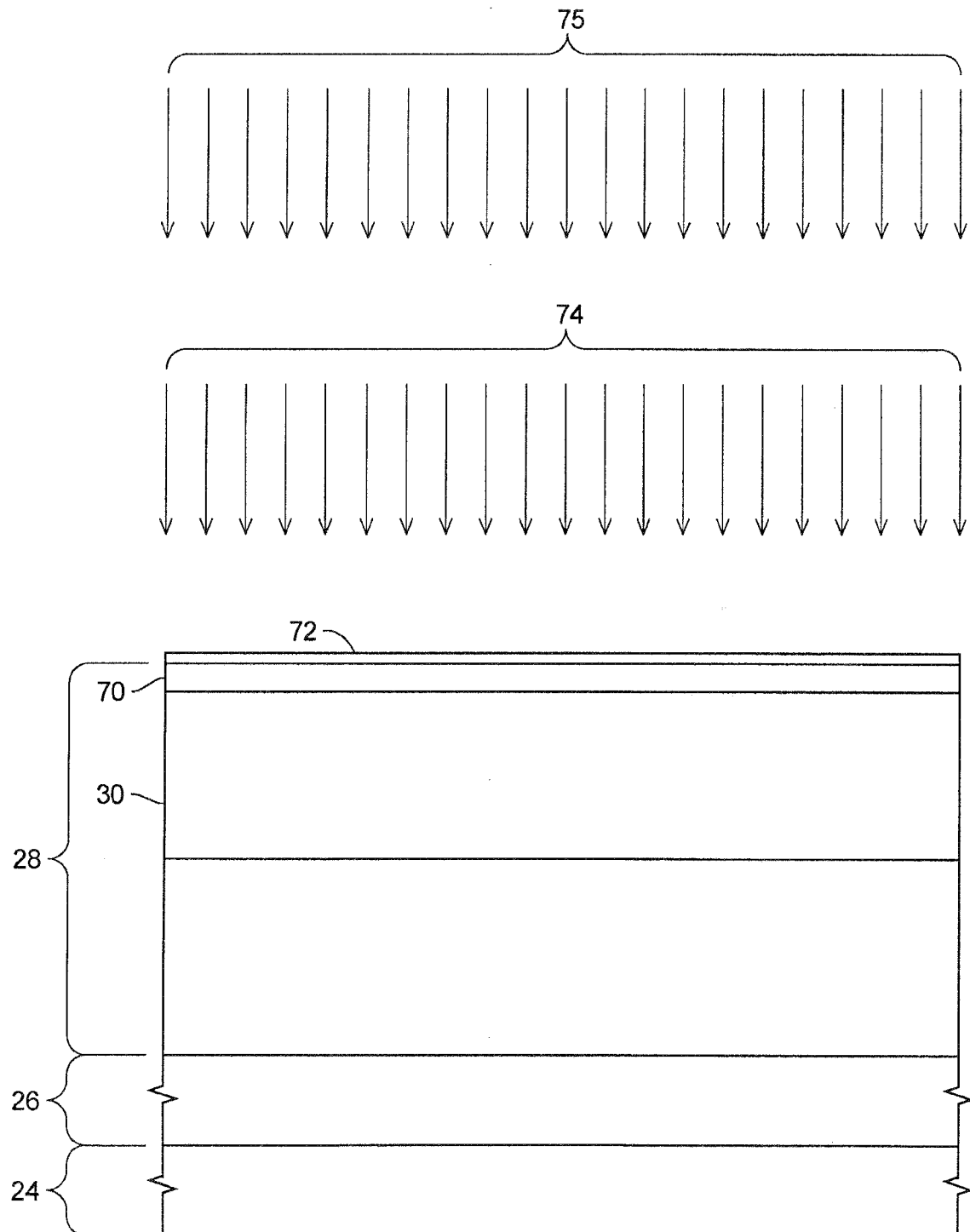


FIG. 2B

5/18

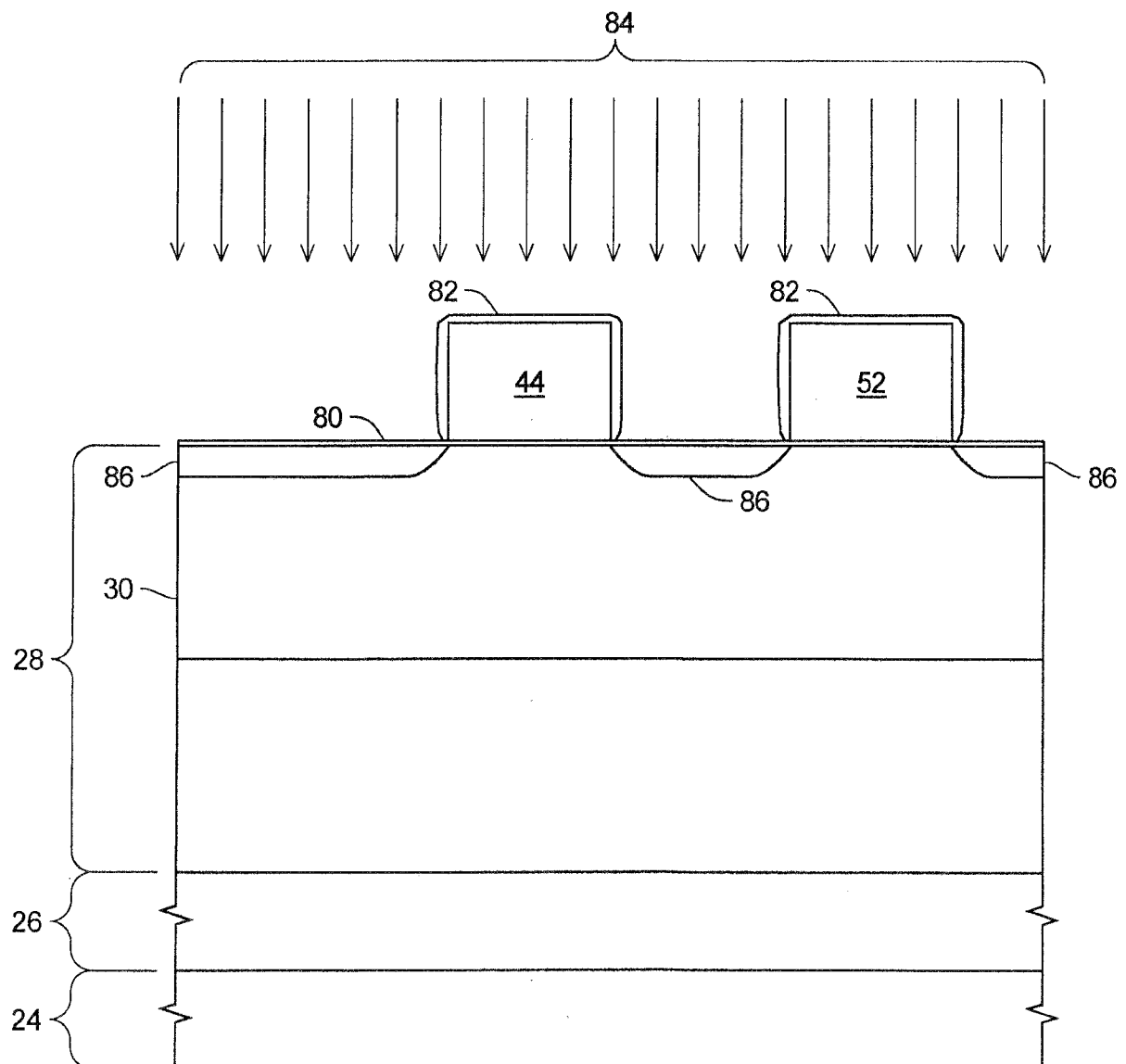


FIG. 2C

6/18

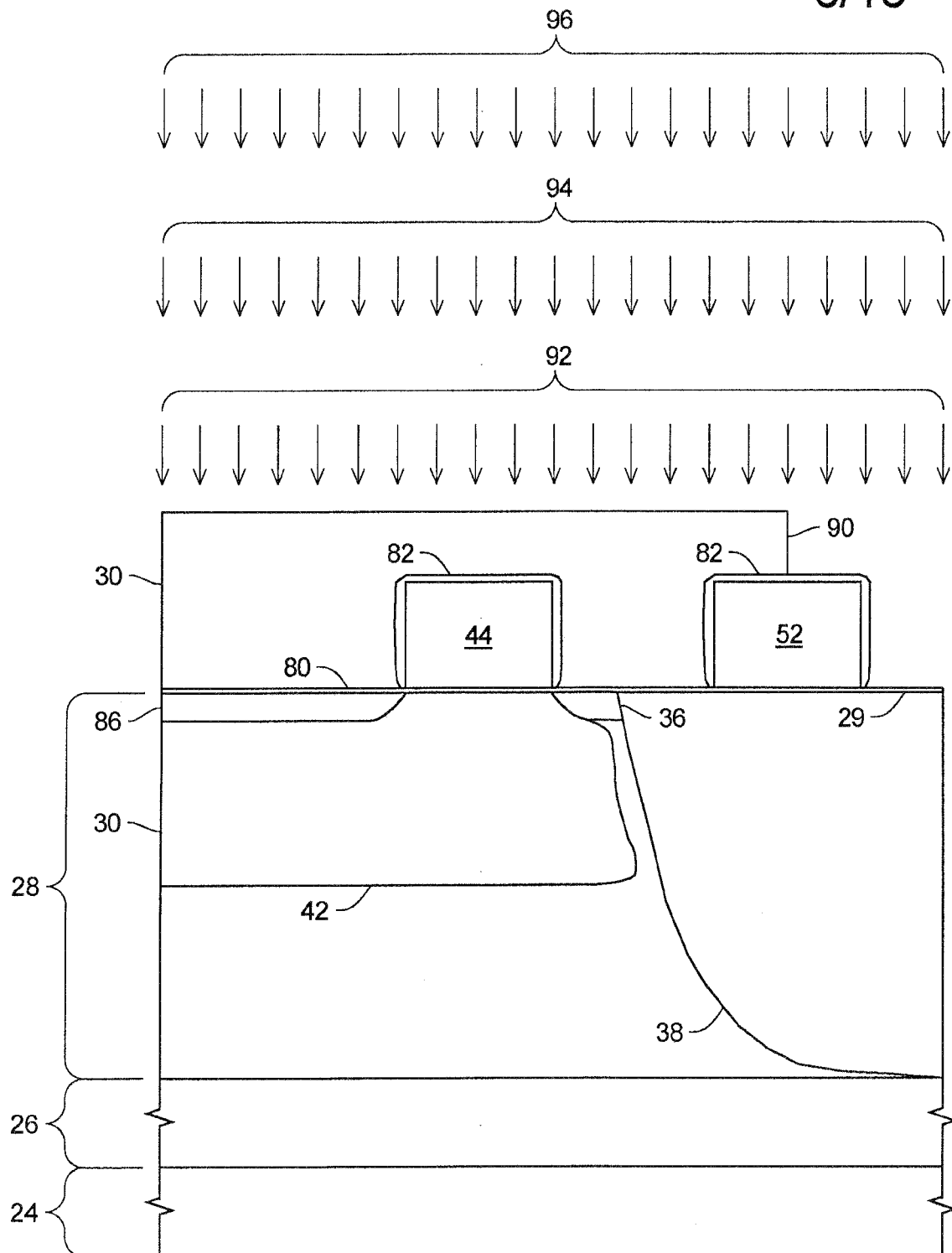


FIG. 2D

7/18

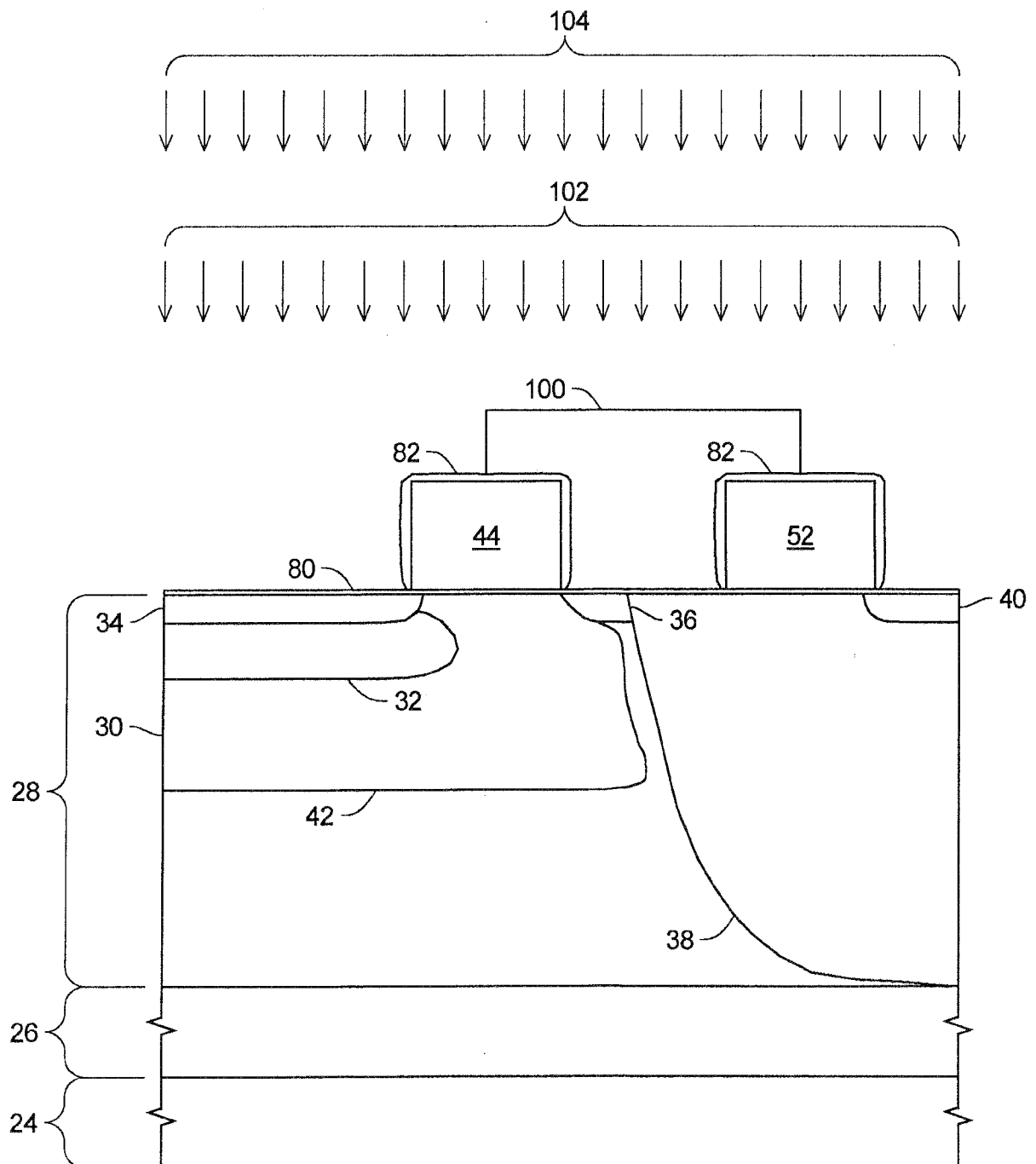


FIG. 2E

8/18

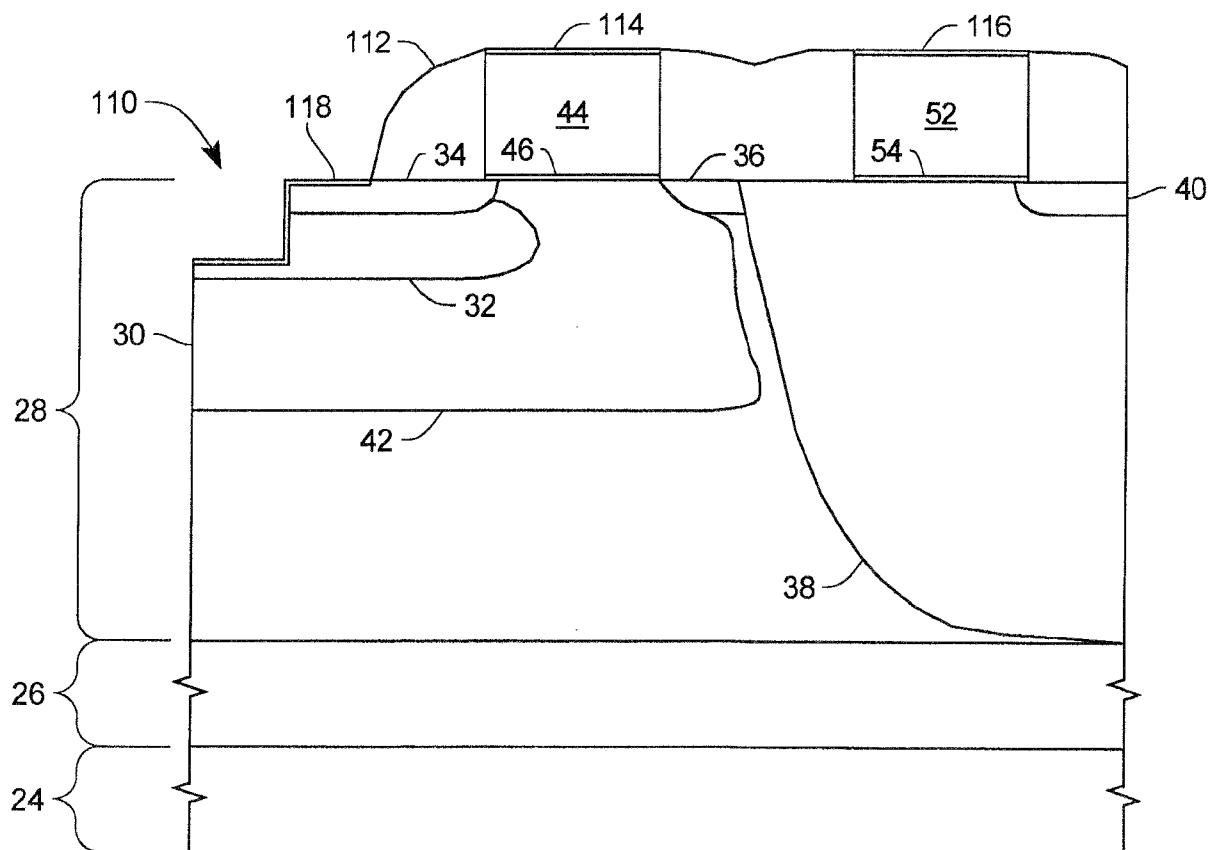


FIG. 2F

9/18

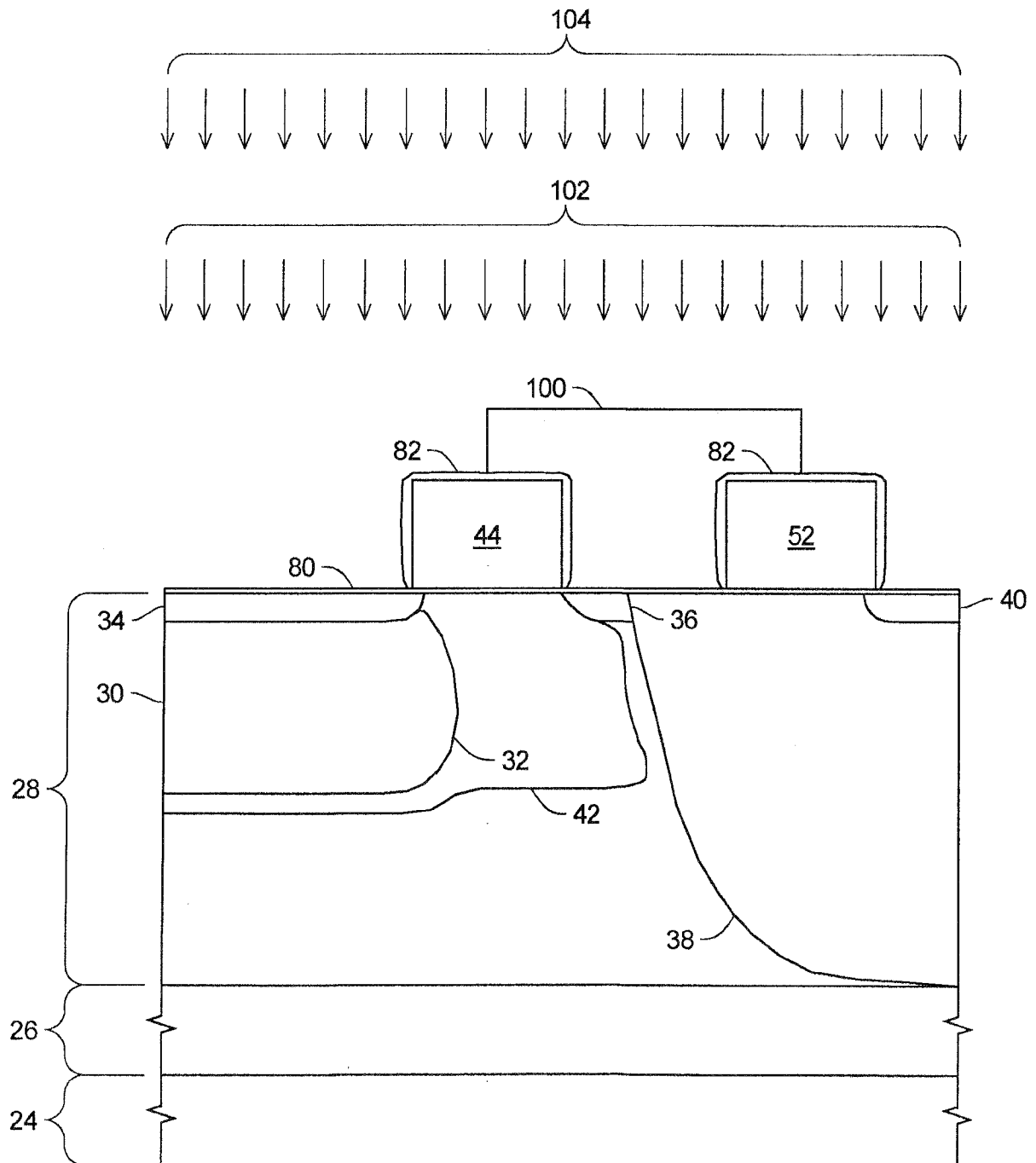


FIG. 2G

10/18

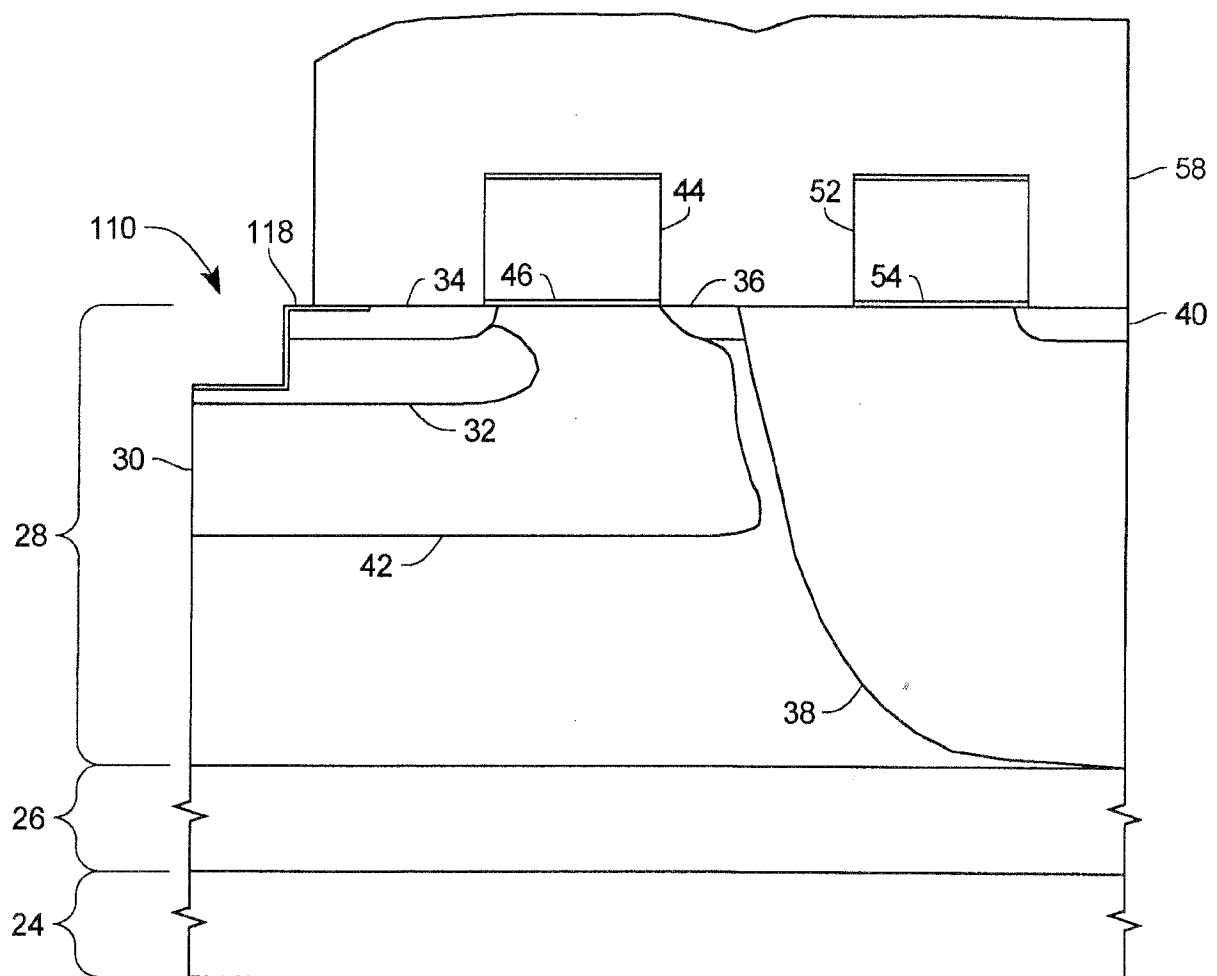


FIG. 2H

11/18

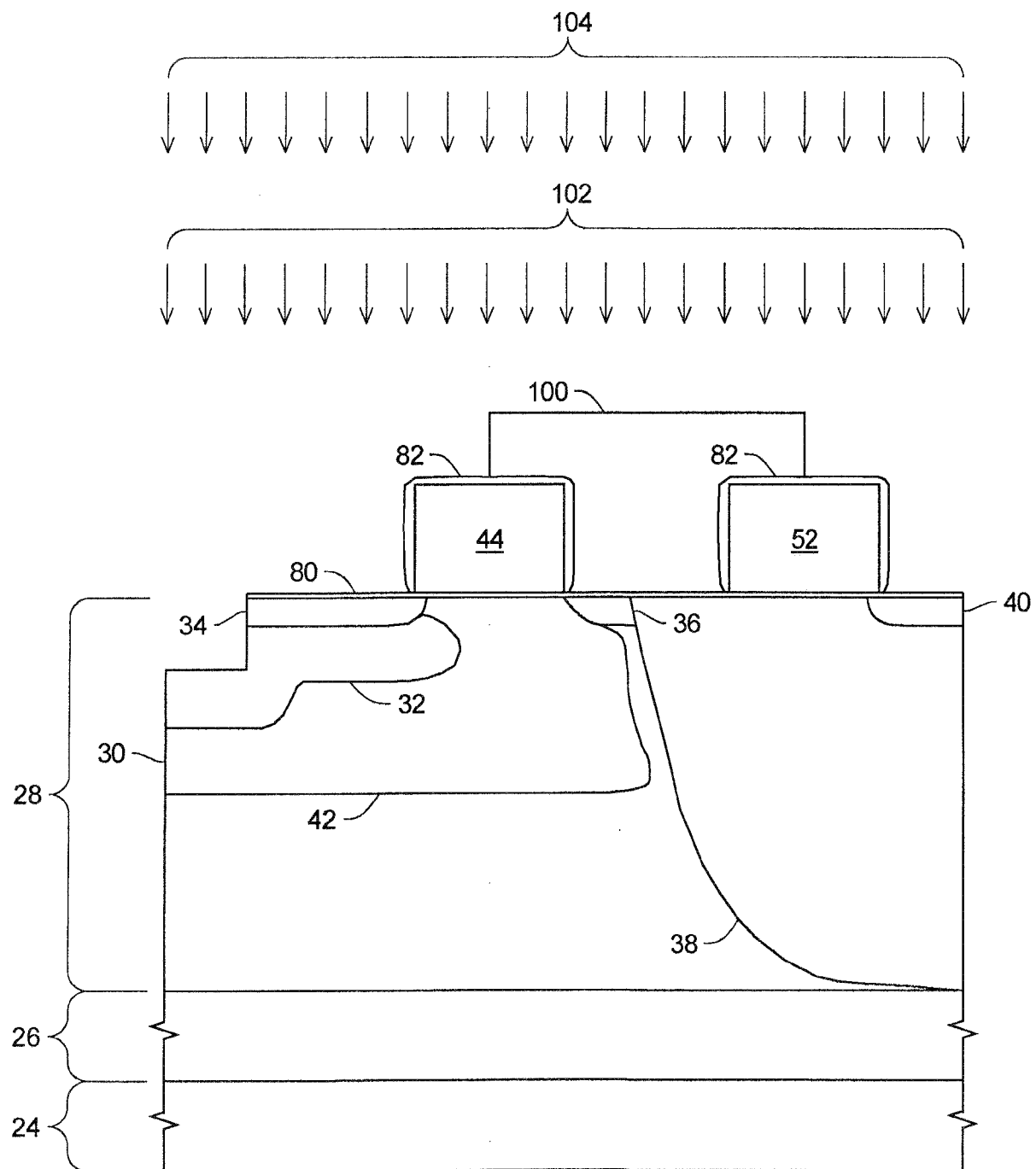


FIG. 2I

12/18

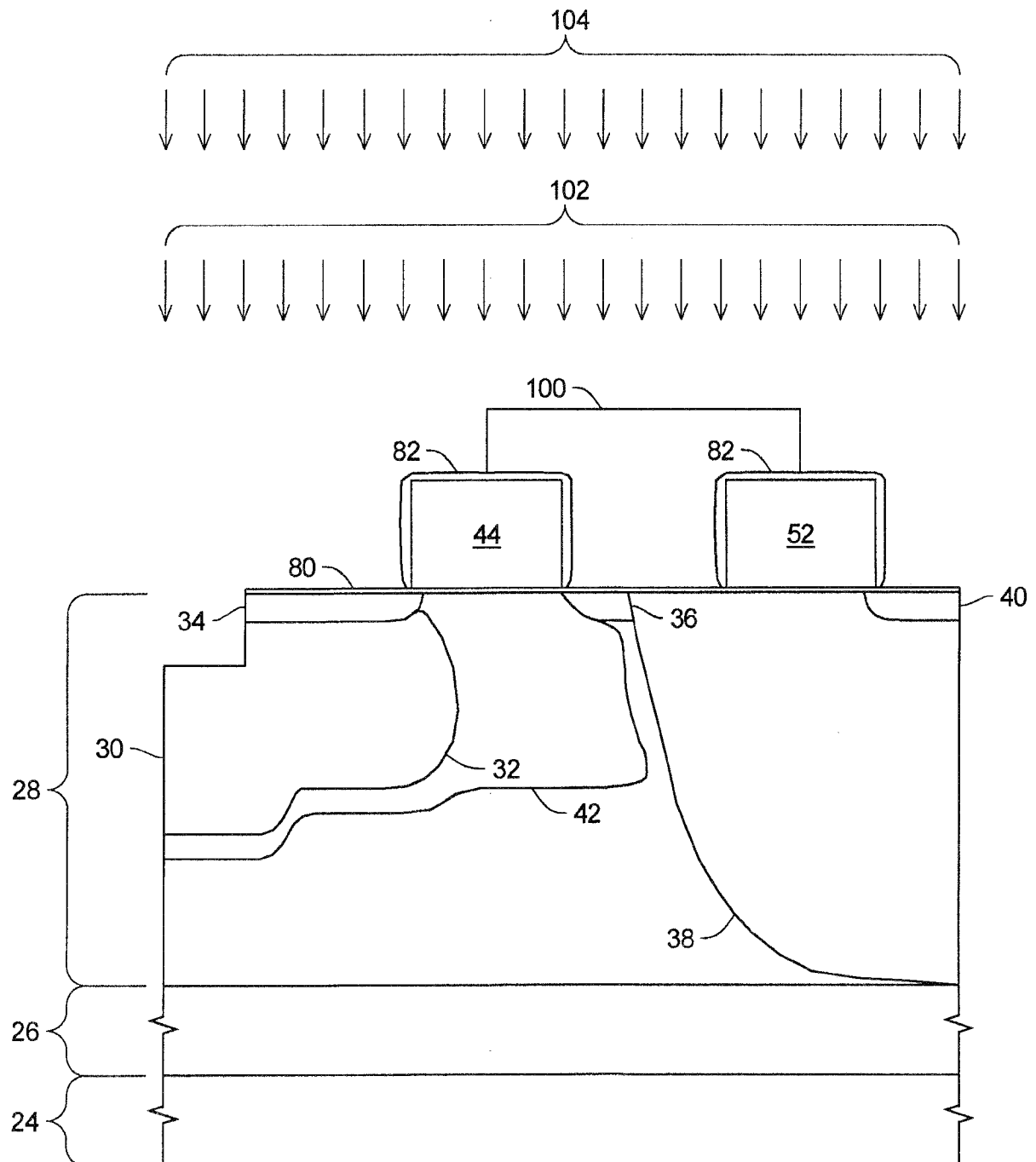


FIG. 2J

13/18

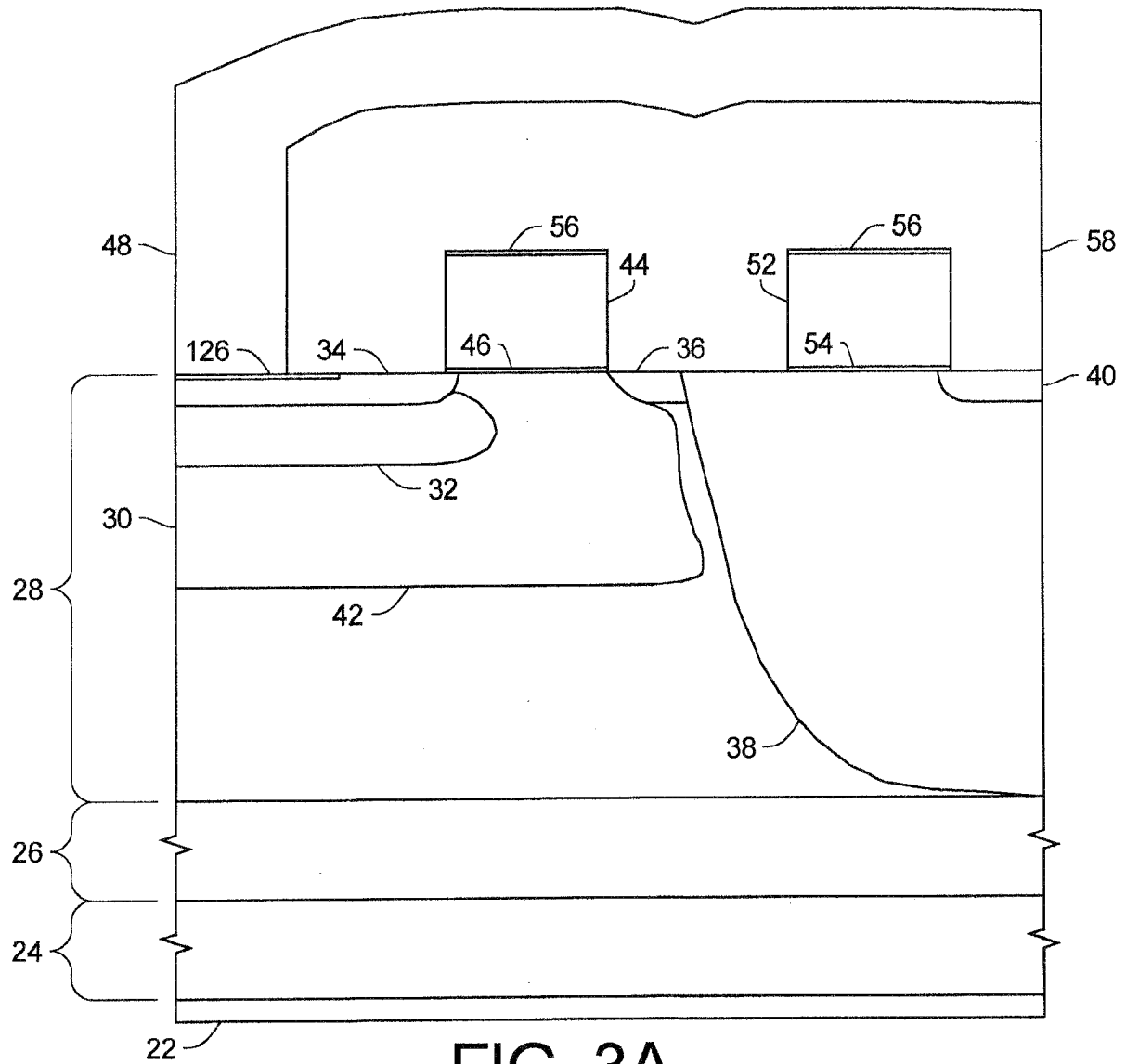


FIG. 3A

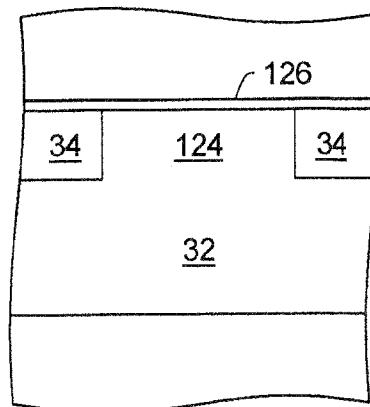


FIG. 3B

14/18

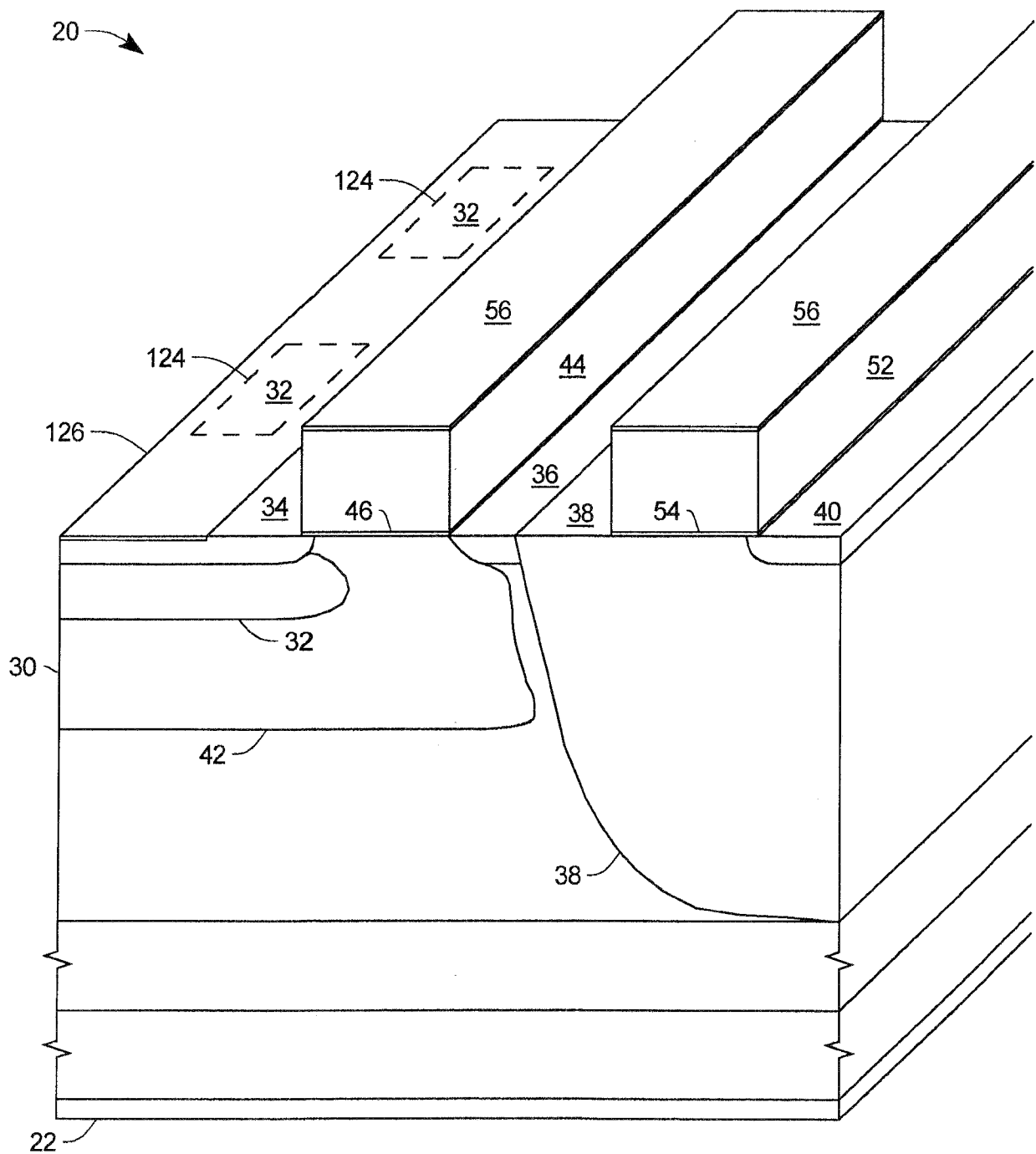


FIG. 3C

15/18

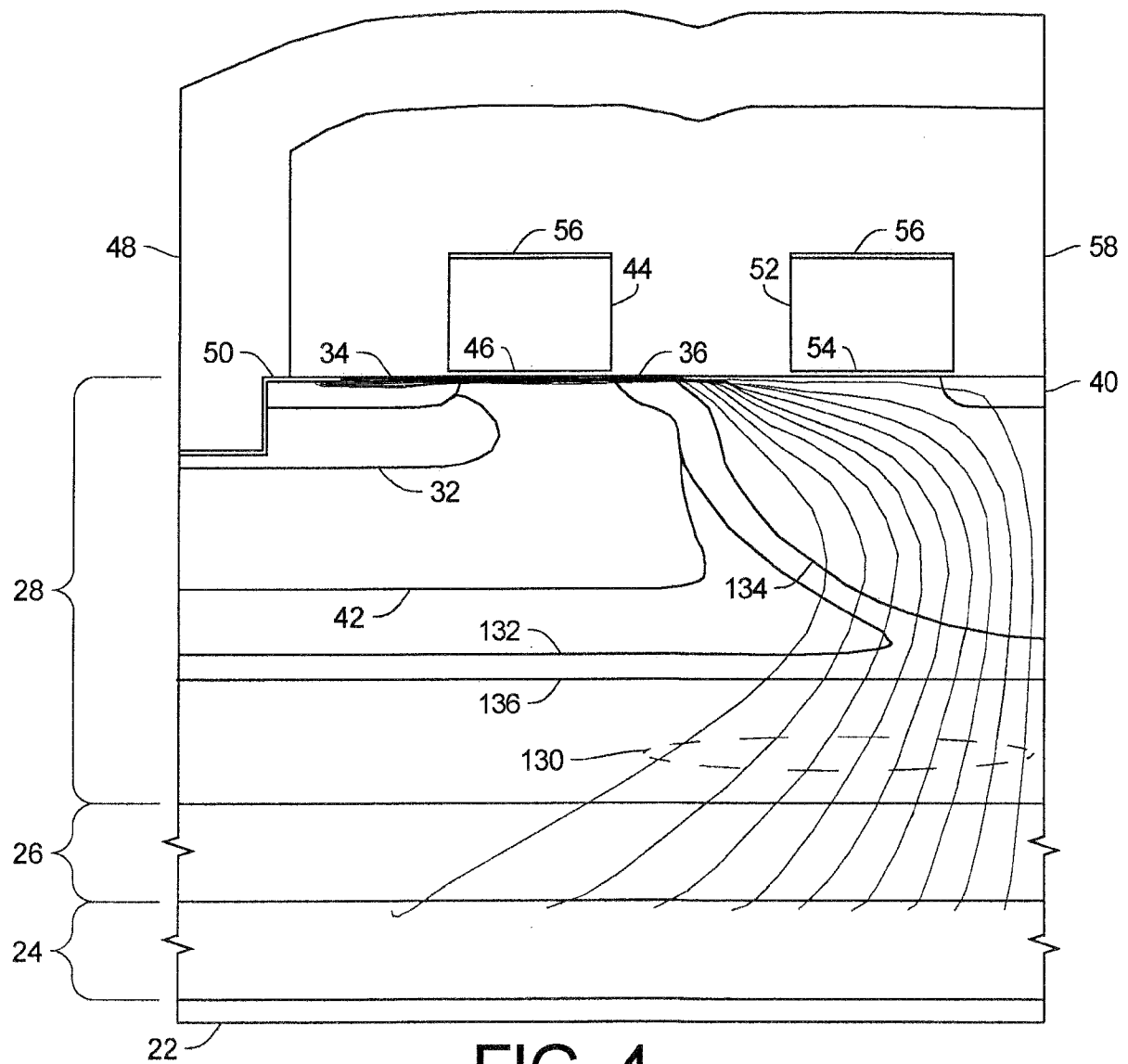


FIG. 4

16/18

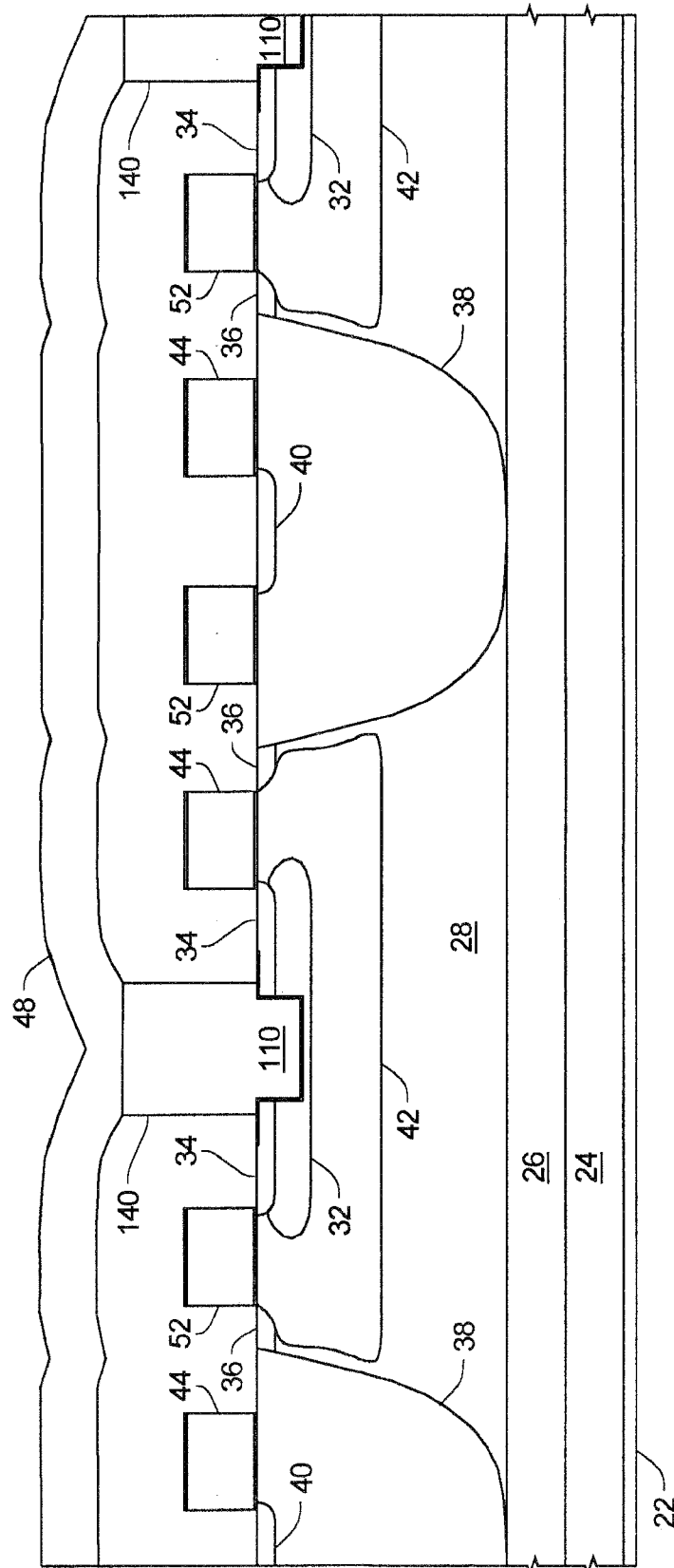


FIG. 5

17/18

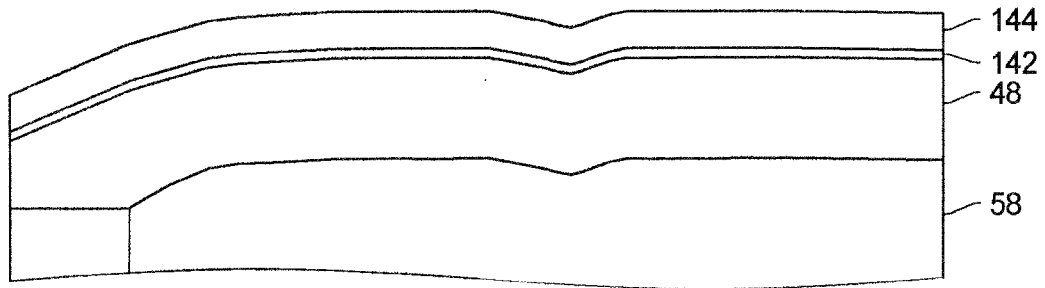


FIG. 6A

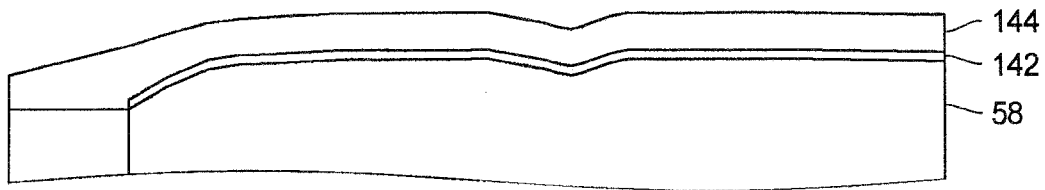


FIG. 6B

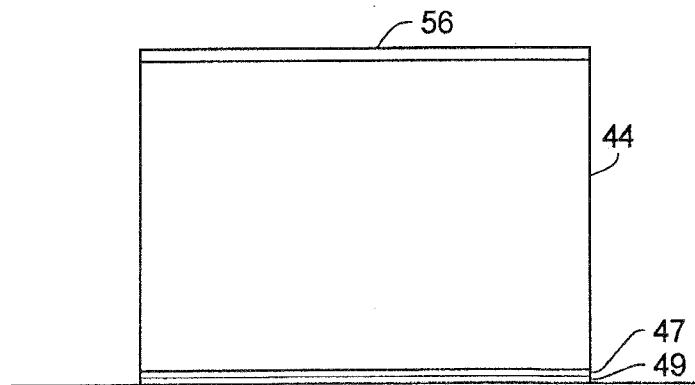


FIG. 7

18/18

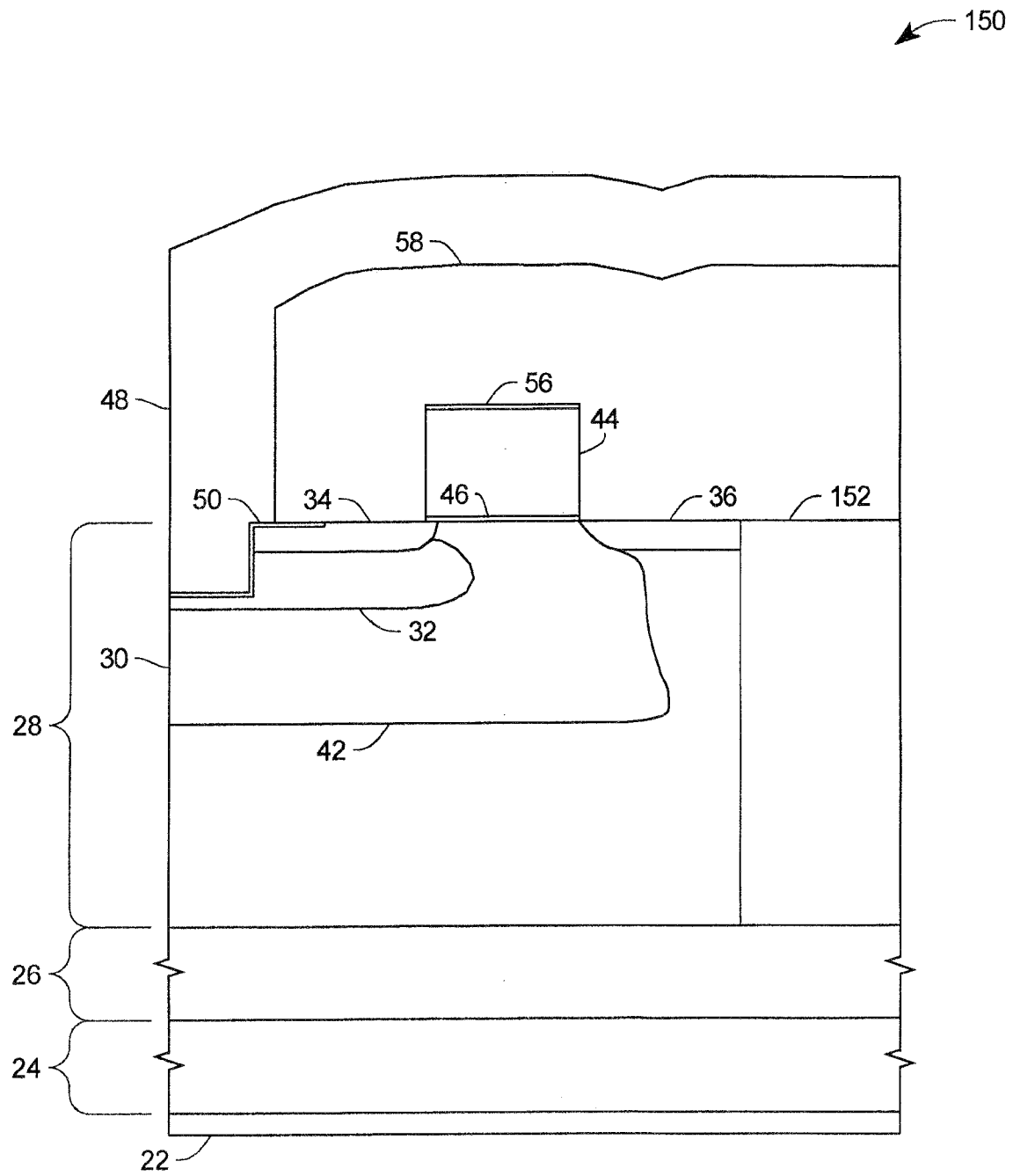


FIG. 8