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[Continued on next page]

(54) Title: INTEGRATED THIN FILM RESISTOR AND MIM CAPACITOR

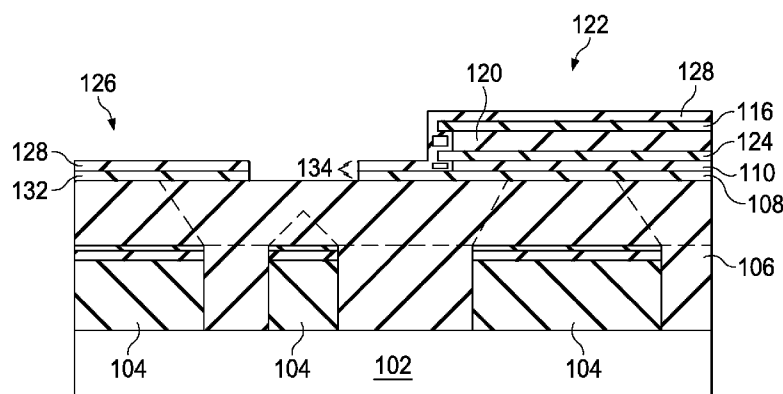


FIG. 7

(57) Abstract: In described examples, an electronic device includes a semiconductor structure (102) having a back end capacitor (122) and a back end thin film resistor (126). The semiconductor structure (102) includes a first dielectric layer (106), a bottom plate (134) of the capacitor (122) and a thin film resistor body (132). The bottom plate (134) and the resistor body (132) are laterally spaced apart portions of the same thin film layer (108). The bottom plate (134) further includes a conductive layer (110) overlying the thin film layer (108). A second dielectric layer (124) is disposed on the conductive layer (110) of the bottom plate (134) of the capacitor (122). A top plate (120) of the capacitor (122) is disposed on the second dielectric layer (124).



— *as to the applicant's entitlement to claim the priority of
the earlier application (Rule 4.17(iii))*

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INTEGRATED THIN FILM RESISTOR AND MIM CAPACITOR

[0001] This relates to an electronic device that includes a semiconductor structure having a back end thin film resistor and a back end capacitor with a low serial resistance, and to a method of manufacturing the electronic device.

BACKGROUND

[0002] Back end thin film capacitor structures according to the prior art “compete” with interconnect metallization routing in the metallization layers of a semiconductor device. Patent Application Publication No. US 2007/0170546 A1 discloses a back end thin film capacitor structure having a thin film capacitor including a top plate, which is located in a metallization layer of a semiconductor device. However, this top plate of the capacitor consumes valuable floor space in the metallization routing layer.

[0003] A conventional thin film capacitor, such as a metal-insulator-metal (MIM) capacitor, consumes area in the interconnect level on which it has been built. For example, an area that is occupied by a top plate or by a bottom plate of a thin film capacitor is not available for regular metallization routing in the metallization layer. Frequently, chip size increases, or a level of interconnects increases, due to the addition of a thin film capacitor in a semiconductor structure.

SUMMARY

[0004] In described examples, an electronic device includes a semiconductor structure having a back end thin film resistor and a back end capacitor with low serial resistance. The capacitor and the resistor are easily integrated in existing semiconductor processes, and chip area of the capacitor and the resistor do not compete with metallization routing in the semiconductor device.

[0005] In at least one described example, an electronic device includes a semiconductor structure having a back end capacitor and a back end thin film resistor. The semiconductor structure includes a first dielectric layer, a bottom plate of the capacitor, and a thin film resistor body. The bottom plate and the resistor body are laterally spaced apart portions of the same layer, which are disposed on the first dielectric layer, and which are composed of a same thin film material. The bottom plate further includes a conductive layer overlying the thin film material. Furthermore, a second dielectric layer is disposed on the conductive layer

of the bottom plate of the capacitor. A top plate of the capacitor is disposed on the second dielectric layer in a region of the second dielectric layer, which is defined by the lateral dimensions of the bottom plate of the capacitor.

[0006] A method of fabricating the electronic device includes sequentially depositing a thin film layer, a first conductive layer, a capacitor dielectric layer, and a second conductive layer. The second conductive layer and capacitor dielectric layer are removed in the resistor area. The first conductive layer is also removed in the resistor area. The thin film layer is etched to laterally separate the resistor body portion of the thin film layer from the capacitor bottom plate portion of the thin film layer. The capacitor bottom plate includes a portion of the thin film layer and the first conductive layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIGS. 1 to 8 schematically illustrate successive process steps involved in manufacturing a thin film back end capacitor and thin film back end resistor in an electronic device, according to example embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0008] Patent No. US 8,803,287 B2 describes related subject matter and is hereby incorporated by reference.

[0009] FIGS. 1 to 6 illustrate an electronic device including a semiconductor structure having a thin film capacitor and thin film resistor at various stages of fabrication. The back end thin film capacitor and the back end thin film resistor can be interconnected by a single level of interconnect metallization. Thin film layer thicknesses typically range between ~ 30 to ~ 3000 Å, depending on layer purpose and application. Thin film resistor layers vary typically between 30Å (e.g., 1000 ohm/sq SiCr) and 500Å (e.g., 50 ohm/sq NiCr), depending on desired sheet resistance. Capacitor dielectric thin films typically are thinner than 500Å , depending on material and desired specific capacitance. Top and bottom plate metal electrode thicknesses can vary between several hundreds and a few thousand Å, depending on specific resistance of the material, the desired serial resistance and/or process limitations.

[0010] Herein, the term “back end” describes the integration of components, including the integration of thin film capacitors and thin film resistors on a partially fabricated integrated circuit structure. Previously, transistors and polycrystalline silicon structures have been formed in the integrated circuit. While a so-called “front end” process typically includes process steps that are performed at process temperatures in a range of 600°C to 700°C , a “back end” process typically includes process steps that are performed at lower temperatures, which are roughly about 450°C .

[0011] A deposition in a region of another structure (in this case in the region defined by the lateral dimensions of the bottom plate of the capacitor) means that the lateral dimensions of the deposited structure are equal to or smaller than the lateral dimensions of the structure that is underneath. Accordingly, in a top view, an area of the top plate of the capacitor is equal to or smaller than the area of the bottom plate of the capacitor. Furthermore, a deposition of a first layer on top of a second layer may be read as a deposition directly on top of the respective layer.

[0012] Referring to FIG. 1, a starting semiconductor substrate 102 (e.g., a silicon substrate) may include various active and passive devices (not shown), such as bipolar transistor and / or MOS transistors that have been formed already in various areas of the semiconductor substrate 102. A standard metallization and routing level 104 is provided on the semiconductor substrate 102. The routing traces are covered by a first intermetal dielectric layer 106. After deposition, this first intermetal dielectric layer 106 may be planarized according to conventional process steps in semiconductor fabrication.

[0013] Still referring to FIG. 1, a thin film layer 108 (such as sicrome (SiCr), SiCr:C, NiCr, or NiCrAl), a first conductive layer 110, and a second dielectric layer 112 (such as a silicon nitride layer (Si_3N_4) or silicon dioxide layer (SiO_2)) are deposited sequentially on top of the first intermetal dielectric layer 106. For example, these layers may be directly adjacent to each other. When sicrome is used for thin film layer 108, it may have a typical sheet resistance ranging from 30 Ω/square to 2000 Ω/square . The thin film layer 108 is deposited on the upper surface of the first intermetal dielectric layer 106. The first conductive layer 110 is deposited on the thin film layer 108. First conductive layer 110 has a lower sheet resistance than the thin film layer 108 and functions to reduce the serial resistance of the subsequently formed capacitor bottom plate. For example, first conductive layer 110 may include TiN at 10-20 ohms/sq. Other conductive materials, such as aluminum, may alternatively be used. The second dielectric layer 112 (Si_3N_4) is deposited on top of the first conductive layer 110. In one example: (a) the thin film layer 108 may have a thickness in the range of 400Å and is formed directly on the first dielectric layer 106; (b) the first conductive layer 106 may have a thickness in the range of 500Å and is formed directly on the thin film layer 108; and (c) the second dielectric layer 110 may have a thickness in the range of 250Å and is formed directly on the first conductive layer 108.

[0014] Referring to FIG. 2, a second conductive layer 114 for forming the top plate of the capacitor is deposited over the second dielectric layer 112, and a hard-mask layer 116 is deposited over the second conductive layer 114. Second conductive material 114 includes a

conductive material, such as TiN or TiW. Hard-mask layer 116 may include an oxide, nitride or oxynitride. A mask pattern 118 is deposited over second conductive material 114. Mask pattern 118 covers an area designated for the back end capacitor and exposes an area for the back end thin film resistor. Although the first and second conductive layers 114 may include metal, neither are part of a conventional metallization level. Rather, they are formed between metallization levels.

[0015] In FIG. 3, first patterning and etch back steps have been performed to provide: (a) a top plate 120 of the thin film capacitor 122 in the second conductive layer 114; and (b) a capacitor dielectric 124 in the second dielectric layer 112. The first patterning and etching includes a hard-mask etch (e.g., dry etch using an etch chemistry, such as C_xF_y/O_2), a top plate etch (e.g., dry etch of TiN 114 stopping in the second dielectric layer 112 using an etch chemistry, such as $BCl_3/Cl_2/N_2$) and a second dielectric layer 112 etch (e.g., a dry etch stopping in the TiN layer 110 using an etch chemistry, such as C_xF_y/O_2). Accordingly, the hard-mask layer 116, second conductive layer 114, and second dielectric layer 112 are removed from the area designated for the thin film resistor. Advantageously, the second dielectric layer 112 provides an etch stop during the standard patterning and etch back steps, which may be performed using conventional photoresist deposition, etching and cleaning steps, etc., according to conventional semiconductor technology.

[0016] Referring to FIG. 4, the mask pattern 118 is removed, such as by an ashing process. Then, using the remaining portion of hard mask layer 116 to protect the capacitor 122, a wet etch is performed to remove first conductive layer 110 from an area designated for the thin film resistor 126, leaving only the thin film layer 108 in the thin film resistor area. This wet etch may result in some undercutting of the top plate 120 and first conductive layer 110 in capacitor 122.

[0017] Referring to FIG. 5, a hard-mask layer 128 is deposited. Hard-mask 128 may also include an oxide, nitride or oxynitride.

[0018] Referring to FIG. 6, a mask pattern 130 is formed. Mask pattern 130 covers capacitor 122 and thin film resistor 126 and exposes an area between capacitor 122 and thin film resistor 126. The exposed portion of hard-mask 128 is removed by etching, where the etch stops in the thin film layer 108. Mask pattern 130 is then removed (e.g., ashing). Standard post ash clean-up processes may also be performed.

[0019] The thin film layer 108 and conductive layer 110 are applied for manufacturing a bottom plate of a thin film capacitor. The thin film layer 108 alone is used in forming a body of a thin film resistor. To provide a bottom plate of the thin film capacitor that is separate or

laterally spaced apart from the body of the thin film resistor, the thin film layer 108 is etched using hard-mask 128 as a pattern, as shown in FIG. 7.

[0020] In FIG. 7, etching of the thin film layer 108 has been performed to provide a laterally separate thin film resistor body 132 of resistor 126 (a first portion of the thin film layer 108) and bottom plate 134 of the thin film back end capacitor 122 (a second portion of the same thin film layer 108). Bottom plate 134 includes the thin film layer 108 and first conductive layer 110. Including first conductive layer 110 in bottom plate 134 provides an advantage of lower serial resistance.

[0021] In FIG. 8, a second intermetal dielectric layer 140, which is the third dielectric layer, is deposited on top of the structure of FIG. 7. This second intermetal dielectric layer 140 may undergo further process steps, such as planarization. The second intermetal dielectric layer 140 provides a basis for further metallization levels, which may be used for routing of traces in a semiconductor structure.

[0022] In FIG. 8, a further metallization level 142 is deposited on top of the second intermetal dielectric layer 140. Also, vertical conductive vias 144-150 are formed for electrically coupling the thin film resistor body 132 (via 144), the metallization level 104 (via 146), the bottom plate 134 (via 148) and the top plate 120 (via 150) of the capacitor 122 to this second metallization level 142. Although thin film resistor 126 and capacitor 122 may include metal layers, they are not part of conventional metallization levels. Rather, as shown in FIG. 8, they are formed between metallization levels 104 and 142. Metallization level 104 is level M_N (e.g., M_2), and metallization level 142 is level M_{N+1} (e.g., M_3).

[0023] The electronic device 160 of FIG. 8 may include further active and passive components, which (for simplification of the drawings) are not shown.

[0024] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An electronic device comprising:
a semiconductor structure having: a first dielectric layer; a resistor body of a resistor including a first portion of a thin film layer on the first dielectric layer; a bottom plate of a capacitor including a second portion of the thin film layer and a conductive layer overlying the second portion of the thin film layer; a second dielectric layer disposed on the bottom plate of the capacitor; and a top plate of the capacitor disposed on the second dielectric layer over the bottom plate;
wherein the bottom plate and the resistor body are laterally spaced apart layers, which are disposed on the first dielectric layer, and which are composed of a same thin film material.
2. The electronic device of claim 1, wherein the thin film material of the bottom plate and the resistor body is metallic material, and the material of the top plate of the capacitor is metallic material.
3. The electronic device of claim 1, wherein the first dielectric layer is deposited on a first metallization level of the semiconductor structure.
4. The electronic device of claim 1, further comprising:
a third dielectric layer disposed over the top plate of the capacitor and over the resistor body; and
a second metallization level of the semiconductor structure disposed on the third dielectric layer.
5. The electronic device of claim 4, further comprising a first conductive via that extends through the third dielectric layer to the top plate of the capacitor.
6. The electronic device of claim 5, further comprising a second conductive via that extends through the third dielectric layer to the bottom plate of the capacitor.
7. The electronic device of claim 6, further comprising a third conductive via that extends through the third dielectric layer to the thin film resistor body.
8. The electronic device of claim 7, wherein the first conductive via, the second conductive via, and the third conductive via are all connected to the second metallization level.
9. The electronic device of claim 8, further comprising a hard-mask layer on the top plate of the capacitor and on the resistor body.
10. The electronic device of claim 1, wherein the thin film layer for the bottom plate of

the capacitor and for the thin film resistor body is composed of SiCr, the conductive layer is TiN, the second dielectric layer is composed of silicon nitride, and the top plate of the capacitor is composed of TiN.

11. A method of manufacturing an electronic device, the method comprising:
 - depositing a first dielectric layer over a semiconductor substrate;
 - depositing a thin film layer for a bottom plate of a capacitor and a resistor body;
 - depositing a first conductive layer over the thin film layer;
 - depositing a second dielectric layer on the first conductive layer;
 - depositing a second conductive layer on the second dielectric layer;
 - patterning and etching to remove the second conductive layer and the second dielectric layer in a resistor area and form a top plate of the capacitor and a capacitor dielectric;
 - removing the first conductive layer in the resistor area, leaving a portion of the first conductive layer in the capacitor;
 - etching a portion of the thin film layer to form the resistor body and the bottom plate of the capacitor, wherein the bottom plate further includes the portion of the first conductive layer;
 - wherein the bottom plate and the resistor body layer are deposited on the first dielectric layer in a common process step, and wherein the bottom plate and the resistor body are laterally spaced apart portions of the same thin film layer.
12. The method of claim 12, further comprising:
 - forming a first metallization level over the semiconductor substrate before depositing the first dielectric layer;
 - depositing a third dielectric layer on the top plate of the capacitor; and
 - forming a second metallization level over the third dielectric layer.
13. The method of claim 11, wherein patterning and etching to remove the second conductive layer and the second dielectric layer includes:
 - forming a first hard mask layer over the second conductive layer;
 - forming a first mask pattern over the first hard mask layer; and
 - etching the second conductive layer and the second dielectric layer using the first mask pattern.
14. The method of claim 13, wherein removing the first conductive layer in the resistor area includes wet etching the first conductive layer using the first hard mask layer to protect the capacitor.

15. The method of claim 13, wherein etching the second conductive layer and the second dielectric layer includes:

dry etching the first hard mask layer;

dry etching the second conductive layer stopping on the second dielectric layer; and

dry etching the second conductive layer stopping on the first conductive layer.

16. The method of claim 15, wherein etching the portion of the thin film layer to form the resistor body and the bottom plate of the capacitor includes:

depositing a second hard mask layer over the thin film layer and top plate of the capacitor;

forming a second mask pattern over the second hard mask layer;

etching the second hard mask layer stopping on the thin film layer using the second mask pattern;

removing the second mask pattern; and

etching the thin film layer using the etched second hard mask layer as a mask.

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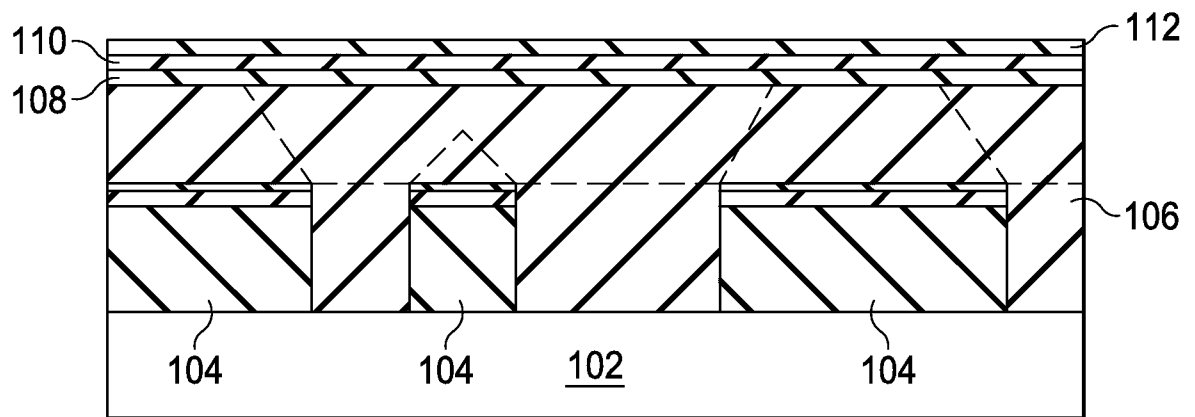


FIG. 1

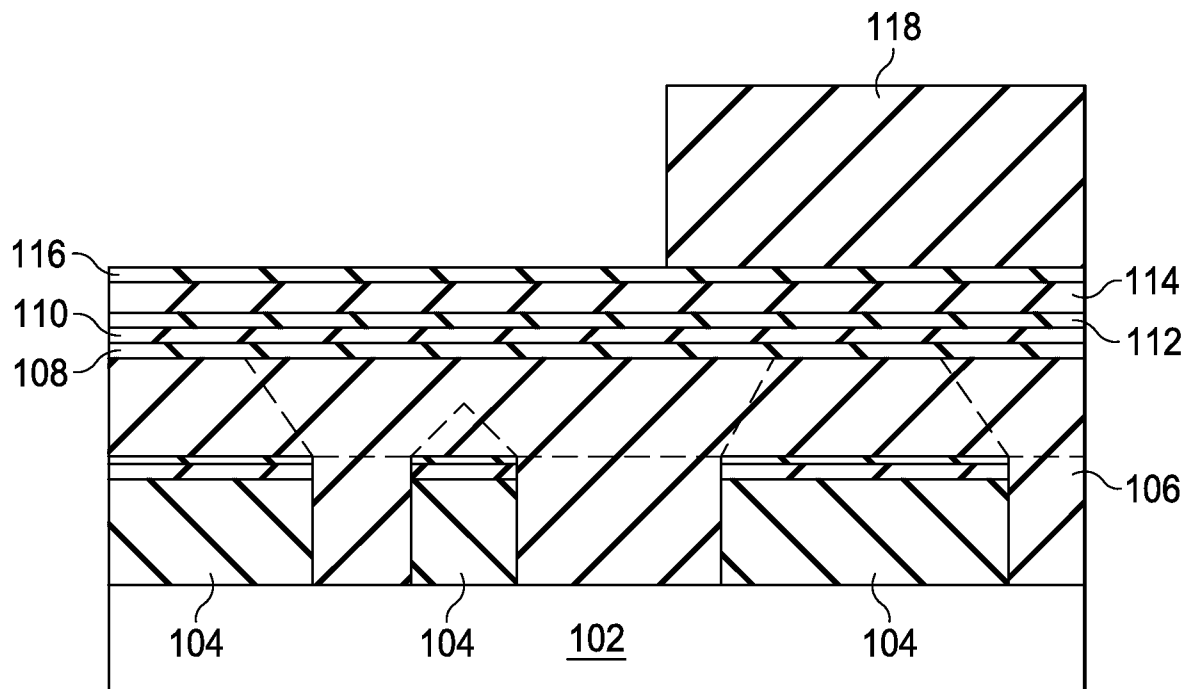


FIG. 2

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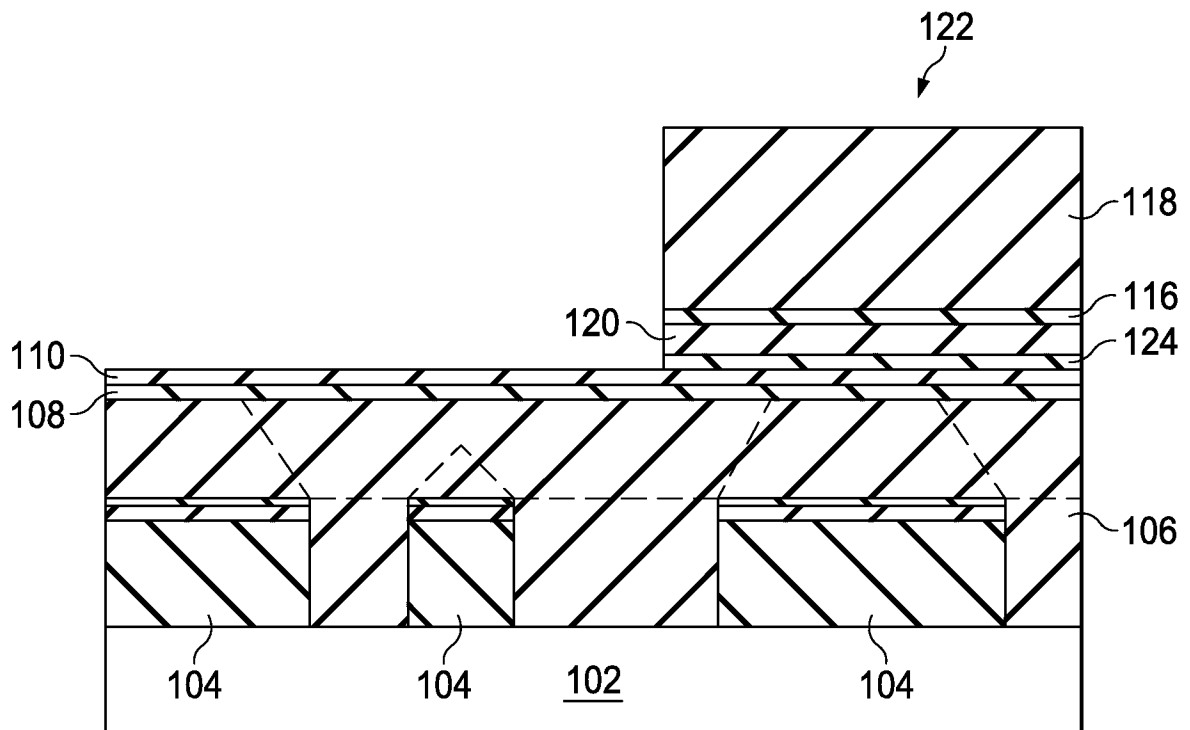


FIG. 3

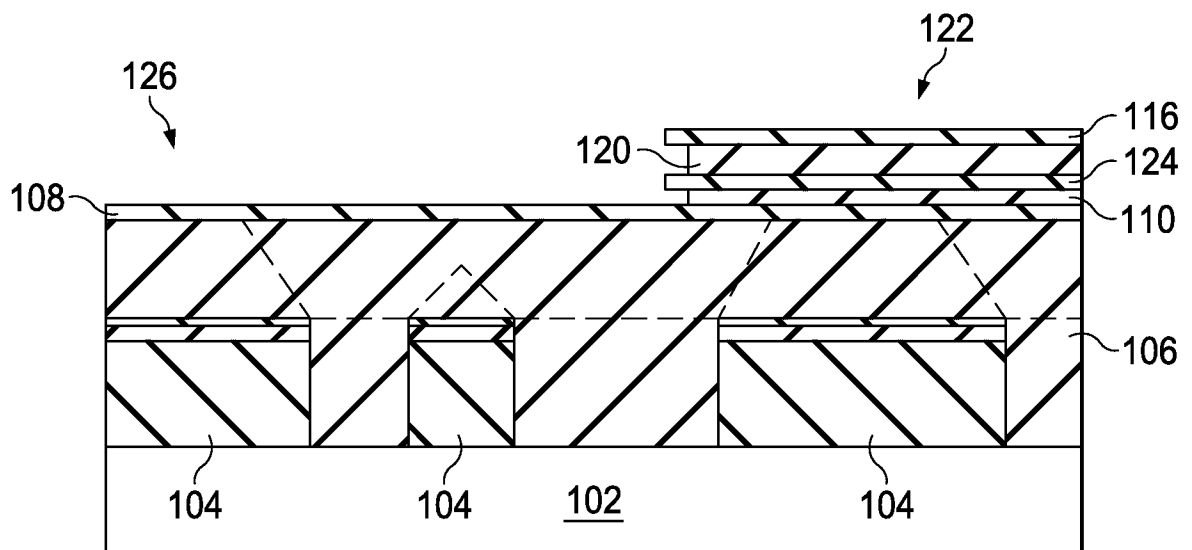


FIG. 4

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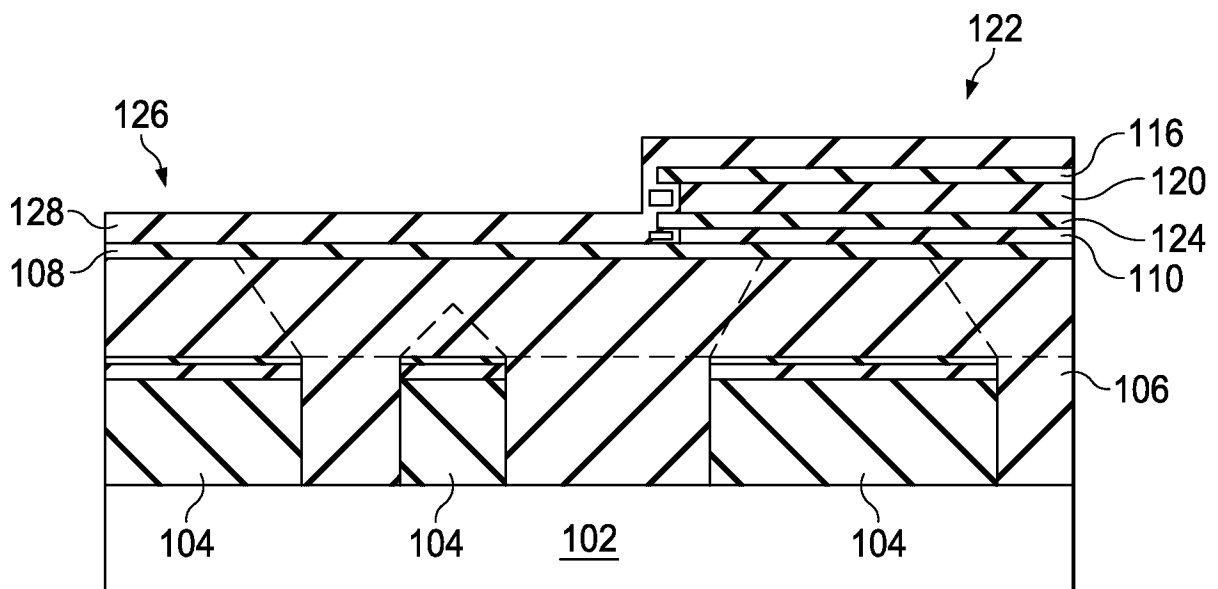


FIG. 5

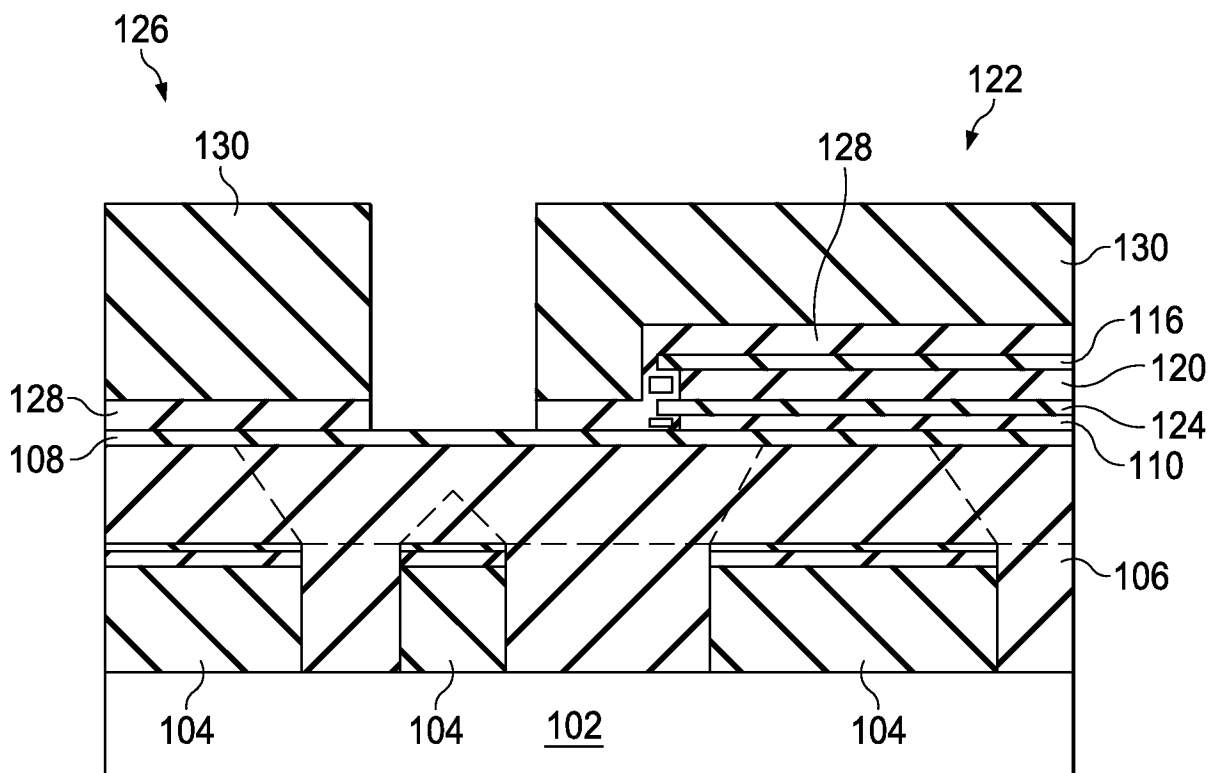


FIG. 6

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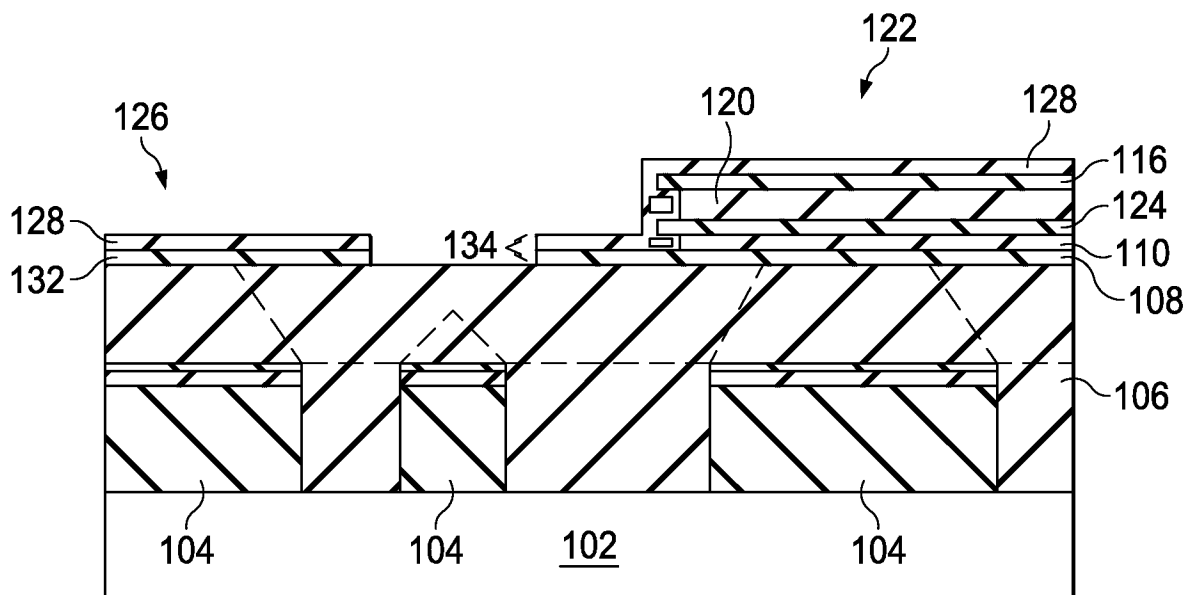


FIG. 7

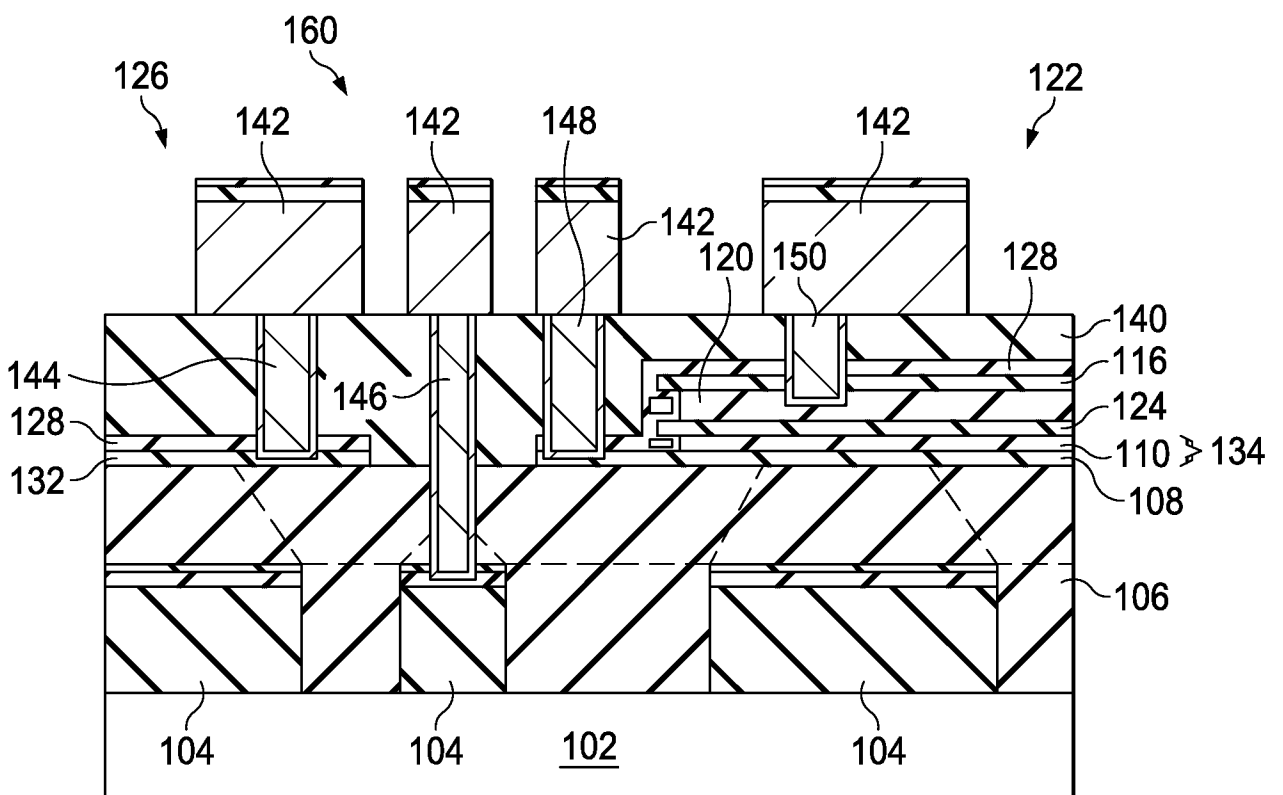


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2015/029317

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/102 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/00-27/07, 21/82-21/8249

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014/0103489 A1 (TEXAS INSTRUMENTS DEUTSCHLAND GMBH) 17.04.2014	1-16
A	US 2007/0170546 A1 (TEXAS INSTRUMENTS INCORPORATED) 26.07.2007	1-16
A	US 2013/0341759 A1 (TEXAS INSTRUMENTS INCORPORATED) 26.12.2013	1-16
A	US 2004/0130434 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 08.07.2004	1-16
A	US 6365480 B1 (ANALOG DEVICES, INC.) 02.04.2002	1-16



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

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