

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
12 November 2009 (12.11.2009)

(10) International Publication Number
WO 2009/137286 A1

(51) International Patent Classification:

H01L 25/065 (2006.01) H01L 23/373 (2006.01)
H01L 23/367 (2006.01)

(21) International Application Number:

PCT/US2009/041780

(22) International Filing Date:

27 April 2009 (27.04.2009)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

12/115,076 5 May 2008 (05.05.2008) US

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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ,

CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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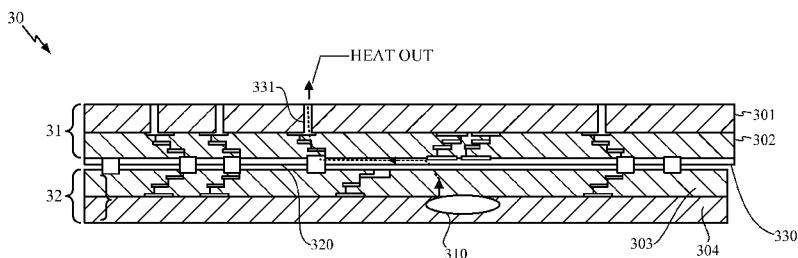
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(54) Title: 3-D INTEGRATED CIRCUIT LATERAL HEAT DISSIPATION

FIG. 3



(57) Abstract: By filling an air gap between tiers (31,32) of a stacked IC device with a thermally conductive material (320) heat generated at one or more locations within one of the tiers can be laterally displaced. The lateral displacement of the heat can be along the full length of the tier and the thermal material can be electrically insulating. Through silicon-vias (331) can be constructed at certain locations to assist in heat dissipation away from thermally troubled locations (310).

3-D INTEGRATED CIRCUIT LATERAL HEAT DISSIPATION

FIELD OF DISCLOSURE

[0001] This disclosure relates to integrated circuits (ICs), and more specifically to multi-tiered (3-D) ICs, and even more specifically to systems and methods for enhancing heat dissipation in 3-D ICs.

BACKGROUND

[0002] In IC technology there is a need to stack the chips (dies) together to form multi-tiered or three-dimensional (3-D) IC devices. One result of such 3-D IC stacking is a decrease of signal propagation time during signal processing, due to the reduced distance signals must travel when they remain within a single package.

[0003] One method for tier bonding is to bring two (or more) dies together and then encapsulate the dies into a single structure. Electrical conductors and/or contacts on the surface of the respective dies serve to carry electrical signals between components on the different dies.

[0004] One problem when dies are positioned in close proximity to each other is that thermal density increases. Moreover, because of the reduced size of stacked ICs, (substrate thickness going from 700-100 microns to below 20 microns), the lateral thermal conductivity is reduced. Thus, hot spots could exist with little ability to move the heat away from the heat source.

[0005] One method for increasing lateral thermal conductivity is to increase the substrate thickness of at least one of the tiers. Another method is to increase the metal layers in the chip to be able to dissipate heat. This, in turn, negatively impacts the desired aspect ratio of the package, as well as degrades the signal transmission speeds.

[0006] An additional problem exists when more than one tier is bonded. In such situations, the stacked IC device contains multiple layers of oxide between tiers. Oxide, being a poor thermal conductor, adds to the heat dissipation problem.

[0007] There are several approaches that could be taken to help with the thermal conductivity issues. One such approach could use through-silicon-vias (TSVs) to move the heat from an inner portion to a surface layer, and then remove the heat using traditional methods, such as a high thermal conductivity material positioned on a surface of the IC package. A problem with such a solution is that a circuit layout may

prevent positioning a TSV at the necessary location because of devices constructed in the various tiers in proximity to the hot spot generating the heat.

[0008] Another method is to circulate cooling material through the stacked IC device to cool the various hot spots. This is costly to manufacture because the moving liquid requires a pumping mechanism and tight tolerances for liquid channels. Also, it may not be possible to channel the cooling material to the necessary location. The channeling problem could be overcome, to some extent, by forcing cooling liquid through the substrate itself, but this method is not without a further set of problems and costs.

SUMMARY OF THE DISCLOSURE

[0009] Embodiments of the invention fill an air gap between stacked dies with a thermally conductive material, which allows heat generated at one or more locations within each die to be laterally displaced. The lateral displacement of the heat can be along the full length of the die or along a portion of the length. In one embodiment, the thermal material is electrically insulating. In one embodiment, TSVs, perhaps using carbon nanotubes can be constructed at certain locations to assist in heat dissipation away from thermally troubled locations.

[0010] In one embodiment, a multi-tiered semi-conductor has a thermally conductive material disposed between first and second tiers wherein the material has a higher thermal conductivity than the thermal conductivity of said first and second tiers.

[0011] In another embodiment, a method of manufacturing a tiered semi-conductor is disclosed in which a thermally conductive material is applied to at least one mating surface of a first die and the mating surface of that die is brought into mated contact with a mating surface of a second die.

[0012] In still another embodiment, a method for heat dissipation in a stacked IC device is disclosed which allows heat from a thermally troubled area of one layer of a multi-tiered IC device to flow to an inter-layer between adjacent tiers of the device, such that lateral heat flow is facilitated in the inter-layer area to at least one heat dissipation location in thermal communication with the inter-layer area. In one embodiment, the heat dissipation area is a via constructed through at least one layer of a tier of the device. In another embodiment, the heat dissipation area is a gap between adjacent dies in a same tier.

[0013] The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description that follows may be better understood. Additional features and advantages will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiments disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims. The novel features which are believed to be characteristic of the invention, both as to its organization and method of operation, together with further objects and advantages will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] For a more complete understanding of the present disclosure, reference is now made to the following descriptions taken in conjunction with the accompanying drawings.

[0015] FIGURE 1 is a cross sectional side view illustrating one aspect of thermal trouble conditions that could exist with 3-D integrated circuits.

[0016] FIGURE 2 is a cross sectional side view illustrating one exemplary solution to the heat removal problem.

[0017] FIGURE 3 is a cross sectional side view showing one embodiment of the concepts of the disclosure.

[0018] FIGURE 4 shows one embodiment of method for constructing stacked IC device in accordance with the teaching of the disclosure.

DESCRIPTION OF THE EMBODIMENTS OF THE INVENTION

[0019] FIGURE 1 illustrates one aspect of thermal trouble conditions that could exist with 3-D integrated circuits. As shown in FIGURE 1, a die 11 is stacked with a die 12. The active layer of die 11 is a layer 102 and the active layer of

die 12 is a layer 103. This is an exemplary arrangement as the active layers of the dies could be in any orientation, up or down.

[0020] Vias 105 run through the substrate layer 101 of the die 11. Vias could be constructed in the layers 102, 103 and/or 104 as desired. Electrical paths 107 and 108 form an interconnect between the dies. Seal 109 acts to prevent non-desired contaminants from entering the area 120 between the respective dies 11, 12..

[0021] Element 108 is normally on the scale of 30 microns or less and normally forms a copper or a tin copper metal to metal bond. Area 120 is usually an air gap. The gap 120 can be in the range of less than 10 micron.

[0022] A hot spot 110 is on the die 12 and the challenge is to move heat from this relatively small area 110 to an external portion of the die stack. Note that elements 111 are directly above the hot spot 110 and would be affected by heat from the hot spot 110 moving upward through the layers 103, 102, 101.

[0023] FIGURE 2 illustrates one discussed solution to the heat removal problem. In this solution, a TSV array 200 having individual TSVs 201, 202, and 203 is positioned to provide thermal conductivity for heat from the hot spot 110. The heat passes through the layer 103, which is the active area of bottom die 12. The heat then passes through the active layer 102 of the die 11 and is then pulled out to the exterior via the TSV array 200. The vias 201, 202, 203 may be copper or tungsten lined to increase thermal conductivity, but any thermally conductive material would work. In one embodiment, carbon nanotubes (CNTs) can be used to fill the vias 201, 202, 203. In another embodiment, CNTs partially fill the vias 201, 202, 203 and metal fills the remainder of the vias 201, 202, 203. An advantage of the CNTs is improved electrical and thermal conductivity, as well as improved current density.

[0024] FIGURE 3 shows one embodiment 30 in which the concepts of the disclosure are utilized. Thermally conductive material 320 is positioned within a gap between the dies 31 and 32. In another embodiment, the thermally conductive material 320 is between metal layers (not shown) of one of the active layers 302, 303 of the tiers 31, 32. The thermally conductive material 320 ideally would have thermal conductivity greater than 10 W/m/K so as to facilitate lateral heat transfer. The material 320 is thermally conductive, and in one embodiment electrically insulating so that it does not short circuit the electrical connections that connect the dies 31, 32, which would interfere with the operation of elements contained in the dies 31, 32. The

material 320 can be positioned by a variety of methods, for example, spun on or deposited by chemical vapor deposition (CVD), and/ or physical vapor deposition (PVD). The material 320 may be a diamond matrix or a diamond film pattern.

[0025] Although only shown on one layer 302 of one of the dies 31, the material 320 can be positioned on a surface of each of the two mating layers 302, 303, so that the material 320 on each layer 302, 303 actually touches each other when the dies 31, 32 are stacked. Alternatively, the material 320 may be placed only on one of the mating layers 302, 303.

[0026] In operation, heat from hot spot 310 passes upward through the layer 303 of the die 32 and into the material 320. The heat then travels laterally along the material 320 either to an edge of the device, such as over hanging edge 330 or more typically, the heat will pass up through one or more heat dissipating vias, such as through the via 331 constructed in the layer 301 of the die 31. Because of the lateral movement of the heat, there is a better uniformity of the temperature across the device 30. This benefit allows heat to spread relatively quickly across the whole device 30, thereby causing the device 30 to evenly heat up. The removal of heat from a larger area, such as the entire device 30 or the package of the device is easier to accomplish than removing heat from a small, internal area.

[0027] Note that the heat dissipating via 331 can pass up through die 31, or down through die 32 (or both). One advantage of the thermally conductive material 320 is that the heat dissipating via 331 can be laterally offset from the thermally troubled area 310 thereby freeing areas directly above the troubled area to be used for circuitry or other elements constructed in the various layers 301, 302, 303. Also note that the heat need not flow directly upward through the layers 301, 302, 303 but rather the via 331 could, for example, be angled and/or curved. Another advantage of the lateral heat dissipation is that fewer TSVs are needed.

[0028] For multi-tiered devices having more than two tiers, multiple inter-layer heat dissipating material structures can be used. Thus, the heat can move laterally from the heat source a first distance within a first inter-layer area and then pass up one tier with the assistance of a via and then again move laterally (in any direction) in a second inter-layer area, provided thermally conductive material is positioned in both first and second inter-layer areas.

[0029] One system for allowing even greater heat removal from the material 320 is to make one of the layers, such as the dies 31 circumferentially larger than the other die 32 thereby creating a surface area, such as surface area 330 on an overhanging lip on the larger of the dies. Note that this same technique would work for several tiers which, if desired, could be staggered as to diameter. The composition of the material 320 need not be the same across the entire surface and the differences in the material 320 could be used to assist in heat conductivity away from the hot spot(s) 310.

[0030] In one embodiment, a bottom die is larger than a top die. Thus, a gap would exist between two top dies (of a single tier) that rest on the bottom die. According to the present disclosure, gap fill material can be provided within this gap between the top dies. The gap fill material can be thermally conductive and can be any material with good thermal conductivity, such as a diamond film. In one embodiment, the thermally conductive gap fill material is thermally coupled to the material 320 to help transfer heat out of the stacked IC device.

[0031] FIGURE 4 shows one embodiment 40 of a method for constructing stacked IC devices in accordance with the teachings of the disclosure. Process 401 determines if a die has been selected for constructing a stacked IC device. If not, then process 402 controls a wait time. After a die has been selected, process 403 determines if a thermally conductive material should be added to at least one lateral surface of the die. The thermally conductive material can be deposited under control of process 404 by any one of the methods discussed above, such as CVD or PVD processing, or the material can be spun on, or applied as a film.

[0032] Processes 405 and 406 wait for a next die to be selected for mating with the previously selected die. Process 407 and 408 add thermally conductive material to this next die, if appropriate, and process 409 then bonds the dies together. Process 410 determines if more dies are to be added. When all the dies have been selected and coated with thermally conductive material (if appropriate), process 411 completes the IC package which is then available for testing and/or usage.

[0033] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, although the material 320 has been described as being non-electrically conductive, it is possible to make the

material electrically conductive. In this embodiment, the electrically conductive material should be patternable, i.e., capable of being patterned, such that it can be separated from some vias to prevent electrical connections while still thermally dissipating heat.

[0034] The scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein, may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS

What is claimed is:

1. A multi-tiered semi-conductor comprising:

first and second tiers having elements constructed therein; and

a first thermally conductive material disposed between said first and second tiers wherein the first material has a higher thermal conductivity than a thermal conductivity of said first and second tiers.

2. The semi-conductor of claim 1 wherein said thermal conductivity of the first material is at least 10 W/m/K.

3. The semi-conductor of claim 2 wherein the first thermal conductive material is electrically insulating.

4. The semi-conductor of claim 1 wherein said first thermal conductive material is a patterned film.

5. The semi-conductor of claim 1 further comprising:

a second thermally conductive material disposed at an end of at least one tier, said second thermally conductive material being thermally coupled to said first thermally conductive material disposed between said tiers.

6. The semi-conductor of claim 1 wherein said thermally conductive material is selected from the list of: diamond matrix; and diamond film pattern.

7. The semi-conductor of claim 1 further comprising at least one thermally conductive via positioned through at least a portion of a layer of one tier at a location laterally displaced from a thermally troubled area within said semi-conductor.

8. The semi-conductor of claim 7 in which the via is filed at least partially with carbon nanotubes.

9. A method of manufacturing a tiered semi-conductor, said method comprising:

selecting a first die;
applying a thermally conductive material to at least one mating surface of said die; and
bringing said mating surface of said first die having said thermally conductive material applied thereto into mated contact with a mating surface of a second die.

10. The method of claim 9 wherein said applying material comprises:
mating a patterned film onto said die.
11. The method of claim 10 wherein said patterned film contains diamonds.
12. The method of claim 11 further comprising:
repeating said selecting, applying and bringing for an additional die.
13. A method for heat dissipation in a stacked IC device, said method comprising:
allowing heat from a thermally troubled area of one tier of a multi-tiered IC device to flow to an inter-layer area between adjacent tiers of said device; and
facilitating heat flow laterally in said inter-layer area to at least one heat dissipation location in thermal communication with said inter-layer area.
14. The method of claim 13 wherein said heat dissipation location is a via constructed through a portion of at least one tier of said device.
15. The method of claim 13 wherein said heat dissipation area is an overhang of one tier.
16. The method of claim 13 wherein said heat dissipation area is thermally conductive material in a gap between adjacent dies in a same tier of said device, the thermally conductive material in the gap dissipating heat towards a first surface of the device.

17. The method of claim 16 wherein said thermally conductive material is electrically insulating.

18. The method of claim 13 wherein said positioning comprises:

depositing thermally conductive material on a surface of a tier by at least one of the following: CVD, PVD, spin on, screen on.

19. The method of claim 18 wherein said thermally conductive material is a patterned film.

20. The method of claim 17 wherein said thermally conductive material comprises diamonds.

21. A multi-tiered semi-conductor comprising:

first and second tiers having elements constructed therein; and

a thermally conductive material disposed between metal layers within said first and second tiers wherein the thermally conductive material has a higher thermal conductivity than a thermal conductivity of said first and second tiers.

22. The semi-conductor of claim 21 wherein said thermally conductive material comprises diamonds.

(PRIOR ART)

FIG. 1

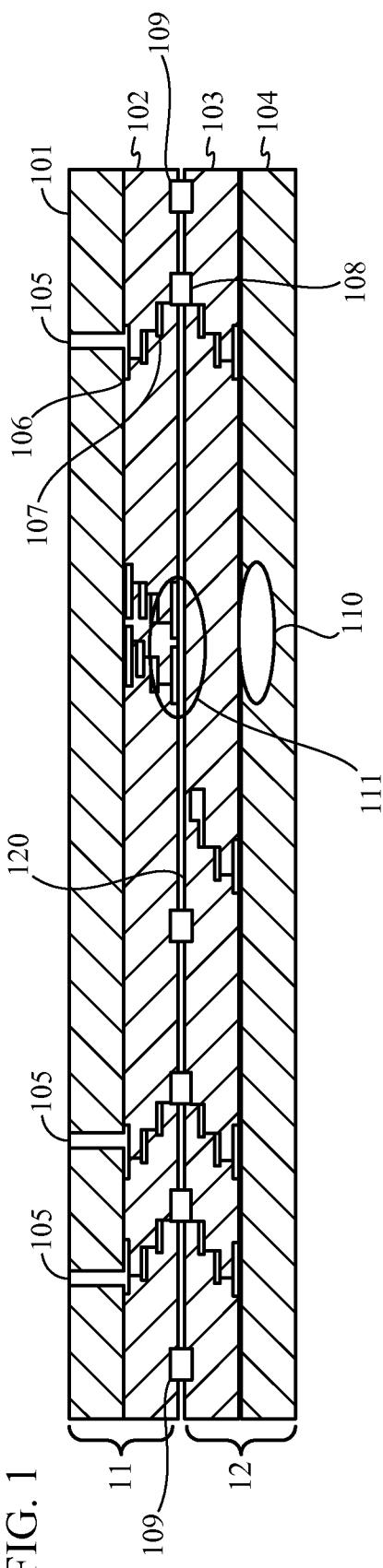
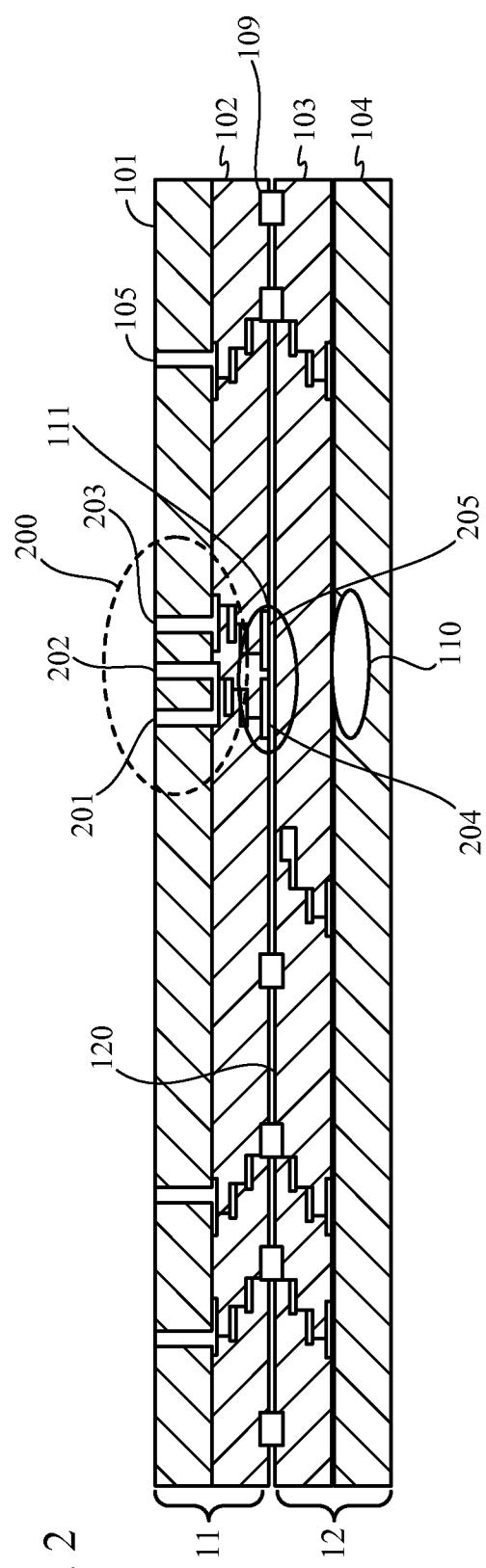
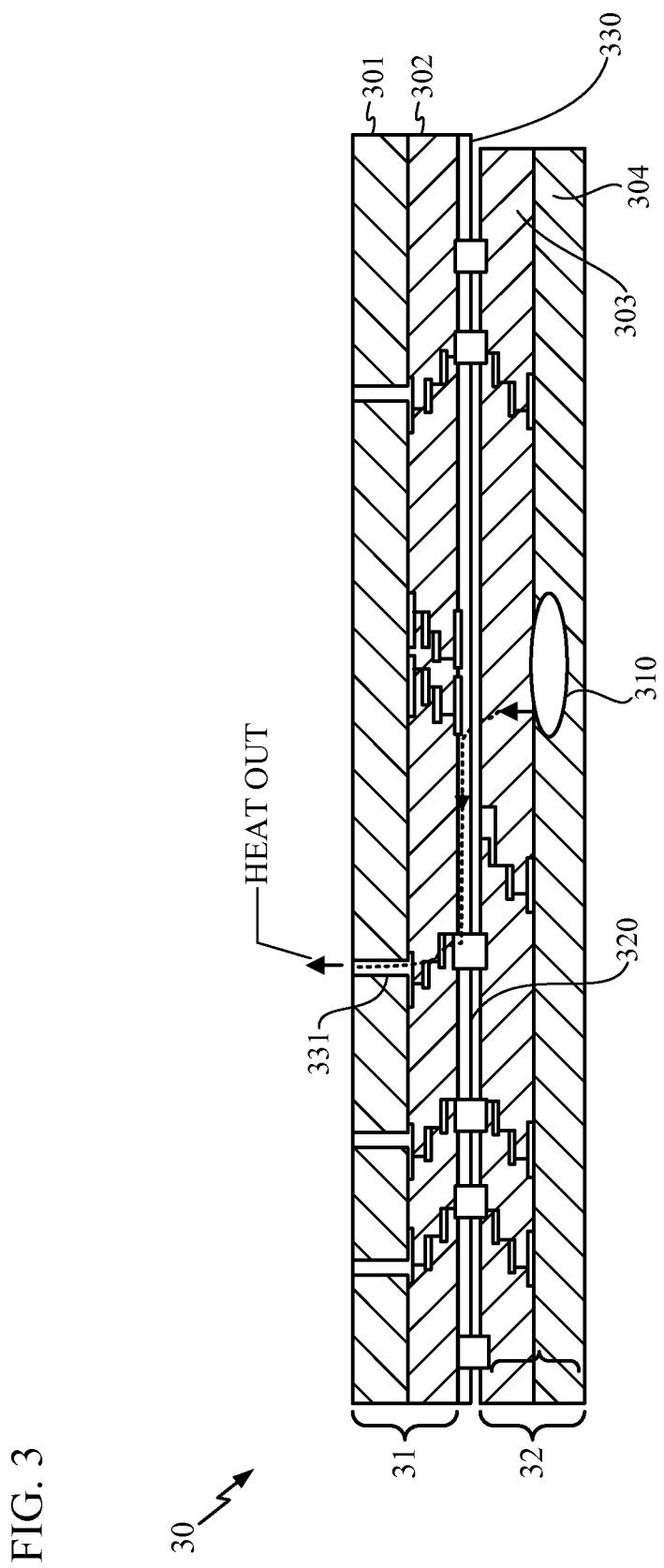


FIG. 2

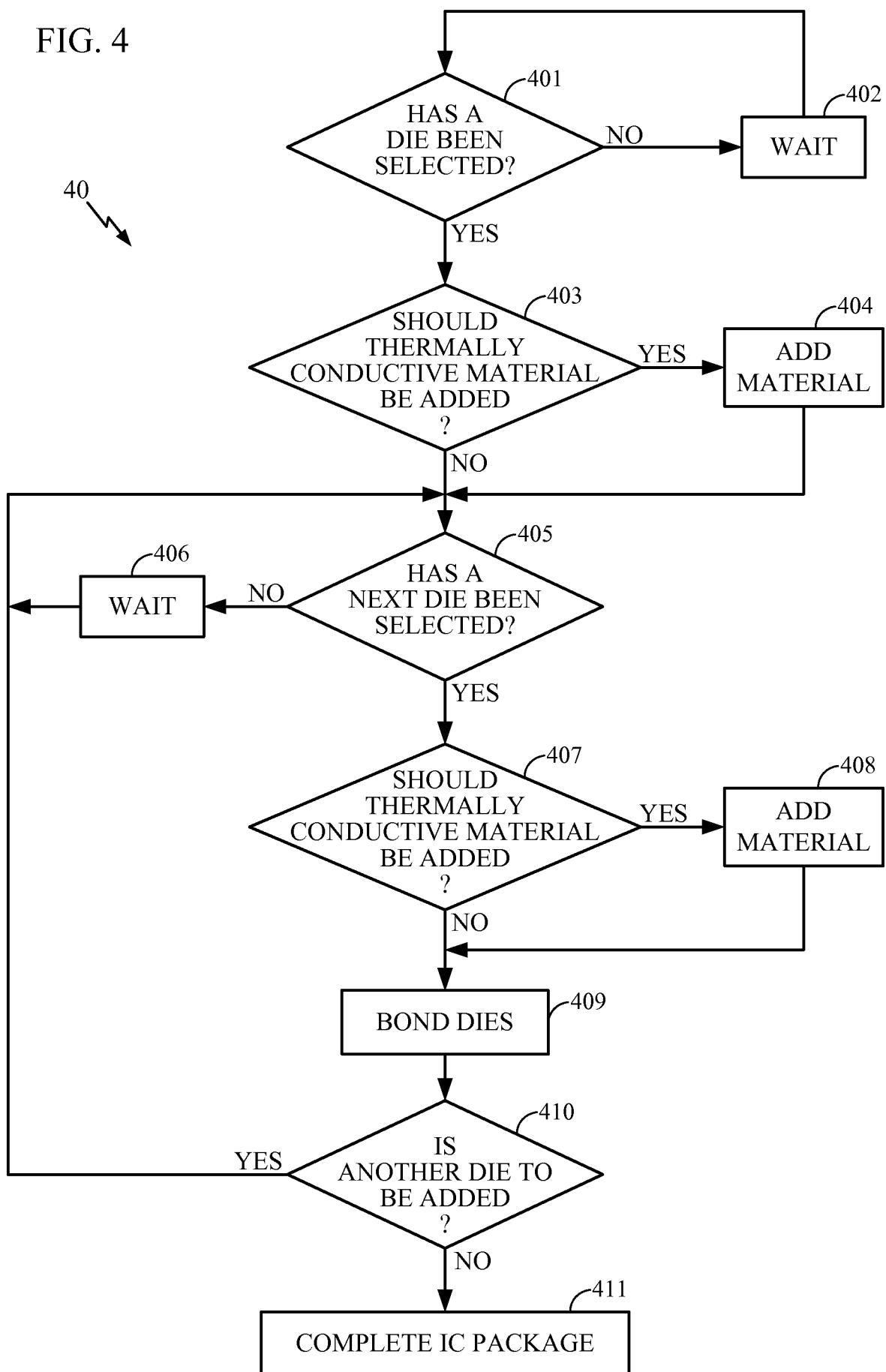


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3/3

FIG. 4



INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/041780

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L25/065 H01L23/367 H01L23/373

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 764 804 A (SAHARA KUNIZO [JP] ET AL) 16 August 1988 (1988-08-16) column 2, line 54 - column 5, line 7; figures 1,2 column 6, lines 35-39; figure 3	1-6, 9-13, 15-22
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Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

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X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

& document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 August 2009	01/09/2009
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Le Gallo, Thomas

INTERNATIONAL SEARCH REPORT

International application No PCT/US2009/041780

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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