(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

PCT

(43) International Publication Date
24 March 2011 (24.03.2011)

(10) International Publication Number
WO 2011/032831 A1

(51) International Patent Classification:
H01L 29/78 (2006.01) *H01L 21/84* (2006.01)
H01L 21/336 (2006.01) *H01L 27/12* (2006.01)

(21) International Application Number:
PCT/EP2010/062721

(22) International Filing Date:
31 August 2010 (31.08.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/561,880 17 September 2009 (17.09.2009) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP,

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(54) Title: DUAL DIELECTRIC TRI-GATE FIELD EFFECT TRANSISTOR

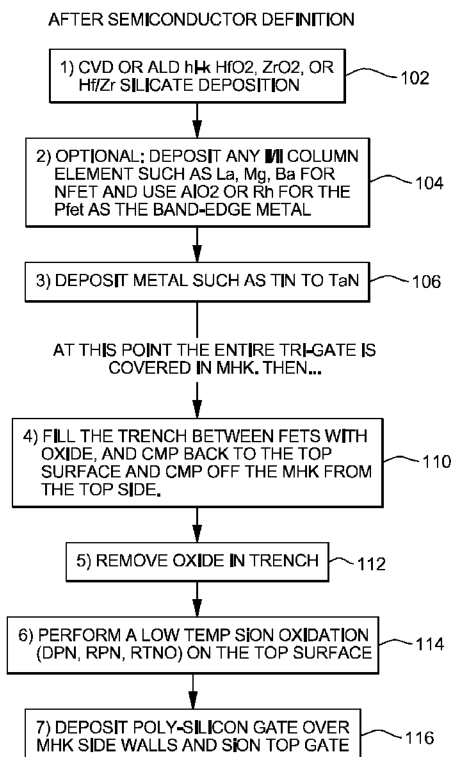

FIG. 7

(57) Abstract: A dual dielectric tri-gate field effect transistor, a method of fabricating a dual dielectric tri-gate field effect transistor, and a method of operating a dual dielectric tri-gate effect transistor are disclosed. In one embodiment, the dual dielectric tri-gate transistor comprises a substrate, an insulating layer on the substrate, and at least one semiconductor fin. A first dielectric having a first dielectric constant extends over sidewalls of the fin, and a metal layer extends over the first dielectric, and a second dielectric having a second dielectric constant is on a top surface of the fin. A gate electrode extends over the fin and the first and second dielectrics. The gate electrode and the first dielectric layer form first and second gates having a threshold voltage Vt1, and the gate electrode and the second dielectric layer form a third gate having a threshold voltage Vt2 different than Vt1.

WO 2011/032831 A1

KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

DUAL DIELECTRIC TRI-GATE FIELD EFFECT TRANSISTOR

Field of the Invention

5 This invention generally relates to semiconductor devices, and more specifically, to tri-gate field effect transistors.

Background

10 Due to the increasing difficulty in shrinking complementary metal-oxide-semiconductor (CMOS) transistor gate lengths while simultaneously controlling leakage current, the traditional single-gate metal-oxide-semiconductor field-effect transistor (MOSFET) structure may be supplanted by dual-or triple-gate MOSFET structures. These structures, by increasing the gate's control of the channel potential, allow greater ability to turn off 15 MOSFETs with ultra-short channel lengths. Of the various multi-gate MOSFETs structures explored in recent years, the most promising in terms of manufacturability and performance are typically variations of the so-called "FinFET" structure. In these devices, a strip or "fin" of silicon is formed, and subsequently the gate material is deposited and etched, so that the resulting gate surrounds the fin on the three exposed sides. The channel region of the 20 device is located in the fin. Because the gate electrode and the gate dielectric surround the semiconductor body on three sides, the transistor essentially has three separate channels and gates.

Tri-gate device structures, in particular, are receiving substantial attention as a candidate for 25 22 nm technologies and beyond. Because there are three separate channels formed in the semiconductor body, the semiconductor body can be fully depleted when the transistor is turned on, thereby enabling the formation of a fully depleted transistor with gate lengths of less than 30 nanometers without requiring the use of ultra-thin semiconductor bodies or requiring photolithographic patterning of the semiconductor bodies to dimensions less than 30 the gate length of the device.

Tri-gate device structures offer better electrostatic control, permitting gate length scaling. In addition, the current available per planar layout is potentially increased, as the sidewalls are gated regions.

5 Brief Summary

Embodiments of the invention provide a dual dielectric tri-gate field effect transistor, a method of fabricating a dual dielectric tri-gate field effect transistor, and a method of operating a dual dielectric tri-gate field effect transistor. In one embodiment, the dual
10 dielectric tri-gate field effect transistor comprises a semiconductor substrate, an insulating layer on said substrate, and at least one semiconductor fin on and extending upward from said insulating layer. A first dielectric layer having a first dielectric constant extends over first and second sidewalls of the fin. A metal layer extends over this first dielectric layer, and this metal layer and the first dielectric form a metal-dielectric layer. A second dielectric
15 layer having a second dielectric constant, different than the first dielectric constant, is on a top surface of the fin. A gate electrode extends over the fin, the metal-dielectric layer, and the second dielectric layer. The gate electrode and the metal-dielectric layer form first and second gates having a threshold voltage Vt1, and the gate electrode and the second dielectric layer form a third gate having a threshold voltage Vt2 different than Vt1.

20

In one embodiment, the first dielectric layer is a high-k dielectric, and the metal layer and the first dielectric layer form a metal-high-k dielectric. For example, the high-k dielectric may be HfO_2, ZrO_2 or Hf/Zr, and the metal layer may be comprised of TiN or TaN.

25 An embodiment of the invention provides a method of fabricating a dual dielectric tri-gate field effect transistor. This method comprises providing a base structure comprising a semiconductor substrate, an insulating layer, and at least one semiconductor fin extending upward from the insulating layer, said fin having first and second lateral sides and a top. This method further comprises forming a first dielectric material layer extending over the
30 first and second lateral sides of the fin, forming a metal layer over the first dielectric material layer, and forming a second dielectric material layer, different that the first dielectric material layer, extending over the top of the fin. A gate electrode is formed extending over

the fin and the first and second dielectric layers; and the gate electrode and the first dielectric layer form first and second gates having a threshold voltage Vt1, and the gate electrode and the second dielectric layer form a third gate having a threshold voltage Vt2 different than Vt1.

5

In an embodiment, the first dielectric material is a high-k dielectric and the metal layer and the first dielectric material form a metal-high-k (MHK) dielectric. In an embodiment, the first dielectric layer extends over substantially all of the first and second sides of the fin, the second dielectric layer extends over substantially all of the top surface of the fin, and the
10 gate electrode is comprised of an electrode material extending over both the first and second dielectric layers.

An embodiment of the invention provides a method of operating a dual dielectric tri-gate field effect transistor (FET) comprising first, second and third gates, where the first and
15 second gates have a threshold voltage of Vt1, and the third gate has a threshold voltage of Vt2 that is greater than Vt1. This method comprises applying a supply voltage Vdd to the first, second and third gates of the FET, and operating the FET in a low power mode when Vdd is less than Vt2 and greater than Vt1.

20 In an embodiment of the invention, the top surface of the gated region is engineered to have a threshold voltage Vt1 with a polysilicon gated SiON based dielectric and with metal high-k gated side surfaces to both have Vt2. A device with these properties will operate excellently in low Vdd (Vt2>Vdd>Vt1), low power mode, and when Vdd is increased above Vt2, the device will operate in a high performance mode. In the low power mode, the device will
25 also consume lower active power, as the gate capacitance of polysilicon gated SiON FETs will be much lower than MHK gated devices.

Brief Description Of The Several Views Of The Drawings

30 Fig. 1 shows a dual dielectric tri-gate structure in accordance with an embodiment of the invention.

Fig. 2 illustrates a base structure from which the tri-gate structure of Fig. 1 is fabricated.

Fig. 3 depicts the formation of a high-k dielectric on the structure of Fig. 2

5 Fig. 4 illustrates a metal deposition on the high-k dielectric.

Fig. 5 shows a SiO_2 deposited on the structure of Fig. 4.

Fig. 6 illustrates a SiON grown on the Si fins shown in Fig. 5.

10

Fig. 7 shows a fabrication flow chart diagram according to an embodiment of the invention.

Fig. 8 depicts a bulk semiconductor substrate that may also be used, in an embodiment of the invention, in the fabrication of a transistor.

15

Fig. 9 illustrates an oxide layer on the bulk semiconductor substrate of Fig. 8.

Detailed Description

20 In the following description, numerous specific details are set forth, such as particular structures, components, materials, dimensions, processing steps and techniques, in order to provide a thorough understanding of the present invention. However, it will be appreciated by one of ordinary skill in the art that the invention may be practiced with a wide range of specific details. In other instances, well-known structures or processing steps have not been
25 described in detail in order to avoid obscuring the invention.

Fig. 1 shows a dual dielectric tri-gate structure according to one embodiment of the present invention. Structure 10 comprises a base semiconductor substrate 12, an insulator layer 14, a plurality of semiconductor fins 16, Hi-K dielectric 20, metal layer 22, top gate dielectric 24,
30 and gate electrode 26.

The base semiconductor substrate layer 12 may comprise any semiconductor material including, but not limited to: Si, SiC, SiGe, SiGeC, Ge alloys, GaAs, InAs, InP, other III-V or II-VI compound semiconductors, or organic semiconductor structures. In some embodiments of the present invention, the base semiconductor substrate layer 12 may be comprised of a Si-containing semiconductor material, i.e., a semiconductor material that includes silicon. Further, the base semiconductor substrate layer 12 may be doped or contain both doped and undoped regions. Although the base semiconductor substrate layer 12 may be a bulk semiconductor structure, it may also include a layered structure with one or more buried insulator layers (not shown).

The insulator layer 14 may comprise any suitable insulator material(s), and it typically comprises a buried oxide (BOX), a nitride, or an oxynitride in either a crystalline phase or a non-crystalline phase. The buried insulator layer 14 may be a homogeneous, continuous layer, or it may contain relatively large cavities or micro- or nano-sized pores (not shown). The physical thickness of the buried insulator layer 14 may vary widely depending on the specific applications, but it typically ranges from about 10 nm to about 500 nm, with from about 20 nm to about 200 nm being more typical. The present invention, in an embodiment, may utilize a bulk substrate, referred to as bulk FinFET or Trigat/FinFET on bulk substrate, discussed in more detail below.

The semiconductor fins 16 may comprise any semiconductor material including, but not limited to: Si, SiC, SiGe, SiGeC, Ge alloys, GaAs, InAs, InP, other III-V or II-VI compound semiconductors, or organic semiconductor structures. In some embodiments of the present invention, it may be preferred that the semiconductor fins 16 be comprised of a Si-containing semiconductor material, i.e., a semiconductor material that includes silicon. Further, the semiconductor fins 16 may be doped or contain both doped and undoped regions therein. The physical thickness of the fins 16 may vary widely depending on the specific applications. As will be understood by those of ordinary skill in the art, fins 16 may be formed in other ways. For example, Side wall Image Transfer (SIT) may be used to define the fins.

Gate dielectric layer 20 extends over the sidewalls of semiconductor fins 16 and on or adjacent the insulating layer 14. Gate dielectric layer 20 can be any suitable dielectric material. For instance, the gate dielectric layer may be a silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y) or a silicon nitride (Si_3N_4) dielectric layer. In an embodiment of the
5 present invention, the gate dielectric layer 20 may be a silicon oxynitride film formed to a thickness of between 5-20 Å. In an embodiment of the present invention, gate dielectric layer 20 may be a high K gate dielectric layer, such as a metal oxide dielectric, such as but not limited to tantalum pentaoxide (Ta_2O_5), and titanium oxide (TiO_2). Gate dielectric layer 20 can be other types of high K dielectric, such as but not limited to PZT (Lead Zirconate
10 Titanate).

Metal layer 22 extends over gate dielectric layer 20, and this layer 22 may be formed of a variety of suitable materials such as, but not limited to, tungsten, tantalum, titanium, and their nitrides. As another example, layer 22 may comprise polycrystalline silicon doped to a
15 concentration density between $10^{19} – 10^{20}$ atoms/cm^3. Also, layer 22 need not necessarily be a single material and can be a composite stack of thin films, such as but not limited to a polycrystalline silicon/metal electrode or a metal/polycrystalline silicon electrode.

Top gate dielectrics 24 are positioned on or adjacent top surfaces of fins 16. Dielectrics 24,
20 similar to dielectric layer 20, can be any suitable dielectric material; and, for example, dielectrics 24 may be a silicon oxynitride SiON or a silicon nitride dielectric layer. In an embodiment of the invention, the gate dielectric 24 may be a silicon oxynitride film formed to a thickness of between 5 – 20 A.

25 The gate electrode layer 26 may comprise polycrystalline silicon (poly-silicon), metal such as Al, Cu, W, Ti, Ta, TiN, TaN, NiSi, CoSi, and/or other proper conductive materials. The gate electrode layer 26 may be formed by CVD, PVD, plating, ALD, and other suitable processes. The gate electrode layer 26 may have a multilayer structure and may be formed in a multiple-step process.

30

Figs. 2-6 illustrate processing steps in the fabrication of the structure 10 shown in Fig. 1, and Fig. 7 shows a fabrication flow chart diagram according to an embodiment of the invention.

Generally, in embodiments of the invention, conventional fabrication steps can be used to form semiconductor substrate 12, insulator layer 14 and fins 16, as shown in Fig. 2. For example, in the manufacture of the device 10, a silicon substrate 12 forming a silicon semiconductor body may be provided with an insulating layer 14 and on top thereof a monocrystalline silicon layer. Such a semiconductor body can, for example, be obtained by implanting oxygen ions into a monocrystalline silicone substrate. However, other techniques to obtain such a start-point semiconductor body are feasible, such as using thermal oxidation of a semiconductor substrate. Subsequently, an implant may be performed to tune the electrical properties of the semiconductor/silicon layer 12.

After this, a hard mask layer, e.g., of silicon nitride or a silicon oxide, may be deposited and patterned on the semiconductor layer at the location at which fins are to be formed and where source and drains regions are envisaged for forming a FinFET device. This may be followed by an etching step to form the fins 16. Optionally, this may be followed by a surface treatment like an H_2 annealing step. Then, a poly silicon layer or hard mask layer is deposited and patterned, after which source and drain implants are done for forming source and drain regions that border the fin. During each of these two implants, the other regions of the structure are protected by, for example, a photo resist spot. After the source and drain implants are completed, the hard mask layer N is removed, also by (selective) etching.

With reference to Figures 3 and 7, after the formation of structure 30 of Fig. 2, high-k dielectric layer 20 is formed at step 102. This may be done, for example, by a chemical vapor deposition (CVD) or an atomic layer deposition (ALD) hi-k HfO_2, ZiO_2 or Hf/Zr silicate deposition. The high-k dielectric layer 20 may contain any of the materials known in the art, including, but not limited to oxides of Zr, Hf, Al, HfSi, HfSiN, and combinations thereof. The thickness of high-k dielectric layer 20 may be between about 1.0 nm and about 2.5 nm.

An optional step 104 is to depost a band-edge metal on the hi-k dielectric layer 20. For an NFET, this may be done, for instance, by depositing any II/II column element such as La, MG, or Ba. For a PFET, AlO_2 or Rh may be deposited to form a base-edge metal.

Step 106, illustrated in Fig. 4, is a metal deposition step to form metal layer 22. This layer extends over gate dielectric layer 20, and the metal layer 22 may be formed of a variety of suitable materials such as, but not limited to, tungsten, tantalum, titanium, and their nitrides. As another example, layer 22 may comprise polycrystalline silicon doped to a concentration
5 density between $10^{19} - 10^{20}$ atoms/cm^3. Also, layer 22 need not necessarily be a single material and can be a composite stack of thin films, such as but not limited to a polycrystalline silicon/metal electrode or a metal/polycrystalline silicon electrode.

At step 110, silicon dioxide (SiO_2), shown in Fig. 5 at 32, is deposited to fill the trenches
10 between the fins 16 and to cover layer 22. In one embodiment, a silicon oxide layer is thickly deposited to cover the entire structure. Subsequently, Chemical-Mechanical Polishing (CMP) is performed to planarize the silicon oxide layer and to expose the tops of the fin-shaped structures 16.

15 At step 112, the oxide is removed from the trenches, and top gate dielectrics 24 are then grown, at step 114, on the tops of fins 16, as shown in Fig. 6. These top gate dielectrics can be any suitable dielectric material, and for example, dielectrics 24 may be a silicon oxynitride SiON or a silicon nitride dielectric layer. In an embodiment of the invention, the gate dielectric 24 may be a silicon oxynitride film formed to a thickness of between 5–20 A.
20 Dielectrics 24 may be formed, for example, by rapid thermal processing (RTP) oxide, decoupled plasma nitridation (DPN) or by rapid thermal oxidation using NO gas (RTNO).

At step 116, polysilicon gate 26 (shown in Fig. 1) is deposited over the metal-hi-k (MHK) sidewalls and the SiON top gate dielectrics 24. This gate electrode layer 26 may comprise
25 polycrystalline silicon (poly-silicon), metal such as Al, Cu, W, Ti, Ta, TiN, TaN, NiSi, CoSi, and/or other proper conductive materials. The gate electrode layer 26 may be formed by CVD, PVD, plating, ALD, and other suitable processes. Also, the gate electrode layer 26 may have a multilayer structure and may be formed in a multiple-step process.

30 With the above-described design, FET device 10 essentially has three separate channels and gates. Each fin 16 forms a top channel and two side channels. The top dielectric 24 and

polysilicon material 26 form a first, top gate with a threshold voltage Vt1, and metal-hi-k dielectric layer 20, 22 and the polysilicon material 26 form two additional side gates with a threshold voltage Vt2.

5 As mentioned above, in an embodiment, the invention may be fabricated using a bulk substrate, referred to as a bulk Fin FET or Trigat/FinFET on bulk Si substrate. Fig. 8 shows such a bulk substrate, with fins 42. Any suitable bulk substrate may be used, and fins 42 may be formed thereon in any suitable way. As shown in Fig. 9, an oxide insulator layer 44 is deposited on substrate 44, between the fins 42. Any suitable oxide material may be used, 10 and the oxide layer 44 may be formed or deposited on substrate 40 in any suitable manner. After layer 44 is formed, the resulting structure may be processed, for example, as described above in connection with Fig. 2-7 to fabricate a dual dielectric trigate field effect transistor.

Embodiments of the invention have significant utility. For instance, in an embodiment of the invention, the top surface of the gated region may be engineered to have a threshold 15 voltage Vt1 that is less than the threshold voltage Vt2 of the metal high-k gated side surfaces. A device with these properties will operate excellently in low Vdd (Vt2>Vdd>Vt1), low power mode, and when Vdd is increased above Vt2, the device will operate in a high performance mode. In the low power mode, the device will also consume lower active power, as the gate capacitance of polysilicon gated SiON FETs will be much 20 lower than MHK gated devices.

While it is apparent that the invention herein disclosed is well calculated to fulfill the objects discussed above, it will be appreciated that numerous modifications and embodiments may be devised by those skilled in the art, and it is intended that the appended claims cover all 25 such modifications and embodiments as fall within the true scope of the present invention.

CLAIMS

1. A dual dielectric tri-gate field effect transistor comprising:
a semiconductor substrate;
an insulating layer on said substrate;
at least one semiconductor fin on and extending upward from said insulating layer, said fin including first and second sidewalls and a top surface;
a first dielectric layer having a first dielectric constant extending over the first and second sidewalls of the fin;
a metal layer extending over the first dielectric layer;
a second dielectric layer having a second dielectric constant, different than the first dielectric constant, on the top surface of the fin; and
a gate electrode extending over the fin and the first and second dielectric layers, wherein the gate electrode and the first dielectric layer form first and second gates having a threshold voltage Vt1, and the gate electrode and the second dielectric layer form a third gate having a threshold voltage Vt2 different than Vt1.

2. The dual dielectric tri-gate field effect transistor according to Claim 1, wherein Vt2 is greater than Vt1.

3. The dual dielectric tri-gate field effect transistor according to Claim 1 or 2, wherein the first dielectric layer is a high-k dielectric, and the metal layer and the first dielectric layer form a metal-high-k dielectric.

4. The dual dielectric tri-gate field effect transistor according to Claim 3, wherein the high-k dielectric is HfO_2, ZrO_2 or Hf/Zr.

5. The dual dielectric tri-gate field effect transistor according to Claim 3 or 4, wherein the metal layer is comprised of TiN or TaN.

6. The dual dielectric tri-gate field effect transistor according to any preceding Claim, wherein the second dielectric layer is a SiON dielectric.

7. The dual dielectric tri-gate field effect transistor according to any preceding Claim, wherein the gate electrode is a polysilicon.

8. The dual dielectric tri-gate field effect transistor according to any preceding Claim, further comprising a band-edge metal deposited on the semiconductor substrate.

9. The dual dielectric tri-gate field effect transistor according to any preceding Claim, wherein:

the first dielectric layer extends over substantially all of the first and second sides of the fin;

the second dielectric layer extends over substantially all of the top surface of the fin; and

the gate electrode is comprised of an electrode material extending over both the first and second dielectric layers.

10. A dual dielectric tri-gate field effect transistor according to any preceding claim comprising:

at least one further semiconductor fin on and extending upward from said insulating layer, each of said fins including first and second sidewalls and a top surface;

said first dielectric layer having a first dielectric constant extending over substantially all of the first and second sidewalls of the fins;

said second dielectric layer having a second dielectric constant, different than the first dielectric constant, extending over substantially all of the top surfaces of the fins; and

said gate electrode extending over the fins and the first and second dielectric layers.

11. A method of fabricating a dual dielectric tri-gate field effect transistor comprising:

providing a base structure comprising a semiconductor substrate, an insulating layer, and at least one semiconductor fin extending upward from the insulating layer, said fin having first and second lateral sides and a top;

forming a first dielectric material layer extending over the first and second lateral sides of the fin;

forming a metal layer over the first dielectric material layer;

forming a second dielectric material layer, different that the first dielectric material layer, extending over the top of the fin; and

forming a gate electrode extending over the fin and the first and second dielectric layers, wherein the gate electrode and the first dielectric layer form first and second gates having a threshold voltage Vt1, and the gate electrode and the second dielectric layer form a third gate having a threshold voltage Vt2 different than Vt1.

12. The method according to Claim 11, wherein Vt2 is greater than Vt1.

13. The method according to Claim 11 or 12, wherein the first dielectric material is a high-k dielectric and the metal layer and the first dielectric material form a metal-high-k dielectric.

14. The method according to Claim 11, 12 or 13, wherein the first dielectric layer extends over substantially all of the first and second sides of the fin.

15. The method according to any of Claims 11 to 14, wherein

the second dielectric layer extends over substantially all of the top surface of the fin; and

the gate electrode is comprised of an electrode material extending over both the first and second dielectric layers.

16. A method of operating a dual dielectric tri-gate field effect transistor (FET) according to any of claims 1 to 10, the method comprising:

applying a supply voltage Vdd to the first, second and third gates of the FET; and

operating the FET in a low power mode when Vdd is less than Vt2 and greater than Vt1.

17. The method according to Claim 16, further comprising operating the FET in a high
5 pwer mode when Vdd is greater than Vt2.

18. The method according to Claim 16 or 17, wherein the FET includes a semiconductor fin, and the first and second gates comprise a metal-high-k dielectric and polysilicon gate electrode extending over a sidewall of said fin.
10

19. The method according to Claim 18, wherein the third gate comprises a SiON dielectric and said polysilicon gate electrode extending over a top surface of the fin.

20. The method according to Claim 18 or 19, whererin the metal-high-k dielectric
15 comprises a TiN or TaN metal layer and a HfO_2, ZrO_2 or Hf/Zr high-k dielectric layer.

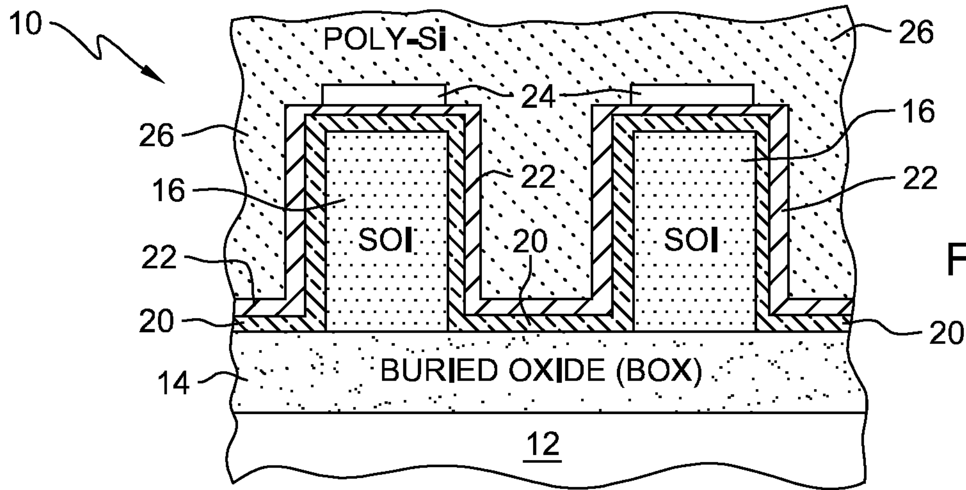

FIG. 1

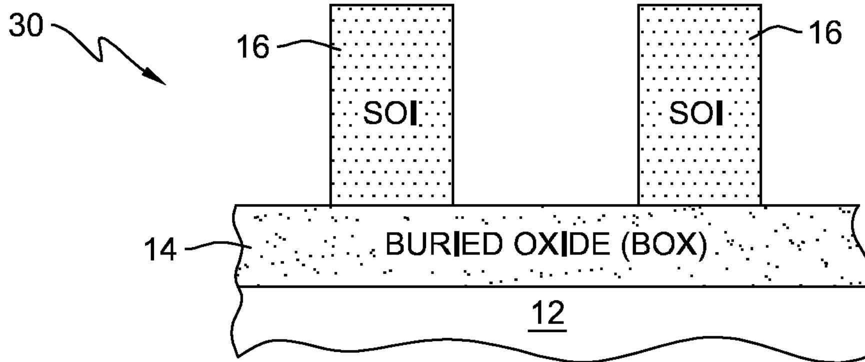

FIG. 2

START WITH PATTERNED Si FINs

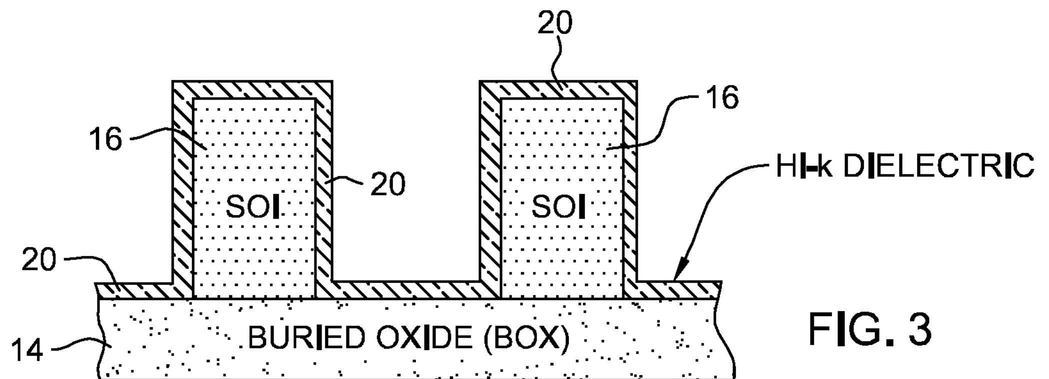

FIG. 3

1) DIELECTRIC FORMATION

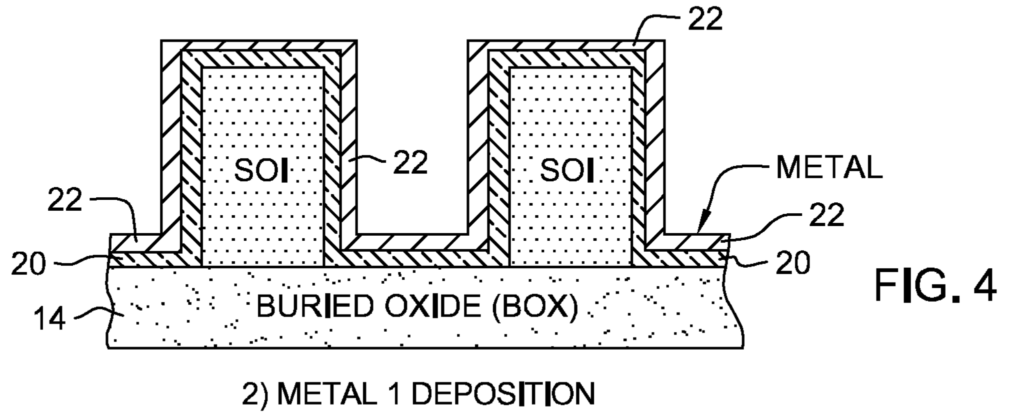

FIG. 4

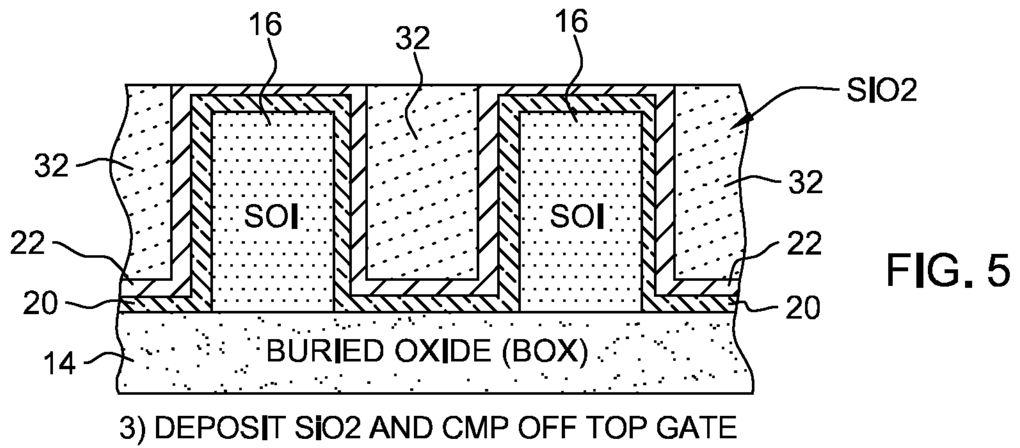

FIG. 5

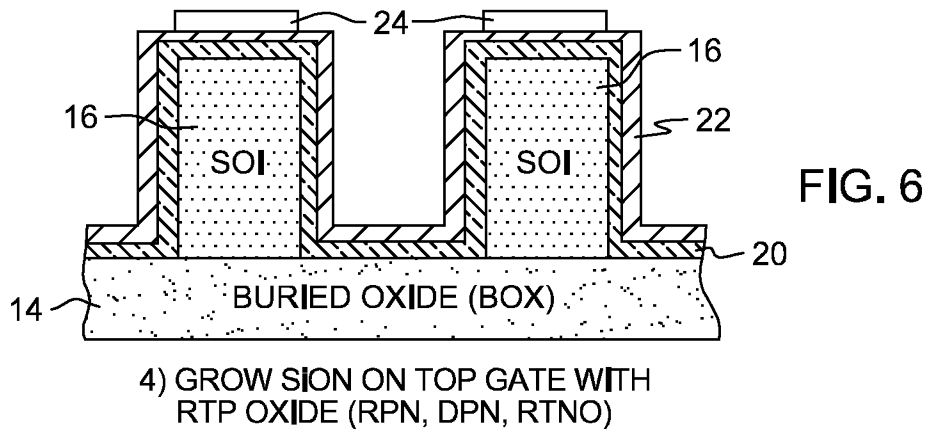

FIG. 6

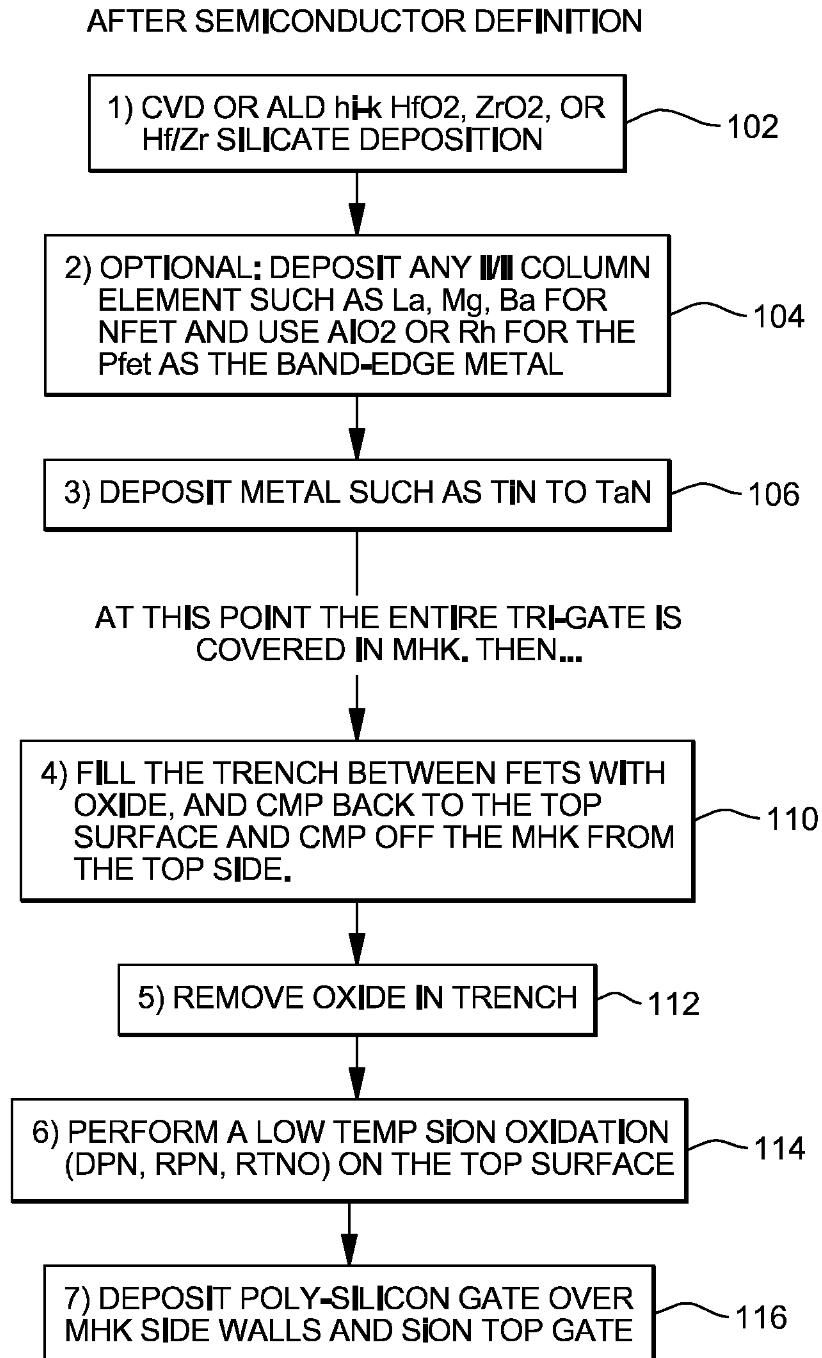

FIG. 7

FIN INFORMATION ON BULK SI SUBSTRATE

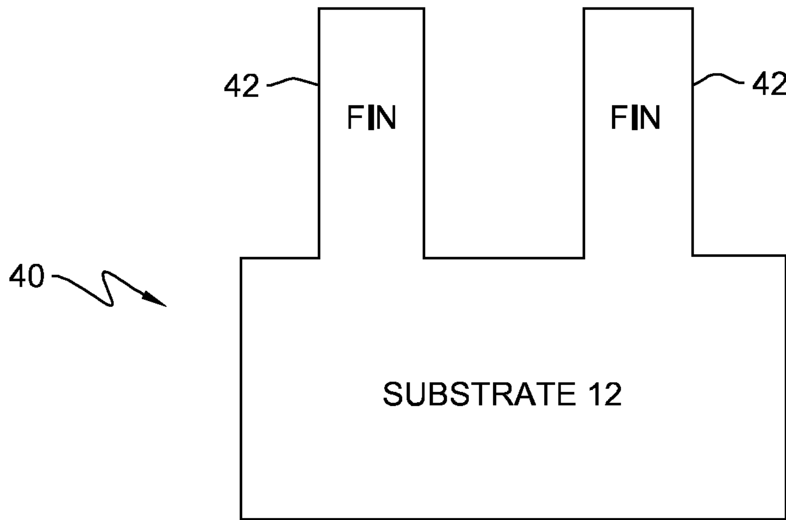

FIG. 8

FILL IN OXIDE ISOLATION BETWEEN FINS

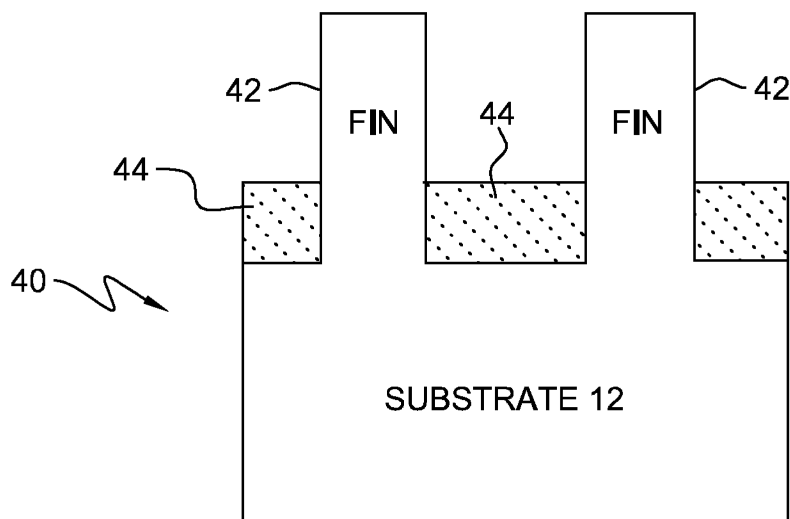

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/062721

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/78 H01L21/336 H01L21/84 H01L27/12
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/011612 A1 (HIEDA KATSUHIKO [JP]) 31 January 2002 (2002-01-31) paragraph [0208] paragraph [0234] - paragraph [0239] paragraph [0285] - paragraph [0290] figures 21A-C	1-20
X	US 5 844 278 A (MIZUNO TOMOHISA [JP] ET AL) 1 December 1998 (1998-12-01) column 4, line 40 - line 49 column 10, line 38 - column 12, line 64; figures 10-12	1-20
X	US 7 148 526 B1 (AN JUDY XILIN [US] ET AL) 12 December 2006 (2006-12-12) column 4, line 62 - column 6, line 28; figures 11-17	1-20

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
5 November 2010	12/11/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Hoffmann, Niels

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2010/062721

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