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(71) Applicant: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, New York 10504 (US).

(72) Inventors: **FRANKLIN, Aaron D.**; 1101 Kitchawan Road, Yorktown Heights, New York 10598 (US). **KOSWATTA, Siyuranga O.**; 1101 Kitchawan Road, Yorktown Heights, New York 10598 (US). **SMITH, Joshua T.**; 1101 Kitchawan Road, Yorktown Heights, New York 10598 (US).

(74) Agent: **SULLIVAN, Sean F.**; Cantor Colburn LLP, 20 Church St., 22nd Floor, Hartford, Connecticut 06103-3207 (US).

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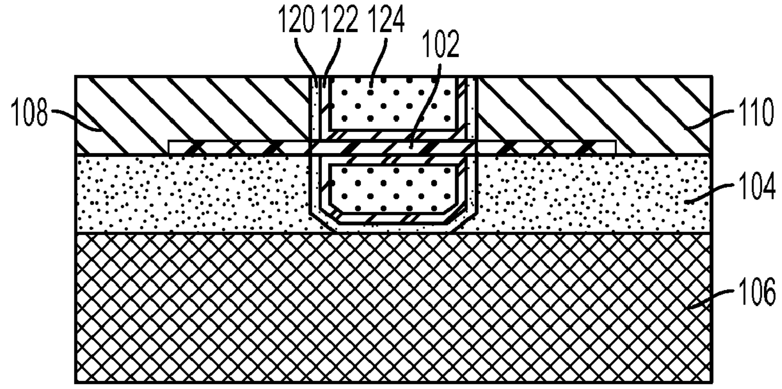


FIG. 7

(57) Abstract: A method of fabricating a semiconducting device is disclosed. A carbon nanotube is formed on a substrate. A portion of the substrate is removed to form a recess below a section of the carbon nanotube. A doped material is applied in the recess to fabricate the semiconducting device. The recess may be between one or more contacts formed on the substrate separated by a gap.

GATE-ALL-AROUND CARBON NANOTUBE TRANSISTOR WITH DOPED SPACERS

BACKGROUND

[0001] The present disclosure relates to semiconductor devices and, in particular, to carbon nanotube transistors and methods of manufacturing carbon nanotube transistors.

[0002] Carbon nanotube field-effect transistors (CNT FETs) can provide low-voltage performance with channel lengths scaled into the sub-10 nanometer (nm) regime. A self-aligned gate structure is used for CNT FETs in highly integrated digital applications. When considering a CNT FET for such applications, it is useful to get the voltage required to switch between ON and OFF states as low as possible. Decreasing this operating voltage improves the quality and applicability of the CNT FET for such applications.

SUMMARY

[0003] According to one embodiment, a method of fabricating a semiconducting device includes: forming a carbon nanotube on a substrate; removing a portion of the substrate to form a recess below a section of the carbon nanotube; and applying a doped material in the recess to fabricate the semiconducting device.

[0004] According to another embodiment, a method of fabricating a transistor includes: forming a carbon nanotube material on a substrate; forming one or more contacts on the substrate to define a gap between the one or more contacts; removing a portion of the substrate in the gap; and applying a doped material in the gap to fabricate the transistor.

[0005] According to another embodiment, a method of making a self-aligned carbon nanotube transistor includes: forming a carbon nanotube on a substrate; forming a source contact on the substrate over the carbon nanotube; forming a drain contact on the substrate over the carbon nanotube, wherein the drain contact is separated from the source contact by a gap; removing a portion of the substrate in the gap between the source contact and the drain contact; and applying a doped material in the gap to make the self-aligned carbon nanotube transistor.

[0006] Additional features and advantages are realized through the techniques of the present disclosure. Other embodiments and aspects of the disclosure are described in detail herein and are considered a part of the claimed disclosure. For a better understanding of the disclosure with the advantages and the features, refer to the description and to the drawings.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0007] The subject matter which is regarded as the disclosure is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other features, and advantages of the disclosure are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[0008] Figure 1 shows a carbon nanotube placed at a selected location on a substrate at an initial production stage of the exemplary carbon nanotube field-effect transistor;

[0009] Figure 2 shows a first contact and a second contact formed on the silicon substrate in a second production stage;

[0010] Figure 3 shows a recess formed in the silicon layer of the substrate;

[0011] Figure 4 illustrates a coating stage in which a spacer material is deposited;

[0012] Figure 5 shows a high-k dielectric deposition stage;

[0013] Figure 6 illustrates a gate deposition stage;

[0014] Figure 7 depicts an exemplary carbon nanotube field-effect transistor made using the exemplary methods disclosed herein;

[0015] Figure 8 illustrates an alternate embodiment of the exemplary carbon nanotube field-effect transistor with a portion of the metal gate removed;

[0016] Figure 9 shows a flowchart illustrating an exemplary method of producing the carbon nanotube field-effect transistor disclosed herein; and

[0017] Figure 10 illustrates an effect of doping a spacer material of the carbon nanotube field-effect transistor has on a relation between drain current and gate-source voltage.

DETAILED DESCRIPTION

[0018] Figures 1-6 show various stages of production or manufacture of an exemplary semiconductor device of the present disclosure. In an exemplary embodiment, the semiconductor device is a carbon nanotube field effect transistor (CNT FET) having a doped gate region. The exemplary method of manufacturing the CNT FET disclosed herein produces self-aligned CNT FETs as a result of depositing the source and drain contacts prior to gate formation, and forming the gate with respect to the deposited source and drain contacts. The source and drain contacts may serve as a mask with respect to etchant used in gate formation and provide anisotropic etching that defines at least one dimension of the gate region. Additionally, the gate region includes a carbon nanotube bridge that extends between source and drain contacts. A configuration of spacer material and/or high-k dielectric is deposited in the gate region to dope the gate region. In an exemplary embodiment, only a doped spacer material is provided. The gate material may be deposited in the gate region to surround the CNT bridge circumferentially.

[0019] Figure 1 shows a carbon nanotube 102 placed at a selected location on a substrate at an initial production stage of the exemplary CNT FET. In the exemplary embodiment, the substrate may be a silicon-on-insulator wafer that includes a top layer or silicon layer 104 on top of an insulating layer such as a BOX (buried oxide) layer 106 that may include silicon-dioxide. The carbon nanotube 102, which serves as a transistor device channel, is deposited on surface 130 of the silicon layer 104. In various embodiments, the carbon nanotube 102 is a semiconducting material.

[0020] Figure 2 shows a first contact 108 and a second contact 110 formed on the silicon substrate 104 in a second production stage. Both the first contact 108 and the second contact 110 may be deposited on the substrate to cover a portion of the carbon nanotube bridge 102 between contact and the substrate 104. The first contact 108 and the second contact 110 are separated by a selected distance or gap. The first contact 108 and second contact 110 may be formed on the substrate using various techniques for aligning the transistor contacts at the selected distance or gap. An exemplary method of forming the first contact 108 and the second contact 110 may include using lithography and lift-off techniques. Alternately, a blanket layer of contact material may be deposited and the selectively etched. In one embodiment, the covered portions of the carbon nanotube may be axial ends of the carbon nanotube. In an exemplary embodiment, one of the first contact 108 and the second contact

110 is a source contact of the completed CNT FET and the other of the first contact 108 and the second contact 110 is a drain contact of the completed CNT FET. In one embodiment, at least one of the first contact 108 and second contact 110 includes a conductive metal such as palladium (Pd).

[0021] Figure 3 shows a recess 112 formed in the silicon layer 104 of the substrate. In various embodiments, the surface 130 of the substrate 104 is a surface that can be effectively etched using a wet etchant. For a silicon layer, an exemplary surface may be a (110) surface, wherein (110) represents Miller indices denoting a direction of a crystallographic plane or surface. A surface 132 that is perpendicular to the (110) surface (such as a (111) surface) is also shown. Wet etchant generally dissolves surface 130 relatively effectively, while surface 132 is generally resistant to wet etching. The silicon substrate 104 is deposited on the BOX layer 106 to orient these surfaces along the directions shown in Figure 3. Exemplary wet etchants include potassium hydroxide (KOH), tetramethylammonium hydroxide (TMAH), etc. The first contact 108 and second contact 110 provide an etch mask that protects the silicon beneath the contacts during etching. Applying the contacts 108 and 110 prior to wet etching allows the contacts to define the gate region of the resulting transistor by the selected separation distance of the contacts 108 and 110 and to produce a self-aligned gate. Wet etching therefore creates a recess 112 in a volume between the contacts. In an exemplary embodiment, the recess 112 is etched to the surface of the insulator layer 106. Additionally, due to the orientation of the reactive surface 130 and the resistive surface 132, the substrate layer is etched anisotropically. Etching the recess 112 yields a suspended CNT, otherwise referred to herein as a CNT bridge or a CNT channel, that extends from the first contact 108 to the second contact 110.

[0022] Figure 4 illustrates a coating stage in which a spacer material 120 is deposited. The spacer material 120 is deposited on the exposed surfaces, except for the carbon nanotube, to provide an insulating layer between a subsequently formed gate material and the first and second contacts 108 and 110. The spacer material 120 may be a doped dielectric material. An exemplary spacer material 120 may include hafnium oxide (HfO_2), or some other dielectric that contains fixed charge to electrostatically dope the carbon nanotube. In an exemplary embodiment, the spacer material is selectively doped to include a fixed charge, thereby providing a fixed charge and an accompanying voltage bias in the gate region. A fixed charge may include a fixed non-zero charge. In another embodiment, the spacer material may be etched away at the carbon nanotube to expose the carbon nanotube at the spacer region. Then, a chemical charge-transfer dopant may be applied to the portion of the carbon nanotube in the etched spacer region. In general, the spacer material adheres to the contacts 108 and 110 as well as the substrate 104 and BOX layer 106 but does not adhere to the CNT bridge during deposition. The spacer may be formed using atomic layer deposition (ALD) or chemical vapor deposition (CVD), for example.

[0023] Figure 5 shows a high-k dielectric deposition stage. A high-k dielectric material 122 is then deposited to conform to the exposed surfaces, including the exposed carbon nanotube channel. The high-k dielectric material 122 nucleates on and annularly coats the CNT bridge 102 between the first contact 108 and the second contact 110, thereby providing a gate dielectric material all around the CNT bridge. The high-k material separates that gate metal (see Figure 6) from the carbon nanotube bridge. The high-k dielectric material may be deposited using, for example, ALD. Exemplary high-k dielectric material may include HfO_2 and Al_2O_3, among others. In an exemplary embodiment, the high-k dielectric material is undoped. When operating the completed CNTFET, dopant charges from the spacer material 120 may be transferred to the high-k dielectric at the CNT bridge to provide a voltage bias at the CNT bridge.

[0024] Figure 6 illustrates a gate deposition stage. Once the high-k dielectric material is deposited, a gate material is deposited. The gate material may be a metal such as palladium (Pd), tungsten (W) or other suitable gate metal. The gate metal may be deposited using atomic layer deposition, sputtering techniques or other known techniques or combination of techniques. After deposition, a portion of the gate metal is disposed the volume between the first contact 108 and the second contact 110 including the etched recess 112. The gate therefore surrounds the carbon nanotube bridge on all sides, forming a gate-all-around transistor. The gate-all-around geometry is enabled by the formation of the suspended nanotube bridge during the etching stage. The gate-all-around geometry reduces an impact of stray change and/or adsorbed molecules.

[0025] During the gate deposition, some portion of the deposited gate metal may overfill and reside on top of the high-k dielectric surface that coats the first contacts 108 and second contact 110. After the gate metal is deposited, the gate overfill metal may be polished by chemical mechanical planarization/polishing (CMP) as illustrated in Figure 7, so that the overfilled metal is removed, thereby revealing top surfaces of the first contact (source) 108, gate 124, and second contact (drain) 110.

[0026] Figure 7 thus depicts an exemplary carbon nanotube field-effect transistor made using the exemplary methods disclosed herein. The exemplary CNT FET includes a substrate, having a carbon nanotube 102 disposed directly thereon. A first (source) contact 108 and a second (drain) contact 110 are disposed on the substrate 104 so that each contact covers a portion of the carbon nanotube between the contact and the substrate 104. The first contact and the second contact are separated by a gap having a selected distance. In various embodiments, the selected distance may be about 30 nanometers. A portion of the carbon nanotube 102 spans the distance between the first contact 108 and the second contact 110 to form a carbon nanotube bridge or carbon nanotube channel. A gate material 124 is deposited in an etched recess between the first contact 108 and the second contact 110 in order to surround the carbon nanotube bridge, thereby providing a gate-all-around carbon nanotube transistor. Since the gate formation is related to the source 108 and the drain 110, the transistor is self-aligned. In various embodiments, the gate metal extends to an insulating layer 106 of the substrate. Additionally, the carbon nanotube bridge may be circumferentially surrounded by a high-k dielectric material is formed between the carbon nanotube bridge and the gate metal. Spacer material 120 may provide a separation between the gate region and the source and drain contacts. The spacer may be selectively doped to provide a voltage bias in the gate region. Thus, the doped CNT FET may be operated as an n-type semiconductor. In an exemplary embodiment, the surfaces of the source 108, gate 124 and drain 110 are substantially coplanar. In an alternate embodiment, some of the gate metal 124 may be etched so that a top surface 140 of the gate metal is recessed below the top surface defined by the source 108 and drain 110, as shown in Figure 8. Recessing additional gate metal above the CNT 102 may reduce parasitic capacitances associated with the gate.

[0027] In various alternative embodiments, a layer of thin contacts may be made upon their deposition. The contacts may then be topped by a layer of low-k dielectric material, which is polished away during the polishing of the gate metal overfill. In another alternative embodiment, the spacer material and the high-k dielectric may both include the same material, such as hafnium oxide (HfO_2). In an exemplary embodiment, the dopant charges are confined to the spacer material.

[0028] Figure 9 shows a flowchart 900 illustrating an exemplary method of producing a CNT FET disclosed herein. In box 901, a carbon nanotube is deposited on a substrate. In various embodiments, the carbon nanotube is a semiconducting material. The substrate generally resides on an insulating layer (BOX layer). In box 903, source and drain contacts are formed on the substrate. The source and drain contacts are formed on top of portions of the carbon nanotube and are separated from each other by a selected distance to provide a gap for deposition of a gate metal. In box 905, the substrate between the source and drain contacts are wet etched to create a recess between the source and drain contacts. The wet etching process leaves the carbon nanotube which thereby forms a carbon nanotube bridge between the source and drain. The substrate is etched to the BOX layer in an exemplary embodiment. In box 907, a doped spacer material is deposited on the exposed surfaces except for the carbon nanotube to provide a spacer between the gate and each of the source and drain contacts. The spacer material grows from the sides of the contacts and the silicon substrate to encompass a portion of the carbon nanotube but does not coat the carbon nanotube along its length. The doped spacer material provides a dopant that provides charge transfer to the CNTFET upon completion of the CNTFET. In box 909, a high-k material is deposited on the exposed spacer material surfaces and the exposed carbon nanotube bridge to annularly coat the carbon nanotube bridge. The high-k dielectric material provides an electrical field to the carbon nanotube bridge when a voltage is applied at the gate. Charge transferred to the high-k dielectric from the spacer material provides a voltage bias at the carbon nanotube bridge. In box 911, gate material is deposited (sputtered) on to the transistor to fill in the recess in the substrate and volume between the source and drain contacts. The deposited gate material forms a gate all around the carbon nanotube bridge.

[0029] Figure 10 is a graph that illustrates an effect of doping a spacer material of the CNTFET has on a relation between drain current (I_d) and gate-source voltage (V_{gs}). The relation corresponds to a CNTFET having a channel length of 30 nm and a source-drain is shown for a voltage of 0.5 V. Curve 1001 shows relation for a CNTFET having a dopant applied only to spacer material at a concentration of 0.4/nm. As V_{gs} increases, the I_d of curve 1001 changes from an OFF state current at about 10^{-9} to an ON state current at about 10^{-5} A. Curve 1003 shows relation for a CNTFET having a dopant applied to spacer material and to the dielectric material at the carbon nanotube bridge at a concentration of 0.4/nm. As V_{gs} increases, the I_d of curve 1003 changes from an OFF state current at about 10^{-11} to an ON state current at about 10^{-5} A. Therefore, selective doping at the spacer only increases the ON current and has a smaller leakage current and better switching behavior (i.e., the slope of Id.) than the CNTFET having dopant at the spacer and dielectric.

[0030] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms “a”, “an” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises” and/or “comprising,” when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one more other features, integers, steps, operations, element components, and/or groups thereof.

[0031] The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present disclosure has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the disclosure in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the disclosure. The embodiment was chosen and described in order to best explain the principles of the disclosure and the practical application, and to enable others of ordinary skill in the art to understand the disclosure for various embodiments with various modifications as are suited to the particular use contemplated.

[0032] The flow diagrams depicted herein are just one example. There may be many variations to this diagram or the steps (or operations) described therein without departing from the spirit of the disclosure. For instance, the steps may be performed in a differing order or steps may be added, deleted or modified. All of these variations are considered a part of the claimed disclosure.

[0033] While exemplary embodiments of the disclosure have been described, it will be understood that those skilled in the art, both now and in the future, may make various improvements and enhancements which fall within the scope of the claims which follow. These claims should be construed to maintain the proper protection for the disclosure first described.

CLAIMS

What is claimed is:

1. A method of fabricating a semiconducting device, comprising:

forming a carbon nanotube on a substrate;

removing a portion of the substrate to form a recess below a section of the carbon nanotube; and

applying a doped material in the recess to fabricate the semiconducting device.

2. The method of claim 1, wherein the section of the carbon nanotube is in a gap between a first contact and a second contact formed on the carbon nanotube.

3. The method of claim 2, further comprising forming the first contact and the second contact aligned to provide a self-aligned gate structure of the semiconducting device.

4. The method of claim 1, wherein applying the doped material further comprises applying a spacer material having a fixed charged density to exposed surfaces in the recess.

5. The method of claim 4, wherein the portion of the substrate in the gap forms a carbon nanotube bridge, further comprising coating the carbon nanotube bridge with a non-doped high-k dielectric material.

6. The method of claim 5, wherein the high-k dielectric material provides a chemical transfer of charge from the doped spacer material to the carbon nanotube bridge.

7. The method of claim 1, wherein the doped material include hafnium oxide.

8. The method of claim 1 wherein the doped material enables operation of the semiconductor device as an n-type semiconductor.

9. The method of claim 1, wherein removing the substrate further comprises anisotropic etching of the substrate.

10. A method of fabricating a transistor, comprising:

forming a carbon nanotube material on a substrate;

forming one or more contacts on the substrate to define a gap between the one or more contacts;

removing a portion of the substrate in the gap; and

applying a doped material in the gap to fabricate the transistor.

11. The method of claim 10, wherein removing the substrate in the gap forms a carbon nanotube bridge in the gap.

12. The method of claim 11, wherein applying the doped material further comprises applying a spacer material having a fixed charged density to exposed surfaces in the gap.

13. The method of claim 12, further comprising coating the carbon nanotube bridge with a non-doped high-k dielectric material.

14. The method of claim 13, wherein the high-k dielectric material provides a chemical charge transfer of charge from the doped spacer material to the carbon nanotube bridge.

15. The method of claim 10, wherein the doped material includes hafnium oxide.

16. The method of claim 10, further comprising forming the one or more contacts to provide a self-aligned gate structure of the transistor.

17. A method of making a self-aligned carbon nanotube transistor, comprising:

forming a carbon nanotube on a substrate;

forming a source contact on the substrate over the carbon nanotube;

forming a drain contact on the substrate over the carbon nanotube, wherein the drain contact is separated from the source contact by a gap;

removing a portion of the substrate in the gap between the source contact and the drain contact; and applying a doped material in the gap to make the self-aligned carbon nanotube transistor.

18. The method of claim 17, wherein applying the doped material further comprises applying spacer material having a fixed charged density to exposed surfaces in the gap except for a surface of the carbon nanotube.

19. The method of claim 18, further comprising etching a portion of the spacer material and applying a chemical charge-transfer dopant to the exposed carbon nanotube in the spacer region.

20. The method of claim 17, further comprising coating the carbon nanotube in the gap with a non-doped high-k dielectric material.

21. A semiconducting device, comprising:

a carbon nanotube on a substrate;

a recess formed in a portion of the substrate below a section of the carbon nanotube; and

a doped material in the recess.

22. The semiconducting device of claim 21, wherein the section of the carbon nanotube is in a gap between a first contact and a second contact formed on the carbon nanotube.

23. The semiconducting device of claim 22, wherein the first contact and the second contact are aligned to provide a self-aligned gate structure.

24. The semiconducting device of claim 21, wherein the doped material further comprises a spacer material having a fixed charged density deposited on surfaces of the recess.

25. The semiconducting device of claim 24, wherein the portion of the substrate in the gap forms a carbon nanotube bridge, further comprising a non-doped high-k dielectric material configured to coat the carbon nanotube bridge.

26. The semiconducting device of claim 25, wherein the high-k dielectric material is configured to provide a chemical transfer of charge from the doped spacer material to the carbon nanotube bridge.

27. The semiconducting device of claim 21, wherein the doped material include hafnium oxide.

28. The semiconducting device of claim 21 wherein the doped material is configured to enable operation of the semiconductor device as an n-type semiconductor.

29. The semiconducting device of claim 21, wherein the portion of the substrate is configured to be removed via anisotropic etching of the substrate.

30. A transistor, comprising:

a carbon nanotube material on a substrate;

one or more contacts formed on the substrate to configured to define a gap between the one or more contacts;

a removed portion of the substrate in the gap; and

a doped material in the removed portion in the gap.

31. The transistor of claim 30, the carbon nanotube in the in the gap forms a carbon nanotube bridge.

32. The transistor of claim 31, wherein the doped material further comprises a spacer material having a fixed charged density deposited on exposed surfaces in the gap.

33. The transistor of claim 32, further comprising a non-doped high-k dielectric material configured to coat the carbon nanotube bridge.

34. The transistor of claim 33, wherein the high-k dielectric material provides a chemical charge transfer from the doped spacer material to the carbon nanotube bridge.

35. The transistor of claim 30, wherein the doped material includes hafnium oxide.

36. The transistor of claim 30, further comprising forming the one or more contacts to provide a self-aligned gate structure of the transistor.

37. A self-aligned carbon nanotube transistor, comprising:

a carbon nanotube on a substrate;

a source contact on the substrate over the carbon nanotube;

a drain contact on the substrate over the carbon nanotube, wherein the drain contact is separated from the source contact by a gap;

a recess in the gap between the source contact and the drain contact formed by removing a portion of the substrate in the gap; and

a doped material in the gap.

38. The self-aligned carbon nanotube transistor of claim 37, wherein the doped material further comprises a spacer material having a dopant deposited on exposed surfaces of the recess except for the carbon nanotube.

39. The self-aligned carbon nanotube transistor of claim 38, further comprising etching a portion of the spacer material and applying a chemical charge-transfer dopant to the exposed carbon nanotube in the spacer region.

40. The self-aligned carbon nanotube transistor of claim 37, further comprising a non-doped high-k dielectric material configured to coat the carbon nanotube in the gap.

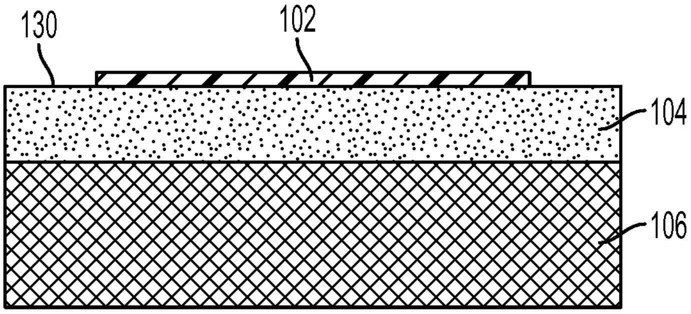


FIG. 1

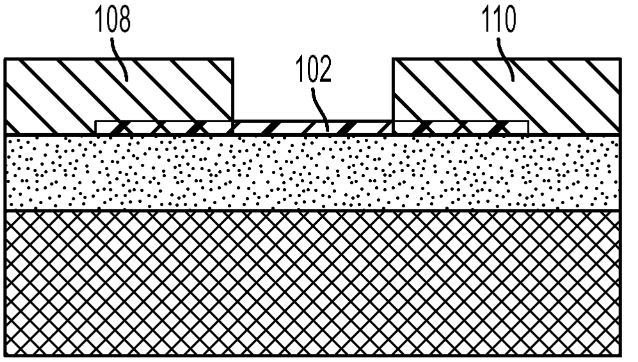


FIG. 2

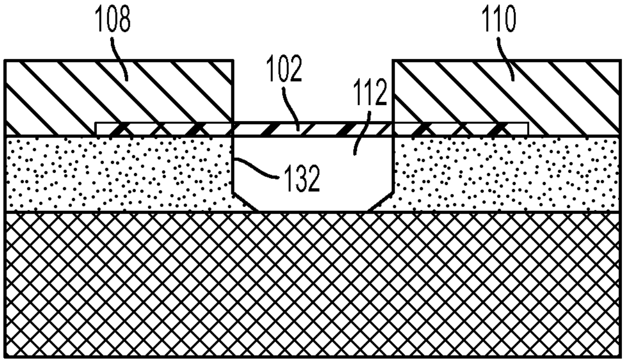


FIG. 3

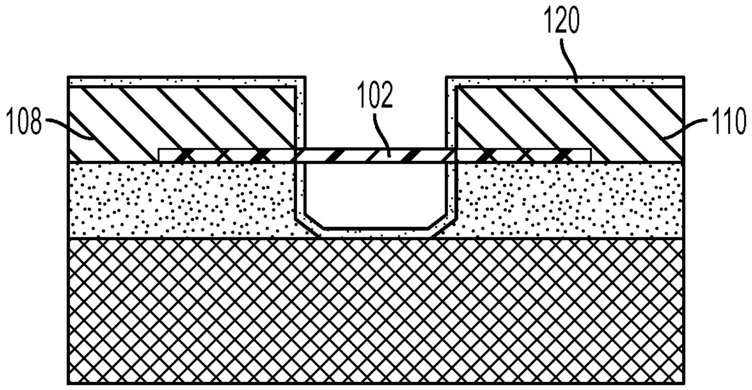


FIG. 4

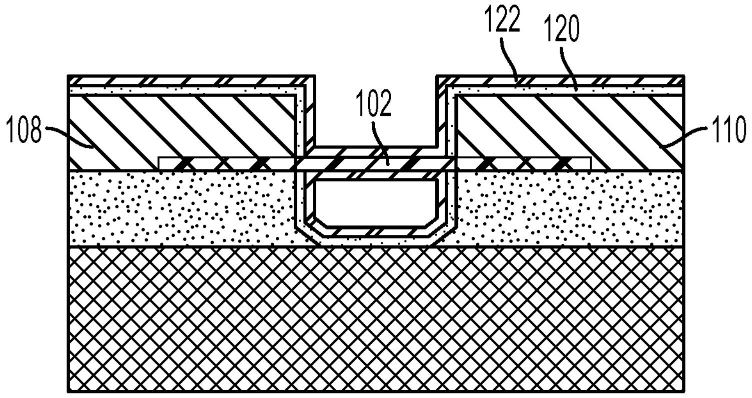


FIG. 5

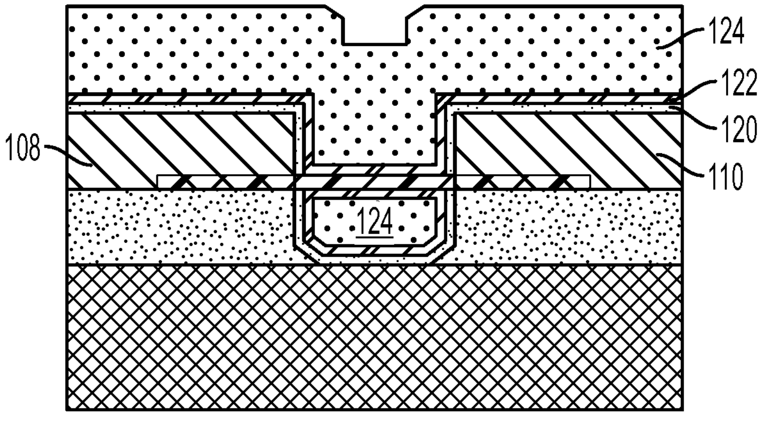


FIG. 6

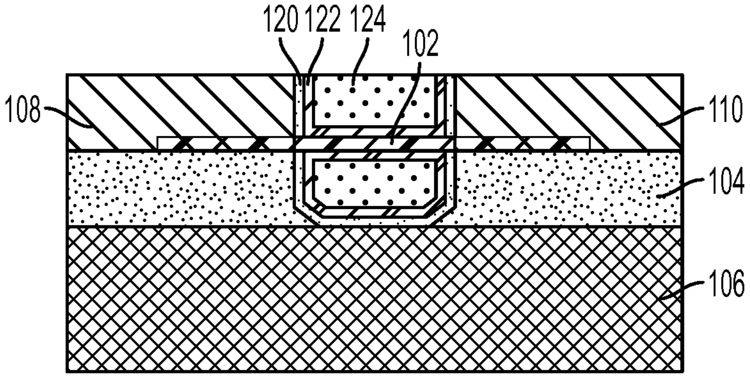


FIG. 7

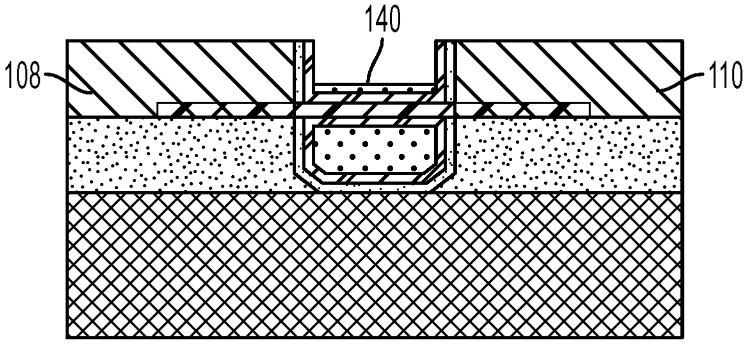


FIG. 8

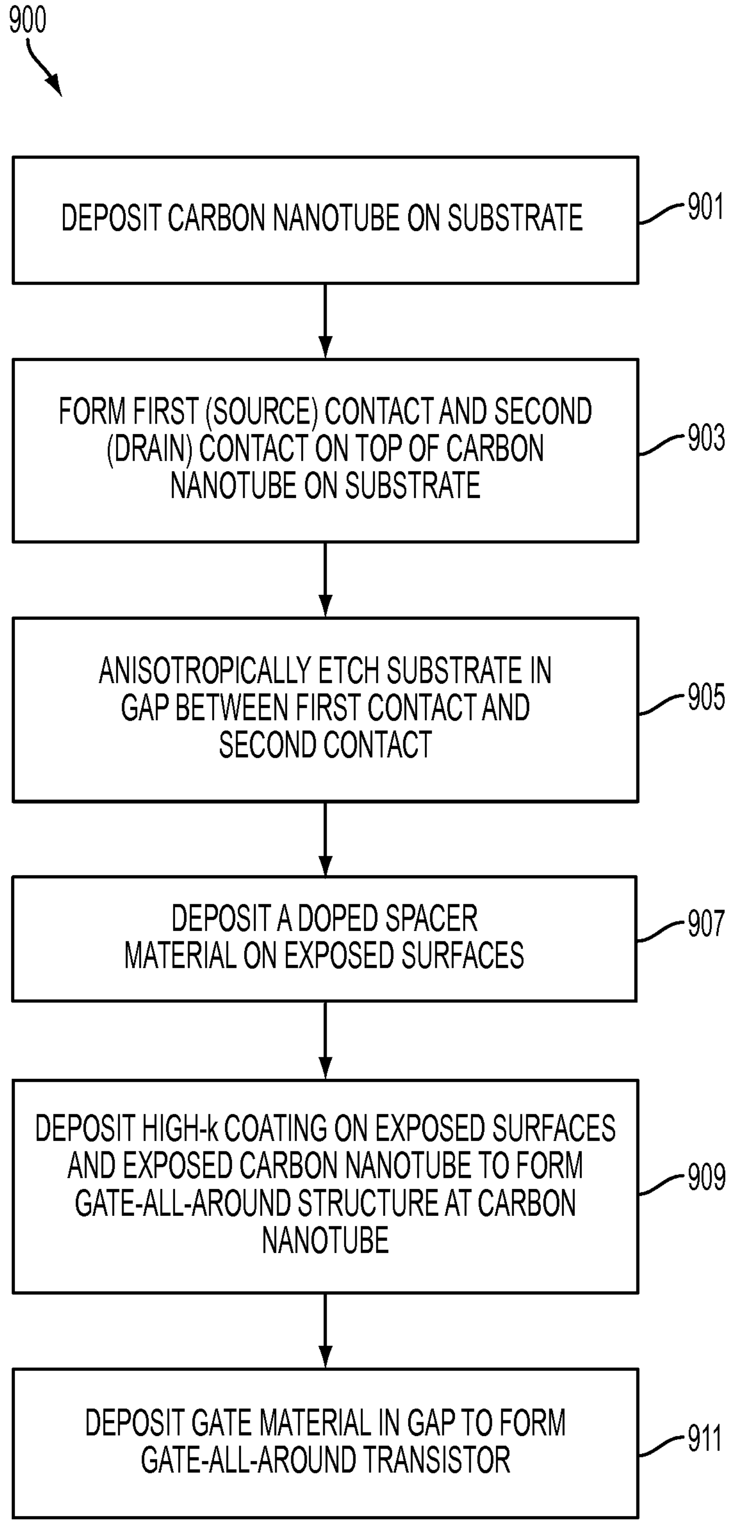
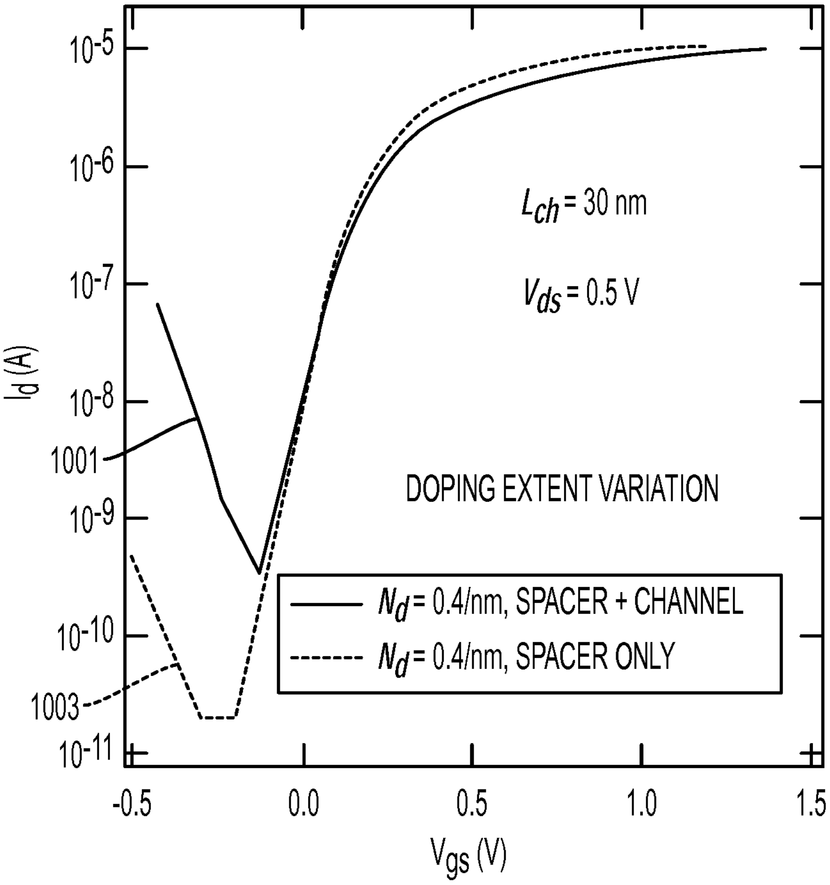

900
DEPOSIT CARBON NANOTUBE ON SUBSTRATE
901
FORM FIRST (SOURCE) CONTACT AND SECOND (DRAIN) CONTACT ON TOP OF CARBON NANOTUBE ON SUBSTRATE
903
ANISOTROPICALLY ETCH SUBSTRATE IN GAP BETWEEN FIRST CONTACT AND SECOND CONTACT
905
DEPOSIT A DOPED SPACER MATERIAL ON EXPOSED SURFACES
907
DEPOSIT HIGH-k COATING ON EXPOSED SURFACES AND EXPOSED CARBON NANOTUBE TO FORM GATE-ALL-AROUND STRUCTURE AT CARBON NANOTUBE
909
DEPOSIT GATE MATERIAL IN GAP TO FORM GATE-ALL-AROUND TRANSISTOR
911

FIG. 9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1001
1003
-0.5
0.0
0.5
1.0
1.5
V_{gs} (V)
L_{ch} = 30 nm
V_{ds} = 0.5 V
DOPING EXTENT VARIATION
N_d = 0.4/nm, SPACER + CHANNEL
N_d = 0.4/nm, SPACER ONLY

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US13/55270

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/336 (2013.01)
USPC - 438/197; 977/938
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) Classification(s): H01L 21/336, 21/84, 21/82 (2013.01)
USPC Classification(s): 438/151, 197, 299, 300; 977/842, 938

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US Granted, US Applications, EP-A, EP-B, WO, JP, DE-G, DE-A, DE-T, DE-U, GB-A, FR-A); ProQuest (Derwent, INSPEC, NTIS, PASCAL, Current Contents Search, Dissertation Abstracts Online, Inside Conferences); IP.com; IEEE.com; Google Scholar, Self aligned contact, carbon nanotube, doped recess, anisotropic etch, all around gate, hafnium oxide

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7,646,045 B2 (KREUPL, F. et al.) January 12, 2010; Figures 1 and 2F, column 6, lines 38-column 7, line 22.	1-40
A	US 2009/0149012 A1 (BRASK, J. et al.) June 11, 2009; Entire Document.	1-40
A	US 2012/0298949 A1 (CHANG, J. et al.) November 29, 2012; Entire document.	1-40
P, X	FRANKLIN, A. et al. Scalable and Fully Self-Aligned n-Type Carbon Nanotube Transistors with Gate-All-Around. In: 2012 IEEE International Electron Devices Meeting. San Francisco, CA, IEEE, December 10, 2012. ISBN: 978-1-4673-4872-0. <DOI: 10.1109/IEDM.2012.6478979>. Pages 4.5.1-4.5.4.	1-40

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search
16 December 17 2013 (16.12.2013)

Date of mailing of the international search report
22 JAN 2014

Name and mailing address of the ISA/US
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450
Facsimile No. 571-273-3201

Authorized officer:
Shane Thomas
PCT Helpdesk: 571-272-4300
PCT OSP: 571-272-7774