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(71) Applicant: **VISHAY-SILICONIX** [US/US]; 2201 Laurelwood Road, Santa Clara, CA 95054 (US).

(72) Inventors: **PARK, Chanho**; 20 Descanso Drive, Unit 1432, San Jose, CA 95134 (US). **SHIBIB, Ayman**; 1462 Puebla Court, San Jose, CA 95118 (US). **TERRIL, Kyle**; 3385 Londonderry Drive, Santa Clara, CA 95050 (US).

(74) Agent: **ZARBIS, William A.**; Murabito Hao & Barnes LLP, 2 N Market St., 3rd Floor, San Jose, CA 95113 (US).

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(54) Title: SEMICONDUCTOR DEVICE WITH NON-UNIFORM TRENCH OXIDE LAYER

(57) Abstract: A semiconductor device includes a trench formed in an epitaxial layer and an oxide layer that lines the sidewalls of the trench. The thickness of the oxide layer is non-uniform, so that the thickness of the oxide layer toward the top of the trench is thinner than it is toward the bottom of the trench. The epitaxial layer can have a non-uniform dopant concentration, where the dopant concentration varies according to the thickness of the oxide layer.

Fig. 2

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SEMICONDUCTOR DEVICE WITH NON-UNIFORM TRENCH OXIDE LAYER

BACKGROUND

Breakdown voltage provides an indication of the ability of a semiconductor device (e.g., a metal oxide semiconductor field effect transistor (MOSFET) device) to withstand breakdown under reverse voltage conditions. To realize an energy efficient power conversion system, power MOSFETs (e.g., MOSFETs designed to handle medium to high voltage levels) should have low conduction losses. Conduction losses can be lowered by reducing RDS(on), the on-state resistance between the drain and the source. However, reducing RDS(on) adversely affects breakdown voltage.

The drift region in a MOSFET is a relatively high resistivity layer grown by epitaxial (epi) technology, and is designed to achieve particular values for electrical characteristics such as breakdown voltage and on-state resistance. For medium voltage (e.g., 100 V) to high voltage (e.g., 600 V) devices, the major portion of the on-state resistance comes from drift region resistance. For example, for a 200 V device, an analysis shows that 88 percent of the total on-state resistance is due to drift region resistance, while only six percent is due to channel resistance, five percent is due to package resistance, and one percent is due to substrate resistance. Consequently, reducing drift region resistance can make a significant contribution to reducing the total on-state resistance.

However, while a reduction in resistivity in the drift region of the epitaxial layer can positively affect RDS(on), conventionally such a reduction means that breakdown voltage would be expected to be negatively affected as noted above.

Accordingly, a semiconductor device (e.g., MOSFET) that provides reduced resistivity in the drift region and hence lower on-state resistance, but does not negatively impact breakdown voltage, would be valuable.

SUMMARY

In overview, embodiments according to the present invention pertain to semiconductor devices, such as but not limited to power MOSFETs including but not

limited to dual trench MOSFETs, that have non-uniform oxide layers lining the trenches that are connected to the source electrode. Such devices will have lower resistivity in the drift region and lower on-state resistance but will have the same or about the same breakdown voltage as conventional but otherwise comparable MOSFETs.

5

More specifically, in an embodiment, a semiconductor device includes an epitaxial layer disposed adjacent to the substrate layer and trenches formed in the epitaxial layer. An oxide layer lines the sidewalls of each of the trenches. The trenches are filled with a material such as polysilicon that is connected to a source electrode. The oxide layer has a

10 non-uniform thickness along the sidewalls of each trench. For example, the thickness of the oxide layer at a first distance from the bottom of a trench is less than the thickness of the oxide layer at the bottom, and the thickness of the oxide layer at a second distance from the bottom (greater than the first distance) is less than the thickness of the oxide layer at the first distance. Generally, in embodiments according to the invention, the oxide layer

15 is thinnest at or near the top of the trench, and is thicker toward the bottom of the trench.

In an embodiment, the epitaxial layer has a non-uniform dopant concentration. In such an embodiment, the dopant concentration varies according to the thickness of the oxide layer. More specifically, in an embodiment, the dopant concentration is higher where

20 the oxide layer is thinner and lower where the oxide layer is thicker. Thus, in the above example, the dopant concentration at the first distance is less than the dopant concentration at the second distance.

Non-uniform oxide layer thicknesses in the trenches in embodiments according to

25 the present invention provide the opportunity to improve charge balance in the drift region in the epitaxial layer by tailoring the dopant concentration in the epitaxial layer according to the thickness of the oxide layer, resulting in reduced (improved) on-state resistance at the same breakdown voltage.

30 These and other objects and advantages of embodiments according to the present invention will be recognized by one skilled in the art after having read the following detailed description, which are illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. Like numbers denote like elements throughout the drawings and specification. The figures may not be drawn to scale.

Figure 1A illustrates an example of a portion of a semiconductor device in an embodiment according to the present invention.

Figure 1B illustrates an example of a portion of a semiconductor device in an embodiment according to the present invention.

Figure 2 illustrates an example of a portion of a semiconductor device in an embodiment according to the present invention.

Figure 3 illustrates an example of a portion of a semiconductor device in an embodiment according to the present invention.

Figure 4 illustrates an example of a portion of a semiconductor device in an embodiment according to the present invention.

Figure 5 is a flowchart of an example of operations for fabricating a semiconductor device in an embodiment according to the present invention.

Figures 6, 7, 8, 9, 10, 11, 12, and 13 illustrate a portion of a semiconductor device at various stages of a fabrication process in an embodiment according to the present invention.

DETAILED DESCRIPTION

In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one skilled in the art that the present invention may be

practiced without these specific details or with equivalents thereof. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

5 Some portions of the detailed descriptions that follow are presented in terms of procedures, logic blocks, processing, and other symbolic representations of operations for fabricating semiconductor devices. These descriptions and representations are the means used by those skilled in the art of semiconductor device fabrication to most effectively convey the substance of their work to others skilled in the art. In the present application, a
10 procedure, logic block, process, or the like, is conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise
15 as apparent from the following discussions, it is appreciated that throughout the present application, discussions utilizing terms such as “forming,” “performing,” “producing,” “depositing,” “etching,” “adding,” “removing” or the like, refer to actions and processes (e.g., process 500 of Figure 5) of semiconductor device fabrication.

20 It is understood that the figures are not necessarily drawn to scale, and only portions of the devices and structures depicted, as well as the various layers that form those structures, are shown. For simplicity of discussion and illustration, the process is described for one or two devices or structures, although in actuality more than one or two devices or structures may be formed.

25

The term “channel” is used herein in the accepted manner. That is, current moves within a MOSFET in a channel, from the source connection to the drain connection. A channel can be made of either n-type or p-type semiconductor material; accordingly, a MOSFET is specified as either an n-channel or p-channel device. The disclosure is
30 presented in the context of an n-channel device; however, embodiments according to the present invention are not so limited. That is, the features described herein can be utilized in a p-channel device. The disclosure can be readily mapped to a p-channel device by

substituting, in the discussion, n-type dopant and materials for corresponding p-type dopant and materials, and vice versa.

As used herein, the letter "n" refers to an n-type dopant and the letter "p" refers to a p-type dopant. A plus sign "+" or a minus sign "-" is used to represent, respectively, a relatively high or relatively low concentration of the dopant. For example, "n+" would indicate a higher concentration of n-type dopant than "n," which would indicate a higher concentration of n-type dopant than "n-."

In general, the term "trench" is used in the art to refer to an empty trench that is formed in, for example, an epitaxial (epi) layer, and is also often used to refer to a trench that is partially or completely filled with one or more materials. The term "trench structure" may be used herein at times to distinguish a filled or partially filled trench from an empty or unfilled trench. At other times, the manner in which these terms are being used will be evident from the context of the surrounding discussion.

Figure 1A is an example of a cross-sectional view of a portion of a semiconductor device 100 in an embodiment according to the present invention. In the example of Figure 1A, the device 100 includes an epitaxial layer 15 (e.g., an n-type epitaxial layer) formed over and adjacent to a substrate layer 5. The device 100 also includes a first trench structure 31 formed in a first trench 30 that is formed in the epitaxial layer 15, and also includes a second trench structure 33 formed in a second trench 32 formed in the epitaxial layer.

In embodiments according to the present invention, the trench 30 is lined with an oxide layer 21, and the trench 32 is lined with an oxide layer 22. The oxide layers 21 and 22 may be referred to as shield oxides. The oxide layer 21 lines the bottom and sidewalls of the trench 30, and the oxide layer 22 lines the bottom and sidewalls of the trench 32.

In the Figure 1A embodiment, the volumes within the oxide layers 21 and 22 are filled with material to form the trench structures 31 and 33, respectively. In an embodiment, the material is a polysilicon material. In an embodiment, the material in the

trench structures 31 and 33 is connected to a source electrode 81. Accordingly, the trench structures 31 and 33 may be referred to as source trenches.

Significantly, in embodiments according to the present invention, the oxide layers 21 and 22 have non-uniform thicknesses along the sidewalls of the trenches 30 and 32. For example, in the Figure 1A embodiment, the thickness x1 of the oxide layer 21 at a first distance d1 from the bottom of the trench structure 31 is less than the thickness of the oxide layer at the bottom, and the thickness x2 of the oxide layer at a second distance d2 from the bottom (the second distance greater than the first distance) is less than the thickness of the oxide layer at the first distance. The thickness of the oxide layer 22 can be similarly described.

In the Figure 1A embodiment, the oxide layers 21 and 22 get thinner as a function of distance from the bottoms of the trenches 30 and 32. In other words, in the Figure 1A embodiment, the thickness of the oxide layer 21 is not constant or uniform between the distance d1 and the distance d2 or from d2 to the top of the trench 30. The thickness of the oxide layer 22 can be similarly described.

In an embodiment, the thickness of the oxide layer 21 decreases linearly between the distances d1 and d2. That is, the thickness of the oxide layer 21 can essentially be represented using a straight line drawn from d1 to d2. The thickness of the oxide layer 21 can continue to decrease linearly beyond the distance d2 as shown in the example of Figure 1A. The thickness of the oxide layer 22 can be similarly described.

However, the thicknesses of the oxide layers do not necessarily have to decrease linearly as the distance from the bottom of the trench increases. The oxide layers can have different profiles (cross-sections). In general, the oxide layers are thinnest at or near the top of a trench, and are thicker toward the bottom of the trench.

In the example of Figure 1A, a structure or device is formed between (adjacent to) the trench structures 31 and 33. In an embodiment, the structure/device includes a trench 51 filled with material (e.g., oxide and polysilicon), body regions 61 and 62 (e.g., p-type

body regions), and source regions 71 and 72 (e.g., n-type source regions). In an embodiment, the material in the trench 51 is shielded (insulated) from the source electrode 81 by a dielectric region 41. While a particular type of structure/device between the trench structures 31 and 33 is shown in Figure 1A and in other figures below (e.g., Figures 1B, 2,
5 and 3), embodiments according to the present invention are not so limited. For example, the structure/device may be a type of Schottky device or insulated-gate bipolar transistor (IGBT) instead of the type of structure/device shown in the figures.

In embodiments according to the present invention, the design of the epitaxial layer
10 15 can be tailored to complement the non-uniform thicknesses of the oxide layers 21 and 22. More specifically, the epitaxial layer 15 can have a non-uniform dopant concentration, where the dopant concentration varies according to the thickness of the oxide layers. Thus, non-uniform oxide layer thicknesses in the trenches in embodiments according to the present invention provide the opportunity to tune the dopant concentration and improve
15 charge balance in the drift region (the region in the epitaxial layer between the trench structures 31 and 33 and under the body regions 61 and 62), in order to reduce resistivity in the drift region and thereby reduce (and improve) the total on-state resistance. Importantly, in embodiments according to the present invention, on-state resistance can be reduced without affecting breakdown voltage.

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Figure 1B is an example of a cross-sectional view of a portion of a semiconductor device 150 in an embodiment according to the present invention, in which the dopant concentration varies according to the thickness of the oxide layers. In the example of Figure 1B, the epitaxial layer 15 includes three sub-layers or regions 10, 11, and 12. In an
25 embodiment, each of the sub-layers 10, 11, and 12 extend across the entire distance between the adjacent trench structures 31 and 33.

In the example of Figure 1B, the region 10 corresponds to (neighbors, or is adjacent to) the bottom portions of the trench structures 31 and 33, the region 11 corresponds to the
30 distance d1, and the region 12 corresponds to the distance d2. The term “corresponds to,” as used above and hereinafter, means that the region 10 overlaps the bottom of the trench structures 31 and 33, the region 11 overlaps portions of the oxide layers 21 and 22 that

have a thickness that is greater than the thickness x2, and that the region 12 overlaps portions of the oxide layers 21 and 22 that have a thickness that is less than the thickness x1.

5 In the example of Figure 1B, the dopant concentration (e.g., n-) in the region 10 is less than the dopant concentration (e.g., n) in the region 11, and the dopant concentration in the region 11 is less than the dopant concentration (e.g., n+) in the region 12. However, embodiments according to the invention are not so limited. That is, the dopant concentration does not necessarily have to decrease with depth as just described. In 10 general, the dopant concentration is higher where the oxide layer is thinner, and lower where the oxide layer is thicker. Thus, the relative dopant concentrations in different regions of the epitaxial layer 15 can be less than, equal to, or greater than one another depending on the corresponding thickness of the oxide layers 21 and 22. While three dopant concentration levels/regions are described in Figure 1B and in other figures below 15 (e.g., Figures 2 and 3), the present invention is not so limited; there can be more or less than three dopant concentration levels/regions.

According to an analysis of a conventional device versus the device 150, the conventional device has a breakdown voltage of 220 V and an on-state resistance of 12.5 20 micro-ohms (mΩ), while the device 150 has a breakdown voltage of 220 V and an on-state resistance of 9.7 mΩ. Thus, embodiments according to the invention can improve on-state resistance by 22 percent with the same breakdown voltage relative to a conventional device.

25 Figure 2 is an example of a cross-sectional view of a portion of a semiconductor device 200 in an embodiment according to the present invention. In the example of Figure 2, the oxide layers 23 and 24 are stepped. More specifically, for example, the oxide layer 23 has a uniform first thickness x1 from a point A that is above the bottom of the trench structure 31 to a first distance d1, a uniform second thickness x2 from the distance d1 to a 30 second distance d2, a uniform third thickness x3 from the distance d2 to a third distance d3, and a uniform fourth thickness x4 from the distance d3 to the top surface of the trench structure 31, where x1 is greater than x2, which is greater than x3, which is greater than

x4. There can be more or less than the number of steps shown in Figure 2. The distances d1, d2, d3, and d4 may or may not be equal. The thickness of the oxide layer 24 can be similarly described.

5 Like the example of Figure 1B, the device 200 can have non-uniform dopant concentrations in the epitaxial layer as shown in Figure 2.

Features of the devices of Figures 1A, 1B, and 2 can be combined. Specifically, with reference to Figure 2, one, some or all of the uniformly thick portions of the oxide
10 layers 23 and 24 can instead be decreasing (e.g., decreasing linearly) with distance from the bottom of the trench structure 31. For example, the thickness of the portion of the oxide layer 23 across the length of the distance d1 can decrease as distance from the bottom increases; for example, the thickness in that portion can decrease linearly from x1 to x2 across the distance d1. Similarly, the thickness of each of the other portions of the
15 oxide layer 23 either can be uniform or can decrease (e.g., decrease linearly) as the distance from the bottom increases. The thickness of the oxide layer 24 can be similarly described.

Also, the rate of change (e.g., the slope) of one portion can be different from that of
20 another portion. For example, the thickness of the oxide layer 23 may decrease across the distance d2, and also may decrease linearly across the distance d3, but the rate at which the thickness decreases across d2 may be different than the rate at which the thickness decreases across d3.

25 Figure 3 is an example of a cross-sectional view of a portion of a semiconductor device 300 in an embodiment according to the present invention. In the example of Figure 3, there is only a single step. More specifically, for example, the oxide layer 25 has a uniform first thickness x1 from a point A that is above the bottom of the trench structure 31 to a first distance d1, and a uniform second thickness x2 from d1 to a second distance d2,
30 where x1 is greater than x2. The thickness of the oxide layer 26 can be similarly described.

Like the examples above, the device 300 can have non-uniform dopant concentration in the epitaxial layer as shown in Figure 3. Also, features described above can be combined with the features of the device 300. Specifically, one or both of the uniformly thick portions of the oxide layers 25 and 26 can instead be decreasing (e.g.,
5 linearly decreasing) with distance from the bottom of the trench structure 31. For example, the thickness of the portion of the oxide layer 25 along the length of the distance d1 can decrease as the distance from the bottom increases; for example, the thickness in that portion can decrease linearly from x1 to x2 across the distance d1. The thickness of the oxide layer 26 can be similarly described.

10

Thus, in general and with reference to Figure 4, an oxide layer lines the bottom and the first and second sidewalls of the trench 30. The oxide layer, in essence, includes at least: a first portion 42 that spans the bottom of the trench 30 from one sidewall to the other; a second portion 43 that extends from the boundary of the first portion along a
15 sidewall up to a certain height; and a third portion 44 that extends from the boundary of the second portion along the sidewall. The oxide layer has a first thickness (e.g., x1) in the second portion 43 and a second thickness (e.g., x2) in the third portion 44, where the second thickness is less than the first thickness. The first thickness x1 does not necessarily extend along the entire length of the second portion 43; that is, the thickness of
20 the second portion 43 is not necessarily uniform, but can decrease as distance from the bottom of the trench 30 increases. The second thickness x2 can be similarly described.

Furthermore, in an embodiment, the epitaxial layer includes a first region 10 neighboring the first portion 42 of the oxide layer, a second region 11 neighboring the
25 second portion 43 of the oxide layer, and a third region 12 neighboring the third portion 44 of the oxide layer. In an embodiment, the first region 10 has a first dopant concentration, the second region 11 has a second dopant concentration, and the third region 12 has a third dopant concentration. In one such embodiment, the third dopant concentration (e.g., n+) is greater than the second dopant concentration (e.g., n), and the second dopant
30 concentration is greater than the first dopant concentration (e.g., n-).

Figure 5 is a flowchart 500 of a method for fabricating a device in an embodiment according to the present invention. Operations described as separate blocks may be combined and performed in the same process step (that is, in the same time interval, after the preceding process step and before the next process step). Also, the operations may be performed in a different order than the order in which they are described below. Furthermore, fabrication processes and steps may be performed along with the processes and steps discussed herein; that is, there may be a number of process steps before, in between, and/or after the steps shown and described herein. Importantly, embodiments according to the present invention can be implemented in conjunction with these other (perhaps conventional) processes and steps without significantly perturbing them. Generally speaking, embodiments according to the present invention can replace portions of a conventional process without significantly affecting peripheral processes and steps. Also, Figure 5 is discussed in the context of a single trench and trench structure; however, multiple trenches and trench structures can be fabricated in parallel.

In block 502 of Figure 5, and with reference to Figure 6, a trench 30 is etched in an epitaxial layer 15 that was formed over a substrate 5. In an embodiment, the trench 30 is etched through an oxide hard mask or some other masking material like silicon nitride or photoresist. The masking material is then removed.

In block 504 of Figure 5, with reference to Figure 7, an oxide layer 75 is deposited or grown across the bottom and along the sidewalls of the trench 30 and also over the upper surface of the epitaxial layer 15. The thickness of the oxide layer 75 is determined by the required breakdown voltage ratings. For example, the thickness of the oxide layer 75 is about 0.7 micrometers (μm) for a device rated at 200 V. In an embodiment, the oxide layer 75 has a uniform thickness along the sidewalls of the trench 30 as shown in the example of Figure 7. In another embodiment, the oxide layer 75 has a non-uniform thickness; that is, the thickness of the oxide layer is thicker toward the bottom of the trench 30 and gets thinner as the distance from the bottom of the trench increases. In the latter embodiment, the thickness of the oxide layer 75 decreases linearly as the distance from the bottom of the trench 30 increases.

In block 506 of Figure 5, with reference to Figure 8, the trench 30 is filled to a specified depth with a material 85 such as doped polysilicon. In an embodiment, the material 85 is deposited past the specified depth, and then etched back to the specified depth. Instead of depositing doped polysilicon, polysilicon can be deposited and then doped by a well-known method using $POCl_3$ (phosphorus oxychloride) or phosphorus implantation and drive-in.

In block 508 of Figure 5, with reference to Figure 9, the oxide layer 75 is etched back to a specified depth (e.g., the distance d1, measured from the bottom of the trench 30). In essence, the material 85 masks the lower portion 91 of the oxide layer 75, so that the lower portion of the oxide layer is not etched back. In an embodiment, only some of the oxide layer 75 is removed in the upper portion 92. As a result, the thickness x2 of the upper portion 92 of the oxide layer 75 is less than the thickness x1 of the lower portion 91 of the oxide layer.

In block 510 of Figure 5, with reference to Figure 10, the operations of blocks 506 and/or 508 are repeated to achieve a desired profile for the oxide layer 75.

More specifically, some or all of the remaining volume of the trench 30 is filled with the same material 85 that was deposited in block 506 above. If only some of the remaining volume is filled similar to the operation of block 506 above, the exposed portion of the oxide layer 75 can be etched back again to further thin that portion of the oxide layer, similar to the operation of block 508.

In general, before the trench 30 is completely filled with the material 85, the operations of blocks 506 and 508 can be repeated as many times as necessary to achieve a desired profile (cross-section) for the oxide layer 75. For example, the operations of blocks 506 and 508 can be performed three times to achieve the profile in the example of Figure 2. If only a single step in the thickness of the oxide layer 75 is to be formed (e.g., as in the example of Figure 3), then the remaining volume of the trench 30 is filled after the oxide layer is etched back a single time in block 508.

Once the trench 30 is completely filled, excess material can be removed using, for example, CMP (chemical mechanical planarization or polishing) so that the top surface of material in the trench 30 (the filler material 85 and the oxide layer 75) is flush with adjacent surfaces.

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In block 512 of Figure 5, with reference to Figure 11, in an embodiment, dopant is added to the epitaxial layer 15 in one or more process steps, to increase the concentration of dopant in some regions of the epitaxial layer relative to other regions of the epitaxial layer, as described above. For example, in an embodiment, additional dopant can be
10 driven into the regions of the epitaxial layer 15 corresponding to the regions 11 and 12, to increase their dopant concentration relative to the region 10. Then, additional dopant can again be driven into the region 12, to increase its dopant concentration relative to the region 11.

15 However, embodiments according to the invention are not limited to the example of Figure 11. In general, as previously described herein, dopant is added to the epitaxial layer 15 to produce a non-uniform concentration of dopant in the epitaxial layer, where the concentration varies according to the thickness of the oxide layer 75. More specifically, the dopant concentration may be higher in a region of the epitaxial layer 15 adjacent to a
20 thinner portion of the oxide layer 75, and the dopant concentration may be lower in a region of the epitaxial layer adjacent to a thicker portion of the oxide layer.

Also, the various dopant concentrations in the epitaxial layer 15 can be introduced at any point before, after, or while the other operations included in the flowchart 500 are
25 performed. For example, the epitaxial layer 15 can be doped before the trench 30 is etched; that is, the trench can be etched in an epitaxial layer that has already been doped.

In block 514 of Figure 5, with reference to Figure 12, a device or structure is formed in the region 120 adjacent to the trench 30. In an embodiment, a second trench 51 (e.g., a
30 gate trench) that is shallower than the trench 30 is formed, an oxide layer (not shown) is grown inside the second trench, a material (e.g., polysilicon) is added inside the second

trench, excess material is removed using CMP for example, the body regions 61 and 62 are formed, and the source regions 71 and 72 are formed.

In block 516 of Figure 5, with reference to Figure 13, openings to the source regions
5 71 and 72 are formed, a dielectric region 41 is formed over the trench structure that includes the trench 51, and a metal layer is deposited to form the source electrode 81 in contact with the material 85 in the source trenches as well as the body regions 61 and 62 and the source regions 71 and 72.

10 Embodiments of semiconductor devices and of methods of fabricating the semiconductor devices are thus described. In these embodiments, semiconductor devices, such as but not limited to power MOSFETs including but not limited to dual trench MOSFETs, have non-uniform oxide layers lining the trenches that are connected to the source electrode. Such devices will have lower resistivity in the drift region and lower on-
15 state resistance but will have the same or about the same breakdown voltage relative to conventional devices.

The features described herein can be used in lower voltage devices (e.g., in the range of 100-250 V) as well as higher voltage devices (e.g., in the range of 400-600 V).
20

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications and variations are possible in light of the above teaching. The embodiments were chosen
25 and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

30

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

5 a substrate layer;

an epitaxial layer adjacent to the substrate layer;

a first trench structure formed in the epitaxial layer and having a bottom and sidewalls, wherein the first trench structure further comprises filler material in contact with a source electrode; and

10 an oxide layer that lines the sidewalls, the oxide layer having a non-uniform thickness along the sidewalls, wherein the thickness of the oxide layer at a first distance from the bottom is less than the thickness of the oxide layer at the bottom, and wherein the thickness of the oxide layer at a second distance from the bottom, greater than the first distance, is less than the thickness of the oxide layer at the first distance.

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2. The semiconductor device of Claim 1, wherein the epitaxial layer has a non-uniform dopant concentration, wherein the non-uniform dopant concentration varies according to the thickness of the oxide layer adjacent thereto.

20 3. The semiconductor device of Claim 1, wherein a region of the epitaxial layer at a depth corresponding to the first distance has a first dopant concentration, and a region of the epitaxial layer at a depth corresponding to the second distance has a second dopant concentration.

25 4. The semiconductor device of Claim 3, wherein the first dopant concentration is less than the second dopant concentration.

5. The semiconductor device of Claim 1, wherein the thickness of the oxide layer deceases linearly along a length of the sidewalls between the first distance and the second

30 distance.

6. The semiconductor device of Claim 1, wherein the oxide layer has a uniform first thickness from above the bottom of the first trench structure to the first distance, and has a uniform second thickness from the first distance to the second distance, the second thickness less than the first thickness.

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7. The semiconductor device of Claim 1, further comprising a structure formed adjacent to the first trench structure, the structure comprising: a second trench filled with material, a body region, and a source region.

10 8. A semiconductor device, comprising:

a substrate layer;

an epitaxial layer adjacent to the substrate layer;

a first trench structure formed in the epitaxial layer, the first trench structure having a bottom, a first sidewall, and a second sidewall, wherein the first trench structure further

15 comprises filler material in contact with a source electrode; and

an oxide layer that lines the bottom and the first and second sidewalls, the oxide layer comprising a first portion that spans the bottom of the first trench structure from the first sidewall to the second sidewall, a second portion extending from the first portion along the first sidewall, and a third portion extending from the second portion along the first

20 sidewall, wherein the oxide layer has a first thickness in the second portion and a second thickness in the third portion, the second thickness less than the first thickness.

9. The semiconductor device of Claim 8, wherein the epitaxial layer comprises a first region neighboring the first portion of the oxide layer, a second region neighboring the

25 second portion of the oxide layer, and a third region neighboring the third portion of the oxide layer, wherein the first region has a first dopant concentration, the second region has a second dopant concentration, and the third region has a third dopant concentration.

10. The semiconductor device of Claim 9, wherein the third dopant concentration is

30 greater than the second dopant concentration, and the second dopant concentration is greater than the first dopant concentration.

11. The semiconductor device of Claim 8, wherein the first thickness decreases linearly as distance from the bottom increases, and wherein the second thickness decreases linearly as distance from the bottom increases.

5 12. The semiconductor device of Claim 8, wherein the first thickness is uniform in the second portion of the oxide layer, and wherein the second thickness is uniform in the third portion of the oxide layer, the second thickness less than the first thickness.

13. The semiconductor device of Claim 8, further comprising a structure formed 10 adjacent to the first trench structure, the structure comprising: a second trench filled with material, a body region, and a source region.

14. A method of forming a semiconductor device, the method comprising:

forming a first trench in an epitaxial layer, the first trench having a bottom and 15 sidewalls;

depositing an oxide layer across the bottom and on the sidewalls of the first trench;

depositing material within the first trench to cover a first portion of the oxide layer and leaving a second portion of the oxide layer exposed;

removing some of the oxide layer in the second portion, wherein after said removing 20 the second portion of the oxide layer has a thickness that is less than a thickness of the first portion of the oxide layer;

depositing the material in the first trench to cover the second portion of the oxide layer; and

forming a source electrode in contact with the material in the first trench.

25

15. The method of Claim 14, further comprising adding dopant to the epitaxial layer to produce a non-uniform concentration of the dopant in the epitaxial layer, wherein the non-uniform concentration of the dopant in the epitaxial layer varies according to the thickness of the oxide layer adjacent thereto.

30

16. The method of Claim 14, further comprising:

adding dopant to a first region of the epitaxial layer at a depth corresponding to the first portion of the oxide layer to produce a first dopant concentration in the first region; and

adding the dopant to a second region of the epitaxial layer at a depth corresponding to the second portion of the oxide layer to produce a second dopant concentration in the
5 second region.

17. The method of Claim 16, wherein the first dopant concentration is less than the second dopant concentration.

10 18. The method of Claim 14, wherein the thickness of the oxide layer deceases linearly through the first portion of the oxide layer and decreases linearly through the second portion of the oxide layer.

19. The method of Claim 14, wherein the first portion of the oxide layer has a
15 uniform first thickness, and wherein the second portion of the oxide layer has a uniform second thickness, the second thickness less than the first thickness.

20. The method of Claim 14, further comprising forming a structure adjacent to the first trench, the structure comprising: a second trench filled with material, a body region,
20 and a source region.

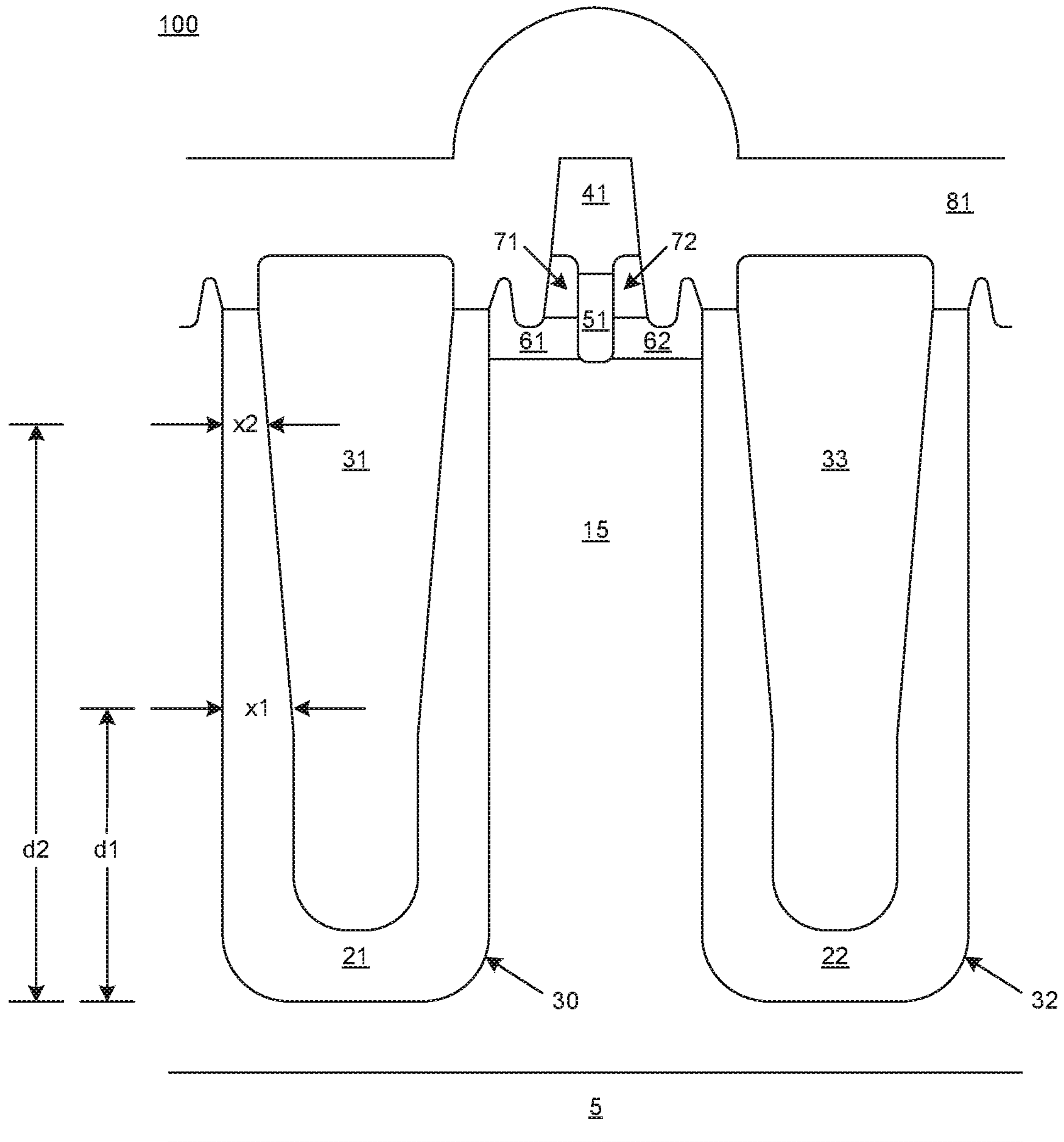

Fig. 1A

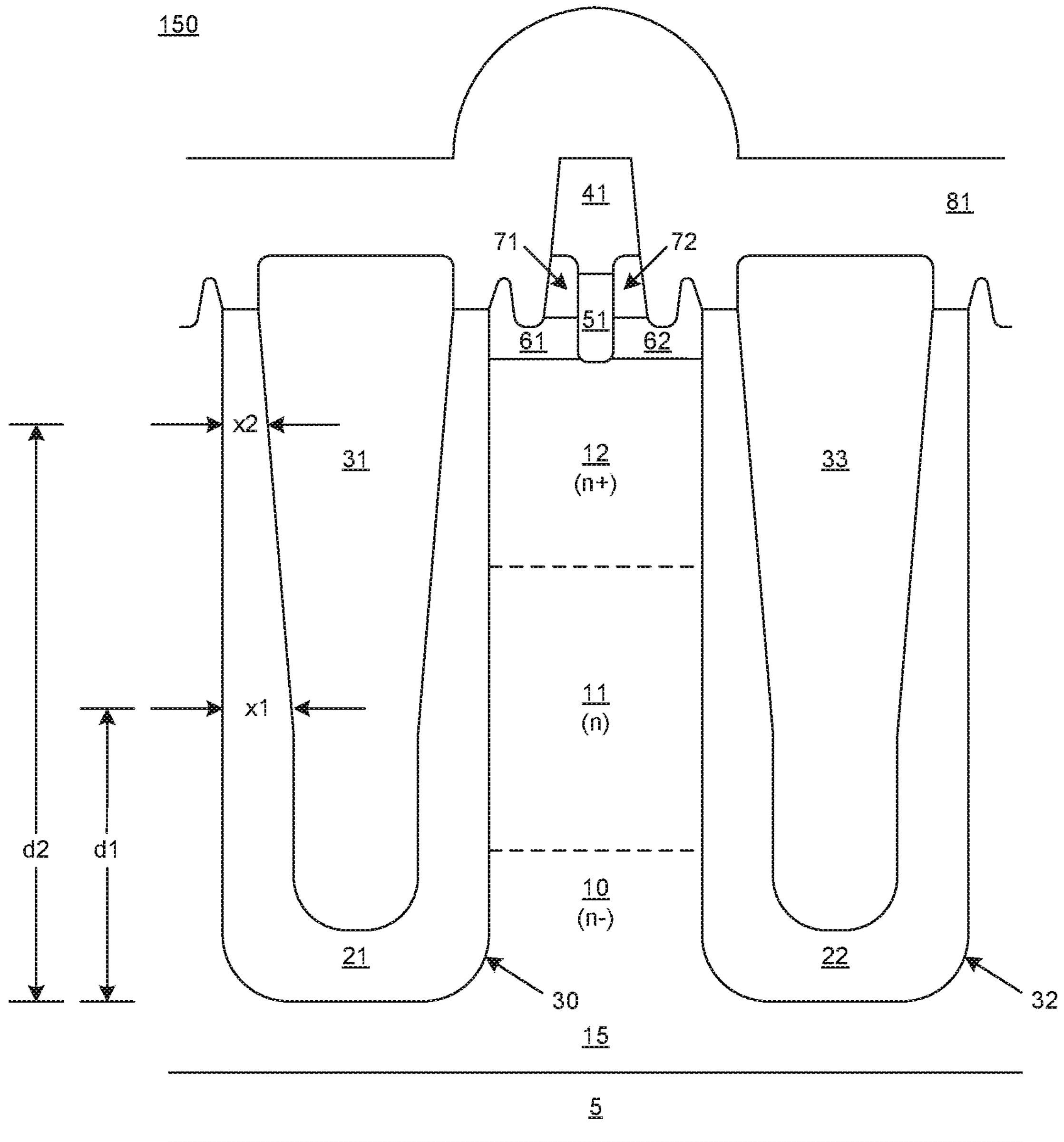

Fig. 1B

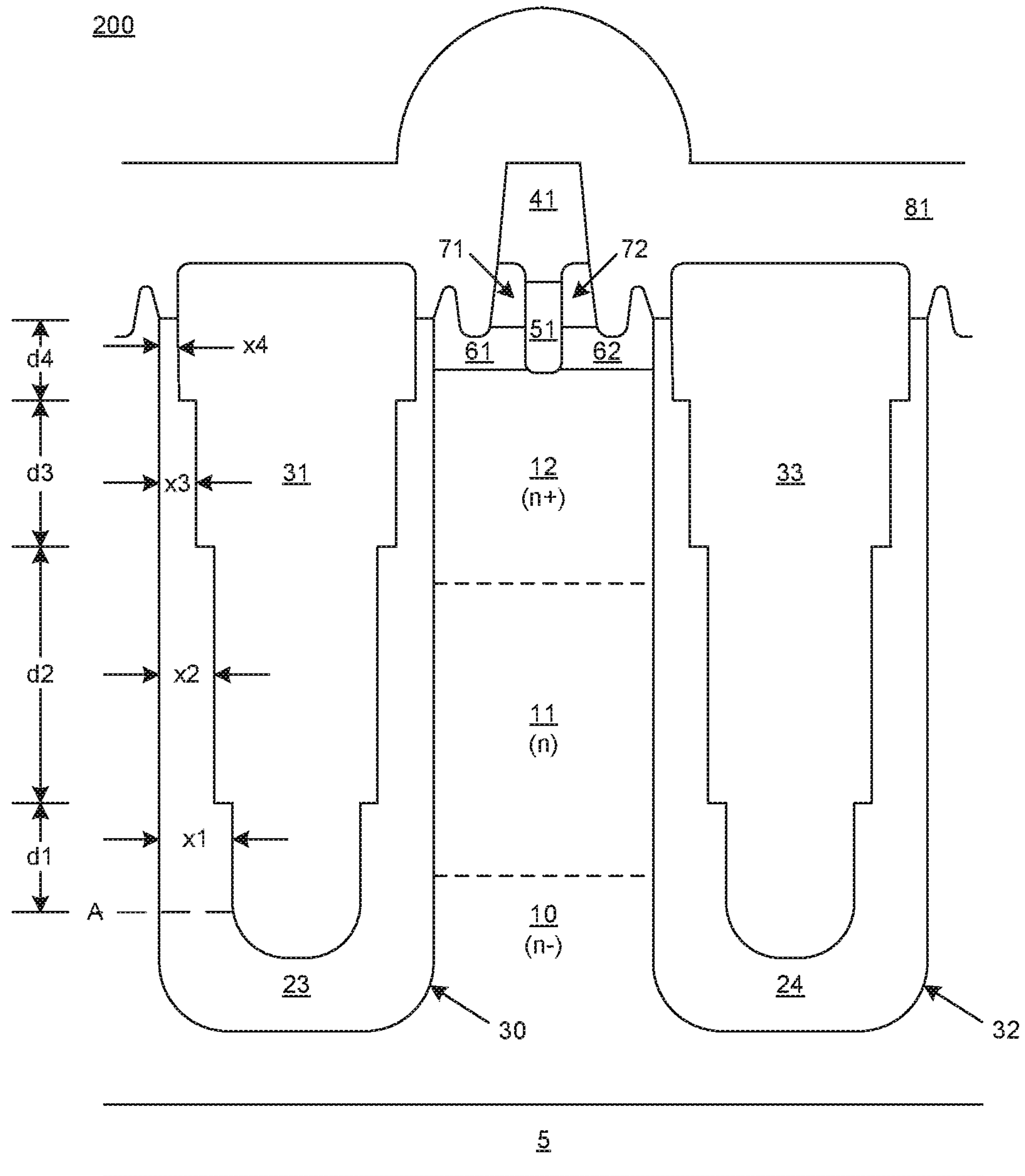

Fig. 2

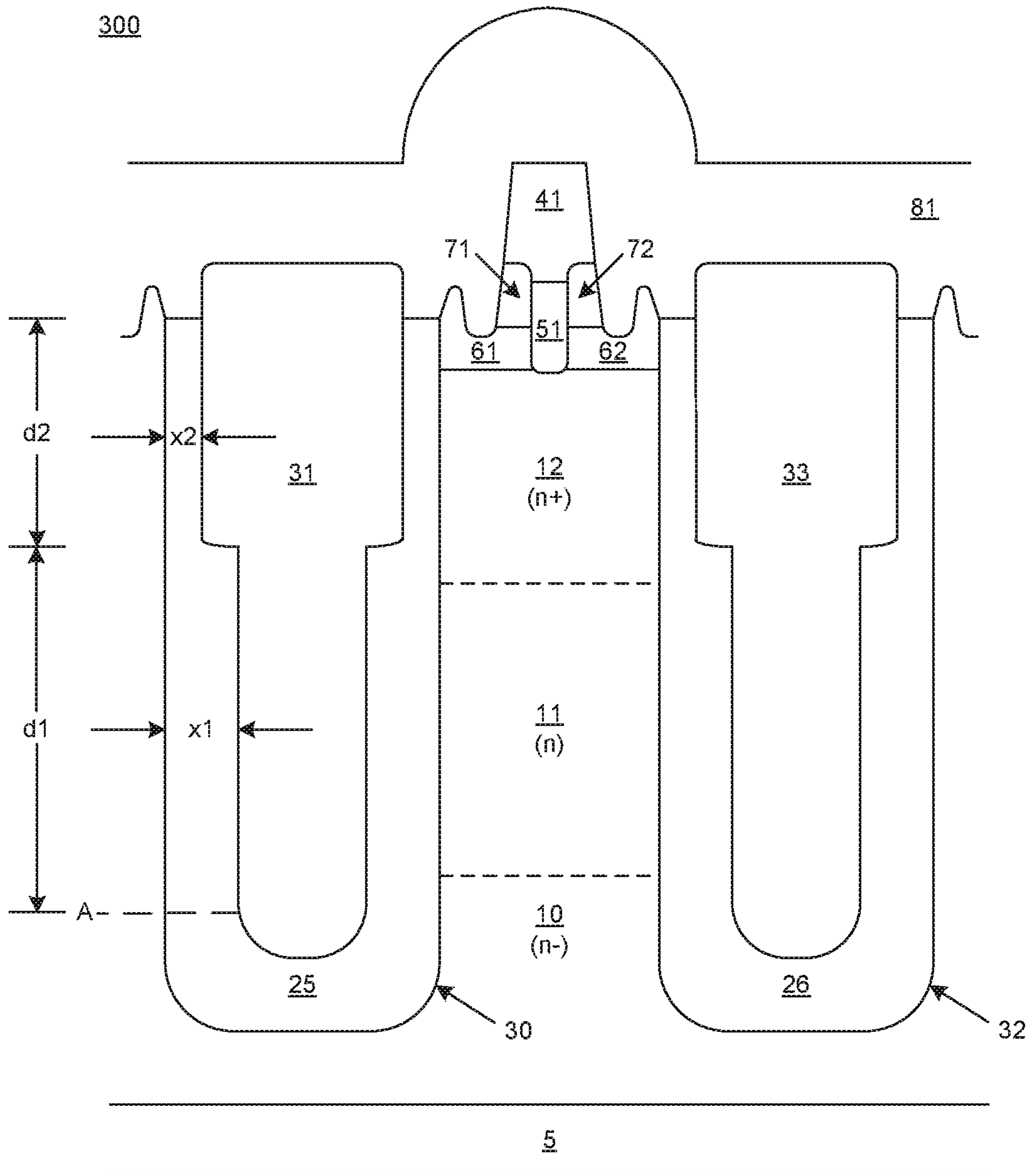

Fig. 3

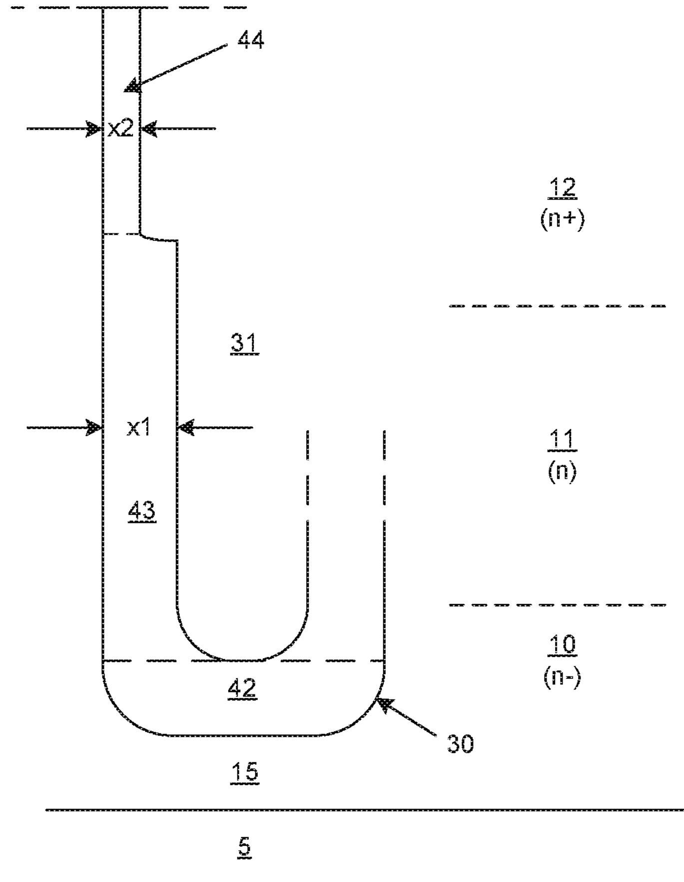

Fig. 4

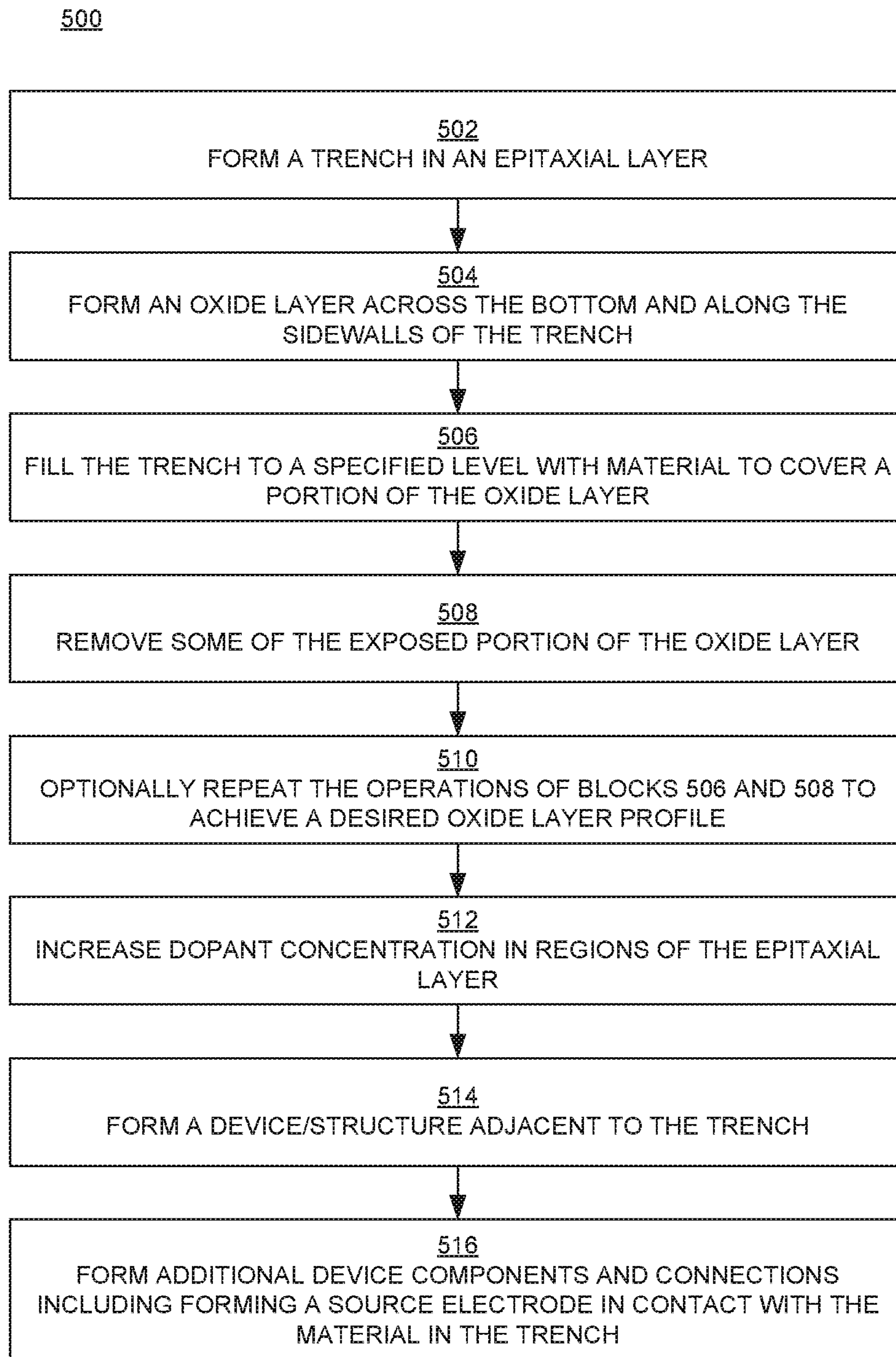

Fig. 5

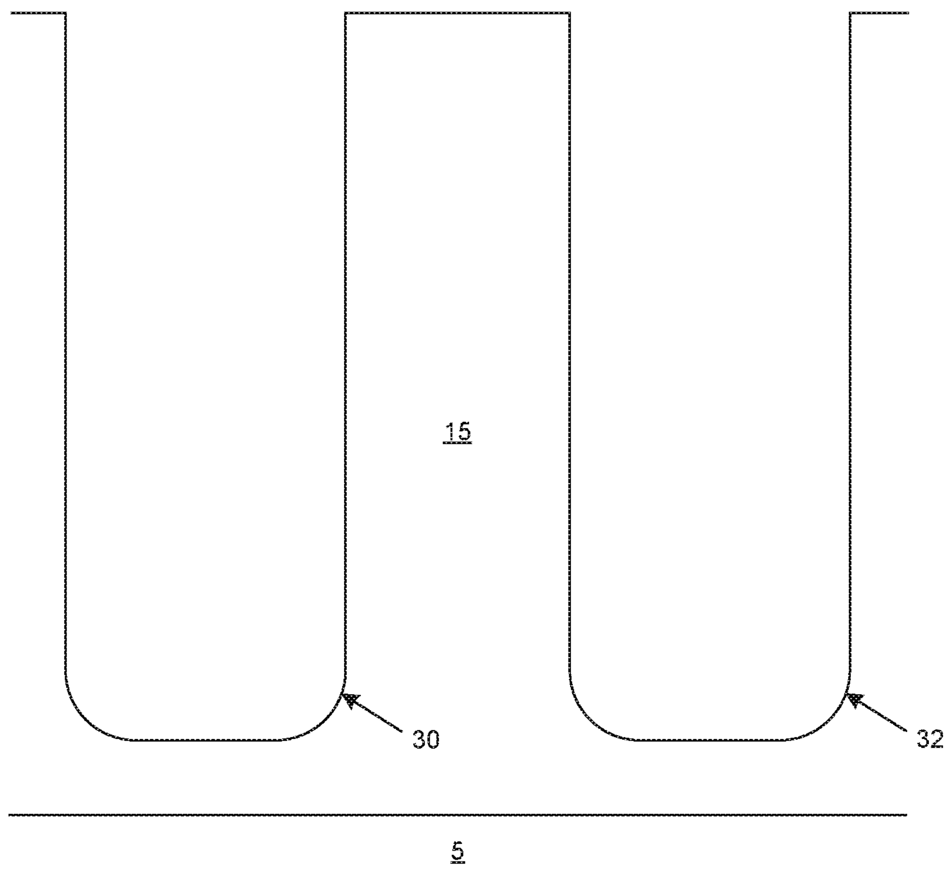

Fig. 6

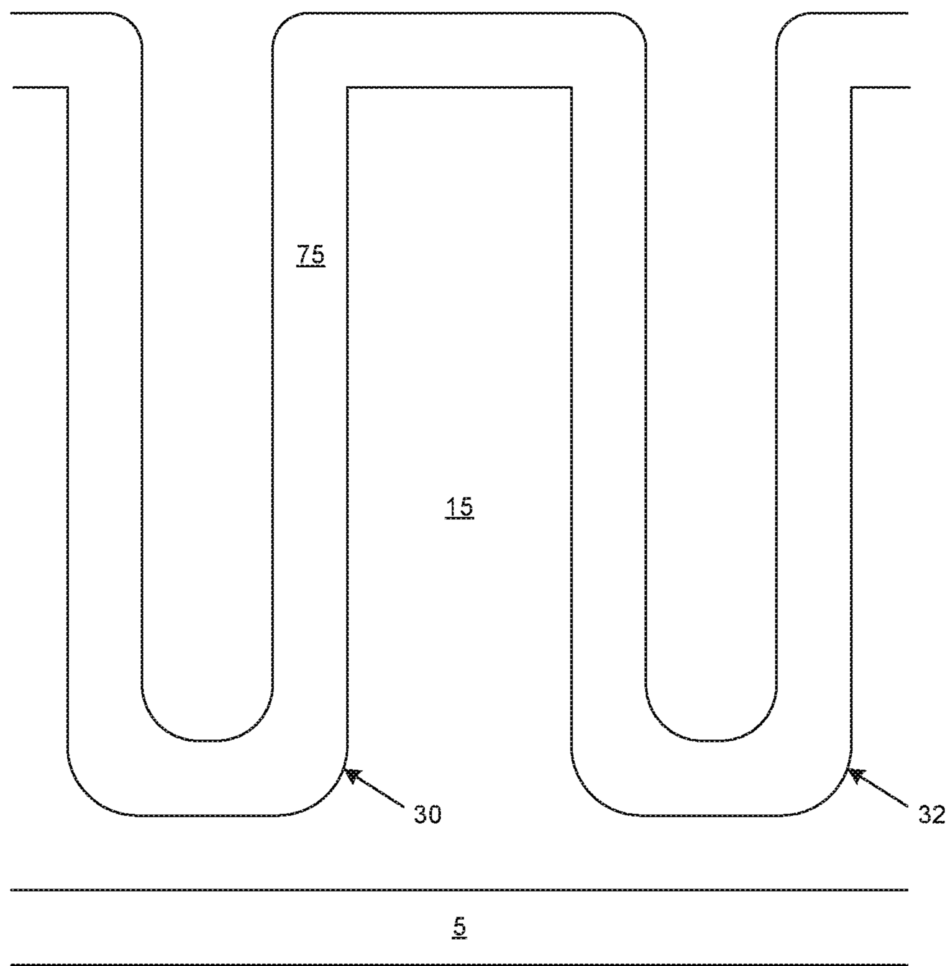

Fig. 7

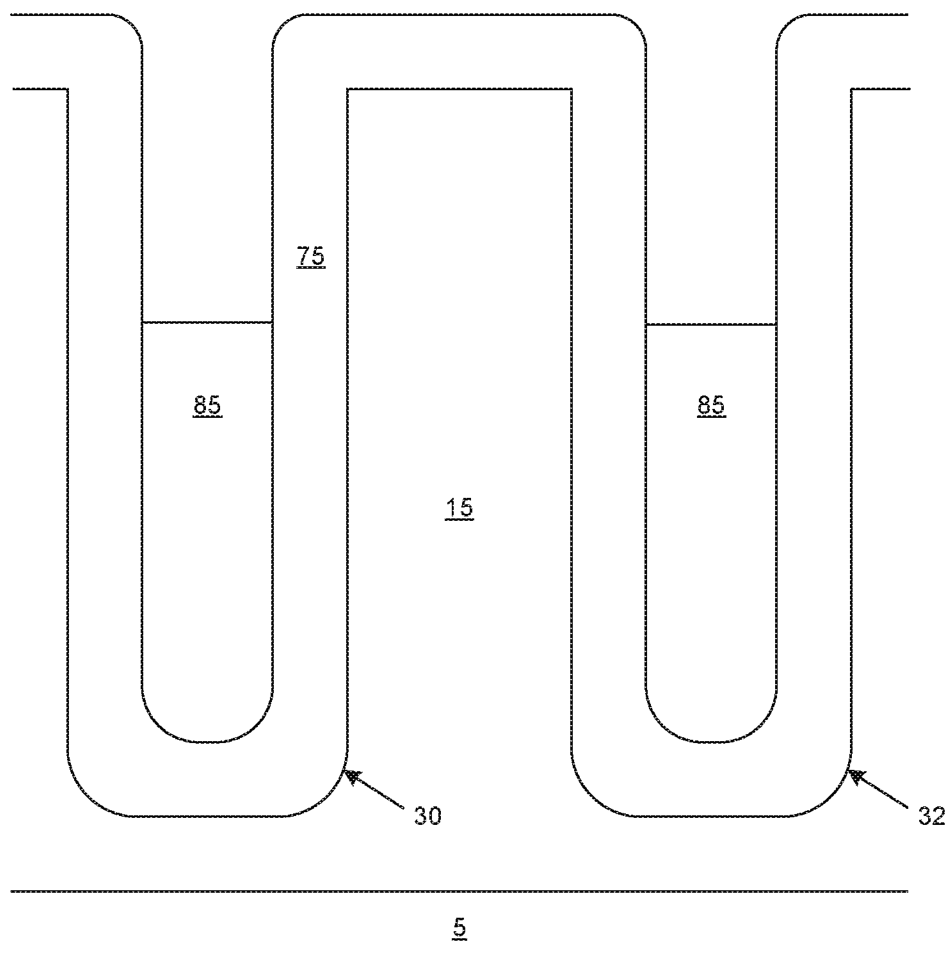

Fig. 8

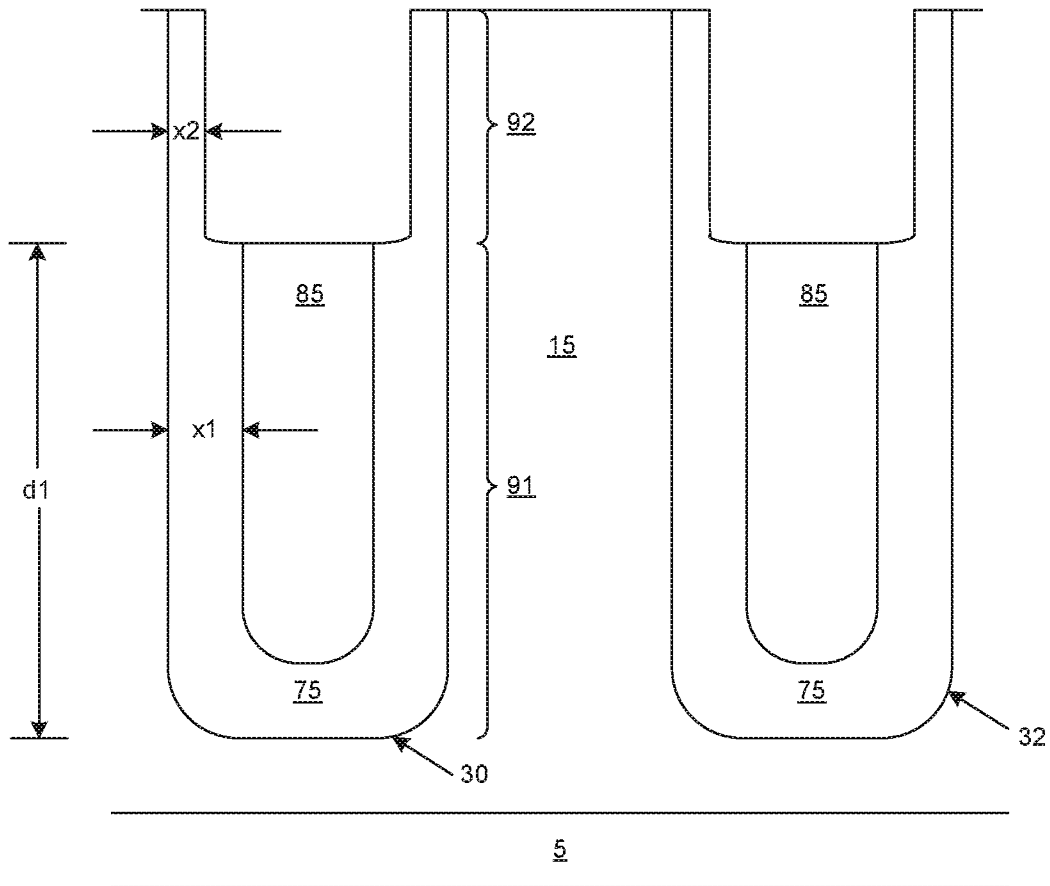

Fig. 9

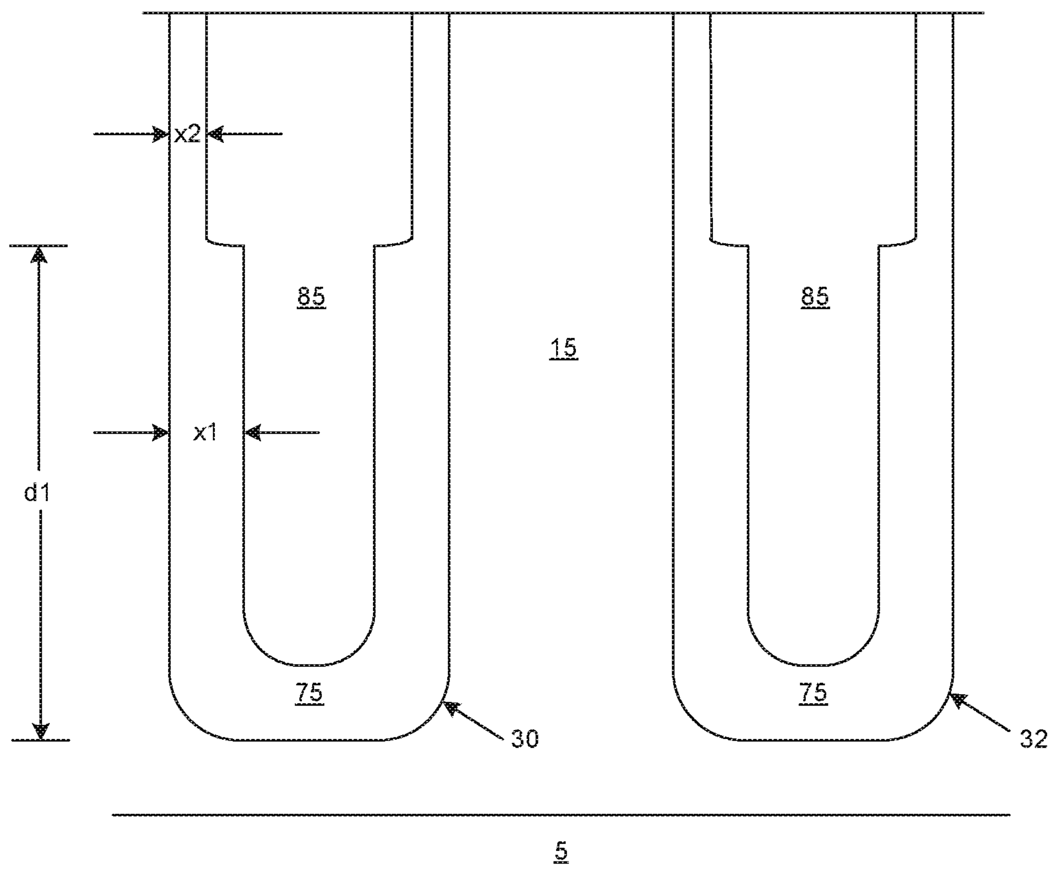

Fig. 10

Fig. 11

120
71 72
51
61 62
x2
12
(n+)
85 85
x1
11
(n)
10
(n-)
75 75
30 32
15
5

Fig. 12

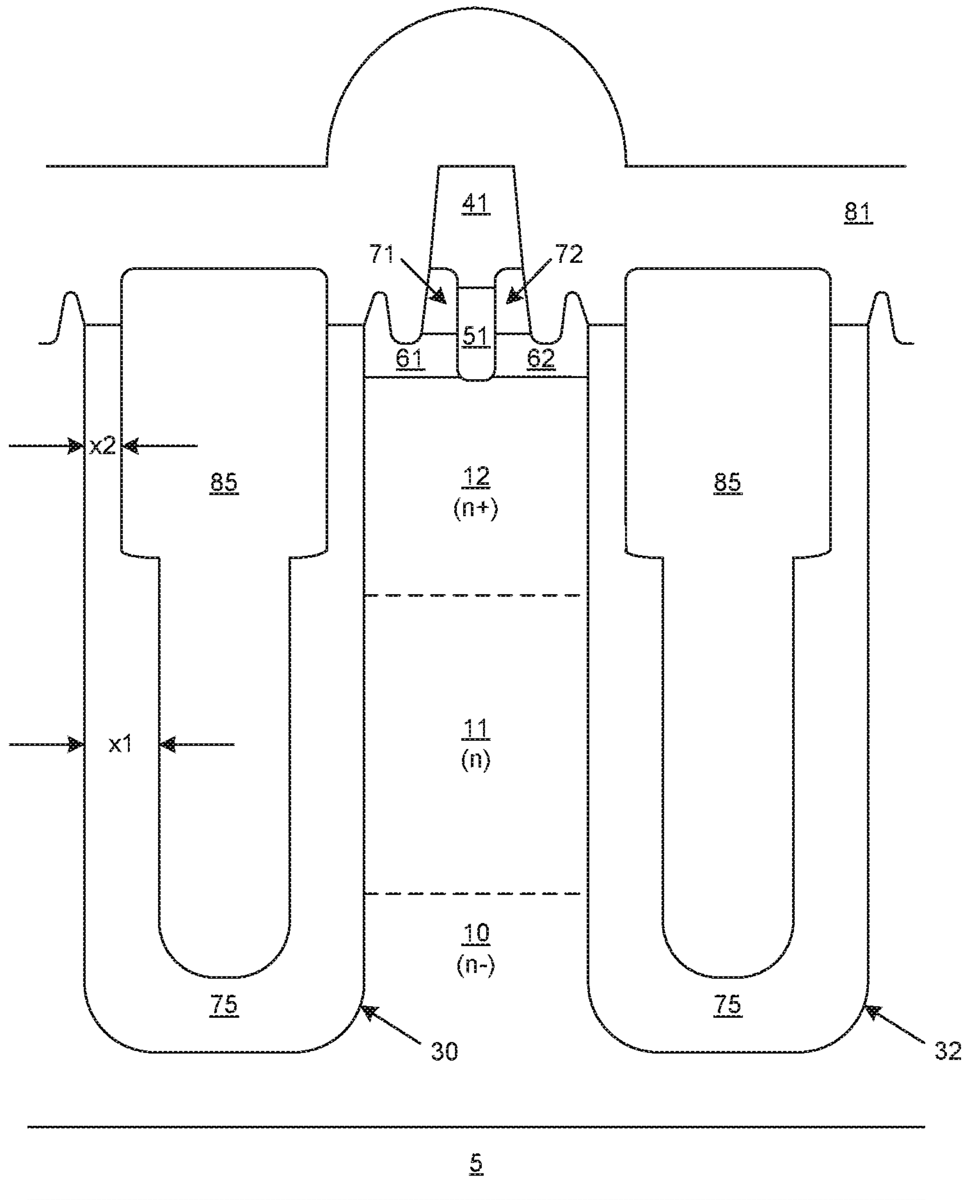

Fig. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/037815

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)I, H01L 29/423(2006.01)I, H01L 21/02(2006.01)I

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/78; H01L 21/336; H01L 29/94; H01L 29/423; H01L 27/08; H01L 21/76; H01L 21/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: epitaxial layer, trench, sidewall, oxide layer, lines, thickness

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y		2-4,9,10
A		14-20
Y	US 2005-0133858 A1 (BANERJEE et al.) 23 June 2005 See abstract, paragraphs [0022]-[0037] and figures 1-8.	2-4,9,10
A	US 2011-0254084 A1 (TERRILL et al.) 20 October 2011 See abstract, paragraphs [0027]-[0052] and figures 2, 3.	1-20
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A	US 2009-0140327 A1 (HIRAO et al.) 04 June 2009 See abstract, paragraphs [0043]-[0072] and figures 1-3.	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
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"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
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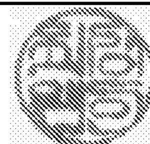
Date of the actual completion of the international search	Date of mailing of the international search report
30 September 2016 (30.09.2016)	**30 September 2016 (30.09.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2016/037815

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