United States Patent

Houser et al.

[15] **3,680,103**

[45] **July 25, 1972**

[54] DATA PROCESSOR AND COMPACTOR THEREFOR

[72] Inventors: **George G. Houser**, San Diego, Calif.; **Robert E. Jenkins**, Owego, N.Y.

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

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[52] **U.S. Cl.** ..... **343/17.1 R**, 343/5 CM

[51] **Int. Cl.** **G01s 7/30**

[58] **Field of Search** ..... 343/5 PD, 17.1 R, 5 CM

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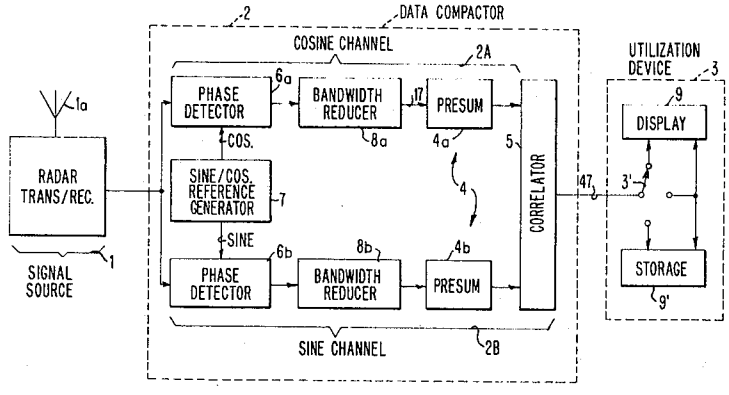
Primary Examiner—T. H. Tubbesing

Attorney—Hanifin and Jancin and Norman R. Bardales

[57] **ABSTRACT**

A data processing system and compaction means therefor sums groups of incoming data signals and provides a composite data signal for each group of signals summed. The composite signals are correlated in a predetermined sequence and provide correlated output signals indicative of the information contained in the plural data signals.

26 Claims, 12 Drawing Figures



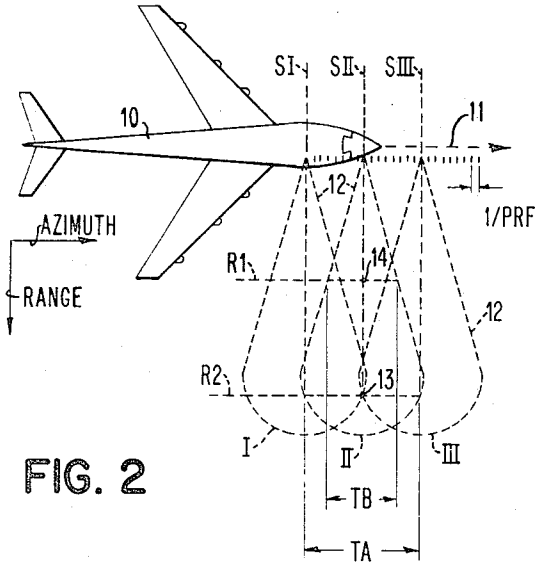


FIG. 2

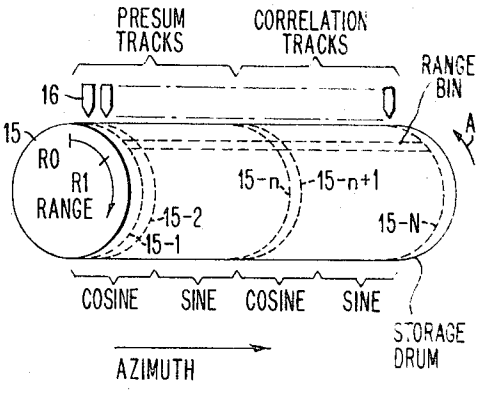


FIG. 4

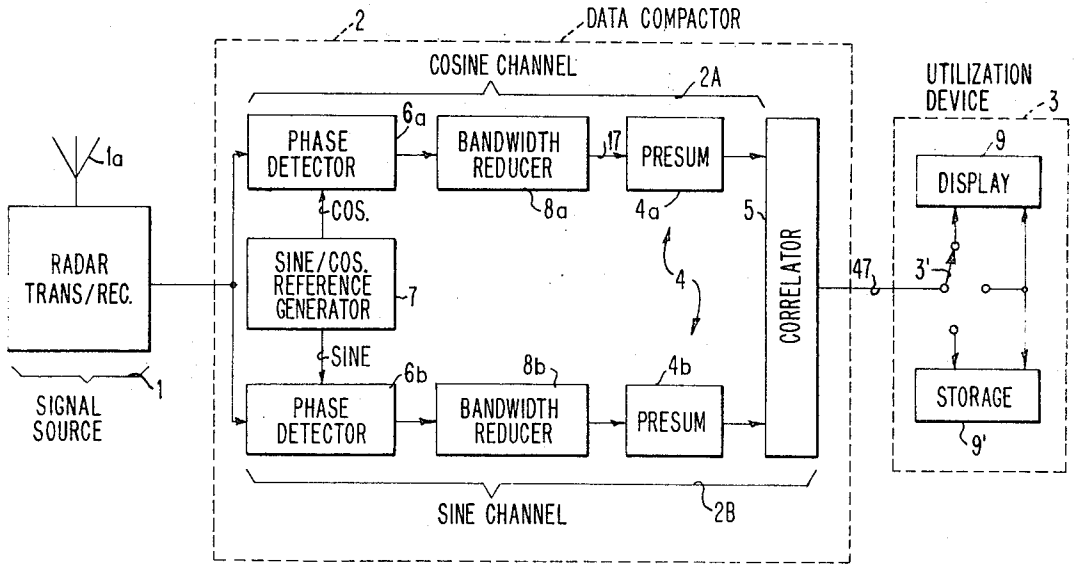


FIG. 1

INVENTORS
GEORGE G. HOUSER
ROBERT E. JENKINS

BY Norman R. Bardales

ATTORNEY

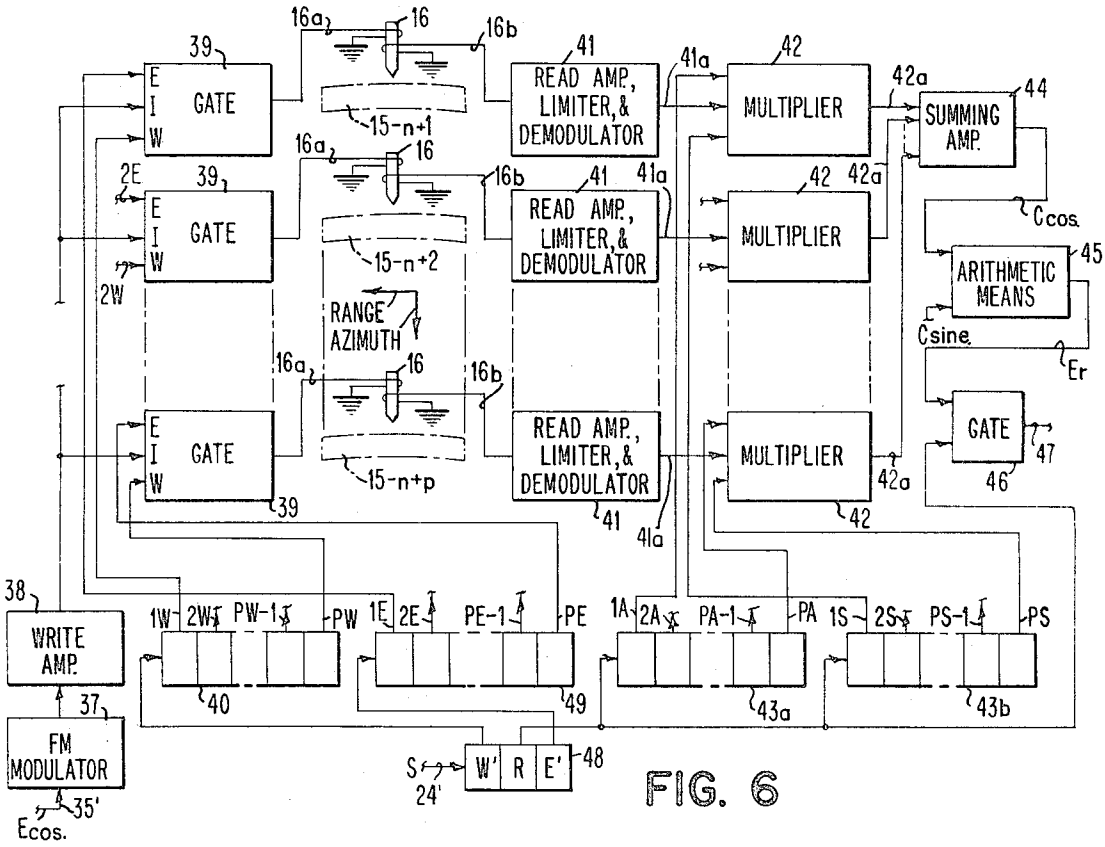


FIG. 6

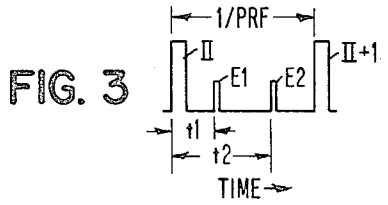


FIG. 3

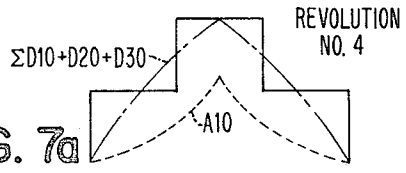


FIG. 7a

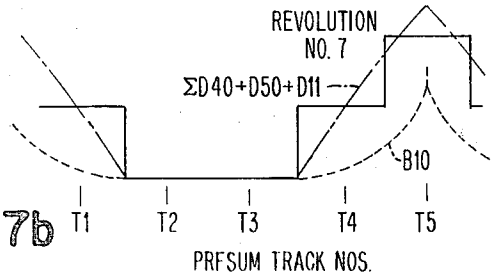


FIG. 7b

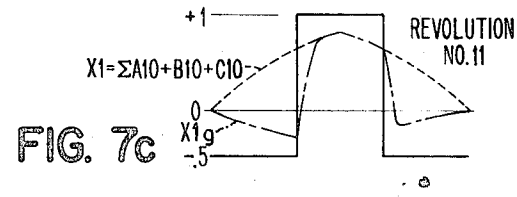


FIG. 7c

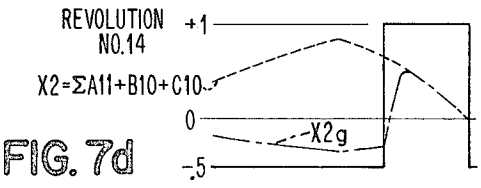


FIG. 7d

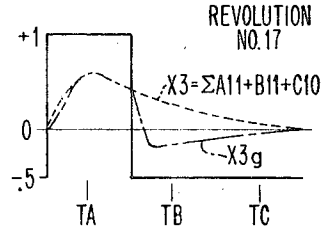


FIG. 7e

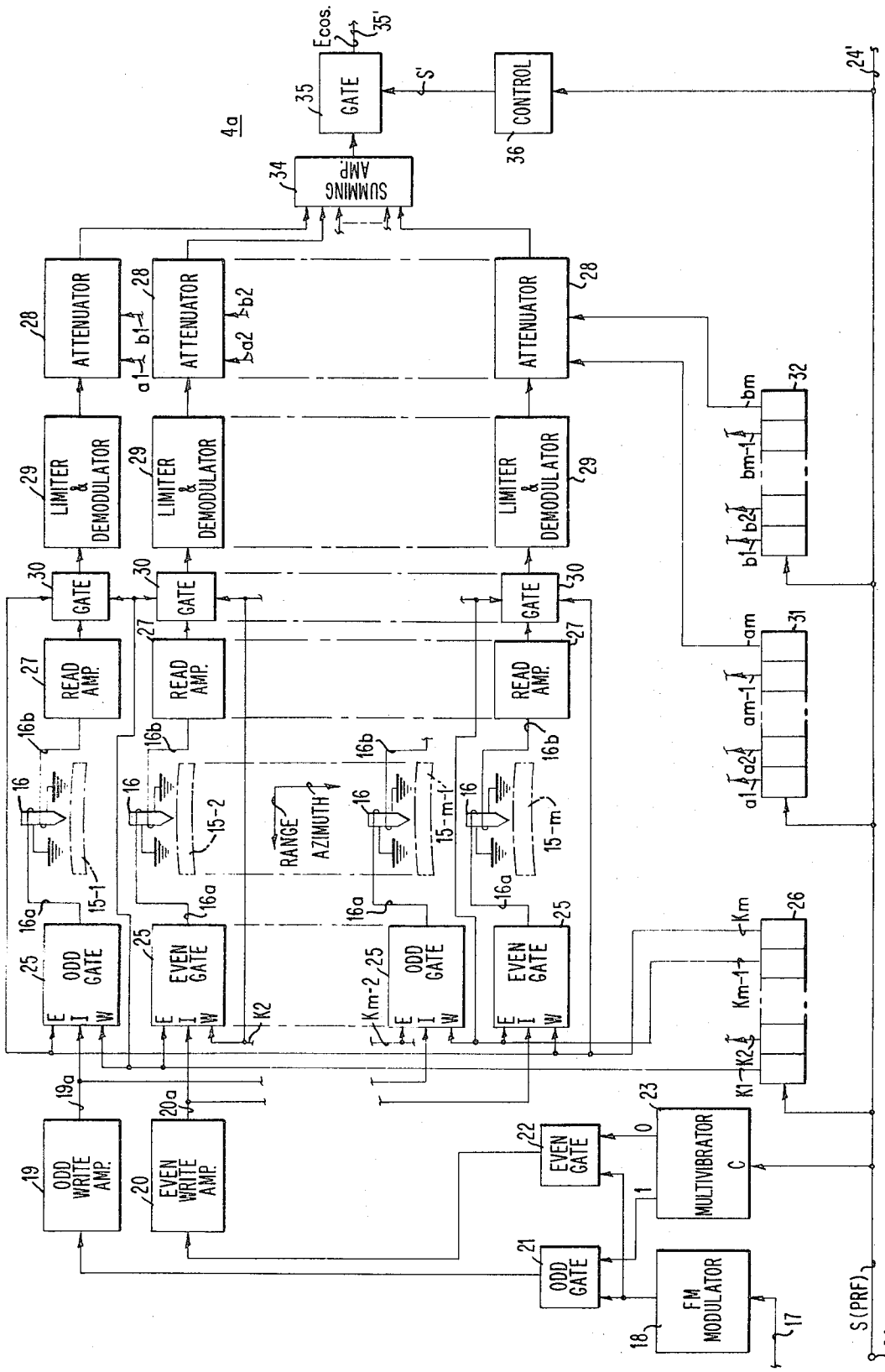

4a
35
GATE
Ecos.
35'
S'
CONTROL
36
24'
34
SUMMING AMP.
28
ATTENUATOR
a1
b1
a2
b2
29
LIMITER & DEMODULATOR
30
GATE
27
READ AMP.
16b
16
15-1
15-2
RANGE
AZIMUTH
15-m-1
15-m
16a
25
ODD GATE
EVEN GATE
E
I
W
K2
Km-2
Km
Km-1
K1
26
32
bm
bm-1
b1
b2
31
am
am-1
a1
a2
19a
20a
19
ODD WRITE AMP.
20
EVEN WRITE AMP.
22
EVEN GATE
21
ODD GATE
23
MULTIVIBRATOR
0
1
C
18
F.M. MODULATOR
17
S(PRF)
24

FIG. 5

REGISTERS

	DRUM								1ST. COEF.					2ND. COEF.					SIGN			AMP		
REV. NO.	PRESUM TRACKS					CORRELATOR TRACKS			STAGES					STAGES					STAGES			STAGES		
	T1	T2	T3	T4	T5	TA	TB	TC	a1	a2	a3	a4	a5	b1	b2	b3	b4	b5	1S	2S	3S	1A	2A	3A
1	D10-W	-E	-R	-R	-R			-W	0	0	0	1	0	0	0	1	0	1	1	0	0	1	0	0
2	D10	D20-W	-E			-R	-R	-R	0	0	0	0	1	1	0	0	1	0	0	1	0	0	1	0
3	D10	D20	D30-W	-E		-E			1	0	0	0	0	0	1	0	0	1	0	1	0	0	1	0
4	D10-R	D20-R	D30-R	D40-W	-E	A10-W			0	1	0	0	0	1	0	1	0	0	0	1	0	0	1	0
5	D10-E	D20	D30	D40	D50-W	A10-R	-R	-R	0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	1
6	D11-W	D20-E	D30	D40	D50	A10	E		0	0	0	1	0	0	0	1	0	1	0	0	1	0	0	1
7	D11-R	D21-W	D30-E	D40-R	D50-R	A10	B10-W		0	0	0	0	1	1	0	0	1	0	0	0	1	0	0	1
8	D11	D21	D31-W	D40-E	D50	A10-R	B10-R	-R	1	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0
9	D11	D21	D31	D41-W	D50-E	A10	B10	-E	0	1	0	0	0	1	0	1	0	0	1	0	0	1	0	0
10	D11-E	D21-R	D31-R	D41-R	D51-W	A10	B10	C10-W	0	0	1	0	0	0	1	0	1	0	1	0	0	1	0	0
11	D12-W	D21-E	D31	D41	D51	A10-R	B10-R	C10-R	0	0	0	1	0	0	0	1	0	1	0	1	0	0	1	0
12	D12	D22-W	D31-E	D41	D51	A10-E	B10	C10	0	0	0	0	1	1	0	0	1	0	0	1	0	0	1	0
13	D12-R	D22-R	D32-W	D41-E	D51-R	A11-W	B10	C10	1	0	0	0	0	0	1	0	0	1	0	1	0	0	1	0
14	D12	D22	D32	D42-W	D51-E	A11-R	B10-R	C10-R	0	1	0	0	0	1	0	1	0	0	0	0	1	0	0	1
15	D12-E	D22	D32	D42	D52-W	A11	B10-E	C10	0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	1
16	D13-W	D22-E	D32-R	D42-R	D52-R	A11	B11-W	C10	0	0	0	1	0	0	0	1	0	1	0	0	1	0	0	1
17	D13	D23-W	D32-E	D42	D52	A11-R	B11-R	C10-R	0	0	0	0	1	1	0	0	1	0	1	0	0	1	0	0
18	D13	D23	D33-W	D42-E	D52	A11	B11	C10-E	1	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0
19	D13-R	D23-R	D33-R	D43-W	D52-E	A11	B11	C11-W	0	1	0	0	0	1	0	1	0	0	1	0	0	1	0	0
20	D13-E	D23	D33	D43	D53-W	A11-R	B11-R	C11-R	0	0	1	0	0	0	1	0	1	0	0	1	0	0	1	0

FIG. 8

DATA PROCESSOR AND COMPACTOR THEREFOR

The invention herein described was made in the course of or under a contract with the Department of Defense.

BACKGROUND OF THE INVENTION

This invention relates to a data processing system and data compaction means therefor, and is particularly useful for radar data processing systems.

Data processing and data compaction systems are well known in the art. For example, one such prior art system is described in U. S. Pat. No. 3,271,765 entitled "Data Compression Processing System," S. R. Pulford, and assigned to the same assignee herein. In that particular patent, the system is embodied in a radar data processing system of the side-looking type. Briefly, the prior art system contemplates utilizing the radar signal returns to modulate the beam intensity of an electronic CRT scanner which is adapted to scan an unexposed recording film in a raster type mode. The start of each scan is synchronized with the interrogating pulses and as the beam sweeps across the photographic recording medium it exposes the emulsion in proportion to the modulation produced by the signal returns. As the successive interrogating signals are transmitted, the resultant successive signal returns coming from the same range are recorded adjacent to each other in the recording medium. Subsequently the roll of film is developed and thereafter when it is desired to read out the azimuth information of the target points in a given range, the developed film transparency is juxtaposed between a flying spot scanner and photomultiplier tube and the beam of the spot scanner is moved along a line transverse to the direction in which the signal returns were recorded. The position of the line of course corresponds to the desired range of interest. For further information concerning the details and operations of the aforedescribed prior art system, reference should be made to the aforementioned patent. While such systems have been found satisfactory, their application for processing radar signals on a real time basis have been limited by the requirement to record each and every radar signal return and subsequently to readout each and every recorded signal return. Furthermore, when the film is utilized as the recording medium additional time is required to develop the film and the system is thus not amenable to processing the data signals on a real time basis. In considering today's state of the art wherein each and every target point in each and every range may be subjected to multiple hits, e.g. 1,500 hits, from successive multiple interrogating pulses, it can be readily seen that an improved data processing and compaction system is required.

SUMMARY OF THE INVENTION

It is an object of this invention to provide an improved data processor and/or data compaction system which processes the information on a substantially real time basis.

It is another object of this invention to provide a data processor and/or data compaction system utilizing magnetic storage means.

It is still another object of this invention to provide a data processor and/or data compaction system utilizing magnetic storage means of the dynamic type and/or particularly of the drum or disk type.

It is still another object of this invention to provide a radar data processor and/or radar data compaction system for processing radar return signals on a substantially real time basis.

Still another object of this invention is to provide a radar data processor and/or radar data compaction system for processing radar return signals of a side-looking radar apparatus.

According to one aspect of the invention there is provided a data compaction system for compacting plural data signals. Each of the data signals has first and second information characteristics. The compaction system has a first means for presumming predetermined groups of the data signals and providing for each group summed an output first signal having

characteristics proportional to the aforementioned first and second information characteristics of the data signals of the particular group. In addition, a second means for correlating the output signals of the first means in a predetermined sequence is provided. The second means provides correlated output signals indicative of the information of the plural data signals.

According to another aspect of the invention there is provided a data processing system which includes the aforementioned data compaction system and which further includes a utilization device responsive to the correlated output signals of the aforementioned second means.

According to still another aspect of the invention the aforementioned data processor system and/or data compaction system are preferably embodied in radar data processing system and/or a radar data compaction system.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of the preferred embodiments of the invention as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a schematic view shown in block form of a preferred embodiment of the invention;

FIG. 2 is a diagrammatic representation of an aircraft in flight with side-looking radar apparatus in operation;

FIG. 3 is a waveform diagram shown in idealized form of an interrogating signal pulse emitted by the radar apparatus of FIG. 1 and the resultant echo return signals;

FIG. 4 is a schematic view of the magnetic storage means employed in the system of FIG. 1;

FIG. 5 is a schematic view shown in block form of the cosine presummer of FIG. 1;

FIG. 6 is a schematic view shown in block form of the cosine portion of the correlator shown in FIG. 1;

FIGS. 7*a*–7*e* are waveform diagrams utilized in the explanation of the present invention; and

FIG. 8 is a table helpful in the explanation of an illustrative example of a preferred recording operational mode employed by the present invention.

In the Figures, like elements are designated with similar reference numerals.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, data signals from a signal source 1 are processed by the data compactor 2. The data signals are compacted by compactor 2 and the compacted data signals in turn are fed to a utilization device 3. Data compactor 2 comprises presum means, generally indicated by the reference numeral 4, and correlator means 5. The presum means 4 sums groups of the input signals and provides a composite signal for each group. The correlator means 5 sequentially correlates the composite signals and provides correlated output signals indicative of the information contained in the data signals. Means 4 and 5 coact to compact the data signals of source 1 as will become apparent from the detailed discussion hereinafter. The correlated output signals are further processed by the utilization device 3. For example, device 3 may be an indicator or a display system 9 and/or a storage system 9'. Preferably, systems 9 and 9' are a CRT display system and a magnetic tape storage system, respectively. A switching means 3' provides independent as well as simultaneous operational modes for systems 9 and 9'.

In the preferred embodiment, the data processing system of FIG. 1 is utilized as a radar data processing system for a side-looking radar system. The side-looking radar system is a coherent, pulsed-Doppler radar which employs a synthetic-aperture antenna, such radar systems being well known in the art. Signal source 1 is accordingly an airborne coherent radar transmitter/receiver apparatus which emits high frequency interrogating signal pulses from the synthetic-aperture antenna 1a and receives thereat the radar returns or target echos. The

receiver portion of apparatus 1 converts the radar return video signals to IF signals at its output in a manner well known to those skilled in the art and the IF signals are fed to the input of the data compactor 2.

For the particular radar system, the video IF signals are preferably processed by the compactor 2 in two quadrature related signal channels to mitigate the effects of signal clutter. These channels are hereinafter referred to sometimes as the cosine and sine channels 2A, 2B, respectively, of compactor 2. Each channel includes one of the respective presummers 4a, 4b, which are part of presum means 4. It should be understood that in other types of radar and/or data processing systems, only one signal channel and consequently only one presummer may be utilized such as, for example, in radar and/or data systems where signal clutter effects are negligible and/or absent. For the particular radar data processor embodiment being described, however, it is preferred that the IF signals are phase detected in the cosine and sine quadrature channels 2A and 2B by means of the respective phase detectors 6a and 6b, respectively. More particularly, the IF signals are phase detected by detectors 6a and 6b with respect to predetermined related cosine and sine reference signals, respectively, provided by the sine and cosine reference signal source or generator 7. Each quadrature signal component has information and clutter sub-components. When the quadrature signal components of channels 2A, 2B are subsequently combined into a resultant signal by the correlator means 5, the respective clutter subcomponents of each effectively cancel each other out. As contemplated herein the cosine and sine quadrature signal components are generated simultaneously from the returns of the same interrogating signal pulse. Alternatively, it should be understood that the cosine and sine quadrature signal components may be generated alternately in a time multiplex fashion from the returns of the successive interrogating pulses. In the latter case a suitable time delay means would be provided in one of the channels which would bring the quadrature signal components into the same time phase relationship with respect to each other prior to their correlation by the correlator means 5.

Moreover, in the particular embodiment being described, the quadrature channels are also further provided with respective bandwidth reduction amplifiers 8*a*, 8*b* as shown in FIG. 1, each of which eliminates the upper and lower sideband components below a desired decibel level, and thus reduces the bandwidth of the signals being processed. It should be understood that in some cases where the bandwidth of the signals being processed are already compatible to the bandwidth response of the data compactor 2, particularly of the presum and correlator means 4, 5 thereof, then the amplifiers 8*a*, 8*b* need not be provided. As is obvious to those skilled in the art, if time multiplexing is employed the quadrature signal components may be processed by certain elements which are common to both channels such as a common phase detector and/or bandwidth reducer.

In order to better appreciate the principles of the present invention, the side-looking radar system and data processor of FIG. 1 will now be described with reference to FIG. 2. As shown therein, an aircraft 10 is traveling at an assumed predetermined constant velocity along a substantially straight line path 11 relative to a ground track in the direction indicated by the arrow. This path coincides for present purposes with what is termed the flight reference vector. The aircraft is equipped with the radar apparatus and data processing system 1–3 of FIG. 1. Accordingly, the on-board transmitter, not shown, of source 1 emits at the antenna 1a successive interrogating pulses of electromagnetic energy at a fixed PRF. The electromagnetic energy is beamed toward the terrain at an angle of substantially 90° to the flight vector of the aircraft 10. For sake of clarity, only three radiation patterns or energy lobes 12 associated with three particular transmitted pulses are shown in FIG. 2, e.g. the lobes designated by the reference characters I, II, and III. The lobes or beams 12 are illustrated in stylized form and are generally tear-shaped with increasing transectional dimensions being encountered at greater distances, i.e. ranges, from the aircraft 10. It should also be understood that the spacing 1/PRF between successive beams is illustrated with an exaggerated or enlarged scale in FIG. 2 for sake of clarity.

Each target point is subjected to a number of multiple hits from successive interrogating beams as the craft 10 moves past the particular point. By way of example, the target point 13 located at the relatively remote range R2 is first hit by beam I when the aircraft 10 is at the azimuth location SI. The target point 13 continues to be hit by each successive interrogating beam transmitted during the time period TA. With the aircraft in the azimuth position SII, as shown in FIG. 2, the beam II is directly abeam of the target point 13, i.e. beam II is at 90° with respect to the target point 13. When the craft 10 reaches the azimuth position SIII, the beam III makes the last hit on target 13.

For sake of comparison, a target point 14 is illustrated in FIG. 2 as being at the same azimuth location SII as target point 13 but at a relatively shorter or closer range R1. Target point 14 is hit by successive interrogating beams transmitted during the time period TB. Due to the aforementioned tear-shaped form of the beams, the number of hits associated with target point 14 is less than that associated with target point 13. Nevertheless, the number of hits in either case is substantially high. For a particular example of radar system of the type being described and a given range, the number exceeds well over 1500 hits. Each time a target point is hit, an echo or return signal is reflected back to the apparatus 1, FIG. 1, and is received by the antenna 1a and receiver portion thereof. The pulse repetition frequency PRF is judiciously selected so that the return signals resulting from a given interrogating beam are received prior to the transmission of the next succeeding interrogating beam in a manner well known to those skilled in the art. Also, as is well known to those skilled in the art, the return times of the respective return signals associated with any given interrogating beam is proportional to the respective range information associated with the target points producing the return signals. Thus, for example, as shown by the idealized waveforms of FIG. 3 for the particular interrogating energy lobe or pulse II, its associated return signals will include a return signal E1 first from the closer target point 14 and then a return signal E2 from the further target point 13, the respective times $t1$, $t2$ of return of each of these last-mentioned return signals being proportional to the ranges R1 and R2, respectively.

Moreover, during successive radar contacts with a target point, as described above, a Doppler effect is produced in the successive return signals associated with the particular point due to the change in relative velocity between the target point and the craft 10 during successive interrogations. The Doppler effect is characterized by the envelope produced by these signals and is utilized to ascertain the azimuth information associated with the target point. Without the present invention the processing of the return signals associated with each of the multiple hits associated with each target point for each range and for each azimuth location would require a complex and vast amount of information channels and data processing equipment. The data processing system of the present invention, however, simplifies and reduces the amount of information channels and data processing equipment required to process the return signals.

In the preferred embodiment both the presum means 4 and the correlator means 5 utilize magnetic storage means and preferably storage means of the drum or disk type such as, for example, the common drum 15 illustrated in FIG. 4. The drum 15 has a finite number of plural tracks 15-1 to 15-N. Tracks 15-1 to 15-n are assigned to the presum means 4 and tracks 15-n+1 to 15-N are assigned to the correlator means 5. Access to the tracks of the drum 15 is provided by the aligned READ/WRITE heads 16, each of which is associated with one of the tracks 15-1 to 15-N. One-half of the allocated presum tracks 15-1 to 15-*n* are further assigned to the presummer 4a

of the cosine channel 2A and the other half are assigned to the presummer 4b of the sine channel 2B. Similarly, one-half of the correlation tracks 15-n+1 to 15-N are allocated to the portion of the correlator means 5 associated with cosine channel 2A and the other half are allocated to the portion of the correlator means 5 associated with the sine channel 2B. The rotation of the drum is synchronized with the PRF of the aforementioned interrogating signals. By way of example, the drum is assumed to make one complete revolution per interrogating signal. Consequently, only a single row of READ/WRITE heads 16 are required for the given example. Each revolution commences from a reference position corresponding, for example, to the closest range R0 for which the radar system is capable of receiving return signals. Thus, for each revolution as the drum rotates in the direction indicated by the arrow A, the return signals associated with a particular interrogating signal, after being phase detected and bandwidth reduced, are recorded via the appropriate READ/WRITE head 16 on one of the cosine and one of the sine presum tracks. For the illustrated counterclockwise direction A, the echo returns, i.e. signal returns, are recorded from the closest range R0 to the remotest range on the particular track in a clockwise direction as indicated by the direction arrow marked RANGE. As the signal returns from successive interrogating pulses are written on successive tracks, the range information associated with corresponding range bins, e.g. the range bin designated R1 in FIG. 2, are recorded in corresponding radial positions of the presum tracks. Thus, in the preferred embodiment successive return signals from the same range which are derived from successive interrogating pulses when recorded on the successive tracks are spatially aligned with respect to each other.

In the presum means 4, a plural number of serial, i.e. sequential, WRITE operations are performed and these are followed by a single parallel READ operation. In the preferred embodiment, the serial WRITE operations are performed on a preselected number of successive presum tracks which is less than the number of assigned presum tracks. After the information has been recorded on a first group of successive presum tracks of the preselected number, the parallel READ operation is performed on this group of presum tracks while a WRITE operation is being performed on the next presum track. Also, the addressing system for the presum tracks is arranged such that as information is being written into one of the tracks the next succeeding track is being erased. After the parallel READ operation is performed, as the tracks of the particular group read out are sequentially erased they become available for recording the information after the last track of the assigned presum tracks is utilized. Each time information has been recorded on a group of successive presum tracks of the preselected number, the parallel READ operation is performed simultaneously while WRITE and ERASE operations are being performed on the next two succeeding presum tracks, respectively. The case of the aforedescribed recording technique will become apparent from the description hereinafter with reference to FIGS. 5 and 8.

Alternatively, because of the high sampling rate or PRF employed, the serial WRITE operations may be performed until all of the assigned presum tracks are utilized before the parallel READ operation is performed. In such a case, the amount of information not recorded during the readout operation is negligible. However, in still another case where it is desired to record all the return signals, the presum tracks may be further assigned into two or more sets of successive tracks so that while a READ operation is being performed in one of the sets, the serial WRITE operation continues in the tracks of the next set. In this latter case, in the preferred embodiment the sine and cosine presum tracks would each be divided into an equal number of plural sets.

In either of the three aforementioned cases, each time a READ operation is performed on the presum tracks there is produced an output signal which is proportional to the information characteristics, i.e. range and azimuth, of the group of signals recorded on the successive presum tracks being read out. It should be understood that in the preferred embodiment the two quadrature components of an input signal which are fed to the presummers 4a and 4b, respectively, are simultaneously written into respective single sine and single cosine presum tracks thereof. Thus, in the preferred embodiment each output signal of the presum means 4 also has two components which are derived from the particular plural cosine and plural sine presum tracks, respectively, being read out. The output signals of the presum means 4 are sometimes referred to hereinafter as composite signals. The foregoing will become more apparent with reference to the detailed description hereinafter of the presummer *4a* illustrated in FIG. 5.

Each composite signal, or in the case of the preferred embodiment, each quadrature component of the composite signal, in turn, is recorded on an exclusive correlator track of the drum 15. Moreover, the composite signals are synchronously recorded on successive correlator tracks such that the range information associated with the same range bin and contained in the successive composite signals are recorded in the same corresponding radial positions of the correlator tracks. In the preferred embodiment, the range bins of the correlator tracks are aligned with the corresponding range bins of the presummer tracks, c.f. range bin R1 illustrated in FIG. 4. The correlator employs a serial WRITE operation when recording on the correlator tracks. In the preferred embodiment, the two quadrature components of a composite signal are simultaneously written into single sine and single cosine correlation tracks, respectively. After each WRITE operation a parallel READ operation is performed on all the correlation tracks. Sometime prior to the next WRITE operation, an erase operation is performed on the next sine and cosine correlation tracks of the sequence which will record the next incoming composite signal. Thus, in the preferred embodiment, the oldest information contained in the sine and cosine quadrature correlation tracks is being continuously removed and updated with the information of the newest or latest incoming composite signal. During the READ operation associated with the correlation tracks, the individual recorded composite signals being read out are weighted with a reference function from which the information relative to the azimuth characteristic is resolved. The weights assigned to the individual reference signals are continuously being shifted in a manner hereinafter described in greater detail with reference to the description of the correlator illustrated in FIG. 6 and the illustrative operational example shown in the table of FIG. 8.

Referring now to FIG. 5, there is shown a preferred embodiment of the presummer *4a* of FIG. 1. It should be understood that the presummers *4a* and *4b* are identically configured and thus only presummer *4a* is shown in FIG. 5 for sake of clarity. Presum means 4 reduces the sampling rate of information to the correlator means 5 with respect to the rate of information being provided by the signal source 1. More particularly, in the preferred radar system embodiment, the sampling rate of the radar data going to the correlator means 5 is reduced with respect to the PRF rate that the basic radar samples the terrain. As shown in FIG. 5 the IF input signals from the receiver portion of the radar apparatus, i.e. signal source 1 of FIG. 1, after being phase detected and bandwidth reduced by the circuits *6a*, *8a*, respectively, of channel 2A, are fed to the input 17 of FM modulator 18 of presummer 4a. The signals at input 17 frequency modulate a carrier signal that is to be recorded on the cosine presum tracks 15-1 to 15-*m* of drum 15, FIG. 4. In the drawing, reference numerals 15-1 to 15-*m* are used to designate the cosine presum tracks and correspond to one-half of the tracks 15-1 to 15-*n* illustrated in FIG. 4. It should be understood that the sine presum tracks, not shown, are designated by the reference numerals 15-m+1 to 15-*n* and are included in the presummer *4b*. The modulated carrier signal is fed to the odd and even write amplifiers 19, 20 via respective gates 21, 22. More particularly, the modulated carrier signal of modulator 18 conditions one of the respective two inputs of

each of the gates **21**, **22**. The other inputs of the respective gates **21** and **22** are coupled to the 1 and 0 outputs of a bi-stable multivibrator **23** which is driven by a synchronization pulse signal S applied to terminal **24**. Synchronization signal S is derived from the interrogating signal of signal source **1** by suitable means, not shown, and has a prf equal to the basic radar PRF. In response to the pulses of the synchronization signal S applied to the complementary input C of multivibrator **23**, the odd and even gates **21** and **22** are alternately actuated. The output **19a** of the odd write amplifier **19** is connected to the data inputs I of each of those gates **25** designated by the legend ODD GATE in FIG. **5**. The outputs of ODD GATES **25**, in turn, are connected to the respective write windings **16a** of the READ/WRITE heads **16** associated with the respective odd tracks **15-1**, **15-3**, **15-5** . . . **15-*m*—1**, it being assumed for sake of explanation that m is an even integer. Similarly, the output **20a** of the even write amplifier **20** is connected to the data inputs I of each of the EVEN GATES **25** whose outputs are connected in turn to the respective heads **16** associated with the even tracks, e.g. tracks **15-2**, **15-4** . . . **15-*m***. Each gate **25** also has two other control inputs, to wit: a write input W and an erase input E. An m stage ring counter **26**, where *m* is greater than one and as aforementioned is assumed to be an even integer, controls the gates **25**.

Each read windings **16b** of the respective heads **16**, FIG. **5**, is connected to the input of a mutually exclusive one of the read amplifiers **27**. The output of each read amplifier **27** is coupled to one of the limiter and demodulator cascaded stages **29**, which are illustrated schematically by a single block for sake of simplicity, via an inhibit gate **30**. The limiter portion of each block **29** amplitude limits the signals from its respectively associated amplifier **27** and the demodulator portion demodulates the frequency modulated signal being read out by its associated amplifier **27**. Actuation of gates **30** are controlled by the ring counter **26**.

In the preferred embodiment a weighting operation is performed in the presum means **4**. Thus as the signals are read out from the groups of the tracks **15-1** to **15-*m***, they are amplitude weighted with respect to a reference function in the respective weighting amplifiers or attenuators **28** which are coupled to the output of the limiter/demodulator stages **29**. The gain of the attenuators **28** are digitally controlled by the output signals of the two m stage shift registers **31** and **32**. The weighting operation provided in the presum means **4** shapes the output signals being read out to a desired filter shape characteristic, e.g. a Gaussian distribution. The digital control signals generated at the outputs *a***1**, *a***2**, . . . *a*m and *b***1**, *b***2**, . . . *b*m of registers **31** and **32**, respectively, thus change the respective gains of the attenuators **28** so that each signal being read out is modified by a particular one of the weighting components which are the inverse Fourier transforms of the desired filter shape characteristic. Shift registers **31** and **32** are advanced by the synchronization signal S which, as aforementioned, has a prf equal to the basic PRF of the interrogating radar signals of the signal source **1**.

Each of the respective outputs of the attenuators **28** is coupled to one of the multi-inputs of summing amplifier **34** which sums the weighted signals. An output of the summing amplifier **34** is coupled to the input of gate **35**. Gate **35** is actuated by the control signal S' generated by gate control circuit **36**. Control circuit **36**, which may include a counter for this purpose, provides in the preferred operational mode an output pulse signal S' every m-2 pulse of signal S applied to its input. As a consequence, each time gate **35** is actuated, an output signal Ecos is provided at the output of gate **35** that is indicative of the information contained in the particular group of tracks **15-1** to **15-*m*** being read out in the presummer **4*a***. The signal Ecos and the signal S are fed to the cosine portion of the correlator means **5** shown in FIG. **6** via conductors **35'** and **24'**, respectively. In a similar manner, presummer **4*b*** provides a signal Esine to the sine portion of the correlator means **5**. Signal S is utilized to drive the counter and shift register counterparts of presummer **4*b*** corresponding to the counter **26** and registers **31**, **32** of presummer **4a**.

Ring counter **26**, as aforementioned, controls the operations of gates **25** and **30**. In the preferred mode of operation as the counter **26** is advanced by signal S, the signals at the outputs K1, K2, . . . Km sequentially open the gates **25** associated with tracks **15-1**, **15-2**, . . . **15-*m***, respectively, by virtue of their respective connections to the write inputs W of the gates **25**. In this manner the alternate FM signals at the outputs of amplifiers **19** and **20** are written on the tracks **15-1**, **15-2**, . . . **15-*m*** in succession, a track being written into each time the gate **25** associated with the particular track is opened. Moreover, the outputs K1, K2, . . . Km are also connected to the erase input E of the gates **25** associated with tracks **15-2**, **15-3**, . . . **15-*m***, **15-1**, respectively. Consequently, as the ring counter **26** advances, it erases the information recorded on the track succeeding the one being written into. In addition, the outputs K1, K2, . . . Kn are connected to one of the control inputs of the inhibit gates **30** associated with the tracks **15-1**, **15-2**, . . . **15-*m***, respectively, as well as the other control inputs of the gates **30** associated with the tracks **15-2**, **15-3**, . . . **15-*m***, **15-1**, respectively. Consequently, when the WRITE and ERASE operations are being simultaneously performed on two adjacent tracks, the gates **30** associated with these two particular tracks are inhibited. As a result, no output signal is available for readout from the tracks whose gates are so inhibited and hence cannot interfere with the READ operation being performed on the other tracks, which readout operation is controlled by the coaction of the gate **35** and control circuit **36** in response to the signal S as previously explained.

Referring now to FIG. **6** there is partially shown a preferred embodiment of the correlator means **5** of FIG. **1**. It should be understood that only the portion of the correlator means **5** associated with the cosine quadrature channel **2A** is illustrated in FIG. **6**. The portion of the correlator means **5** associated with the sine quadrature channel **2B** is identical thereto and hence has been omitted for sake of simplicity. Accordingly, in FIG. **6**, each of the presummed signals Ecos are fed via conductor **35'** to the input of FM modulator **37**. The signals Ecos frequency modulate a carrier signal that is to be recorded on the cosine correlator tracks of drum **15**. In the drawing, reference numerals **15-*n*+1** to **15-*n*+*p*** are used to designate the cosine correlator tracks and correspond to one-half of the tracks **15-*n*+*1*** to **15-N** illustrated in FIG. **4**. It should be understood that the sine correlator tracks, not shown, are designated by the reference numerals **15-*n*+*p*+1** to **15-N** and are included in the portion of the correlator means **5** associated with the sine quadrature channel **2B**. It should also be understood that there are equal numbers of cosine and sine correlation tracks.

The modulated carrier signal is fed to the write amplifier **38**, the output of which is connected to the respective data inputs I of gates **39**. Each write input W of gates **39** is actuated by one of the output signals present at the outputs 1W, 2W,...PW of the p stage write-select ring counter **40** which sequentially addresses the drum tracks **15-*n*+1** to **15-*n*+*p***. Each output of a gate **39** is connected to the write winding **16a** of a mutually exclusive one of the READ/WRITE heads **16** that are associated with tracks **15-*n*+1** to **15-*n*+*p***.

Each read winding **16b** is connected to cascaded read amplifier, limiter, and demodulator stages **41** shown as a single block for sake of simplicity. The read and limiting amplifiers remove all amplitude variations from the recorded frequency modulated signals of the tracks being read. The demodulators demodulate the frequency modulated signals being read. The p outputs **41a** of the demodulators of stages **41** provide p analog signals.

The p analog signals, as aforementioned, are in turn weighted with another reference function. The reference function is indicative of the expected target history that is characteristic for the radar system being employed. The weighting operation is provided by the multipliers **42** which are preferably dual channel amplifiers. For this purpose, each multiplier **42** is connected to the output **41*a*** of one of the read amplifier/limiter/demodulator stages **41**. The gain of the multipliers **42** are digitally controllable by a pair of p stage shift re-

gisters 43*a* and 43*b* which provide the amplitude and sign characteristics, respectively, of the reference function. The weighted signals at the multiplier outputs 42*a* are then summed in a summing amplifier 44 which provides correlated output signal components Ccos. The sine portion of the correlator means 5 simultaneously provides a correlated output signal component Csine. The signals Ccos and Csine are combined by suitable arithmetic circuit means 45 which provides a resultant signal Er in response thereto. Output gate 46 periodically gates the output signal Er to the output 47 which as shown in FIG. 1 is connected to the input of utilization device 3.

Gate 46 is controlled by the read stage R of a shift register 48. The first stage W′ of register 48 also advances the write-select register 40 and its last stage E′ advances the erase-select register 49 whose outputs 1E, 2E, . . . PE are connected to the respective erase inputs E of the gates 39 associated with tracks 15-*n*+1 to 15-*n*+*p*, respectively. Register 48 is advanced by the signal S present at the conductor 24′ which is connected to its input. It should be understood that the arithmetic circuit means 45, gate 46, and register 48 are common to both the sine and cosine portions of the correlator means 5 of FIG. 1.

Shift register 48 provides an output signal at one of its outputs each time the register 48 is advanced by a pulse of the input signal S. Consequently, the register 48 first operates the write-select register 40, next operates the read output gate 46, and next the erase-select register 49, whereupon the cycle is repeated. Moreover, the WRITE, READ and ERASE operations are thus performed in mutually exclusive time periods in the preferred operational mode of the correlator means 5. As aforementioned, during the READ operation registers 43a and 43b are simultaneously operated by virtue of their respective inputs being connected to the output of stage R of register 48.

The first output signal appearing at the output of stage W′ of register 48, it is assumed by way of example, causes the first stage of register 40 to provide an output signal at its output 1W which opens the gate 39 associated with track 15-*n*+1. As a consequence, the FM signal present at the output of amplifier 38 is written on track 15-*n*+1. In the given example, when the next pulse of signal S advances the register 48, there appears at the output of stage R a signal which opens gate 46 and allows the output signal Er to be read out of the correlator means 5 of FIG. 1. During a READ operation all of the correlator tracks in the preferred operational mode are read out in parallel in the correlator means 5. When the next pulse of signal S advances the register 48 it provides an output signal at its stage E′ which advances the erase-select register 49 and causes the latter to provide an output signal at one of its stages which erases the next correlator track into which the next FM signal is to be written. For the given example, this would be track 15-*n*+2 and consequently the register 49 would provide an output signal at its output 2E which is connected to the gate 39 associated with that particular track.

When the next pulse of signal S is applied in the given example to the register 48 it returns to its first stage W′ causing the write-select register 40 to advance and an output signal to be present at the output of its second stage 2W. Consequently, the output signal at output 2W opens the gate 39 associated with track 15-*n*+2 and the FM signal from amplifier 38 is written into track 15-*n*+2. Thereafter there follows the parallel readout operation followed by an ERASE operation of the information on the next track, i.e. track 15-*n*+3. After a WRITE operation has been performed on the last track 15-*n*+*p* and followed by the parallel readout operation, an ERASE operation is performed on the first track 15-*n*+1 and the aforedescribed WRITE/READ/ERASE cycle is repeated. In this manner, the oldest information is being continually updated.

Referring now to FIGS. 7*a*–7*e*, 8 an example illustrating the principles of the preferred operational mode of the presummer and correlator means 4, 5 will now be described. It is assumed in the given example for sake of clarity that only a single channel is utilized in the data compactor 2 and that the number of presum tracks is five and are designated in the table of FIG. 8 as tracks T1–T5. Furthermore, it is also assumed that the number of correlator tracks is three and are designated in the table of FIG. 8 as tracks TA–TC. Thus, for the given example, N=8, *n*=*m*=5, and *p*=*P*=3. Accordingly, tracks T1-T5 correspond to the tracks 15-1, 15-2, 15-3, 15-*m*−1, and 15-*m*, respectively, of FIG. 5 and the tracks TA-TC correspond to tracks 15-n+1, 15-n+2, and 15-n+p of FIG. 6.

Moreover, in the given example the first and second coefficient weighting registers 31 and 32, respectively, of FIG. 5 have five stages each corresponding to the assumed number of presum tracks. The outputs of the five stages of register 31 are designated in the table by the reference characters a1, a2, a3, *a*4 and *a*5 and the outputs of the five stages of registers 32 are designated therein by the reference characters *b*1, *b*2, *b*3, *b*4 and b5. Outputs *a*1–*a*5 of the table correspond to the outputs *a*1, *a*2, *a*3, not shown, *am*-1 and *am*, respectively, of register 31 of FIG. 5. The outputs of *b*1-*b*5 of the table correspond to the outputs *b*1, *b*2, *b*3, not shown, *bm*-1 and *bm*, respectively, of the register 32 of FIG. 5. In a similar manner, the amplitude and sign registers 43a and 43*b* each have three stages corresponding to the number of assumed correlator tracks of the given example. The outputs of the three stages of the amplitude register 43a are designated in the table of FIG. 8 as 1A, 2A and 3A and correspond to the outputs 1A, 2A=PA−1, and PA, respectively, of the register 43*a* of FIG. 6. Likewise, the outputs of the three stages of the sign register 43*b* are designated in the table as 1S, 2S and 3S and correspond to the outputs 1S, 2S=PS−1, and PS, respectively, of register 43b of FIG. 6.

Also, for the given assumed example, the ring counter 26 of FIG. 5 has five stages with output designations K1–K5 in the example corresponding to the designations K1, K2, K3, not shown, KM-1 and KM of the ring counter 26 of FIG. 5. Similarly, each of the shift registers 40 and 49 would have three stages. In the given example, the outputs of register 40 are designated as 1W, 2W and 3W and correspond to the outputs of register 40 designated 1W, 2W=PW−1, and PW, respectively, of the register 40 of FIG. 6. Likewise, in the given example the outputs of the register 49 are designated 1E, 2E and 3E and correspond to the outputs 1E, 2E=PE−1, and PE, respectively, of the register 49 of FIG. 6.

Prior to the recording of the data on the drum 15 of FIG. 4 it is assumed that the tracks thereof do not contain any recorded data. At the start of the first revolution which is synchronized with the first transmitted interrogating pulse, the resultant signal S causes a control signal to be present at the output K1 of counter 26. This control signal in turn is fed to the write input W of the gate 25 associated with the first track T1, i.e. track 15-1, thereby opening the particular gate 25. Accordingly, during the first drum revolution designated No. 1 in the table of FIG. 8, the data D10 derived from the returns of the first interrogating signal of the radar apparatus of signal source 1 is written into the first presum track T1. In the table the operation suffixes W, E and R indicate, respectively, WRITE, ERASE and READ operations.

Simultaneously, during the first operation, an ERASE operation E is performed on the presum track T2 as a result of the control signal at output K1 being fed to the erase input E of the gate 39 associated with track T2. A parallel readout operation is also simultaneously performed on the remaining tracks T3, T4 and T5 due to the absence of any control signals to the gates 30 associated with the tracks T3, T4 and T5. However, the control signal at output K1 inhibits the gates 30 associated with tracks T1 and T2 for the reasons previously explained. Moreover, the gate 35 is opened by the control signal S′ of control circuit 36 in response to the signal S derived from the first interrogating radar signal and the information recorded on the tracks T3–T5 being read out and summed in the amplifier 34 is present at the output 35′ of gate 35 during the first revolution. However, since there is no information in the tracks T3–T5 as well as track T2, the data information

prefixes have been omitted in the table of FIG. 8 during revolution No. 1 for sake of clarity.

During the first revolution a WRITE operation W is simultaneously performed in the correlator track TC which would be the composite signal derived from the information, if present, on the tracks T3, T4, T5, as weighted by the weighting coefficients derived from the coaction of the gain control signals present at the outputs *a*3, *a*4 and *a*5, and *b*3, *b*4 and *b*5 to the respective attenuators 28 associated with tracks T3, T4 and T5. However, since under the assumed conditions that there is no information during the first revolution in tracks T3, T4 and T5, as well as the correlator tracks TA and TB, the data information prefixes associated with tracks TA–TC have been omitted in the table of FIG. 8 for sake of clarity.

For purposes that will become apparent from the discussion hereinafter the binary bits at the outputs a1-a5 are set at the beginning of the first revolution in the sequence 0, 0, 0, 1, 0, respectively; and the binary bits at the outputs *b*1–*b*5 are set at the beginning of the first revolution in the sequence 0, 0, 1, 0, 1, respectively. Also prior to the first revolution the binary bits at the outputs 1S, 2S, 3S and the outputs 1A, 2A, 3A are each in the sequence 1, 0, 0, respectively. Likewise, the register 48 is set at the beginning of the first revolution in response to the first signal S to provide an output signal at its first stage W′ which in turn causes the shift register 40 to generate a control signal at the output 3W of its last stage thereby opening gate 39 associated with the track TC and providing the aforementioned WRITE operation thereof. During the first revolution, the binary bit present at the output 3E of the last stage of register 49 is in an up or 1 state. It should be understood that for each of the registers 40, 48, 49 and the ring counter 26, only one of the outputs is in a binary 1 level and the remainder are at the binary 0 level at any given instant of time as is obvious to those skilled in the art. Each time the binary counter 26 and registers 40, 48, 49 are incremented the output of the next succeeding stage is incremented to a 1 level and the binary level of the preceding stage goes from its previous up or 1 level to a 0 or down level. Whenever an output stage of the counter 26 or register 40, 48, 49 goes from a binary 0 to a binary 1 level it provides the aforementioned control signal at the output of the particular stage.

During the next drum revolution No. 2 the information D10 remains on the recorded track T1. Simultaneously, a WRITE operation is performed on track T2 and the data D20 is written into the track T2 while an ERASE operation is being performed on track T3 due to the incrementing of counter 26 in response to the signal S derived from the second radar interrogating signal. Shift register 48 is also advanced by the signal S during the second revolution causing a parallel readout operation R to be simultaneously performed on the correlator tracks TA, TB, TC due to the binary 1 bit previously present at the output of the first stage W′ of register 48 being advanced or shifted to the output of the second stage R. Again, since there is no information contained in the tracks T3–T5 and TA–TC during revolution No. 2, the corresponding data information prefixes have been omitted for sake of clarity in the table of FIG. 8. The same signal S which provides the lastmentioned output signal at output stage R of register 48 also advances the information in the registers 31 and 32 thus placing respective binary 1 bits at outputs *a*-5 and *b*1 and *b*4. The control signal at the output stage R also advances the registers 43*a*, 43*b* thus placing the respective binary 1 bits at the outputs 2A and 2S, respectively.

During revolution No. 3 data information D10 and D20 remain on tracks T1 and T2, respectively, while new data D30 is written into track T3 and an ERASE operation E is performed on track T4. Register 48 is again advanced and a control output signal appears at its last stage E′. The control signal at the output of stage E′ advances register 49 causing the binary 1 bit previously present at the last output 3E to shift to the first output 1E of register 49. Likewise, the respective binary 1 bits previously present at the outputs *a*5 and *b*1 and *b*4 are shifted to the outputs *a*1, *b*2, and *b*5, respectively. Gate 46 remains closed and registers 43*a* and 43*b* are not advanced due to the absence of a control signal at the output of stage R of register 48.

During the fourth revolution No. 4, the gates 30 associated with tracks T4 and T5 are inhibited by the control signal now present at the output K4 of ring counter 26. Simultaneously, the control circuit 36 generates a signal S′ in response to the fourth signal S derived from the fourth interrogating radar signal. The signal S′ opens gate 35 and a parallel READ operation of the information contained in the tracks T1–T3 is performed. The information on the tracks T1–T3 after being weighted in their respective associated attenuators 28 are summed in the summing amplifier 34 and are fed to the input of the FM modulator 37 of the correlator means 5. Simultaneously, WRITE and ERASE operations are being performed on tracks T4 and T5, respectively. The summed information from tracks T1–T3, after modulating the frequency carrier of modulator 37, are written on the first correlator track TA, the shift register 48 having been advanced to its first stage W′ and in turn causing the binary 1 bit at the output 3W of register 40 to shift to the output 1W. The control signal at output 1W in turn opens the gate 39 associated with track TA allowing the data information associated with the FM composite signal to be written on the track TA, as aforementioned. Again, it should be noted that during revolution No. 4 the registers 31 and 32 have been shifted and as a result the information in the tracks T1–T3 are weighted in accordance with the gain control signal contained in these registers at outputs *a*1, *a*2, *a*3 and *b*1, *b*2, *b*3. Again the gate 46 remains opened and registers 43*a* and 43*b* are not shifted due to the absence of the control signal at the stage R of register 48.

At the next revolution No. 5, the data D20, D30 and D40 remain on tracks T2–T4 and new data D50 is written into track T5 while the old data D10 is being erased from track T1. A simultaneous readout operation is performed on the correlator tracks TA, TB, TC which is correlated in accordance with the sign and amplitude bits of the now shifted registers 43*a*, 43*b*. As the drum continues to revolve, the presum tracks are read out in sequential groups. Thus, as shown in the table of FIG. 8, the tracks T1, T2, T3 are read out during revolution No. 4, tracks T4–T5 and T1 are read out during revolution No. 7, tracks T2, T3, T4 are read out during revolution No. 10, etc. On the other hand, each time a group of presum tracks is read out, on the next revolution all the correlator tracks are read out. Thus, tracks TA–TC are read out during revolution No. 8, No. 11, No. 14, etc. It should be noted that at revolution No. 10 the correlator tracks TA–TC are filled with data A10, B10, C10, respectively. Data A10 is derived from the data D10, D20, D30; data B10 is derived from the data D40, D50, D11; and data C10 is derived from data D21, D31, D41. At revolution No. 14 which corresponds to the next parallel readout operation of the correlator tracks TA–TC the information B10 and C10 are still present on tracks TB and TC but, however, new data A11 is now present on the track TA. Data A11 is derived from the data D51, D12, D22. Thus, as is shown by the table of FIG. 8, the presum and correlator track coact to compact the data information contained in the input signals from signal source 1.

In order to understand the weighting function provided by the presummer means 4, reference is made to the waveforms of FIGS. 7*a* and 7*b*. In the respective FIGS. 7*a* and 7*b* the dash dot waveforms represent by way of example the signal envelopes of the information recorded for a given range position on the tracks T1, T2, T3 during revolution No. 4 and on the tracks T4, T5 and T1 during revolution No. 7 referred to in the table of FIG. 8. The weighting function is shown in solid line form in FIGS. 7*a*, 7*b*. By way of example, in the table of FIG. 8 a binary 1 binary 0 bits present in the corresponding *a* and *b* output stages of registers 31 and 32, respectively, that is the corresponding stages which feed the same attenuator 28, causes the gain of the particular attenuator to provide a weighting operation at the horizontal upper level of the

weighting function. However, binary 0 and 1 bits in the corresponding *a* and *b* outputs, respectively, cause the weighting function to be in its intermediate level, and binary 0 bits in both a and *b* outputs cause the weighting function to be in its lower level, each of which cause corresponding reduction of the gain of the attenuator. In FIG. 7a, after the dash dot signal waveform is attenuated by the attenuators **28** associated with tracks **T1, T2, T3**, it produces a resultant output signal which when written on the tracks TA has an envelope characteristic shown by the short dash waveform designated **A10** therein. During the next readout operation which takes place during revolution No. 7, tracks **T4, T5** and **T1** are read out and the weighting reference function is shown symmetrically distributed across the tracks **T4, T5** and **T1**. Signal **B10** is the resultant signal derived from the attenuated signal envelope representing the data **D40** and **D50** and **D11** on tracks **T4, T5** and **T1**, respectively, during revolution No. 7. Thus, the weighting function provided in the presummer tracks focuses the combined signal returns for the groups of tracks being read out in the aforementioned composite signal and is related to the azimuth characteristic of the target point which generates the signal returns on the particular group of presum tracks being read out.

In FIGS. *7c–7e* the dash line waveforms represent the signal envelope of the signals present on the tracks TA, TB, TC for the same range but in successive readout operations associated with drum revolutions Nos. 11, 14 and 17, respectively. As shown in FIGS. *7c–7e*, when the signal of the tracks TA, TB, TC are correlated with the reference function represented by the solid line step waveform, the resulting signal, e.g. signals X1g–X3g, further focuses, that is identifies, the azimuth characteristic of the return signals from which the data being read out on the tracks TA, TB, TC are derived. By way of example, in the table of FIG. **8**, 1 bits in the outputs of corresponding stages of registers **43***a*, **43***b* provide the upper and positive level, e.g. the +1.0 relative level of the reference function shown in FIGS. *7c–7e*; whereas, 0 bits in the corresponding stages' outputs provide the lower and negative level, e.g. the −0.5 relative level of the reference function shown in FIGS. *7c–7e*.

The range information characteristic associated with the signals recorded on the presum and correlator tracks is derived from the a priori knowledge of the time of transmission of the interrogating signals and the resultant return signals thereof.

It should be understood that while the invention has been described in particular preferred embodiments and a preferred operational mode, that the invention could be practiced with other modifications and/or operational modes. For example, while the invention has been described utilizing a common storage means, e.g. drum **15**, for both the presum and correlation information, separate storage means may be employed for storing the presum and correlation data. Moreover, the invention has been described utilizing one recording track per interrogating signal but, as is obvious to those skilled in the art, the tracks may be sectorized so that the returns from successive interrogating signals may be recorded in separate sectors of the same track in which case the read/write and erase apparatus would be modified accordingly, such as for example, for providing plural rows of aligned read/write heads for each track sector in a manner well known to those skilled in the art. Moreover, it should be understood that while the invention has been described using a simple number of presum and correlation tracks for purposes of explanation the more presum and correlation tracks and/or sectors utilized to practice the invention enhances the data compaction capabilities.

Furthermore, the invention has been described in an operational mode that reads out only new information on the presum tracks each time a read out operation is performed thereon. If desired, as is apparent to those skilled in the art, an operational mode employing overlapping readout techniques may also be utilized by appropriate modification.

Thus, while the invention has been particularly shown and described with reference to the preferred embodiments, it will be understood by those skilled in the art that the foregoing and other changes in form and detail may be made therein without departing from the spirit and scope of the invention.

We claim:

1. A data compaction system for compacting sequential input data signals being applied thereto at a predetermined input rate, said system comprising:

presumming means having first output means, said presumming means including

first storage means and first write apparatus means for storing said input data signals in successive first groups in said first storage means, each of said first groups containing a plural first number of successive data signals, first readout apparatus means for successively reading out in a parallel mode each first group of stored signals, and

first summing means for summing the stored data signals of each first group read out from said first storage means to provide at said first output means a first output signal proportional in a predetermined manner to the data signals of the particular first group being summed, said first output signals of said first summing means being sequentially provided thereby at a first output rate less than said input rate;

correlator means having second output means, said correlator means including

second storage means and second write apparatus means for storing said first output signals in successive second groups in said second storage means, each of said second groups containing a plural second number of successive first output signals, second readout apparatus means for successively reading out each second group of stored signals, and

second summing means for summing the stored first output signals of each second group read out from said second storage means to provide at said second output means a second output signal proportional in a predetermined manner to the first output signals of the particular second group being summed, said second output signals of said second means being sequentially provided thereby at a second output rate less than said input rate; and

control means for providing control signals for actuating said first and second write apparatus means and said first and second readout apparatus means in a predetermined relationship, said second write means being actuated each time said first readout means is actuated.

2. A data compaction system according to claim **1** wherein said first and second storage means are comprised as an integral member.

3. A data compaction system according to claim **2** wherein said integral storage member is of the magnetic storage drum type.

4. A data compaction system according to claim **1** further comprising means for adjusting the respective levels of the data signals of each first group in proportion to a predetermined reference function prior to the summation thereof in said first summing means.

5. A data compaction system according to claim **1** further comprising means for adjusting the respective levels of the first output signals of each second group in proportion to a predetermined reference function prior to the summation thereof in said second summing means.

6. A data compaction system according to claim **1** further comprising first adjusting means for adjusting the respective levels of the data signals of each first group in proportion to a predetermined first reference function prior to the summation thereof in said first summing means, and second adjusting means for adjusting the respective levels of the first output signals of each second group in proportion to a predetermined second reference function prior to the summation thereof in said second summing means.

7. A data processing system comprising:
a signal source for providing data signals at a predetermined first rate;
a data compactor having presumming means and correlation means,
said presumming means having first output means and including
first storing means and first write apparatus means for storing said input data signals in successive first groups in said first storage means, each of said first groups containing a plural first number of successive data signals, first readout apparatus means for successively reading out in a parallel mode each first group of stored signals, and
first summing means for summing the stored data signals of each first group read out from said first storage means to provide at said first output means a first output signal proportional in a predetermined manner to the data signals of the particular first group being summed, said first output signals of said first summing means being sequentially provided thereby at a second rate less than said first rate, and said correlator means having second output means, and including
second storage means and second write apparatus means for storing said first output signals in successive second groups in said second storage means, each of said second groups containing a plural second number of successive first out output signals, second readout apparatus means for successively reading out each second group of stored signals, and
second summing means for summing the stored first output signals of each second group read out from said second storage means to provide at said second output means a second output signal proportional in a predetermined manner to the first output signals of the particular second group being summed, said second output signals of said second means being sequentially provided thereby at a third rate less than said first rate; utilization means responsive to said second output signals; and
control means for providing control signals for actuating said first and second write apparatus means and said first and second readout apparatus means in a predetermined relationship, said second write means being actuated each time said first readout means is actuated.

8. A data processing system according to claim 7 wherein said first and second storage means are comprised as an integral member.

9. A data processing system according to claim 8 wherein said integral storage member is of the magnetic storage drum type.

10. A data processing system according to claim 7 further comprising means for adjusting the respective levels of the data signals of each first group in proportion to a predetermined reference function prior to the summation thereof in said first summing means.

11. A data processing system according to claim 7 further comprising means for adjusting the respective levels of the first output signals of each second group in proportion to a predetermined reference function prior to the summation thereof in said second summing means.

12. A data processing system according to claim 7 further comprising first adjusting means for adjusting the respective levels of the data signals of each first group in proportion to a predetermined first reference function prior to the summation thereof in said first summing means, and second adjusting means for adjusting the respective levels of the first output signals of each second group in proportion to a predetermined second reference function prior to the summation thereof in said second summing means.

13. A radar data processing system comprising;
a radar data signal source for providing radar data signals at a predetermined first rate, each of said data signals having predetermined ranges and azimuth information;
a data compactor having presumming means and correlator means,
said presumming means having first output means and including
first storage means and first write apparatus means for storing said input data signals in successive first groups in said first storage means, each of said first groups containing a plural first number of successive data signals, first readout apparatus means for successively reading out in a parallel mode each first group of stored signals, and
first summing means for summing the stored data signals of each first group read out from said first storage means to provide at said first output means a first output signal proportional in a predetermined manner to the data signals of the particular first group being summed, said first output signals of said first summing means being sequentially provided thereby at a second rate less than said first rate, and
said correlator means having second output means, and including
second storage means and second write apparatus means for storing said first output signals in successive second groups in said second storage means, each of said second groups containing a plural second number of successive first output signals, and
second summing means for summing the stored first output signals of each second group read out from said second storage means to provide at said second output means a second output signal proportional in a predetermined manner to the first output signals of the particular second group being summed, said second output signals of said second means being sequentially provided thereby at a third output rate less than said first rate;
utilization means responsive to said second output signals; and
control means for providing control signals for actuating said first and second write apparatus means and said first and second readout apparatus means in a predetermined relationship, said second write means being actuated each time said first readout means is actuated.

14. A radar data processing system according to claim 13 wherein said first and second storage means are comprised as an integral member.

15. A radar data processing system according to claim 14 wherein said integral storage member is of the magnetic storage drum type.

16. A radar data processing system according to claim 13 further comprising means for adjusting the respective levels of the data signals of each first group in proportion to a predetermined reference function prior to the summation thereof in said first summing means.

17. A radar data processing system according to claim 13 further comprising means for adjusting the respective levels of the first output signals of each second group in proportion to a predetermined reference function prior to the summation thereof in said second summing means.

18. A radar data processing system according to claim 13 further comprising first adjusting means for adjusting the respective levels of the data signals of each first group in proportion to a predetermined first reference function prior to the summation thereof in said first summing means, and second adjusting means for adjusting the respective levels of the first output signals of each second group in proportion to a predetermined second reference function prior to the summation thereof in said second summing means.

19. A radar data processing system according to claim 13 wherein said source of plural radar signals further comprises:
a radar transmitter and receiver therefor of a predetermined radar type.

20. A radar data processing system according to claim 19 wherein said radar type is a side-looking pulsed radar system.

21. A radar data compaction system for compacting sequential plural radar data signals being applied thereto at a predetermined input rate, each of said radar data signals having predetermined range and azimuth information characteristics, said system comprising:

presumming means having first output means, said presumming including

first storage means and first write apparatus means for storing said input data signals in successive first groups in said first storage means, number of said first groups containing a plural first number of successive data signals, first readout apparatus means for successively reading out in a parallel mode each each group of stored signals, and

first summing means for summing the stored data signals of each first group read out from said first storage means to provide at said first output means a first output signal proportional in a predetermined manner to the data signals of the particular first group being summed, said first output signals of said first summing means being sequentially provided thereby at a first output rate less than said input rate;

correlator means having second output means, said correlator means including

second storage means and second write apparatus means for storing said first output signals in successive second groups, each of said second groups containing a plural second number of successive first output signals, and

second summing means for summing the stored first output signals of each second group read out from said second storage means to provide at said second output means a second output signal proportional in a predetermined manner to the first output signals of the particular second group being summed, said second output signals of said second means being sequentially provided thereby at a second output rate less than said input rate; and

control means for providing control signals for actuating said first and second write apparatus means and said first and second readout apparatus means in a predetermined relationship, said second write means being actuated each time said first readout means is actuated.

22. A radar data compaction system according to claim 21 wherein said first and second storage means are comprised as an integral member.

23. A radar data compaction system according to claim 22 wherein said integral storage member is of the magnetic storage drum type.

24. A radar data compaction system according to claim 21 further comprising means for adjusting the respective levels of the data signals of each first group in proportion to a predetermined reference function prior to the summation thereof in said first summing means.

25. A radar data compaction system according to claim 21 further comprising means for adjusting the respective levels of the first output signals of each second group in proportion to a predetermined reference function prior to the summation thereof in said second summing means.

26. A radar data compaction system according to claim 21 further comprising first adjusting means for adjusting the respective levels of the data signals of each first group in proportion to a predetermined first reference function prior to the summation thereof in said first summing means, and second adjusting means for adjusting the respective levels of the first output signals of each second group in proportion to a predetermined second reference function prior to the summation thereof in said second summing means.

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