(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
6 July 2006 (06.07.2006)

PCT

(10) International Publication Number
WO 2006/071197 A1

(51) International Patent Classification:
H03K 3/02 (2006.01) *H03F 1/42* (2006.01)
H03K 7/00 (2006.01)

(21) International Application Number:
PCT/SG2004/000429

(22) International Filing Date:
30 December 2004 (30.12.2004)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **AGENCY FOR SCIENCE, TECHNOLOGY AND RESEARCH** [SG/SG]; 20 Biopolis Way, #07-01 Centros, Singapore 138668 (SG).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: **ZHENG, Yuan, Jin** [CN/SG]; Blk 929, Jurong West Street 92, #08-167, Singapore 640929 (SG).

(74) Agent: **VIERING, JENTSCHURA & PARTNER**; P.O. Box 1088, Rochor Road Post Office, Rochor Road, Singapore 911833 (SG).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 2006/071197 A1

(54) Title: FULLY INTEGRATED ULTRA WIDEBAND TRANSMITTER CIRCUITS AND SYSTEMS

(57) Abstract: Disclosed is a novel design of a fully integrated UWB transmitter. The transmitter includes a pulse generator, a pulse modulator, and an ultra-wideband drive amplifier. A new low voltage low power pulse generator circuit is disclosed which can be fully integrated in CMOS or BiCMOS process. This circuit includes a squaring stage, an exponential stage, and a second-order derivative stage. Based on this, PPM, BPSK and PAM pulse modulator circuits and system are disclosed. The modulated pulse is symmetrical second-order derivative Gaussian pulses with a bandwidth up to 5 GHz and having sufficient swing for UWB applications. An ultra-wideband driver amplifier is proposed to amplify the modulator output and drive the antenna. For the driver amplifier, common source resistor and inductor shunt feedback with current reuse technique is employed to achieve the ultra-wideband bandwidth, high gain, and providing matching for the antenna simultaneously.

Fully Integrated Ultra Wideband Transmitter Circuits and Systems

BACKGROUND

[0001] The present invention relates to transmitter circuits and systems, and more particularly to ultra wideband transmitter circuits and systems.

[0002] Ultra-wide band (UWB) is a new and promising technology for high speed, short range and portable wireless communication systems and devices. UWB technology enables new opportunities in the development of short range and high data rate wireless communication applications such as wireless Personal Area Network (PAN), interactive gaming, office networking and indoor communications.

[0003] The design of the building blocks of the UWB wireless transceiver is very demanding due to its simultaneous requirements for ultra-wide bandwidth, high speed, high throughput, low interference and low power consumption. Critical to operation is the generation of vary narrow pulses (typically 0.2-2 nano-seconds) onto which information is modulated. It is extremely difficult to generate sub-nanosecond pulses in pulse generator/modulator circuits whether the circuit be formed either from discrete components due to interconnection discontinuities, and capacitive coupling between components, or in an integrated circuit due to the low isolation and low current gain of the complementary metal oxide semiconductor (CMOS) or bipolar-complementary metal oxide semiconductor (BiCMOS) processes.

[0004] Furthermore, the pulse generator/modulator output is often times too low to drive the antenna, and accordingly a matching network is many times necessary to provide optimal impedance matching to the UWB antenna. Typically however, the matching circuit is not as broadband as the UWB spectrum (e.g., 3.1-10.6 GHz in the U.S), and thus power loss due to impedance mismatch occurs over some part of the transmission band. Additionally, broadband matching networks are typically quite lossy, and thus provide diminishing returns on bandwidth versus output power.

[0005] Accordingly, a need exists for improved UWB transmitter circuits and systems, and which are preferably capable of monolithic integration using CMOS or BiCMOS semiconductor processes.

SUMMARY

[0006] The present invention provides UWB transmitter circuits including a Gaussian pulse generator, an ultra wideband modulator which is based upon the Gaussian pulse generator design, and a driver amplifier. The modulator circuit is configured to provide second-order derivative Gaussian pulses. The driver amplifier is used to provide gain and a broadband impedance matching between the modulator circuit and transmitting antenna such that the modulated UWB pulse is transmitted with high power and low distortion. The aforementioned circuits can be either fabricated separately, or integrated into a UWB transmitter circuit, or alternately formed in a monolithic integrated circuit using, for example, CMOS or BiCMOS semiconductor processing.

[0007] The Gaussian pulse generator circuit, in an exemplary embodiment, includes a squaring stage, an exponential stage, and a second-order derivative stage. The squaring stage includes a first transistor which is configured to operate in the transistor's saturation region. The exponential stage includes a second transistor coupled to the first transistor, the second transistor configured to operate in the transistor's sub-threshold region. The second-order derivative stage includes a capacitive-inductive network coupled to the second transistor, and an output terminal, wherein, when a load is coupled to the output terminal, the real resistance of the load combines with the capacitive-inductive network to provide a second order derivative response.

[0008] The ultra wideband modulator circuit includes the above-described Gaussian pulse generator circuit and a modulation control circuit. The modulator control circuit includes an input configured to receive a control signal and an output coupled to the Gaussian pulse generator circuit, whereby the modulation control circuit operates to modulate the biasing condition of the exponential stage as a function of the control signal.

[0009] The design of the ultra wideband driver amplifier circuit includes a plurality of serial-coupled amplifier stages, each amplifier stage having parallel coupled first and second amplifier stage transistors and a feedback network. Each of the first and second amplifier stage transistors having first, second and third terminals, whereby the first terminals of the first and second amplifier stage transistors are coupled together at a first node, and the third terminal of the first amplifier stage transistor and the second terminal of the second amplifier stage transistor are coupled together at a second node. The feedback network, which includes inductive and resistive elements, is coupled between the first and second nodes.

[0010] The ultra wideband transmitter circuit includes the above-described ultra wideband modulator circuit and the driver amplifier circuit. In a particular embodiment, the transmitter circuit is fabricated as an integrated circuit using either a BiCMOS or CMOS semiconductor process.

[0011] These and other features of the invention will be better understood when viewed in light of the following drawings and detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Fig. 1 illustrates a circuit block diagram of a UWB transceiver in accordance with an embodiment of the present invention.

[0013] Fig. 2 illustrates a Gaussian pulse generator circuit in accordance with an embodiment of the present invention.

[0014] Fig. 3A illustrates a circuit block diagram of an ultra wideband modulator circuit in accordance with one embodiment of the present invention.

[0015] Fig. 3B illustrates an ultra wideband pulse amplitude modulator circuit in accordance with one embodiment of the present invention.

[0016] Fig. 3C illustrates an ultra wideband bipolar phase shift keyed modulator circuit in accordance with one embodiment of the present invention.

[0017] Fig. 3D illustrates the performance of a BPSK modulator constructed in accordance with the present invention.

[0018] Fig. 4 illustrates an ultra wideband driver amplifier circuit in accordance with one embodiment of the present invention.

[0019] Fig. 5A illustrates a simplified block diagram a transmitter circuit constructed in accordance with the present invention.

[0020] Fig. 5B illustrates the performance of an ultra wideband transmitter constructed in accordance with the present invention.

[0021] For clarity, previously identified features retain their reference indicia in subsequent drawings.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0022] A fully integrated UWB transmitter is presented which includes a pulse modulator, an ultra-wideband drive amplifier and an antenna. A low voltage, low power pulse generator circuit is presented which can be fully integrated in CMOS or BiCMOS

process. Based upon the fully integrated pulse generator circuit, new PPM, BPSK and PAM pulse modulator circuits and system are constructed. The modulated pulse is symmetrical second-order derivative Gaussian pulses with a bandwidth up to 5 GHz and having sufficient swing for UWB applications. The ultra-wideband driver amplifier is used to amplify the modulator output and drive the antenna. Additionally, a new design of shunt feedback current reuse common source driver amplifier with resistor and inductor feedback is proposed to achieve the ultra-wideband bandwidth, high gain, and providing matching for the antenna simultaneously. By proper co-design of the modulator, driver amplifier and antenna, the optimum transmitter performance is achieved.

System Overview

[0023] Fig. 1 illustrates a circuit block diagram of a UWB transceiver 100 in accordance with an embodiment of the present invention. The transceiver 100 includes an ultra wideband antenna 105, and receiver components including a matching network 120, low noise amplifier 130, correlator 140, an analog-to-digital converter 150, and data recovery/baseband circuitry 160, for transmitting and receiving UWB signals. Transmitter components include a Gaussian pulse generator 200, UWB modulator 300, and a UWB driver amplifier 400, each of which is further described below. A circulator, diplexer, or switch 110 is used to separate the transmit and receive signals. Synchronization, clock and control signals are provided by means of digital backend circuitry 170.

[0024] During receiving operation, an UWB signal is received at the UWB antenna 105, and supplied to the LNA 130, a broadband impedance matching network 120 being used to provide optimal impedance matching between the LNA input and the antenna. The amplified received signal is subsequently supplied to the correlator 140, the correlated output signals being subsequently converted to digital signals and the baseband data recovered therefrom. The digital backend control provides for the clock generation, synchronization and data processing.

[0025] During a transmitting operation, the Gaussian pulse generator 200 receives a clock signal, and responsive thereto, produces an ultra wideband Gaussian pulse. The UWB modulator 300 receives and modulates the Gaussian pulse responsive to a received control signal. The UWB driver amplifier 400 amplifies the UWB modulated signal,

simultaneously providing broadband impedance matching to the antenna 105 for optimal power transfer. The amplified UWB signal is transmitted from the UWB antenna 105 to a remote UWB receiver.

Gaussian Pulse Generator Circuit

[0026] Fig. 2 illustrates an exemplary embodiment of the Gaussian pulse generator circuit 200 in accordance with the present invention. The circuit 200 includes a squaring stage 220, an exponential stage 240, and a second-order derivative stage 260. The squaring function stage 220 includes a first transistor 222 having a first terminal 222a configured to receive an input signal, a second terminal 222b coupled to a first resistor 224, and a third terminal 222c, whereby the first transistor is configured for biasing in the transistor's saturation region. Such a biasing condition provides the squaring function of the input signal as needed.

[0027] The exponential stage 240 includes a second transistor 242, a third transistor 244, and a second resistor 246. As shown, the second transistor 242 has a first terminal 242a coupled to the first transistor's second terminal 222b, that connection being made via the third transistor 244. The first terminal 242a is also coupled to the second resistor 246, the second transistor 242 being biased to operate in a sub-threshold region to provide the exponential function of the input signal. The third transistor 244 is employed to level shift the first terminal 242a of the second transistor to the correct voltage.

[0028] The second order derivative stage 260 includes a capacitive-inductive network 262 coupled to the second terminal 242b of the second transistor 242 and an output terminal 264, wherein, when a load R_L is coupled to the output terminal, the real resistance of the load R_L combines with the capacitive-inductive network 262 to provide a second order derivative response.

[0029] The output of the pulse generator can be regarded as a second-order derivative Gaussian pulse, which can be characterized as:

$$V_{out}(t) \approx -\frac{2k_e R_L LCe^{5V_{th}/4}}{\lambda V_{th}}\left[1-\frac{2}{\lambda V_{th}}\left(V_{in}(t)-\frac{3V_{th}}{2}\right)^2\right] e^{\frac{-\left(V_{in}(t)-\frac{3V_{th}}{2}\right)^2}{\lambda V_{th}}}$$

where k_e and λ are parameters of the exponential I-V characteristic equation: $I_{DS} = k_e e^{V_{GS}/\lambda}$ and are process dependent, V_{th} is the threshold voltage of the first and third

(MOSFET) transistors 222 and 244, R_L is the load real resistance, and C and L are respective values of the capacitance and inductance of the capacitive-inductive network.

[0030] In the particular embodiment shown, first and third transistors 222 and 244 are n- and p- channel MOSFETs, respectively, and second transistor 242 is a bipolar junction transistor. The power plane is provided at +1.8 VDC and signal ground for each of the transistors is ground potential. An integrated circuit of this arrangement, as will be apparent to those skilled in the art, can be formed using a BiCMOS semiconductor process. Alternatively, an n-channel device biased for operation in its sub-threshold region may replace the bipolar transistor 242, in which case a corresponding integrated circuit may be fabricated using a CMOS semiconductor process.

UWB Modulator Circuit

[0031] The Gaussian pulse generator circuit described herein may also be used with or incorporated in the design of an ultra wideband modulator. Several types of modulators for UWB transmitters are known in the art, for example, pulse position modulators (PPMs), pulse amplitude modulators (PAMs), and binary phase shift-keyed (BPSK) modulators.

[0032] Fig. 3A illustrates a circuit block diagram of an ultra wideband modulator circuit 300 in accordance with one embodiment of the present invention. The modulator 300 includes a Gaussian pulse generator circuit 200 and a modulation control circuit 320. The Gaussian pulse generator circuit 200 is configured to receive an input signal 305, which may be a clock signal, and a modulation signal 325 generated from the modulation control circuit 320. The modulation signal 325 is generated as a response to a control signal (typically the data to be modulated on the UWB signal) input into the modulation control circuit 320. Responsive to the modulation signal 325 (which may be a spectrum spreading chip signal), the pulse generator circuit 200 outputs a modulated second-order Gaussian pulse 350. Several variations of the modulation control circuit 320 are possible, depending upon the desired modulation type. For example, the modulation control circuit may comprise a double-pole, single-throw switch that, responsive to a control signal 315, is switchable between two modulation states. The two modulation states may comprise high and low amplitude states in a pulse amplitude modulation scheme, advanced and delayed states in a pulse position modulation scheme, or positive and negative phases in a binary phase shift keyed modulation scheme. Tertiary, quadrature, or higher order

switching states are of course possible in other embodiments as well. Further, the pulse generator and modulation control circuits may be separately designed and fabricated, or formed on a monolithic integrated circuit.

[0033] Fig. 3B illustrates a first embodiment of the ultra wideband modulation circuit represented in Fig. 3A, the embodiment representing a UWB pulse amplitude modulation circuit 360. The circuit 360 includes a pulse generator circuit having squaring, exponential, and second-order derivative stages 220, 240 and 260, and a modulation control circuit 320, as described above. The squaring stage of the pulse generator circuit 220 includes a first transistor (e.g., an NMOS FET device) having a first terminal 361a configured to receive the input signal 305, and second and third terminals 361b and 361c, respectively. The squaring stage 220 further includes a resistor 362 coupled to the second terminal 361b of the first transistor 361, the transistor 361 being configured for operation in the saturation region.

[0034] The exponential stage 240 includes a second transistor 362 (e.g. a BJT) having a first terminal 362a coupled to the second terminal 361b of the first transistor 361, that connection being made via a third transistor 363. The third transistor 363 (e.g., a PMOS FET) provides sufficient biasing conditions to the second transistor 362, whereby the second transistor 362 operates in the sub-threshold region to produce an exponential response. The second-order derivative stage 260 includes a capacitive-inductive network 364 coupled to the second terminal 362b of the second transistor and an output terminal 365, wherein, when a load R_L is coupled to the output terminal 365, the real resistance of the load R_L 368 combines with the capacitive-inductive network 364 to provide a second order derivative response. In the illustrated embodiment as shown, the third terminals 361c, 362c, and 363c of the first, second and third transistors are coupled to ground potential.

[0035] The modulation control circuit 320 includes transistor 366 having an input terminal configured to receive the control signal 315 and a current mirror 367 coupled to the second transistor 362, whereby the responsive to the input control signal 315, the current mirror 367 produces a modulation signal 325 which alters the biasing condition of the second transistor 362. Consequently, the second transistor 362 produces a modulated exponential response, which, in combination with the second order response provided by stage 260, produces a pulse amplitude modulated UWB pulse signal 350. The circuit can be fabricated as either discrete components or as an integrated circuit. When fabricated as

an integrated circuit, the illustrated circuit can be monolithically formed using a BiCMOS semiconductor process. Alternatively, an n-channel device biased for operation in its sub-threshold region may replace the bipolar transistor 362, in which case a corresponding integrated circuit may be fabricated using a CMOS semiconductor process.

[0036] Fig. 3C illustrates a second embodiment of the ultra wideband modulation circuit represented in Fig. 3A, the embodiment representing a UWB binary phase-shift keyed modulation circuit 370. The circuit 370 includes the aforementioned squaring, exponential and second order derivative stages of the pulse generator circuit and the modulation control stage 320 generally described in Fig. 3A. In this embodiment, the squaring stage 220 includes a first transistor M1 having a first terminal M1a operable to receive the input signal 305 and resistor R1 coupled to the second port M1b, the first transistor M1 being biased for operation in the saturation region. The exponential stage 240 includes, in addition to the second (BJT) transistor Q1 and third (MOSFET) transistor M2A described in Fig. 3B, fourth transistor Q2 and fifth transistor M2B, the second and fourth transistors Q1 and Q2 being arranged as a differential emitter coupled pair degenerated by inductor L_{CS}. Each of the second and fourth transistors are biased for operation in sub-threshold regions to provide complementary exponential responses, their bias levels being set by means of third and fifth transistors M2A and M2B, respectively.

[0037] The second-order derivative stage 260 also includes two sections, the first capacitive-inductive network (C1 & L1) coupled to the second terminal of the second transistor Q1, and the second capacitive-inductive network (C2 & L2) being coupled to the second terminal of the fourth transistor Q2. The two capacitive-inductive networks are coupled to a common output terminal 372 for connection to the output load.

[0038] The modulation control circuit 320 in this embodiment includes sixth, seventh and eighth transistors M4, M3A and M3B and resistors R3 and R4. When a ramp up signal appears at the first terminal of M1, a Gaussian function current flows though the emitter of Q1 then is folded to Q2 by the tail inductor L_{CS}. Hence, two Gaussian function signals (currents) 325a and 325b with reverse polarities are achieved. These currents flow to the capacitive-inductive networks, and then the second-order derivative current of Gaussian pulses with reverse polarities are formed at the output of the capacitive-inductive networks. Seventh and eighth transistors M3A and M3B are used as two transmission gates, and are biased by complimentary control voltages. Thus, only one of the modulated currents 325a or 325b will pass through their respective inductive-

capacitive networks to the load to form a positive or negative pulse. As can be seen, the polarity of output pulse is determined by the control voltage's level. When level of the control signal 315 is high, e.g. representing a positive phase, the output pulse is positive, and vice versa for a low signal representing a negative phase. In this manner, the complementary phases of a binary phase-shift keyed signal are represented in the generated UWB pulse.

[0039] As noted with the other circuits, the circuit may be formed either in discrete components or as an integrated circuit. In the illustrated embodiment in which BJTs and MOSFETs are employed, a BiCMOS process is most suitable. Alternatively, Q1 and Q2 may be replaced with NMOS transistors configured for sub-threshold biasing, and the circuit fabricated as a CMOS integrated circuit.

[0040] Pulse position modulation (PPM) represents another UWB modulation technique, whereby a different time lag is used to identify binary 1s and 0s. For example, a long time lag may be used to represent a 1 bit and a short time lag may represent a 0 bit. As indicated in the pulse generator circuit, the pulse is generated by the edge of the input (typically clock) signal. To generate PPM pulses, the edge location of the input clock signal is modulated by the information data (control signal), and subsequently the edge location modulated pulses can be passed through a pulse generator to produce PPM pulses.

[0041] Fig. 3D illustrates the performance of a BPSK modulator constructed in accordance with the present invention. When the input control voltage is in low level (for example 0V), M3A and M4 is off and M4B is on, thus the Gaussian pulse with positive polarity is output. On the other hand, when the input control voltage is in high level (for example 1.8V), M3A is on, M4 and M4B is off, thus the Gaussian pulse with negative polarity is output.

UWB Driver Amplifier Circuit

[0042] Fig. 4A illustrates an ultra wideband driver amplifier in accordance with one embodiment of the present invention. The UWB driver amplifier is used to amplify the modulated UWB pulse, as well as to provide a broadband impedance match between the modulator and the antenna.

[0043] As shown in Fig. 4A, the UWB driver amplifier 400 includes one or more amplifier stages 420, each amplifier stage including parallel coupled first and second

amplifier stage transistors 422 and 424. Each of the amplifier stage transistors 422 and 424 has first, second, and third terminals, wherein the first (e.g., gate) terminals 422a and 424a are coupled together to form a first node 425, and the third (drain) terminal 422c of the first transistor and the second (drain) terminal 424b of the second transistor are coupled together at a second node 429. Coupled between the first and second nodes 425 and 429 is an inductive-resistive network 426 which provides shunt feedback. In essence, each stage is configured as a shunt feedback common source amplifier stage with resistor and inductor feedback, in which PMOS-NMOS current reuse technique is employed to improve the gm and gain without sacrificing the bandwidth.

[0044] One or more of the amplifier stages may be used to provide sufficient signal gain for transmission. Three cascaded stages are shown in the illustrated embodiment, although fewer or more stages may be used in alternative embodiments. Preferably, the gate peripheries of the first and second transistors 422 and 424 are substantially the same, although different gate peripheries may be employed in alternative embodiments. Additionally, each amplifier stage may have the same total periphery, or alternatively, different stages may have different total gate peripheries, depending upon the design technique. For example, in one embodiment the UWB drive amplifier may employ amplifier stages of successively increasing gate peripheries in order to provide a higher linear output power (IP3) characteristic. In another embodiment, the UWB driver amplifier may employ amplifier stages of substantially the same gate periphery to provide an extremely wide impedance match. These and other design approaches may be adopted in amplifier's architecture.

[0045] Further included in the exemplary UWB driver amplifier embodiment are input and output capacitors 420 and 430, the values of which may be selected to provide DC blocking and/or AC coupling, the latter being used to attenuate any output signals below the USB spectrum low end (3.1 GHz in the US) to a sufficient degree in order to comply with UWB signal emission regulations.

[0046] Additionally, it is well known that the position of the poles and zeros determine the bandwidth and gain of the amplifier. The bandwidth of the UWB driver amplifier is improved by using dominant pole bandwidth enhancement technique which can increase the bandwidth without compromising gain. The small signal equivalent circuit analysis of each stage amplifier shows reveals 2 zeros and 3 poles. Among them, two zeros and two poles remain close to the origin, but the position of the dominant pole

is very far away from the origin. This pole arrangement helps to increase the bandwidth of the amplifier without compromising on gain.

[0047] In a specific embodiment, a three-stage UWB driver amplifier was designed using 0.18 um CMOS technology. Biasing conditions were simulated at 1.8V @ 18 mA. The performance parameters are summarized in Table I below.

Property	Value
-3dB bandwidth	2.2 – 10.1 GHz
S(1,1)	-2.5 to 3.6 dB in 2.2 – 10.1 GHz
S(1,2)	<-46 dB in 2.2 – 10.1 GHz
S(2,1) or Power gain	21 dB in 2.2 – 10.1 GHz
S(2,2)	<-5 dB in 2.2 – 10.1 GHz
IIP3	-8 dBm
Output NF @ 50Ohm	<3.5 dB in 2.2 – 10.1 GHz
Voltage Gain	15 dB in 2.2 – 10.1 GHz
I@V	18.4 mA @1.8 V
Stability Factor, K	>7.8 in 2.2 – 10.1 GHz
Stability measurement	>1.0 in 2.2 – 10.1 GHz

Table I

UWB Transmitter

[0048] Fig. 5A illustrates a simplified block diagram a transmitter circuit constructed in accordance with the present invention. The particular transmitter employs pulse amplitude modulation to communicate baseband data, although BPSK, PPM or any type of modulation technique may be used in accordance with the present invention.

[0049] As shown in Fig. 5A, an input signal 305 and control signal 315 are supplied to a UWB pulse amplitude modulator 510, an exemplary embodiment of which is shown in Fig. 3B. The pulse amplitude modulator 510 outputs Gaussian pulses 520, the amplitude of which is modulated by the level of the control signal 315. The modulated Gaussian pulse 520 is supplied to the driver amplifier circuit 530, an exemplary embodiment of which is shown in Fig. 4. The driver amplifier outputs an amplified Gaussian pulse 535, and additionally provides broadband matching to the UWB antenna 550 gain for maximum power transfer and UWB signal transmission efficiency.

[0050] Fig. 5B illustrates the input/clock, control/modulation and output pulse signals of an UWB transmitter employing the pulse amplitude modulator of Fig. 3B and the driver amplifier circuit shown in Fig. 4. The input/clock signal generates the UWB Gaussian pulse. The control/modulation signal controls the amplitude of the pulse. At the

antenna output, a high amplitude Gaussian pulse with a peak to peak voltage of 142mV to -80mV is generated by a high control signal voltage and a low amplitude Gaussian pulse with a peak to peak voltage of 79mV to -50mV is generated by a low control voltage.

[0051] As shown, a serial data stream of 1 0 1 0 is transmitted. A high amplitude UWB Gaussian pulse is generated when a digital "1" is transmitted and a low amplitude UWB Gaussian pulse is generated when a digital "0" is transmitted. Advantageously, the system simulation indicated that even with additional distortion applied to the signal after transmission, the demodulation performance was not affected significantly when the receiving and transmitting antennas are substantially the same. The power consumption of the PAM UWB transmitter is 0.043W.

[0052] The foregoing description has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously many modifications and variations are possible in light of the disclosed teaching. The described embodiments were chosen in order to best explain the principles of the invention and its practical application to thereby enable others skilled in the art to best utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto.

CLAIMS

What is claimed is:

1. A Gaussian pulse generator circuit, comprising:

a squaring stage, comprising a first transistor having first, second and third terminals and configured to operate in the saturation region;

an exponential stage, comprising a second transistor having a first terminal coupled to the second terminal of the first transistor, a second terminal, and a third terminal, the second transistor configured to operate in the sub-threshold region; and

a second-order derivative stage, comprising an capacitive-inductive network coupled to the second terminal of the second transistor, and an output terminal, wherein, when a load is coupled to the output terminal, the real resistance of the load combines with the capacitive-inductive network to provide a second order derivative response.

2. The Gaussian pulse generator circuit of claim 1, wherein the squaring stage further comprises a first resistor coupled to the second terminal of the first transistor.

3. The Gaussian pulse generator circuit of claims 1 or 2, wherein the exponential stage further comprises:

a second resistor coupled to the first terminal of the second transistor; and

a third transistor having first a first terminal coupled to the second terminal of the first transistor, a second terminal coupled to the first terminal of the second transistor, and a third terminal.

4. The Gaussian pulse generator circuit of one of claims 1-3, wherein the first and third transistors comprise MOSFET transistors, and the second transistor comprises a BJT transistor.

5. The Gaussian pulse generator circuit of one of claims 1-4, wherein the first, second, and third transistors comprise MOSFET transistors.

6. The Gaussian pulse generator circuit of one of claims 1-4, wherein the output voltage is calculated as:

$$V_{out}(t) \approx -\frac{2k_e R_L LCe^{5V_{th}/4}}{\lambda V_{th}}\left[1-\frac{2}{\lambda V_{th}}\left(V_{in}(t)-\frac{3V_{th}}{2}\right)^2\right] e^{\frac{-\left(V_{in}(t)-\frac{3V_{th}}{2}\right)^2}{\lambda V_{th}}}$$

where k_e and λ are parameters of the exponential I-V characteristic equation: $I_{DS} = k_e e^{V_{GS}/\lambda}$, R_L is the load real resistance, and C and L are respective values of the capacitance and inductance of the capacitive-inductive network.

7. The Gaussian pulse generator circuit of one of claims 1-4, wherein the circuit is an integrated circuit monolithically formed using a BiCMOS semiconductor process.

8. The Gaussian pulse generator circuit of one of claims 1-3 or 5, wherein the circuit is an integrated circuit monolithically formed using a CMOS semiconductor process.

9. An ultra wideband modulator circuit, comprising:

a Gaussian pulse generator circuit, comprising:

a squaring stage, comprising a first transistor having first, second and third terminals, the first transistor configured to receive an input signal at the first terminal and to operate in the saturation region;

an exponential stage, comprising a second transistor having a first terminal coupled to the second terminal of the first transistor, a

second terminal, and a third terminal, the second transistor configured to operate in the sub-threshold region; and

a second-order derivative stage, comprising a first capacitive-inductive network coupled to the second terminal of the second transistor, and an output terminal, wherein, when a load is coupled to the output terminal, the real resistance of the load combines with the first capacitive-inductive network to provide a second order derivative response; and

a modulation control circuit having an input configured to receive a control signal and an output coupled to the Gaussian pulse generator circuit, the modulation control circuit configured to modulate the biasing condition of the exponential stage as a function of the input control signal.

10. The ultra wideband modulator circuit of claim 9, wherein the squaring stage further comprises a first resistor coupled to the second terminal of the first transistor.

11. The ultra wideband modulator circuit of claims 9 or 10, wherein the exponential stage further comprises a third transistor having first a first terminal coupled to the second terminal of the first transistor, a second terminal coupled to the first terminal of the second transistor, and a third terminal.

12. The ultra wideband modulator circuit of one of the claims 9-11, wherein the modulation control circuit comprises:

a fourth transistor having a control port for receiving a control signal, a first port and a second port; and

a current mirror circuit having a first port coupled to the first port of the fourth transistor, a second port coupled to the control port of the second transistor, and a third port coupled to the inductor-capacitor network.

13. The ultra wideband modulator circuit of one of the claims 9-12, wherein the first, third and fourth transistors each comprise a MOSFET transistor, and the second transistor comprises a BJT transistor.

14. The ultra wideband modulator circuit of one of the claims 9-13, wherein the circuit is an integrated circuit monolithically formed using a BiCMOS process.

15. The ultra wideband modulator circuit of one of the claims 9-12, wherein each of the first, second, third and fourth transistors comprise a MOSFET transistor, and wherein the circuit is an integrated circuit monolithically formed using a CMOS process.

16. The ultra wideband modulator circuit of one of the claims 11, wherein the exponential stage further comprises:

a fourth transistor having a first terminal coupled to the third terminal of the first transistor, a second terminal, and a third terminal coupled to the third terminal of the second transistor; and

a fifth transistor having first a first terminal coupled to the second terminal of the second transistor, a second terminal coupled to the third terminal of the first transistor, and a third terminal.

wherein the second and fourth transistors operate in a differential manner.

17. The ultra wideband modulator circuit of claims 16, wherein the second order derivative circuit further comprises a second-order derivative stage coupled to the second terminal of the second transistor and to the output terminal, wherein, (i) when a load is coupled to the output terminal and the second transistor is conducting, the real resistance of the load combines with the first capacitive-inductive network to provide a second order derivative response, and (ii) when a load is coupled to the output terminal and the fourth transistor is conducting, the real resistance of the load combines with the second capacitive-inductive network to provide a second order derivative response.

18. The ultra wideband modulator circuit of claim 17, wherein the modulation control circuit comprises:

a sixth transistor having a first terminal configured to receive the control signal, a second terminal and a third terminal;

a seventh transistor interposed between the first capacitive-inductive network and the output terminal, the seventh transistor having a first terminal coupled to the first terminal of the sixth transistor, a second terminal coupled to the first capacitive-inductive network and a third terminal coupled to the output terminal; and

an eighth transistor interposed between the second capacitive-inductive network and the output terminal, the eighth transistor having a first terminal coupled to the second terminal of the seventh transistor, a second terminal coupled to the output terminal, and a third terminal coupled to the second capacitive-inductive network.

19. The ultra wideband modulator circuit of claim 18, wherein the first, third, fifth, sixth and seventh transistors are MOSFET transistors and the second and fourth transistors are BJT transistors.

20. The ultra wideband modulator circuit of claim 19, wherein the circuit is an integrated circuit monolithically formed using a BiCMOS semiconductor process.

21. A ultra wideband driver amplifier circuit comprising one or more serial-coupled amplifier stages, each amplifier stage comprising:

parallel coupled first and second amplifier stage transistors, each of the first and second amplifier stage transistors having first, second and third terminals, wherein the first terminals of the first and second amplifier stage transistors are coupled together at a first node, and the third terminal of the first amplifier stage transistor and the second terminal of the second amplifier stage transistor are coupled together at a second node; and

a feedback network coupled between the first and second nodes, the feedback network comprising an inductive element and a resistive element.

21. The ultra wideband driver amplifier circuit of claim 20, further comprising a capacitor having a first port for receiving an input signal and a second port coupled to the first node of the first of the one or more amplifier stages.

22. The ultra wideband driver amplifier circuit of claim 21, further comprising a capacitor having a first port coupled to second node of the last of the one or more amplifier stages and a second port for providing an output signal.

23. The ultra wideband driver amplifier circuit of claim 20, wherein the gate periphery of the first and second amplifier stage transistors within the same amplifier stage is substantially matched.

24. The ultra wideband driver amplifier circuit of claim 20, wherein the first and second amplifier stage transistors of different amplifier stages are of different gate peripheries.

25. The ultra wideband driver amplifier circuit of claim 20, wherein the first and second amplifier stage transistors of different amplifier stages are of substantially the same gate periphery.

26. The ultra wideband driver amplifier of claim 20, wherein the first and second amplifier stage transistors comprise a PMOS transistor and an NMOS transistor, respectively, and wherein the circuit is an integrated circuit monolithically formed using a CMOS semiconductor process.

27. The ultra wideband driver amplifier of claim 27, wherein the circuit is an integrated circuit monolithically formed using a BiCMOS semiconductor process.

28. An ultra wideband transmitter circuit, comprising:

an ultra wideband modulator circuit, comprising:

a squaring stage, comprising a first transistor having first, second and third terminals and configured to operate in the saturation region;

an exponential stage, comprising a second transistor having a first terminal coupled to the second terminal of the first transistor, a second terminal, and a third terminal, the second transistor configured to operate in the sub-threshold region;

a second-order derivative stage, comprising an capacitive-inductive network coupled to the second terminal of the second transistor, and an output terminal; and

a modulation control circuit having an input configured to receive a modulation control signal and an output coupled to the Gaussian pulse generator circuit, the modulation control circuit configured to modulate the biasing condition of the exponential stage as a function of the modulation control signal; and

a driver amplifier having an input coupled to the output terminal of the second-order derivative stage and an output, the driver amplifier providing the real resistance component to the capacitive-inductive network to produce a second-order derivative signal at the driver amplifier input, the driver amplifier comprising one or more serial-coupled amplifier stages, wherein each amplifier stage comprises:

parallel coupled first and second amplifier stage transistors, each of the first and second amplifier stage transistors having first, second and third terminals, wherein the first terminals of the first and second amplifier stage transistors are coupled together at a first node, and the third terminal of the first amplifier stage transistor and the second terminal of the second amplifier stage transistor are coupled together at a second node; and

a feedback network coupled between the first and second nodes, the feedback network comprising an inductive element and a resistive element.

29. The ultra wideband transmitter circuit of claim 28, wherein the squaring stage further comprises a first resistor coupled to the second terminal of the first transistor.

30. The ultra wideband transmitter circuit of claims 28 or 29, wherein the exponential stage further comprises a third transistor having first a first terminal coupled to the second terminal of the first transistor, a second terminal coupled to the first terminal of the second transistor, and a third terminal.

31. The ultra wideband transmitter circuit of one of the claims 28-30, wherein the modulation control circuit comprises:

a fourth transistor having a control port for receiving a modulation control signal, a first port and a second port; and

a current mirror circuit having a first port coupled to the first port of the fourth transistor, a second port coupled to the control port of the second transistor, and a third port coupled to the inductor-capacitor network.

32. The ultra wideband transmitter circuit of one of the claims 28-31, wherein the first, third and fourth transistors each comprise a MOSFET transistor, and the second transistor comprises a BJT transistor.

34. The ultra wideband modulator circuit of one of the claims 28-29, wherein the exponential stage further comprises:

a fourth transistor having a first terminal coupled to the third terminal of the first transistor, a second terminal, and a third terminal coupled to the third terminal of the second transistor; and

a fifth transistor having first a first terminal coupled to the second terminal of the second transistor, a second terminal coupled to the third terminal of the first transistor, and a third terminal.

wherein the second and fourth transistors operate in a differential manner.

35. The ultra wideband transmitter circuit of claims 34, wherein the second order derivative circuit further comprises a second-order derivative stage coupled to the second terminal of the second transistor and to the output terminal, wherein, (i) when a load is coupled to the output terminal and the second transistor is conducting, the real resistance of the load combines with the first capacitive-inductive network to provide a second order derivative response, and (ii) when a load is coupled to the output terminal and the fourth transistor is conducting, the real resistance of the load combines with the second capacitive-inductive network to provide a second order derivative response.

36. The ultra wideband transmitter circuit of claim 35, wherein the modulation control circuit comprises:

a fifth transistor having a first terminal configured to receive the modulation control signal, a second terminal and a third terminal;

a sixth transistor interposed between the first capacitive-inductive network and the output terminal, the sixth transistor having a first terminal coupled to the first terminal of the fifth transistor, a second terminal coupled to the first capacitive-inductive network and a third terminal coupled to the output terminal; and

a seventh transistor interposed between the second capacitive-inductive network and the output terminal, the seventh transistor having a first terminal coupled to the second terminal of the fifth transistor, a second terminal coupled to the output terminal, and a third terminal coupled to the second capacitive-inductive network.

37. The ultra wideband transmitter circuit of claim 28, further comprising a capacitor having a first port for receiving an input signal and a second port coupled to the first node of the first of the one or more amplifier stages.

38. The ultra wideband transmitter circuit of claim 37, further comprising a capacitor having a first port coupled to second node of the last of the one or more amplifier stages and a second port for providing an output signal.

39. The ultra wideband transmitter circuit of claim 28, wherein the gate periphery of the first and second amplifier stage transistors within the same amplifier stage is substantially matched.

40. The ultra wideband transmitter circuit of claim 28, wherein the first and second amplifier stage transistors of different amplifier stages are of different gate peripheries.

41. The ultra wideband transmitter circuit of claim 28, wherein the first and second amplifier stage transistors of the different amplifier stages are of substantially the same gate peripheries.

42. The ultra wideband transmitter circuit of one of the claims 28-41, wherein the circuit is an integrated circuit monolithically formed using a BiCMOS process.

43. The ultra wideband transmitter circuit of one of the claims 28-41, wherein the circuit is an integrated circuit monolithically formed using a CMOS process.

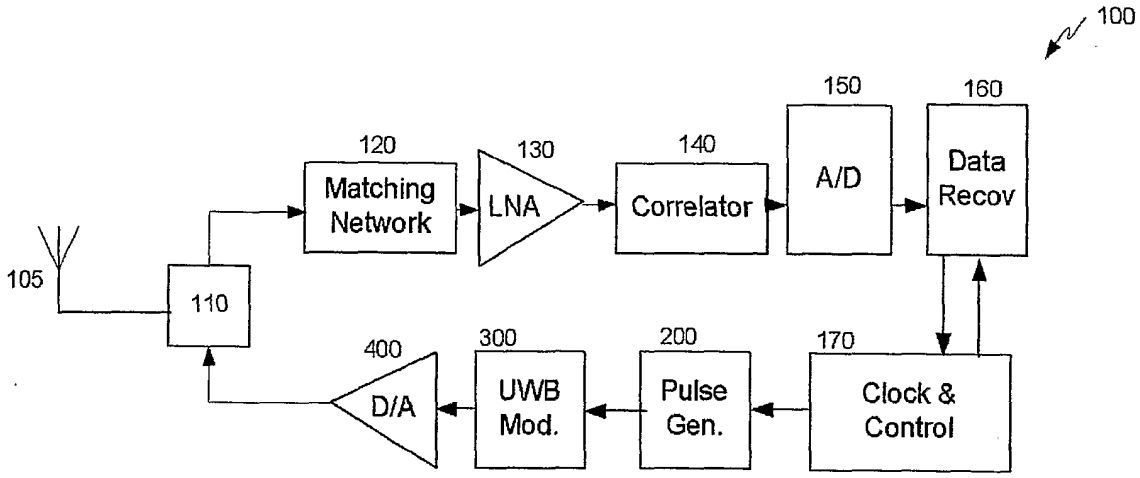
100
105
110
120
Matching Network
130
LNA
140
Correlator
150
A/D
160
Data Recov
170
Clock & Control
200
Pulse Gen.
300
UWB Mod.
400
D/A

Fig. 1

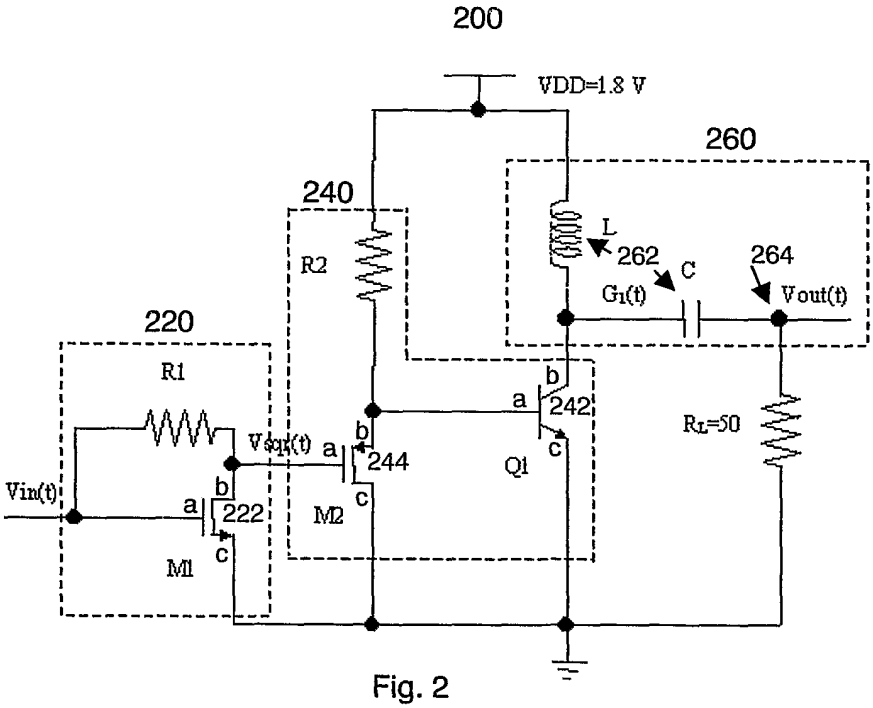
200
VDD=1.8 V
260
240
L
262
C
264
R2
G1(t)
Vout(t)
220
R1
Vin(t)
Vg1(t)
244
242
RL=50
Q1
222
M2
M1

Fig. 2

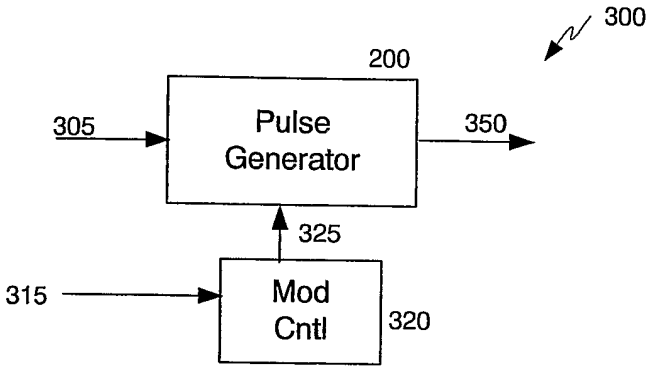
300
200
305
Pulse Generator
350
325
315
Mod Cntl
320

Fig. 3A

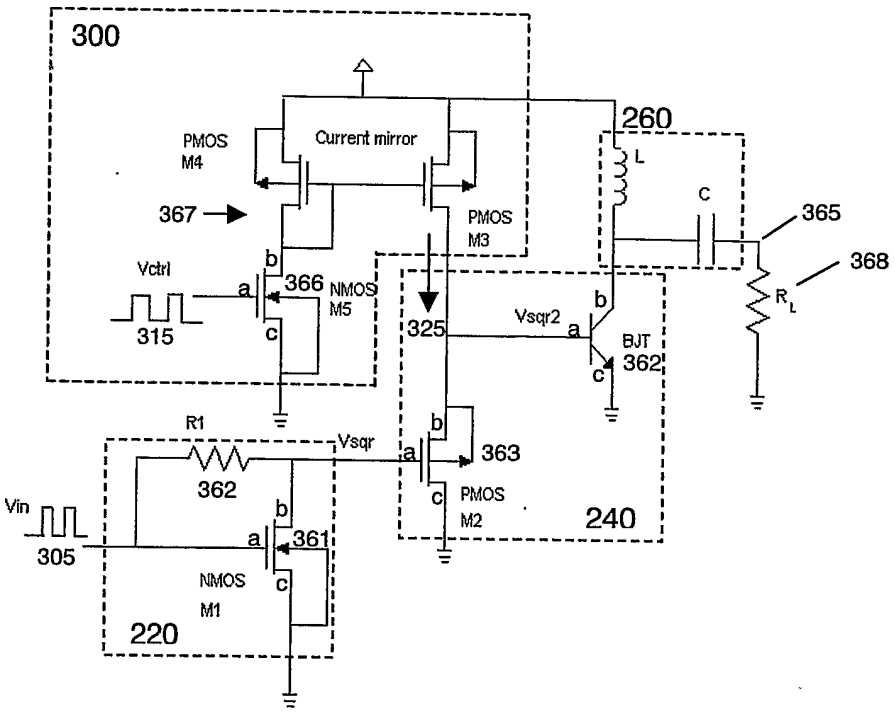
300
PMOS M4
Current mirror
260
L
C
365
368
367
PMOS M3
Vctrl
366
NMOS M5
315
325
Vsqr2
BJT 362
R_L
R1
Vsqr
363
362
PMOS M2
240
Vin
305
361
NMOS M1
220

Fig. 3B

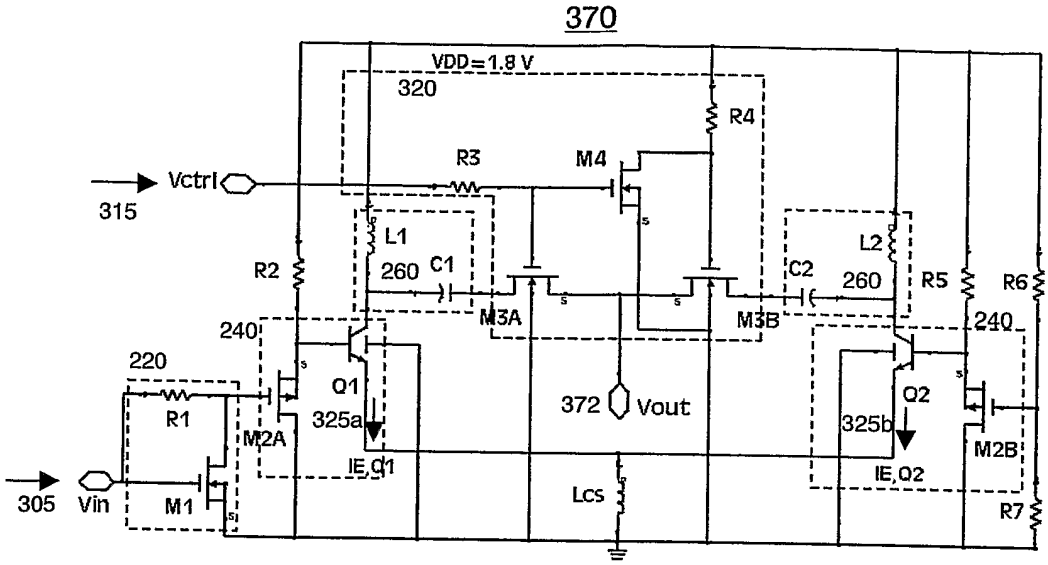
370
VDD=1.8 V
320
R4
R3
M4
Vctrl
315
L1
260
C1
R2
L2
C2
260
R5
R6
M3A
M3B
240
240
220
Q1
325a
372
Vout
Q2
325b
R1
M2A
M2B
IE,Q1
IE,Q2
Lcs
305
Vin
M1
R7

Fig. 3C

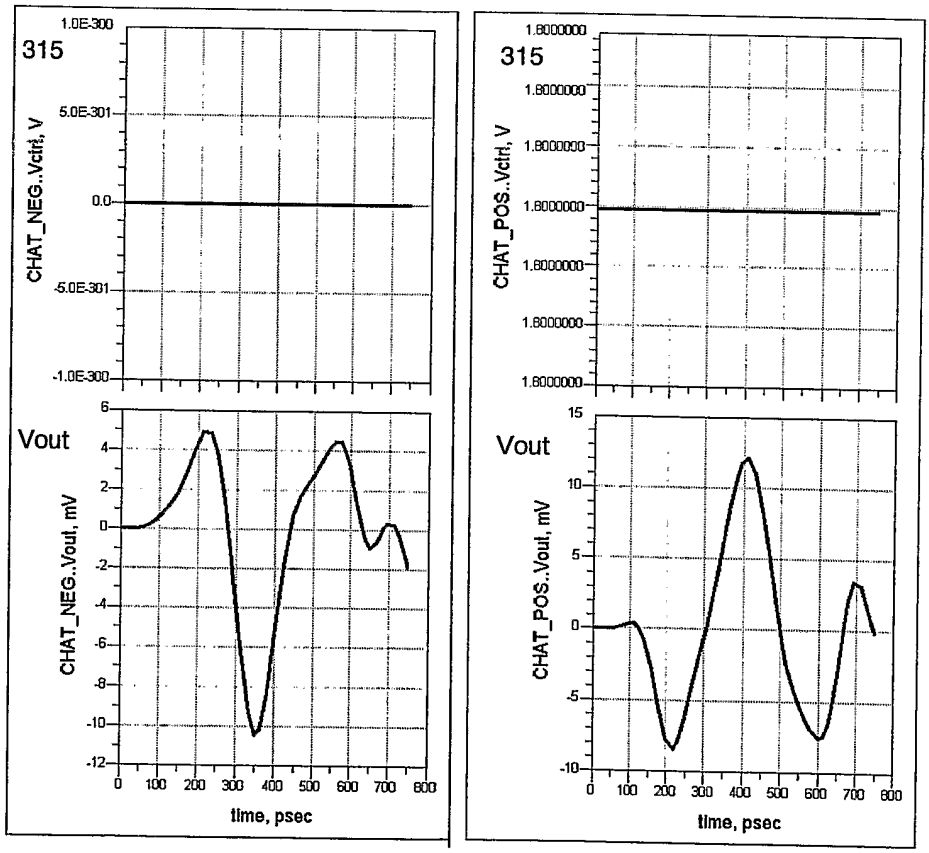
315
CHAT_NEG..Vctrl, V
1.0E-300
5.0E-301
0.0
-5.0E-301
-1.0E-300
Vout
CHAT_NEG..Vout, mV
time, psec
315
CHAT_POS..Vctrl, V
Vout
CHAT_POS..Vout, mV
time, psec

Fig. 3D

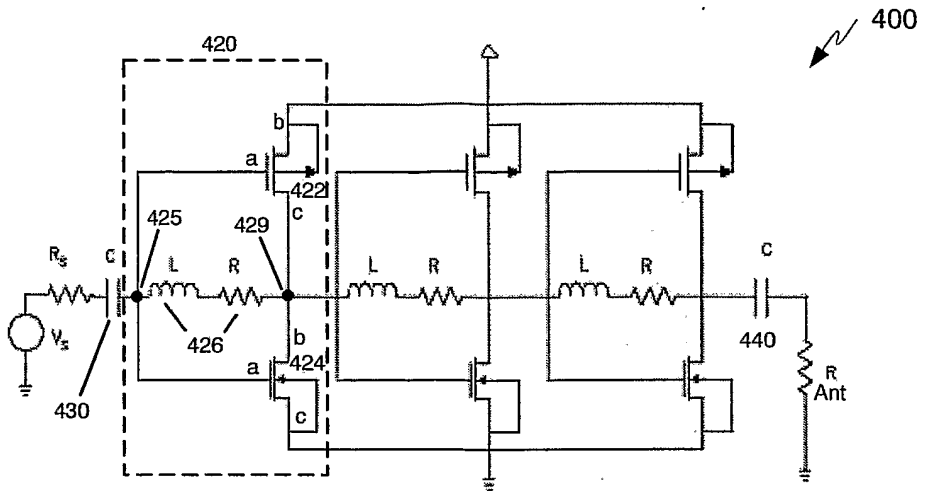
400
420
b
a
422
c
425
429
R_S
C
L
R
L
R
L
R
C
V_S
426
440
b
a
424
c
R
Ant
430

Fig. 4

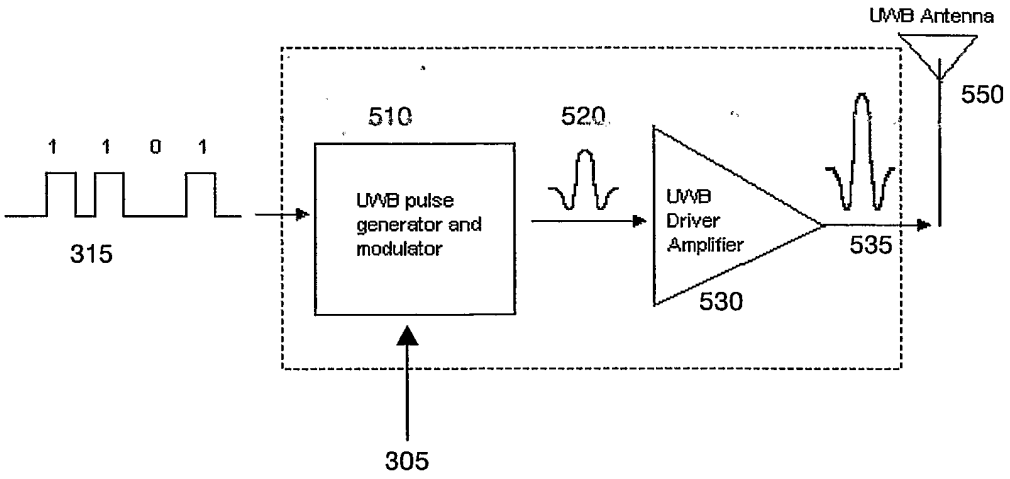
UWB Antenna
550
510
520
1 1 0 1
UWB pulse generator and modulator
UWB Driver Amplifier
535
315
530
305

Fig. 5A

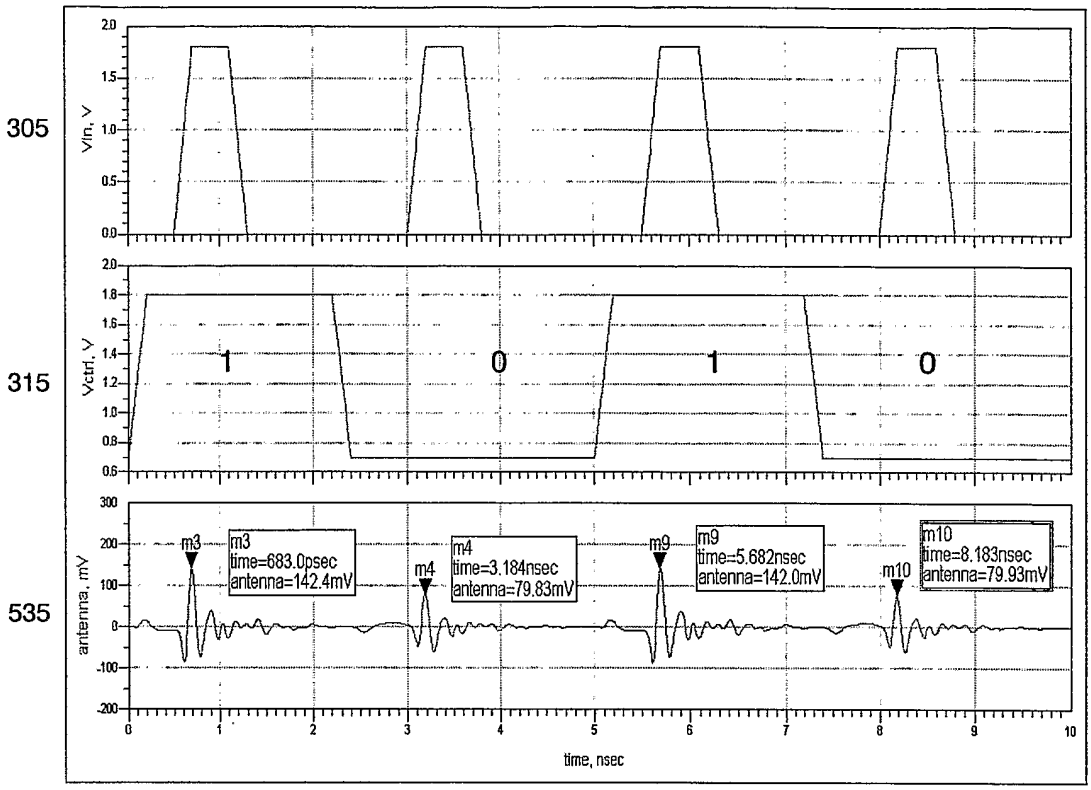
305
315
535
Vin, V
Vctrl, V
1
0
1
0
antenna, mV
m3
time=683.0psec
antenna=142.4mV
m4
time=3.184nsec
antenna=79.83mV
m9
time=5.682nsec
antenna=142.0mV
m10
time=8.183nsec
antenna=79.93mV
time, nsec

Fig. 5B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2004/000429

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. [7]: H03K 3/02, 7/00; H03F 1/42

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPAT, USPTO, JPO, ESP@CE and INTERNET; Keywords (UWB, Gaussian, pulse, modulation, circuit, amplifier, transistors, feedback, parallel) and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN JP 2004-187113 A (SONY CORP.) 2 July 2004	1 – 20, 28 - 43
A	TERADA T., et al., TRANSCEIVER CIRCUITS FOR PULSE BASED ULTRA-WIDEBAND [online], Department of Electrical Engineering, Keio University, Japan, IEEE ISCAS 2004, 26 May 2004, [Retrieved on 10 March 2005], Retrieved from The Internet:< http://www.kuroda.elec.keio.ac.jp/pdf/kuroda/2004/2004_17.pdf	1 – 20, 28 - 43
A	AYADI J., et al., ULTRA-WIDEBAND INVESTIGATIONS FOR LOW DATA RATE WIRELESS PERSONAL AREA NETWORK [online], Centre Suisse d'Electronique et de Microtechnique (CSEM) Wireless Communications Section, Switzerland, SETIT 2004, March 15-20 2004, [Retrieved on 10 March 2005], Retrieved from The Internet:< http://www.imec.be/pacwoman/publications/WP8-CSEM-SETIT2004_457-21-01-2004-V1.0.pdf	1 – 20, 28 - 43

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 March 2005	24 MAR 2005
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized officer **BEN TUOHY** Telephone No : (02) 6283 7918

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2004/000429

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	LOU X., et al., DESIGNING OPTIMAL PULSE-SHAPERS FOR ULTRA-WIDEBAND RADIOS [online], Journal of Communications and Networks, vol. 5, no. 4, December 2003, [Retrieved on 10 March 2005], Retrieved from The Internet :< http://spincom.ece.umn.edu/papers03/jcn03lyg.pdf	1 – 20, 28 – 43
A	US 6670850 B1 (ROACH) 30 December 2003 See whole document	20 – 43
A	PATENT ABSTRACTS OF JAPAN JP 2002-043866 A (SANYO ELECTRIC CO LTD) 8 February 2002	20 – 43
A	PATENT ABSTRACT OF JAPAN JP 2000-101408 A (HITACHI LTD) 7 April 2000	20 – 43
A	DERWENT WORLD PATENT ABSTRACTS Accession No. 87-305054/43, class U23 SU 1298-935 A (AGARKOV E. V.) 23 March 1987	20 - 43

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2004/000429

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See supplemental box

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

Supplemental Box
(To be used when the space in any of Boxes I to VIII is not sufficient)

Continuation of Box No: III

The international application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept. In coming to this conclusion the International Searching Authority has found that there are two inventions:

- Claims 1 – 20 are directed to a Gaussian pulse generator circuit. The circuit configuration of the squaring stage, exponential stage and second-order derivative stage are considered to be a first "special technical feature."
- Claims 21 - 43, directed to an ultra wideband driver amplifier circuit. The circuit configuration of the ultra wideband driver amplifier is considered to be a second "special technical feature."

Since these two groups of claims do not share either of the special technical features identified, a "technical relationship" between the inventions, as defined in PCT rule 13.2, does not exist. Accordingly, the international application does not relate to one invention or to a single inventive concept.

As the search for the second invention will require more than a little additional effort over that for the first, an additional search fee is warranted.

INTERNATIONAL SEARCH REPORT

Information on patent family members

nternational application No.

PCT/SG2004/000429

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report	Patent Family Member
JP	2004187113
US	6670850
JP	2002043866
JP	2000101408
SU	1298935

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX