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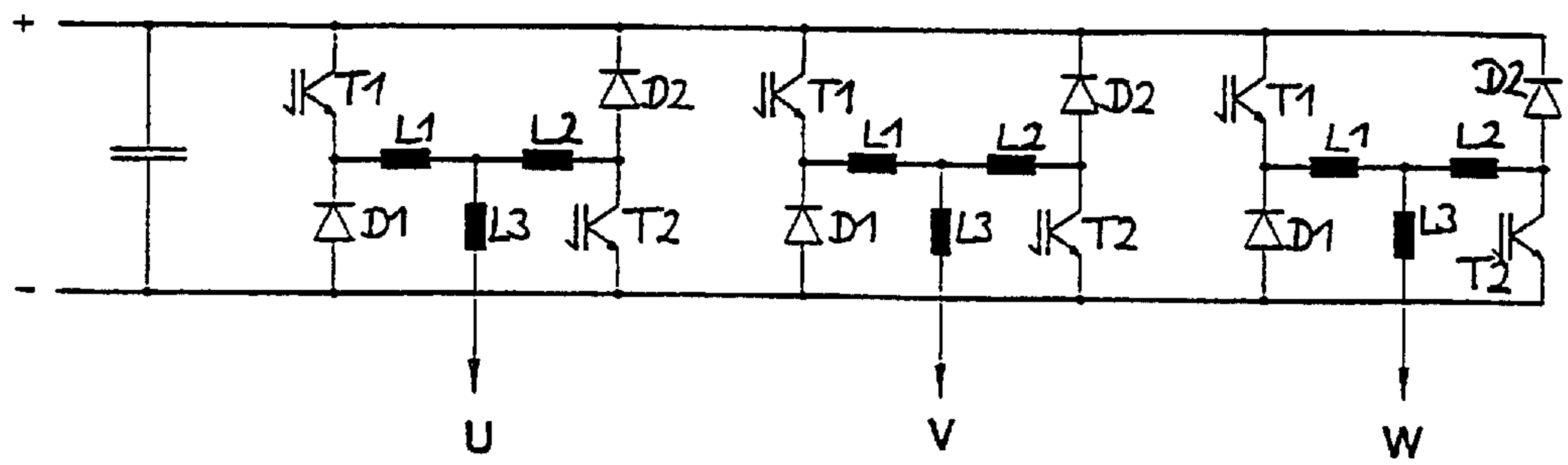
(54) **ONDULEUR POUR L'INJECTION DE COURANTS SINUSOIDAUX DANS UN RESEAU ALTERNATIF**

(54) **INVERTER FOR INPUTTING SINUSOIDAL CURRENTS INTO AN ALTERNATING CURRENT NETWORK**



(57) L'invention concerne un onduleur pour l'injection de courants sinusoïdaux dans un réseau alternatif. Elle vise à améliorer la résistance aux courts-circuits et à en limiter le risque. L'invention part de la conclusion qu'une seule unité de commutation est nécessaire pour la production d'une demi-période d'une oscillation sinusoïdale. Pour la production d'une demi-période positive d'une oscillation sinusoïdale, on utilise donc une autre unité de commutation que pour la production de la partie négative du courant sinusoïdal. Il s'ensuit que pendant la production d'une demi-période positive, un seul commutateur d'une unité de commutation est cadencé ou actionné, et que pendant la production de la demi-période négative d'un courant sinusoïdal, un autre commutateur est actionné. Le risque d'un court-circuit entre ces deux commutateurs est ainsi limité à la durée du passage de la demi-période positive à la demi-période négative ou de la demi-période négative à la demi-période positive.

(57) The invention relates to an inverter for inputting sinusoidal currents into an alternating current network. The invention seeks to improve resistance to short circuiting and to reduce the risk thereof. According to the invention, only one switching unit is used to generate a semi-oscillation of a sinusoidal oscillation. In order to generate a positive semi-oscillation of a sinusoidal oscillation, a second switching unit is used in addition to the one used to generate the negative component of a sinusoidal current. As a result, only one switch pertaining to a switching unit is clocked or actuated to generate a positive semi-oscillation. Another switch is clocked or actuated to generate a negative semi-oscillation of a sinusoidal current. The risk of a short circuit between both switches is thus reduced to the period occurring between switching from the positive to the negative or from the negative to the positive semi-oscillation.

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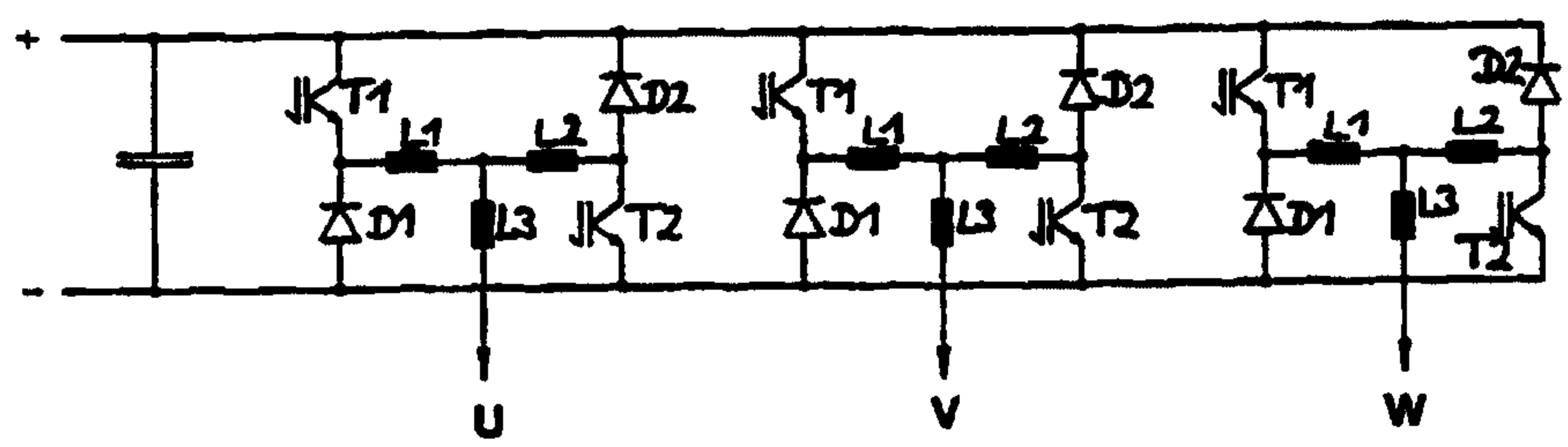
(54) Title: INVERTER FOR INPUTTING SINUSOIDAL CURRENTS INTO AN ALTERNATING CURRENT NETWORK

(54) Bezeichnung: WECHSELRICHTER FÜR DIE EINSPEISUNG SINUSFÖRMIGER STRÖME IN EIN WECHSELSTROMNETZ



(57) Abstract

The invention relates to an inverter for inputting sinusoidal currents into an alternating current network. The invention seeks to improve resistance to short circuiting and to reduce the risk thereof. According to the invention, only one switching unit is used to generate a semi–oscillation of a sinusoidal oscillation. In order to generate a positive semi–oscillation of a sinusoidal oscillation, a second switching unit is used in addition to the one used to generate the negative component of a sinusoidal current. As a result, only one switch pertaining to a switching unit is clocked or actuated to generate a positive semi–oscillation. Another switch is clocked or actuated to generate a negative semi–oscillation of a sinusoidal current. The risk of a short circuit between both switches is thus reduced to the period occurring between switching from the positive to the negative or from the negative to the positive semi–oscillation.

(57) Zusammenfassung

Die Erfindung betrifft einen Wechselrichter für die Einspeisung sinusförmiger Ströme in ein Wechselstromnetz. Es ist Aufgabe der vorliegenden Erfindung, die Kurzschlußfestigkeit zur verbessern und die Kurzschlußgefahr zu verringern. Der Erfindung liegt die Erkenntnis zugrunde, für die Erzeugung einer Halbschwingung einer Sinusschwingung nur eine einzige Schaltungseinheit zu verwenden. Für die Erzeugung einer positiven Halbschwingung einer Sinusschwingung wird somit einen andere Schaltungseinheit verwendet als für die Erzeugung des negativen Teils des Sinusstromes. Dies hat zur Folge, daß während der Erzeugung einer positiven Halbschwingung nur ein Schalter einer Schaltungseinheit getaktet bzw. betätigt wird und während der Erzeugung der negativen Halbschwingung eines Sinusstromes ein anderer Schalter. Die Gefahr eines Kurzschlusses zwischen beiden Schaltern wird somit auf die Zeit während des Wechsels von der positiven zur negativen bzw. von der negativen zur positiven Halbschwingung reduziert.

INVERTER FOR INPUTTING SINUSOIDAL CURRENTS INTO AN ALTERNATING CURRENT NETWORK

Technical Field

The invention relates to an inverter for inputting sinusoidal currents into an alternating current network or a public power supply network.

Background

The power switches used to form such inverters are typically arranged in a prior art three-phase bridge configuration, as shown in Figure 13. The inverter generates alternating current having three phases U, V, and W from a dc voltage source. Anti-parallel switching of power switches T1 to T6, shown in Figure 13, using corresponding diodes, enables four-quadrant operation, facilitating use of such inverter circuits in many applications.

The disadvantage of such an inverter circuit is that in the event of a short circuit across two switches, e.g. T1 and T2, extremely large energy flows occur, which typically causes complete destruction of the inverter, and may start a fire, with consequential destruction of all connected system components. The objective of the present invention is to improve resistance to short circuiting and reduce the risk thereof.

Summary of Invention

The invention uses separate switching circuits to produce different semi-oscillations of a sinusoidal signal. One switching circuit produces the positive semi-oscillation of the sinusoidal signal, and another switching circuit produces the negative semi-oscillation.

Accordingly, one switch in the first switching circuit is clocked or actuated during production of the positive semi-oscillation, while a different switch in a second switching circuit is active during production of the negative semi-oscillation. The danger of a short circuit between the two switches is thus limited to the time during the changeover from the positive to the negative, or from the negative to the positive, semi-oscillation.

Because each switching circuit is responsible for the generation of only one semi-oscillation of the sinusoidal oscillation, the switching circuits responsible for different semi-oscillations can be physically separated. This improves the safety of the switching system components and simplifies the spatial arrangement.

Preferably, the supplied dc voltage is divided into first and second partial dc voltages. The first partial dc voltage is used, e.g. to produce the positive component of the mains current, and the second partial dc voltage is used to produce the negative component. For example, if the two partial dc voltages are 660V each, the total dc voltage is 1320V. The components used in the first switching circuit need only process the first partial dc voltage, while the components of the second switching circuit are maximally loaded by the second partial dc voltage. The equivalent is true for inductances and potential semiconductor switching elements connected to the switching circuits. Thus, considerable cost savings are possible, since the components do not have to be designed to be as puncture proof those employed in the Figure 13 prior art inverter. In other words, the output power of the inverter as a whole can be doubled, while using components that only have to process a partial dc voltage.

Brief Description of Drawings

Figure 1 is an electronic circuit schematic diagram of a switching circuit for generating the positive component of the mains current, in accordance with the invention.

Figure 2 is an electronic circuit schematic diagram of a switching circuit for generating the negative component of the mains current, in accordance with the invention.

Figure 3 is an electronic circuit schematic diagram of a single phase inverter incorporating the switching circuits of Figures 1 and 2.

Figure 4 is an electronic circuit schematic diagram of a three phase inverter incorporating the switching circuits of Figures 1 and 2 to produce an output current having three phases U, V, and W.

Figure 5 is a graph depicting the time and current switching behaviour of triggering switches T1 and T2 depicted in the switching circuits of Figures 1 and 2.

Figure 6 shows how the circuit of Figure 4 can be adapted to produce an output current having a single phase U.

Figure 7 is an electronic circuit schematic diagram of a switching circuit, including a thyristor S1, for generating the positive component of the mains current.

Figure 8 is an electronic circuit schematic diagram of a switching circuit, including a thyristor S2, for generating the negative component of the mains current.

Figure 9 is an electronic circuit schematic diagram of a single phase inverter incorporating the switching circuits of Figures 7 and 8.

Figure 10 is a graph depicting the time and current switching behaviour of triggering switches T1,S1 and T2,S2 depicted in the switching circuits of Figure 9.

Figure 11 is an electronic circuit schematic diagram of a first embodiment of a three phase inverter incorporating the switching circuits of Figures 7 and 8 to produce an output current having three phases U, V, and W.

Figure 12 is an electronic circuit schematic diagram of a second embodiment of a three phase inverter incorporating the switching circuits of Figures 7 and 8 to produce an output current having three phases U, V, and W.

Figure 13 is an electronic circuit schematic diagram of a prior art inverter having a three-phase bridge configuration.

Description

Figure 1 is a circuit diagram of a cross arm or switching circuit 1, for generating the positive component of alternating or three-phase current from a dc input voltage. The switching circuit consists of a power switch T1, e.g. an IGBT (isolated gate bipolar transistor) or GTO (gate turn off), and a diode D1, which are connected in series with the dc voltage connections. Located between switch T1 and diode D1 is a current tap-off point A1, from which current is tapped off by means of an inductor L1.

Figure 2 is a basic circuit diagram of a switching circuit 2 for generating the negative component of alternating or three-phase mains current comprising a series connected power transistor T2, diode D2, central current tap-off point A2, and an inductor L2 connected on the load side.

Figure 3 depicts a parallel connection of switching circuits 1, 2 in which an inductor L3 provides coupling inductance. A capacitor C is connected to the dc supply network, in parallel with switching circuits 1, 2.

Figure 4 shows how three of the Figure 3 parallel-connected switching circuits 1, 2 are interconnected to generate three-phase mains currents having phases U, V, and W.

Figure 5 shows in a timing chart the clocking of switches T1 and T2 used to obtain a sinusoidal current for, e.g., the phase U. Only switch T1 is switched on and off in an assigned timing pattern during the positive half-wave of the sinusoidal current, switch T2 is inactive during this time. A "jagged" sinusoidal current is generated by timing the ON and OFF states of switch T1. Switch T1 is inactive during generation of the negative half-wave of the sinusoidal current, and only switch T2 is switched on and off in predetermined time and clock intervals. The shown "jagged" current behaviour is a result of the current path and the interaction of transistor T1 with diode D1 or transistor T2 with diode D2, as shown in Figure 5. Note that while operating near the current maximum of the positive half-wave, switch T1 remains on for a longer duration than during its operation at lower current levels of the positive half-wave. Similarly, while operating near the negative current maximum of the negative half-wave, switch

T2 remains on for a longer duration than during its operation at lower (i.e. less negative) current levels of the negative half-wave.

Figure 6 shows how the circuit of Figure 4 is adapted to produce an output current having a single phase U, by interconnecting the outputs of the three coupling inductors L3 to form a single switching circuit. Current overshoots can be drastically reduced by such an interconnection and by a time-shifted switching on and off of the corresponding power switches T1 and T2 of the individual switching circuits, while the individual switching circuits or circuit modules are connected in parallel by the coupling inductances L3.

In the circuit of Figure 7, a first switching element S1, such as a thyristor, is connected between the current tap-off A1 of first switching circuit 1 to produce the positive component of the mains current, with coupling inductor L3 connected on the load side. Similarly, as shown in Figure 8, a second switching element S2 is connected between the current tap-off A2 of second switching circuit 2 to produce the negative component of the mains current, with coupling inductor L3 gain being connected on the load side.

Figure 9 shows a series connection of the switching circuits of Figures 7 and 8, with a single inductor L3 serving as a common coupling inductance. In this interconnection of switching circuits 1, 2, the supplied dc voltage is divided into two partial dc voltages, +Ud, -Ud, of equal magnitude. The two capacitive diodes D1, D2 are connected to ground.

The timing chart of Figure 10 illustrates how switches T1, T2 and switching elements S1, S2 are clocked to produce a single phase sinusoidal current. During the positive half-wave of the sinusoidal cycle, T1 is switched on and off according to an assigned clocking pattern, with S1 remaining on throughout the entire positive half-wave. T2 and S2 are switched off during the positive half-wave. By clocking the ON and OFF states of T1, similar to the time behaviour illustrated in Figure 5, a "jagged" sinusoidal current is generated. Similarly, T1, S1 remain off during production of the negative half-wave of the sinusoidal cycle; with T2 being switched on and off at predetermined time and clock intervals and S2 remaining on throughout the entire negative half-wave.

Figure 11 shows how three of the Figure 9 series-connected switching circuits 1, 2 are interconnected to generate three-phase mains currents having phases U, V, and W. In this embodiment, additional inductors L1, L2 are connected between the respective current tap-off points A1, A2 and their corresponding following switching elements, S1, S2 respectively

Figure 12 depicts a circuit for generating three-phase mains current with phases U, V, W. The supplied dc voltage is divided into two partial dc voltages, ±Ud1 and ±Ud2, which in summation are equal to the total dc voltage Ud. In this embodiment diodes D1, D2 are not connected to ground, but to -Ud1 or +Ud2 respectively, as shown in Figure 12.

Figure 13 depicts a prior art inverter which is capable of four-quadrant operation by means of an antiparallel connection of power switches T1-T6 with diodes D1-D6. This circuit has many applications, but also has a high risk of a severe short circuit in case of a short circuit across two switches, e.g. T1, T2. This can destroy the inverter and possibly, if a fire starts, cause complete destruction of all adjacent system components. To produce the positive half-wave of the output sinusoidal current, the Figure 13 inverter successively switches on and off, for example, switches T1 and T2. Thus, during each half-wave, T1 and T2 must be switched on or off several consecutive times during the half-wave, which significantly increases the statistical probability of a short circuit compared to the embodiment of the present invention described above in relation to Figure 5.

The present invention prevents severe short circuits in the interconnection of individual switching circuits (see for example Figure 3), by utilizing separate current branches, i.e. a positive and a negative cross arm. If switches T1, T2 should fail (for example, in the embodiments of Figures 3, 4, or 5), they are decoupled and protected from each other by inductors L1, L2. In the embodiments in Figures 9, 11, or 12, diodes D1, D2 and switching elements S1, S2, reduce the risk of a short circuit.

The spatial arrangement of the two cross arms – positive, negative – can be separated, whereby the mechanical layout of the inverter is simplified. Inverters of very high power can be constructed using the inverter concept of Figure 3 or Figures 4 and 6, as well as Figure 9 or Figs. 11 and 12.

The decoupling impedances L1, L2 between the switches of two interconnected switching circuits can be used as a high frequency choke, and also as a filter for a reduction in dU/dt. Thus, any parasitic radiation is substantially reduced immediately after power switches T1, T2.

As will be apparent to those skilled in the art in the light of the foregoing disclosure, many alterations and modifications are possible in the practice of this invention without departing from the spirit or scope thereof. Accordingly, the scope of the invention is to be construed in accordance with the substance defined by the following claims.

WHAT IS CLAIMED IS:

1. An inverter for producing a sinusoidal alternating current from an input dc voltage, said inverter comprising first and second switching circuits connected in parallel or in series, said first switching circuit for producing a positive component of said sinusoidal alternating current, said second switching circuit for producing a negative component of said sinusoidal alternating current;

said first switching circuit further comprising a first switch connected in series to a first capacitive diode, and a first current tap-off provided between said first switch and said first capacitive diode; and,

said second switching circuit further comprising a second switch connected in series to a second capacitive diode, and a second current tap-off provided between said second switch and said second capacitive diode.

2. The inverter of claim 1, wherein:

said first switching circuit further comprises a first inductor connected between said first current tap-off and a load side output of said first switching circuit;

said second switching circuit further comprises a second inductor connected between said second current tap-off and a load side output of said second switching circuit;

said inverter further comprising a third inductor connected between said load side outputs of said first and second switching circuits and a current output of said inverter.

3. The inverter of claim 1 or 2, wherein:

a first switching element is connected between said first current tap-off and said third inductor; and,

a second switching element is connected between said second current tap-off and said third inductor.

4. The inverter of claim 3, wherein said first and second switching elements are thyristors.

5. The inverter of claim 3 wherein:

said first said switching element is on and said second said switching element is off during production of said positive component of said sinusoidal alternating current; and,

said second said switching element is on and said first said switching element is off during production of said negative component of said sinusoidal alternating current.

6. The inverter of any one of claims 1, 2, 3, 4 or 5, wherein:

said first and second switching circuits are connected in series;

said dc voltage is divided into first and second partial dc voltages; and,

said first partial dc voltage is applied to said first switching circuit to produce said positive component of said sinusoidal alternating current; and, said second partial dc voltage is applied to said second switching circuit to produce said negative component of said sinusoidal alternating current.

7. The inverter of claim 6, wherein:

said first and second partial dc voltages are of equal magnitude; and,

said first and second capacitive diodes are connected to ground.

8. The inverter of any one of claims 1, 2, 3, 4, 5, 6 or 7, further comprising three of said first switching circuits interconnected with three of said second switching circuits to produce a three phase current output.

9. The inverter of any one of claims 1, 2, 3, 4, 5, 6, 7, or 8 wherein said first switching circuits are spatially separated from said second said switching circuits.

10. The inverter of any one of claims 1, 2, 3, 4, 5, 6, 7, 8 or 9, wherein only one of said first and second switches of said respective first and second switching circuits is repeatedly switched on or off during production of said components of said sinusoidal alternating current.

11. The inverter of claim 10, wherein:

only said first switching circuit is repeatedly switched on or off during production of said positive component of said sinusoidal alternating current; and,

only said second switching circuit is repeatedly switched on or off during production of said negative component of said sinusoidal alternating current.

12. The inverter of claim 10 or 11, wherein:

said first switch is switched on during production of a current maxima portion of said positive component for a time duration which is greater than the time during which said first switch is switched on during production of a non-current maxima portion of said positive component; and,

said second switch is switched on during production of a current minima portion of said negative component for a time duration which is greater than the time during which said second switch is switched on during production of a non-current minima portion of said negative component.

13. The inverter of any one of claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, or 12, further comprising two or more of said first switching circuits interconnected with two or more of said second switching circuits to produce a single phase current output.

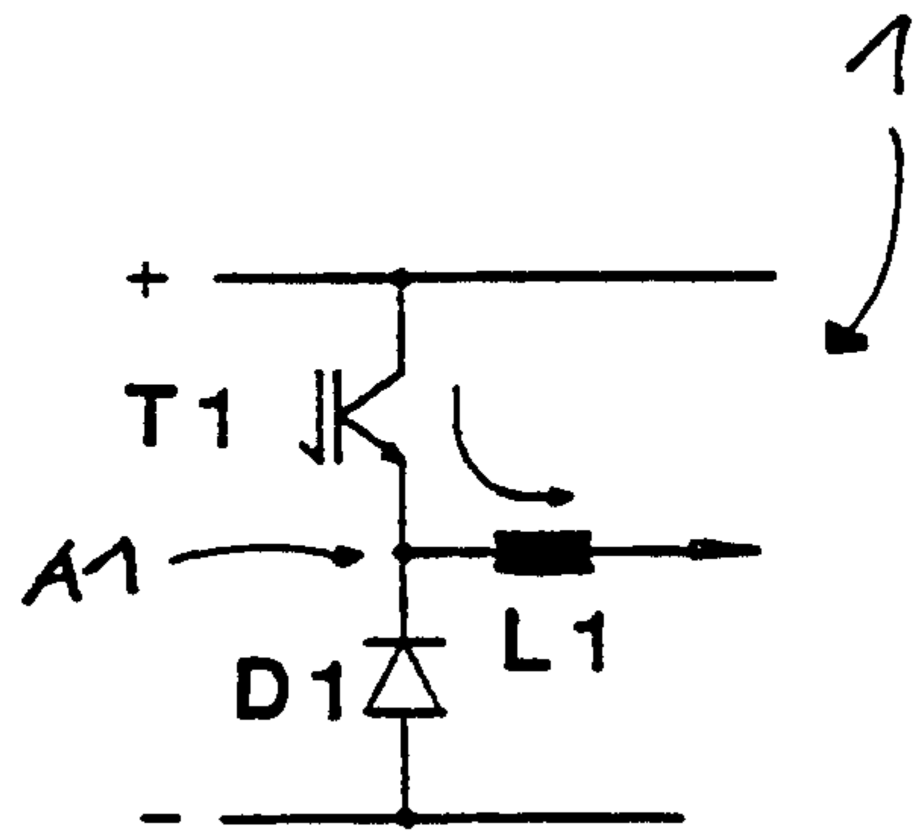


Fig. 1

Positive component

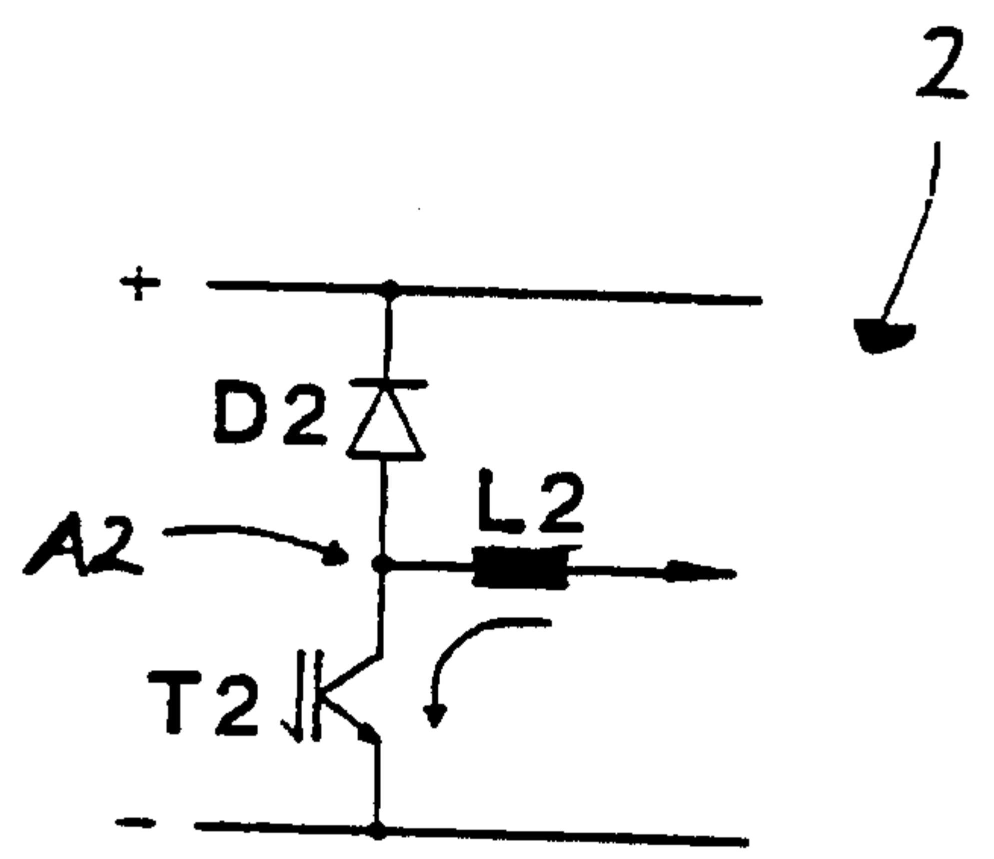


Fig. 2

Negative component

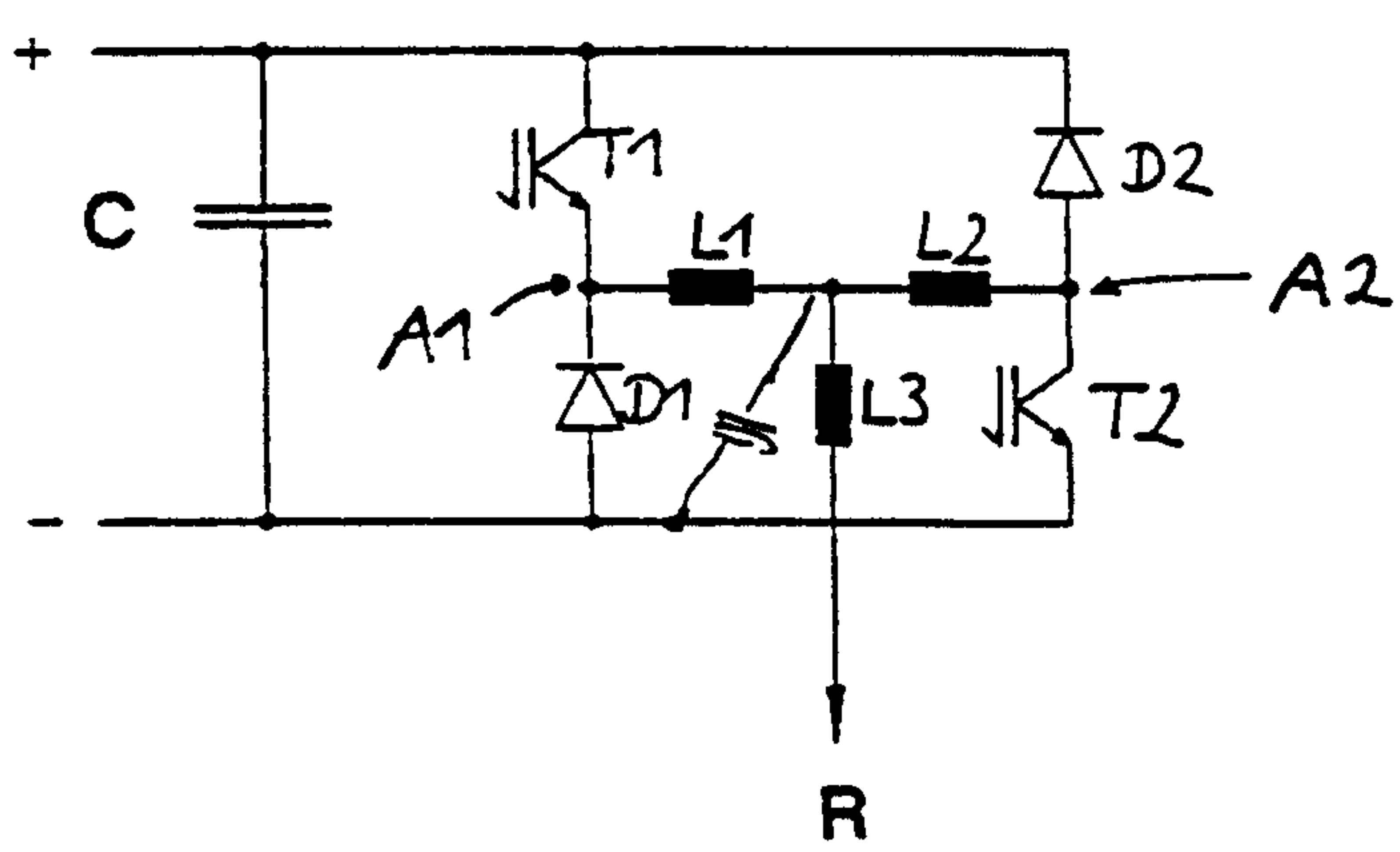


Fig. 3

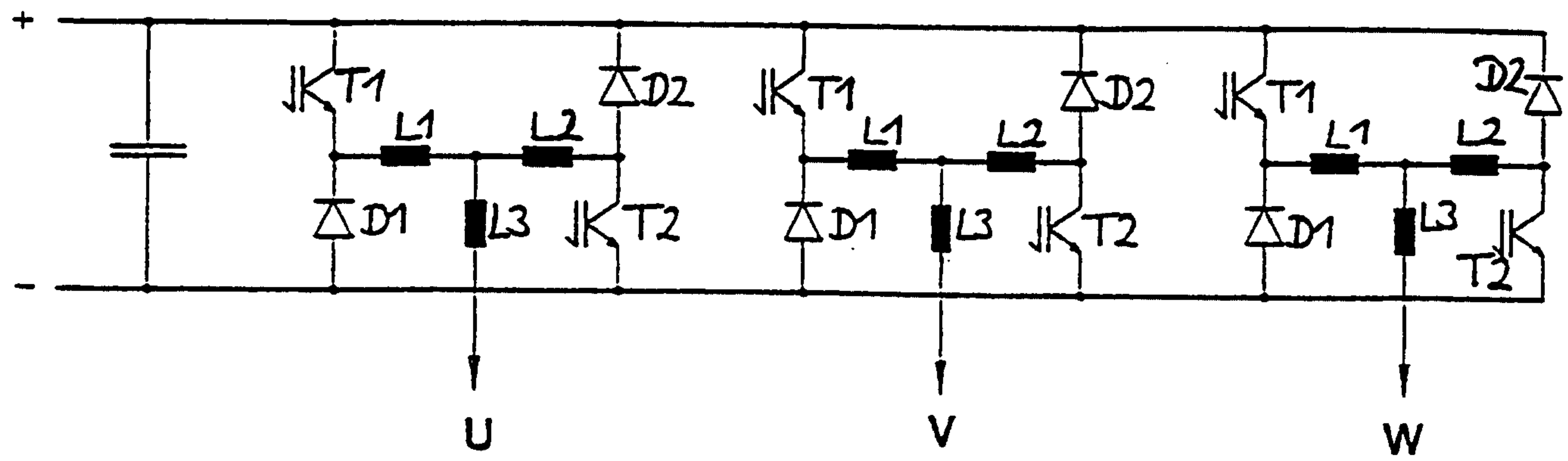


Fig. 4

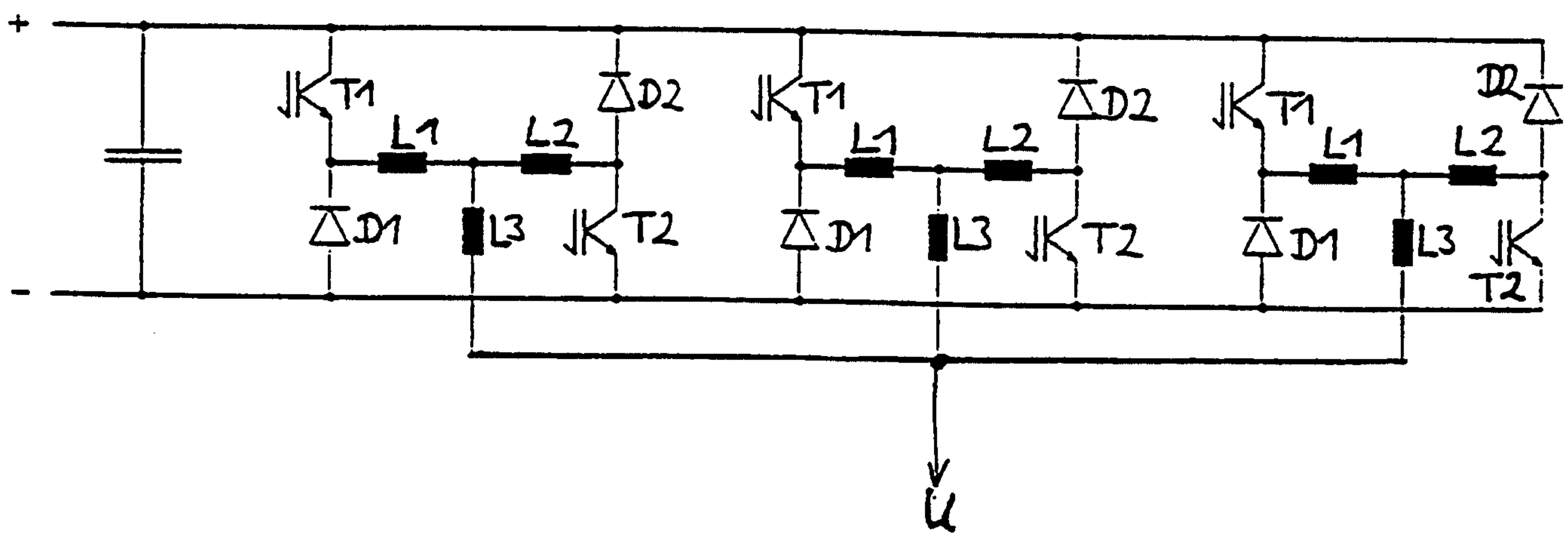


Fig. 6

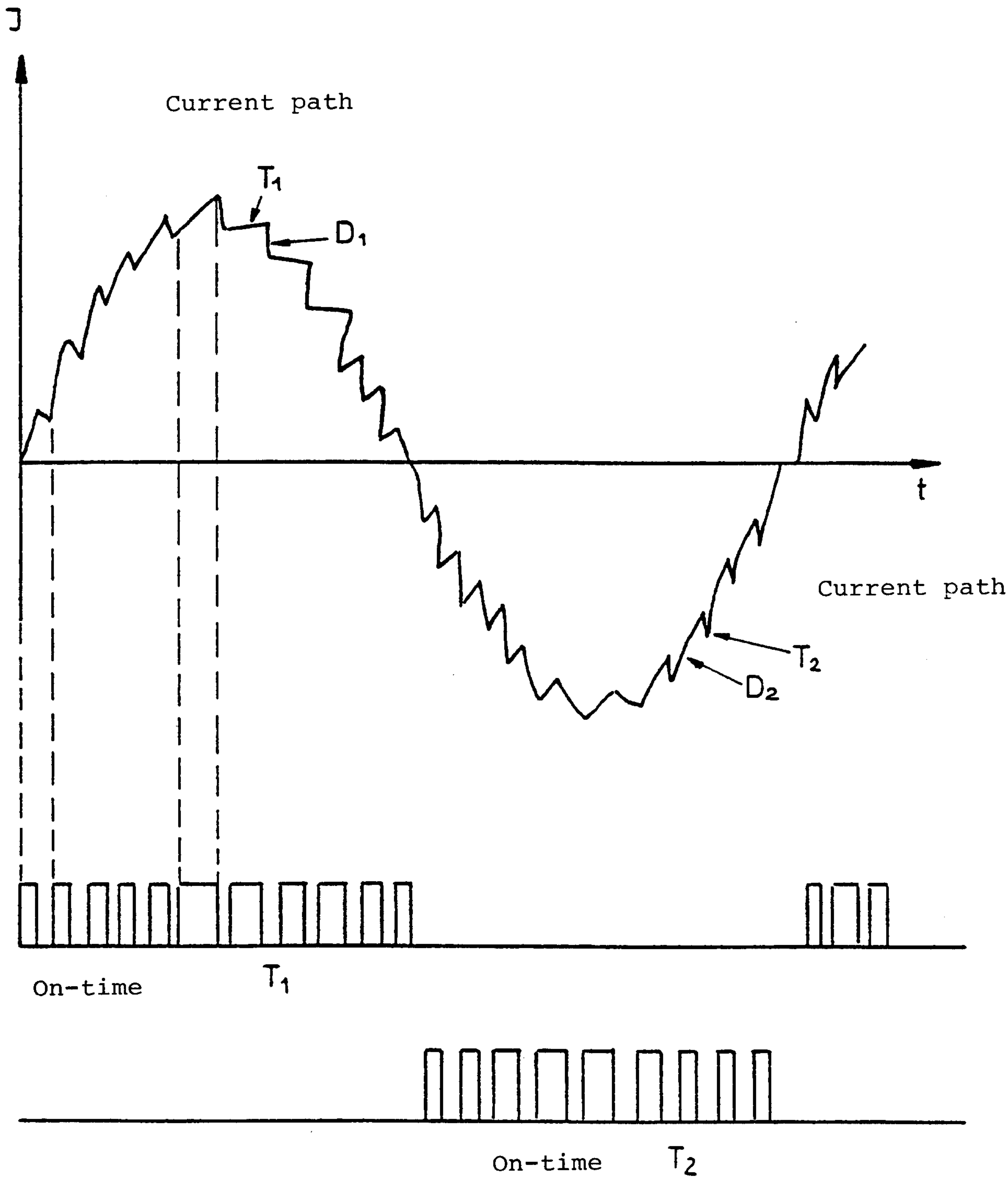


FIG. 5

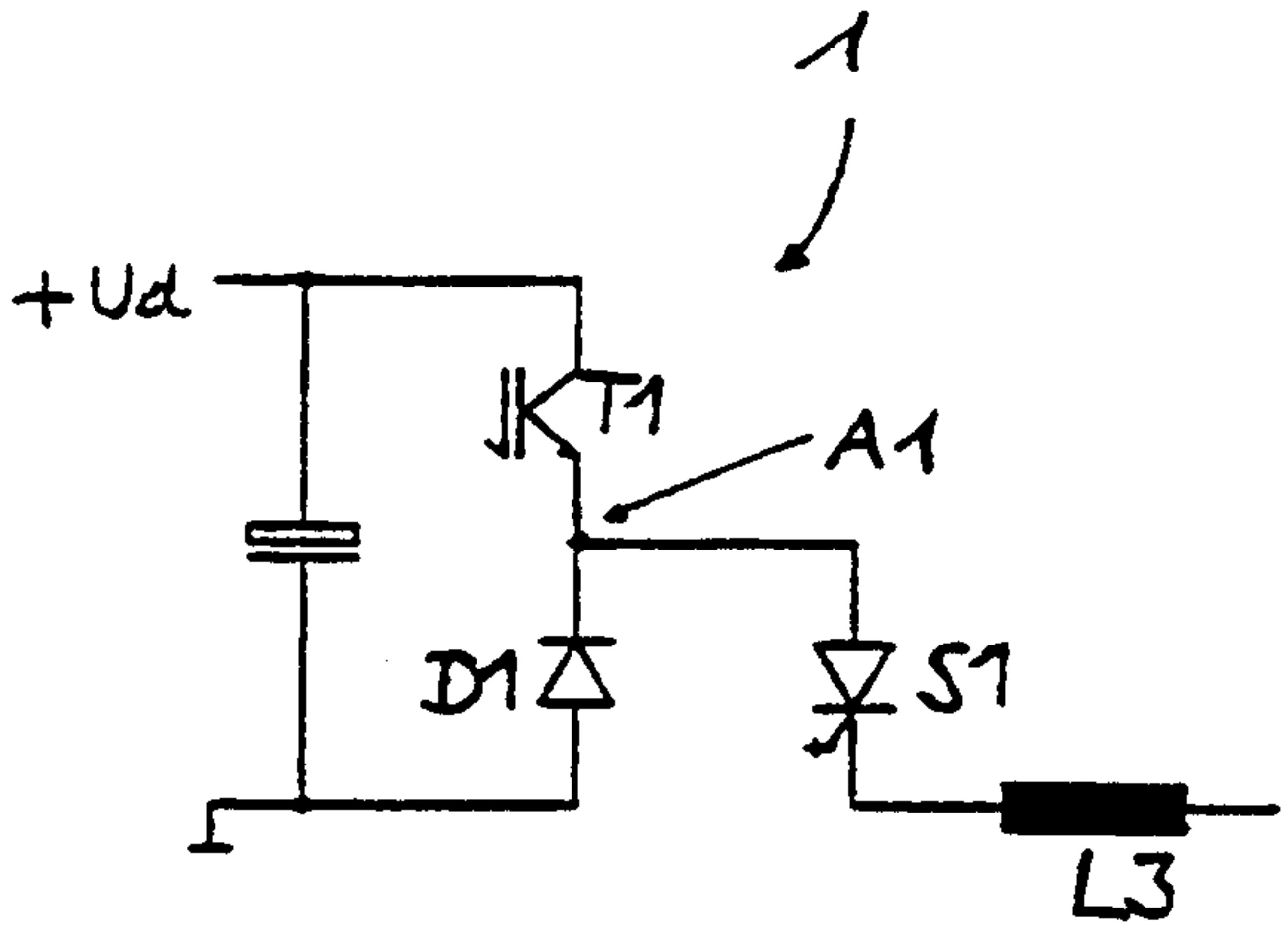


Fig. 7

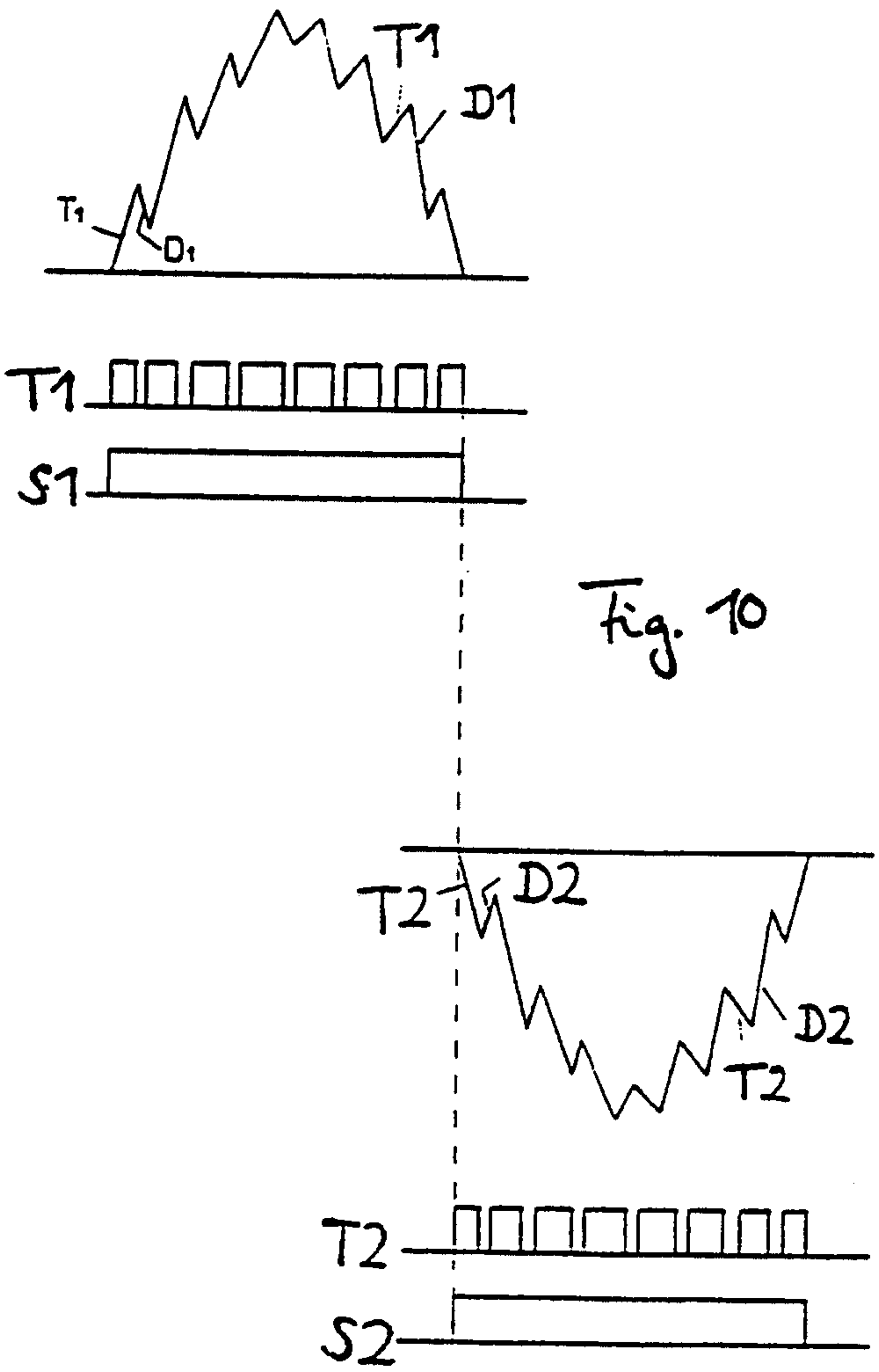


Fig. 10

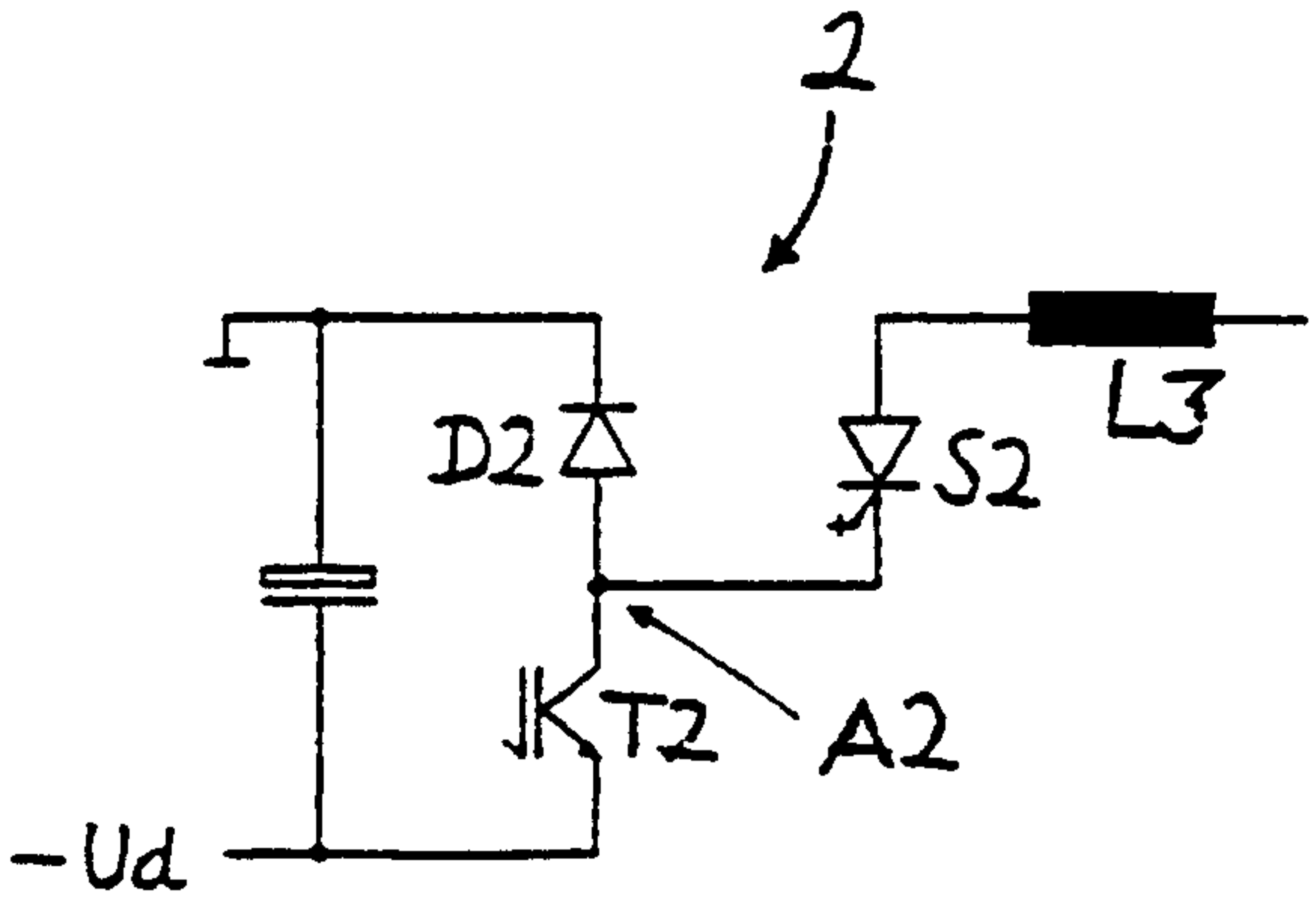


Fig. 8

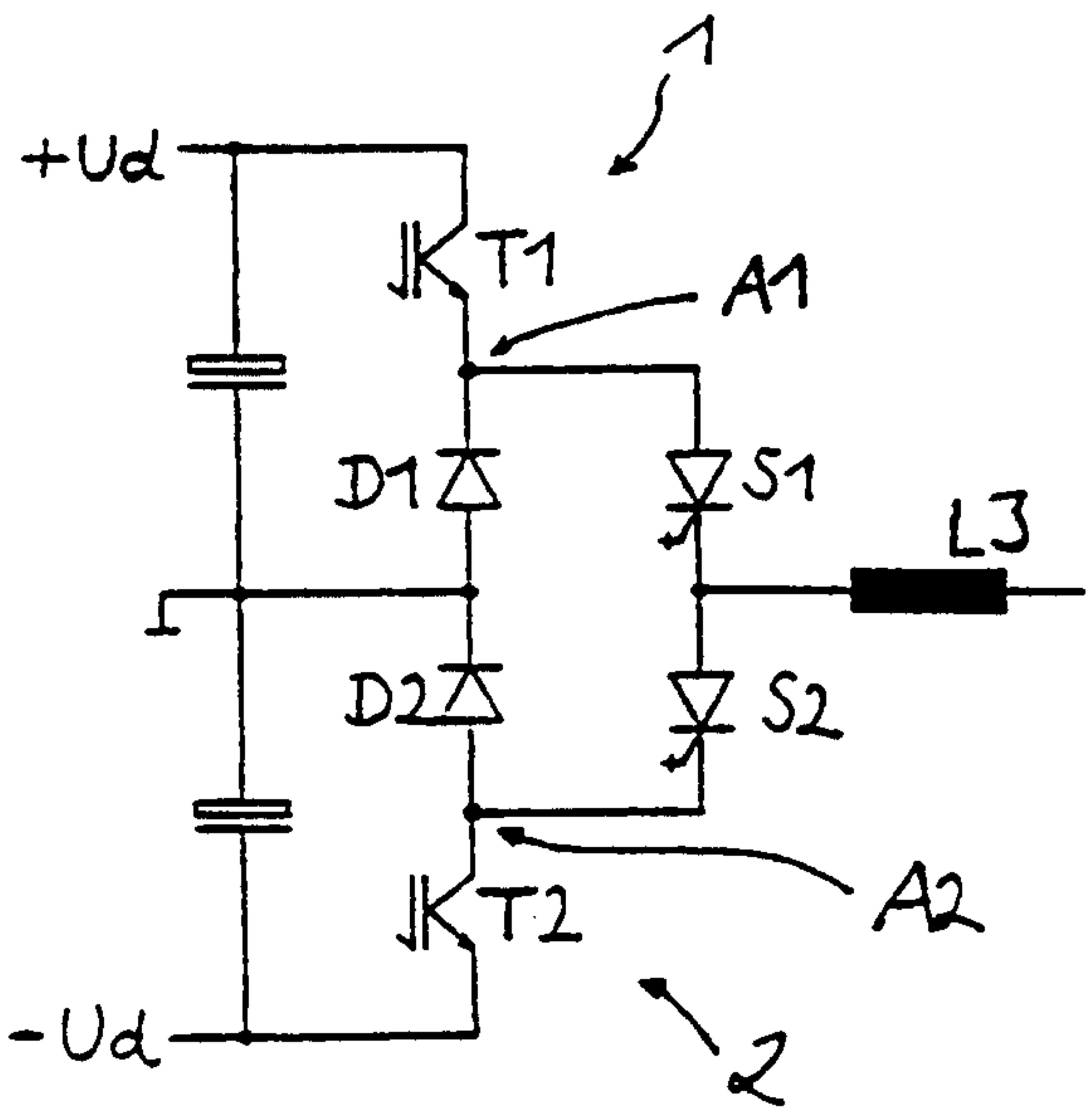


Fig. 9

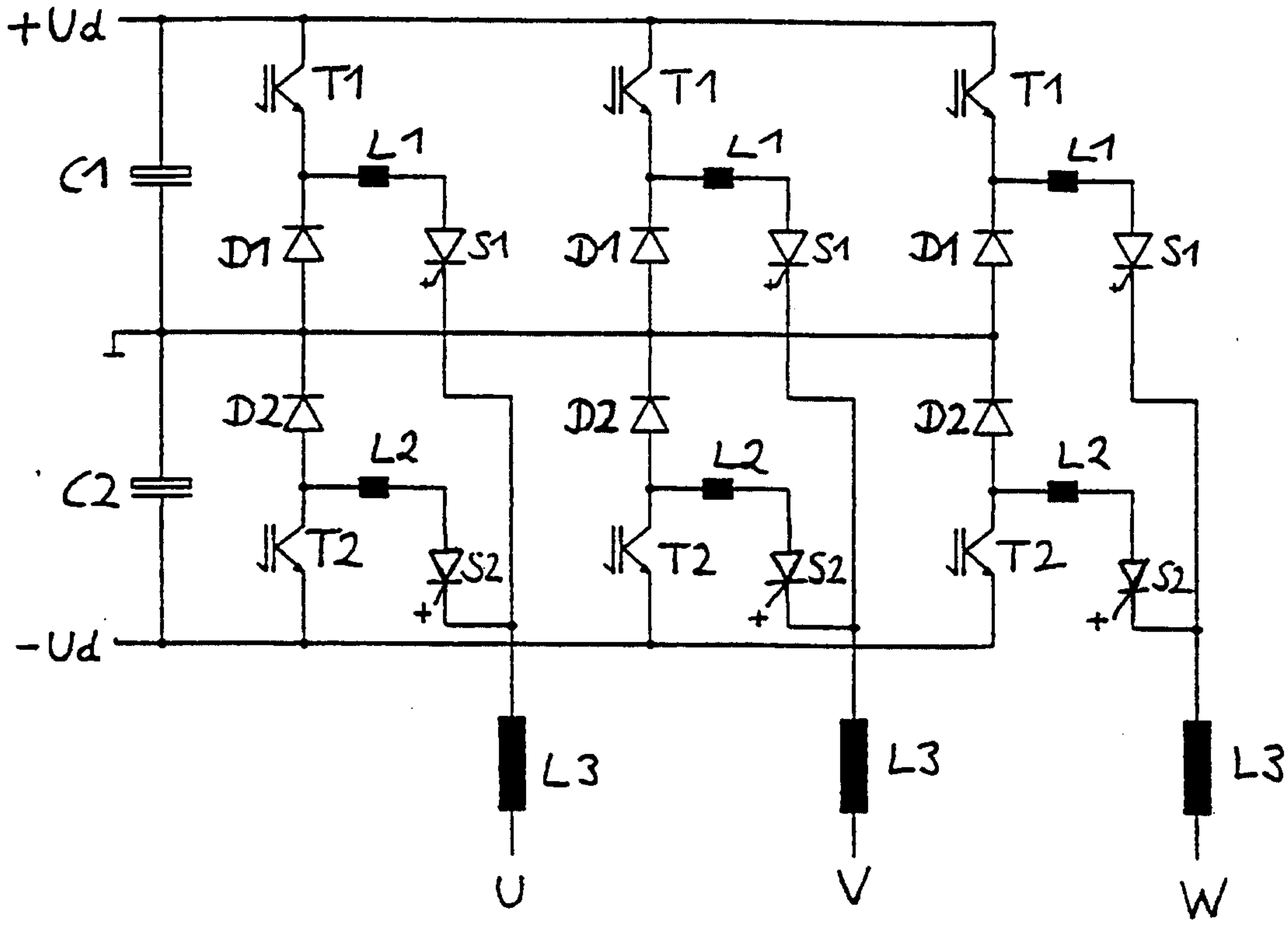

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Fig. 11

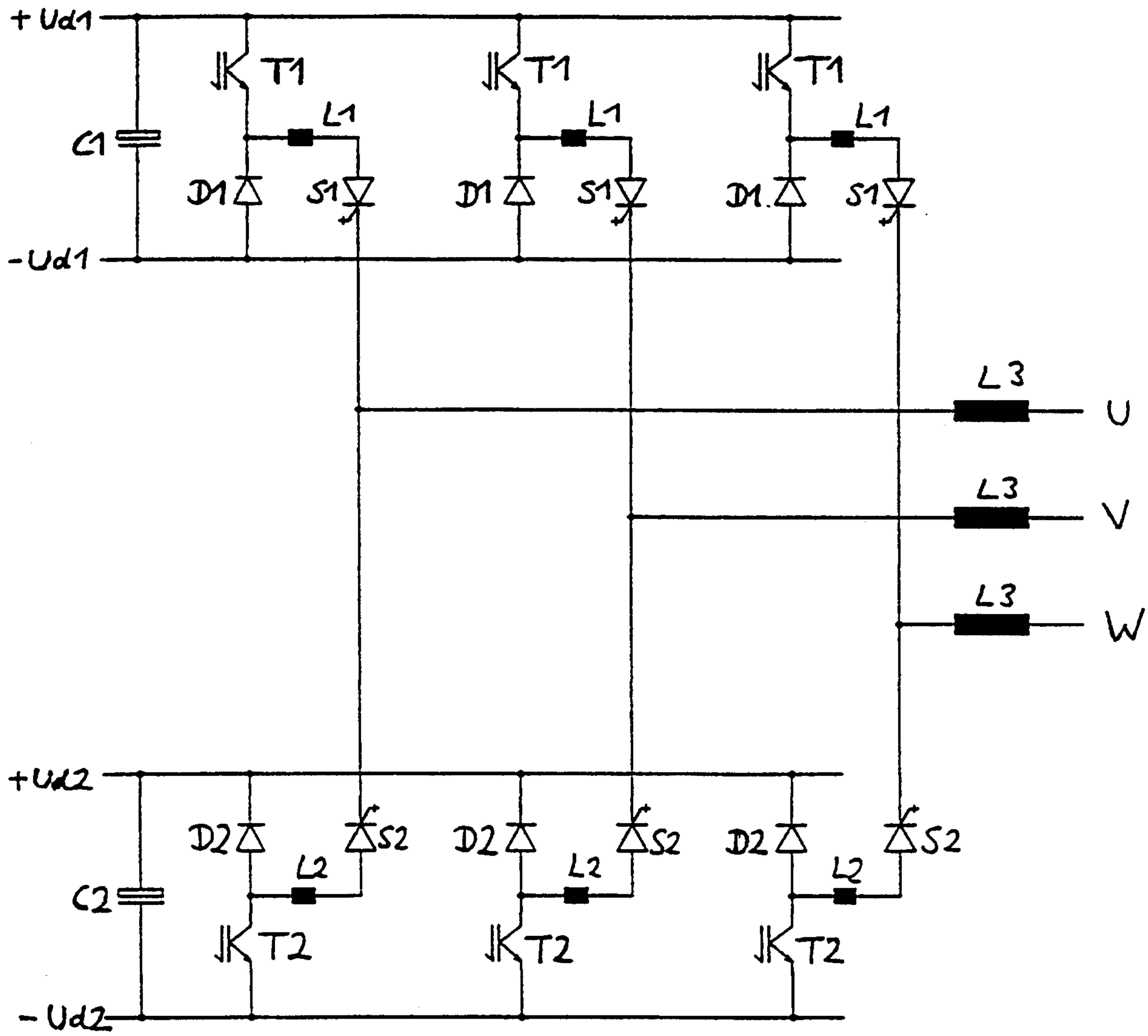
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Fig. 12

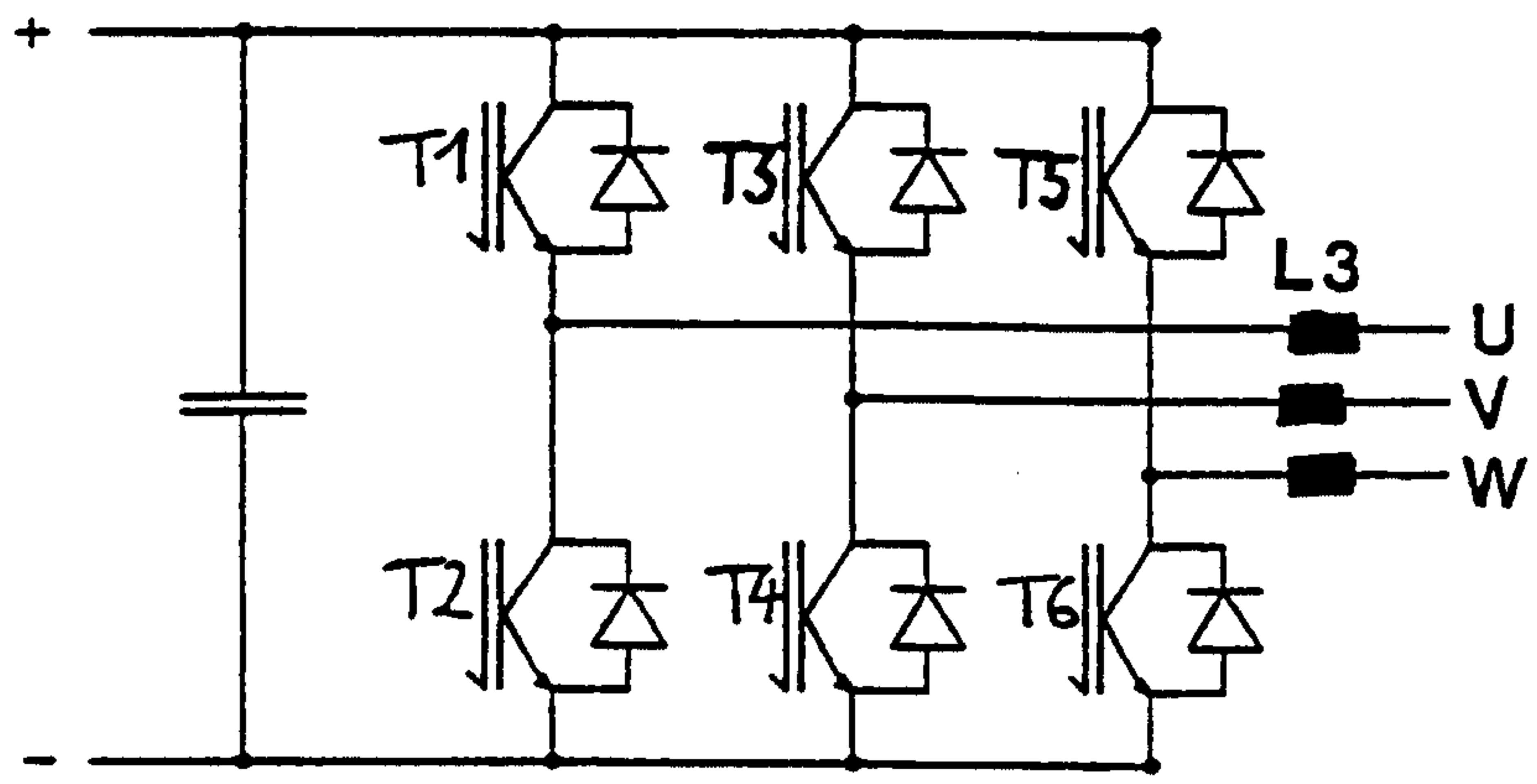
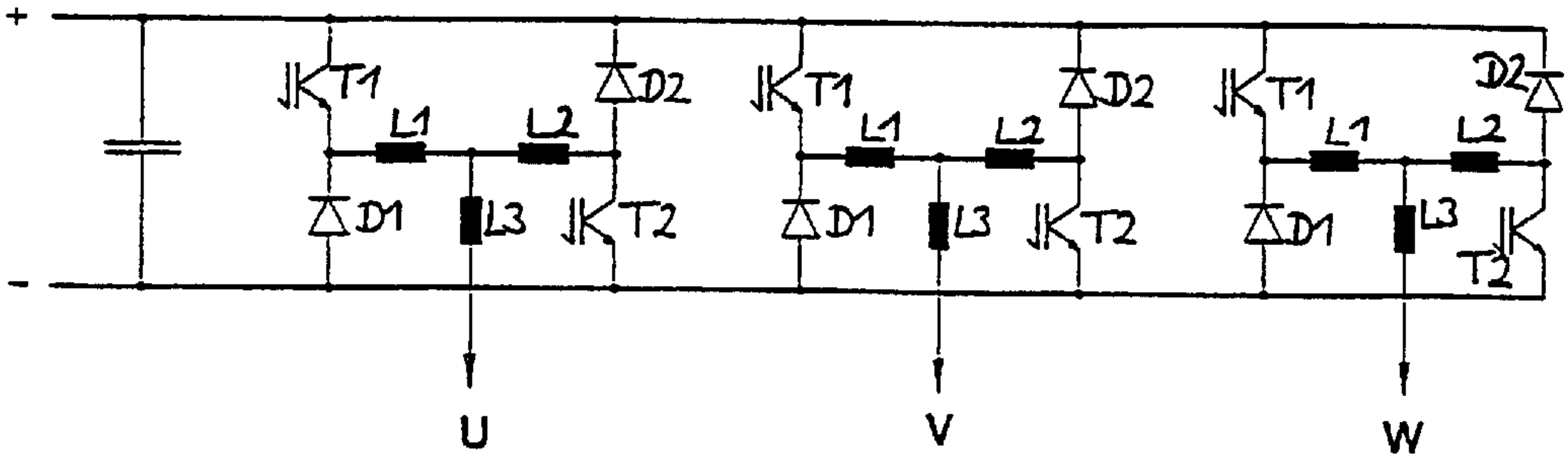


Fig. 13



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