



(12) **EUROPEAN PATENT APPLICATION**  
published in accordance with Art. 153(4) EPC

(43) Date of publication:  
**26.01.2022 Bulletin 2022/04**

(51) Int Cl.:  
**H01L 21/8242<sup>(2006.01)</sup>**

(21) Application number: **21785736.6**

(86) International application number:  
**PCT/CN2021/083131**

(22) Date of filing: **26.03.2021**

(87) International publication number:  
**WO 2021/232937 (25.11.2021 Gazette 2021/47)**

(84) Designated Contracting States:  
**AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR**  
Designated Extension States:  
**BA ME**  
Designated Validation States:  
**KH MA MD TN**

(72) Inventors:  
• **ZHU, Yiming**  
**Hefei**  
**Anhui 230000 (CN)**  
• **YING, Zhan**  
**Hefei**  
**Anhui 230000 (CN)**  
• **ZHANG, Qiang**  
**Hefei**  
**Anhui 230000 (CN)**

(30) Priority: **20.05.2020 CN 202010428539**

(71) Applicant: **Changxin Memory Technologies, Inc.**  
**230000 Hefei City, Anhui (CN)**

(74) Representative: **V.O.**  
**P.O. Box 87930**  
**2508 DH Den Haag (NL)**

(54) **METHOD FOR PREPARING SEMICONDUCTOR STRUCTURE**

(57) The present invention provides a method for manufacturing a semiconductor structure. The method includes that: a substrate having a plurality of first trenches is provided. A first pattern is formed between two adjacent first trenches. A first dielectric layer is formed. The first dielectric layer covers at least side walls of the first pattern. A second dielectric layer is formed. The second dielectric layer fills the first trenches. The first pattern is severed to form a second pattern. The second dielectric layer is removed.

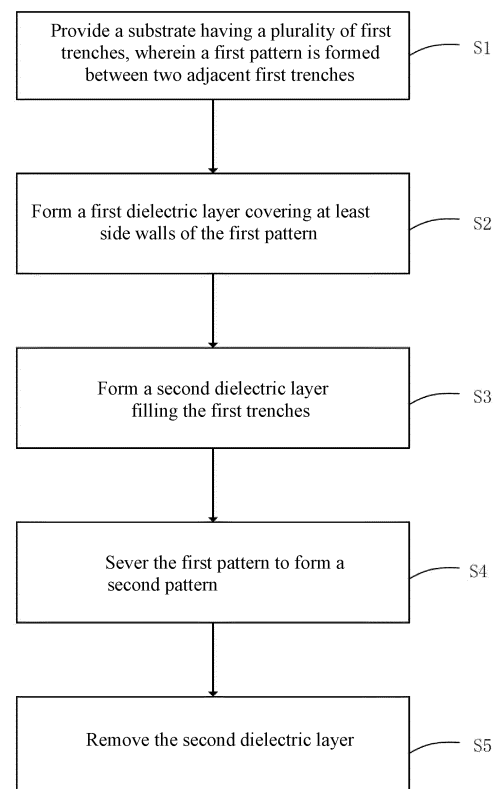


FIG. 1

## Description

### CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This application claims priority to Chinese Patent Application No.: 202010428539.2 filed on May 20, 2020 and titled "METHOD FOR MANUFACTURING SEMICONDUCTOR STRUCTURE", the contents of which are incorporated herein by reference in their entirety.

### TECHNICAL FIELD

**[0002]** The present application relates to a method for manufacturing a semiconductor structure.

### BACKGROUND

**[0003]** A dynamic random access memory (DRAM) is a semiconductor memory widely used in computing systems. As semiconductor integrated circuit device technology continues to advance, the critical size of the dynamic random access memory becomes smaller and smaller. For example, the size of the active area of a memory becomes smaller, which has very high requirement on semiconductor manufacturing processes.

### SUMMARY

**[0004]** Embodiments of the present application provide a method for manufacturing a semiconductor structure. The method includes the following operations.

**[0005]** A substrate having multiple first trenches is provided. A first pattern is formed between two adjacent first trenches.

**[0006]** A first dielectric layer is formed. The first dielectric layer covers at least side walls of the first pattern.

**[0007]** A second dielectric layer is formed. The second dielectric layer fills the first trenches.

**[0008]** The first pattern is severed to form a second pattern.

**[0009]** The second dielectric layer is removed.

**[0010]** The details of one or more embodiments of the present application are set forth in the following drawings and description. Other features and advantages of the present application will become apparent from the description, drawings and claims.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0011]** In order to more clearly illustrate the technical solutions in the embodiments of the present application, the following will briefly introduce the drawings that need to be used in the embodiments. It is apparent that the drawings in the following description are only some embodiments of the present application. Those of ordinary skill in the art can also obtain other drawings from these drawings without creative work.

FIG. 1 illustrates a flowchart of a method for manufacturing a semiconductor structure according to various embodiments of the present invention.

FIG. 2 illustrates a three-dimensional structural diagram of a substrate having multiple first trenches which is obtained by Step S1 in a method for manufacturing a semiconductor structure according to various embodiments of the present invention.

FIG. 3 illustrates a three-dimensional structural diagram of a semiconductor structure obtained by Step S2 in a method for manufacturing a semiconductor structure according to various embodiments of the present invention.

FIG. 4 illustrates a three-dimensional structural diagram of a semiconductor structure obtained after removing a first dielectric layer located at bottom surfaces of the first trenches in a method for manufacturing a semiconductor structure according to various embodiments of the present invention.

FIG. 5 illustrates a three-dimensional structural diagram of a semiconductor structure obtained by Step S3 in a method for manufacturing a semiconductor structure according to various embodiments of the present invention.

FIG. 6 illustrates a three-dimensional structural diagram of a semiconductor structure obtained by Step S42 in a method for manufacturing a semiconductor structure according to various embodiments of the present invention.

FIG. 7 illustrates a three-dimensional structural diagram of a semiconductor structure obtained by Step S5 in a method for manufacturing a semiconductor structure according to various embodiments of the present invention.

FIG. 8 illustrates a three-dimensional structural diagram of a semiconductor structure obtained by Step S6 in a method for manufacturing a semiconductor structure according to various embodiments of the present invention.

Reference signs:

**[0012]** 1. Substrate; 11. First pattern; 111. Second pattern; 112. Second trench; 12. First trench; 2. First dielectric layer; 3. Patterned mask layer; 31. Opening pattern; 4. Second dielectric layer; 5. Third dielectric layer.

### DETAILED DESCRIPTION OF THE EMBODIMENTS

**[0013]** When the width of the active area becomes very small, use of existing etching process to etch and form the active area may damage the ends of the elongated active area.

**[0014]** To better understand the objectives, technical solutions, and technical effects of the present invention, the following disclosure describes the present invention with reference to drawings and various embodiments. Further, various embodiments described herein are

merely used to illustrate the present invention, and not to limit the present invention.

**[0015]** Unless stated otherwise, all technical and scientific terms used herein have the same meanings as those commonly understood by a person skilled in the art. Terms used herein are merely intended to describe specific embodiments, and not intended to limit the present application. The term "and/or" used herein includes any and all combinations of one or more related listed items.

**[0016]** In the case of using "include", "have", and "comprise" described herein, another component or method can further be added unless explicit qualifiers, such as "only" and "consist of", are used. Unless stated to the contrary, terms in the singular forms can include the plural forms and cannot be construed to mean a quantity of one.

**[0017]** In conventional semiconductor processes, dry etching is performed on a substrate through a one-step etching process to form shallow trenches on the substrate, so that a plurality of active areas can be separated on the substrate. Insulating material layers are then filled into the shallow trenches to form a trench isolation structure. In particular, as the size of a semiconductor structure decreases, ends of active areas can be more elongated. When a dry etching process is used to directly etch the substrate to form the active areas, etching gas used in the dry etching process can contain high-energy charged particles or groups, so that as the substrate is bombarded with the high-energy charged particles or groups to form the shallow trenches, the ends of the active areas can be damaged or destroyed, thereby causing adverse impact to performance of the device.

**[0018]** Therefore, based on the problems described above, a method for manufacturing a semiconductor structure is required, so as to reduce damage to ends of an active area during an etching process.

**[0019]** As shown in FIG. 1, the present invention provides a method for manufacturing a semiconductor structure. The method includes the following steps.

**[0020]** At Step S1, a substrate having a plurality of first trenches is provided. A first pattern is formed between two adjacent first trenches.

**[0021]** At Step S2, a first dielectric layer is formed. The first dielectric layer covers at least side walls of the first pattern.

**[0022]** At Step S3, a second dielectric layer is formed. The second dielectric layer fills the first trenches.

**[0023]** At Step S4, the first pattern is severed to form a second pattern.

**[0024]** At Step S5, the second dielectric layer is removed.

**[0025]** According to the method for manufacturing the semiconductor structure of the present invention, the first dielectric layer is formed on the at least one side wall of the first pattern in the substrate as a protective layer. The first pattern is severed to form the second pattern constituting active areas. As such, when the first pattern is severed to form the second pattern constituting the active

areas, because the side walls of the first pattern are protected by the first dielectric layer, ends of the second pattern (i.e., ends of the active areas) formed by severing can be better protected in severing processes.

**[0026]** As shown in FIG. 2, the Step S1 includes the following steps.

**[0027]** At Step S11, the substrate 1 is provided.

**[0028]** At Step S12, the substrate 1 is etched to form the first trenches 12 on the substrate 1. A first pattern 11 is formed between two adjacent first trenches 12.

**[0029]** In various embodiments, the substrate 1 can be, but is not limited to, a silicon substrate, a gallium nitride substrate, a silicon-on-insulator, a silicon carbide substrate, or the like. In one embodiment, the substrate 1 can be a silicon substrate. Doped well regions may be formed on the substrate 1 through an ion implantation process. A doped well region can either be P-type or N-type.

**[0030]** In some embodiments, the first pattern 11 and the first trenches 12 can constitute a strip-shaped array structure. The first pattern 11 can be plate-shaped wall structures. Specifically, the first pattern 11 can be, but are not limited to, rectangular plate-shaped wall structures. Multiple first patterns 11 can be spaced apart in an array by the first trenches 12 formed between two adjacent first patterns 11. Specifically, the multiple first patterns 11 are parallelly spaced.

**[0031]** In some embodiments, as shown in FIG. 2, a width  $d$  of the first pattern 11 in the Step S12 can be set based on actual needs. The width  $d$  can be a length of a cross section perpendicular to an extension direction of the first pattern 11 in a horizontal direction of the substrate 1. Preferably, the width  $d$  of the first patterns 11 can be less than or equal to 20 nm. More specifically, the width  $d$  of the first pattern 11 can be 20 nm, 15 nm, or 10 nm, or the like. Within this width range, the technical problem described in the present invention can be more pronounced, and the technical solutions described herein can have better economical and beneficial technical effects. A distance  $L$  between adjacent first patterns 11 can be set based on actual needs. Specifically, the distance  $L$  between adjacent first patterns 11 can be less than or equal to 30 nm. More specifically, the distance  $L$  between adjacent first patterns 11 can be 30 nm, 25 nm, 20 nm, 15 nm, or 10 nm, or the like. In other embodiments, the distance  $L$  between adjacent first patterns 11 is not limited to the above distances. It should be noted that, for the distance  $L$  between adjacent first patterns 11 being of less than or equal to 30 nm, this distance is referred to as a center-to-center distance between two adjacent first patterns 11.

**[0032]** In some embodiments, in the Step 12, a self-aligned double patterning (SADP) process or a self-aligned quadruple patterning (SAQP) process can be used to form the strip-shaped array structure on the substrate 1 including the first patterns 11 and the first trenches 12. The SADP process and the SAQP process are known to a person skilled in the art and are not described

in detail herein.

**[0033]** In some embodiments, as shown in FIG. 3, the Step S2 includes the following steps.

**[0034]** The first dielectric layer 2 is formed onto side surfaces and bottom surfaces of the first trenches 12. In such a case, the first dielectric layer 2 can serve as a protective layer. Optionally, the first dielectric layer 2 can be formed on the side surfaces of the first trenches 12, the bottom surfaces of the first trenches 12, and top surfaces of the first patterns 11. In this way, the first dielectric layer 2 can effectively protect the first pattern 11 from subsequent etching of second trenches.

**[0035]** Specifically, a thicknesses of the first dielectric layer 2 can be determined based on actual needs. More specifically, the thicknesses of the first dielectric layer 2 can be less than half of a width of the first trenches 12. In such a case, there can still be gaps within the first trenches 12 after the first dielectric layer 2 is formed. Preferably, the thickness of the first dielectric layer 2 can range from 1 nm to 5 nm. In this range, the first dielectric layer 2 not only can provide enough protection for the first pattern 11, it can also leave enough space for subsequent filling of a third dielectric layer.

**[0036]** In various embodiments, the first dielectric layer 2 can be formed through a physical vapor deposition process, a chemical vapor deposition process, an atomic layer deposition process, a thermal oxidation process, or the like. The first dielectric layer 2 which serves as the protection layer can be, but not limited to, a silicon dioxide ( $\text{SiO}_2$ ) layer, a silicon monoxide ( $\text{SiO}$ ) layer, a silicon nitride ( $\text{SiN}$ ) layer, a silicon oxynitride ( $\text{SiON}$ ) layer, or the like. In some embodiments, the first dielectric layer 2 can be a silicon dioxide layer.

**[0037]** In some embodiment, as shown in FIG. 4, after forming the first dielectric layer 2 and before forming the second dielectric layer 4, the method further includes: the first dielectric layer 2 located at bottom surfaces of the first trenches 12 are removed. As such, the bottom surfaces of the first dielectric layer 2 are separated to form a discontinuous separation structure. In this way, accumulation of charge carriers at the bottom surfaces of the first trenches 12 can be avoided. Therefore, electric leakage caused by the accumulation of holes or electrons in the transistor substrate near the first dielectric layer 2 can be avoided. It should be noted that, all or some of the first dielectric layer 2 at the bottom surfaces of the first trenches 12 can be removed. In some embodiments, all of the first dielectric layer 2 at the bottom surfaces of the first trenches 12 are removed. Specifically, the first dielectric layer 2 located at the bottom surfaces of the first trenches 12 can be removed through a dry etching process or the like.

**[0038]** As shown in FIG. 5, the Step S5 includes the following steps.

**[0039]** The second dielectric layer 4 is formed within the first trenches 12. The second dielectric layer 4 fills the first trenches 12.

**[0040]** In various embodiments, the second dielectric

layer 4 can be formed through a physical vapor deposition process, a chemical vapor deposition process, an atomic layer deposition process, a spin-coating process, or the like. A material of the second dielectric layer 4 can be different from a material of the first dielectric layer 2. Specifically, a hardness of the first dielectric layer 2 can be greater than a hardness of the second dielectric layer 4. In this way, the first dielectric layer 2 can provide better protection for the first pattern 11, and moreover, a removal rate of the second dielectric layer 4 can be higher than a removal rate of the first dielectric layer 2 under the same etching condition. This difference in removal rates ensures that the first dielectric layer 2 on upper surfaces of the first pattern 11 is more resistant to removal in subsequent removal of the second dielectric layer 4. More specifically, in some embodiments, the second dielectric layer 4 can be, but not limited to, a spin-on carbon (SOC) layer, a spin-on glass (SOG) layer, or the like. In general, any material layer that meets the above criteria can be used herein.

**[0041]** More specifically, the Step S3 includes the following steps.

**[0042]** At Step 31, a second dielectric material layer (not shown) is formed. The second dielectric material layer fills the first trenches 12 and covers the first dielectric layer 2 on upper surfaces of the first patterns 11. Specifically, the second dielectric material layer can be formed through a physical vapor deposition process, a chemical vapor deposition process, an atomic layer deposition process, a spin-coating process, or the like.

**[0043]** At Step 32, the second dielectric material layer that covers the first dielectric layer 2 on upper surfaces of the first patterns 11 is removed while retaining the second dielectric material layer (i.e., the second dielectric layer 4) in the first trenches 12. Specifically, the second dielectric material layer that covers the first dielectric layer 2 on the upper surfaces of the first patterns 11 can be removed through a chemical mechanical polishing process or the like. In other examples, the second dielectric material layer is also located on the first dielectric layer 2 of the upper surfaces of the first patterns 11. The second dielectric material layer on the first dielectric layer 2 of the upper surfaces of the first patterns 11 and the second dielectric material layer in the first trenches 12 have a continuous flat upper surface.

**[0044]** The Step S4 includes the following step. Multiple second trenches 112 are formed on each of the first patterns 11 to cut the first pattern 11 into multiple second patterns 111.

**[0045]** Specifically, the Step S4 includes the following steps.

**[0046]** At Step S41, a mask layer is formed on the upper surface of the substrate 1.

**[0047]** At Step S42, the mask layer is patterned to obtain the patterned mask layer 3. As shown in FIG. 6, the patterned mask layer 3 can include a plurality of opening patterns 31 penetrating through the mask layer. The plurality of opening patterns 31 can define positions and

shapes of the second trenches. Optionally, shapes of the opening patterns 31 can be circular, elliptical, rectangular, or the like.

**[0048]** At Step S43, the first patterns 11 can be etched based on the patterned mask layer 3 to form the multiple second trenches 112 on each of the first patterns 11. In this way, each of the first patterns 11 can be cut into the multiple second patterns.

**[0049]** At Step S44, the patterned mask layer 3 is removed.

**[0050]** In various embodiments, in the Step S41, the mask layer can be, but is not limited to, an amorphous carbon layer, a silicon oxynitride layer, a silicon oxide layer, or a combination of at least two of the aforementioned layers. Specifically, the mask layer can be formed through at least one of a physical vapor deposition process, a chemical vapor deposition process, an atomic layer deposition process, a spin-coating process, or the like.

**[0051]** In some embodiments, in the Step S42, the mask layer can be patterned based on a photolithography process to obtain the patterned mask layer 3. In some embodiments, a size of the plurality of opening patterns 31 can be greater than the width of the first pattern 11. Specifically, the size of the plurality of opening patterns 31 can be a size in a width direction of the first pattern 11. In some cases, the size of the plurality of opening patterns 31 can be a maximum size in a horizontal direction of the substrate. For instance, the width of the first pattern 11 can be less than or equal to 20 nm, the size of the second trenches 112 can be less than or equal to 15 nm, the thickness of the first dielectric layer 2 can range from 1 nm to 5 nm, and the size of the plurality of opening patterns 31 can be less than 30 nm. In general, allowing the size of the plurality of opening patterns 31 to be greater than the width of the first pattern 11 can be helpful in increasing a process window and increasing a product yield. It should be noted that, the size of the second trenches 112 can be a size in the width direction of the first pattern 11, or in some cases, can be a maximum size in the horizontal direction of the substrate.

**[0052]** In some embodiments, in the Step S43, the first pattern 11 can be etched based on the patterned mask layer 3 through a dry etching process. In some embodiments, the second trenches 112 can be separated from the first pattern 11 without separating the first dielectric layer 2 on the side walls of the first pattern 11. Specifically, the first pattern 11 can be etched to form the second trenches 112 using the plurality of opening patterns 31 and through an etching process with an etching selection ratio greater than 8 between the first pattern 11 and the first dielectric layer 2. The second patterns 111 are formed between the first trenches 12 and the second trenches 112. The first dielectric layer 2 on the side walls of the first pattern 11 is not separated during the etching process. An etching process with a high etching selection ratio is used to only etch and separate the first pattern 11 while retaining the intact first dielectric layer 2. Therefore, shapes of ends of the second pattern 111 can be

better ensured, thereby improving performance of the device.

**[0053]** In some embodiments, in the Step S44, the patterned mask layer 3 can be removed through an etching process or a chemical mechanical polishing process.

**[0054]** As shown in FIG. 7, in some embodiments, an extension direction of the first pattern 11 obliquely intersects an arrangement direction of adjacent second trenches 112 spaced apart by a shortest distance in different columns. Specifically, the second trenches 112 on the same first pattern 11 are spaced apart, and the second trenches 112 on adjacent first patterns 11 are staggered. More specifically, the second trenches 112 of the first patterns 11 in odd columns are staggered with the second trenches 112 of the first patterns 11 in even columns. The second trenches 112 of the adjacent first patterns 11 in odd columns are in one-to-one correspondences. The second trenches 112 of the adjacent first patterns 11 in even columns are in one-to-one correspondences. In some embodiments, the first pattern 11 can be active areas of a storage device, and the above arrangement manner helps maximize a storage density of the storage device.

**[0055]** In some embodiments, as shown in FIG. 2 and FIG. 7, a depth H1 of the first trenches 12 can be greater than or equal to a depth H2 of the second trenches 112. In such embodiments, the depth H1 of the first trenches 12 can be greater than the depth H2 of the second trenches 112. Allowing the depth of the first trenches 12 to be greater than the depth of the second trenches 112 can achieve a better separation effect and avoid mutual impact between adjacent active areas. Specifically, the depth H1 of the first trenches 12 can be etched differently than the depth H2 of the second trenches 112 by etching the first trenches 12 first and etching the second trenches 112 second through any of the aforementioned etching processes, that is, by etching the substrate 1 twice.

**[0056]** In some embodiments, as shown in FIG. 2 and FIG. 7, a width D1 of the first trenches 12 can be less than or equal to a width D2 of the second trenches 112. In such embodiments, the width D1 of the first trenches 12 can be less than the width D2 of the second trenches 112. It should be noted that, the width of the second trenches 112 refers to a size in the extension direction of the first pattern 11.

**[0057]** In the Step S5, the second dielectric layer 4 located in the first trenches 12 can be removed, as shown in FIG. 7.

**[0058]** For example, the second dielectric layer 4 in the first trenches 12 can be removed by using a wet etching process or a dry etching process. Specifically, in this embodiment, the second dielectric layer 4 in the first trenches 12 can be removed by using a wet etching process. More specifically, the second dielectric layer 4 in the first trenches 12 can be removed by using an etchant solution, and the etchant solution does not remove the first dielectric layer 2 on upper surfaces of the first patterns 11 and not remove the substrate 1.

**[0059]** In some embodiments, after removing the second dielectric layer 4 in the first trenches 12, the method further includes the following step.

**[0060]** At Step S6, a third dielectric layer 5 can be filled into the first trenches 12 and the second trenches 112. The third dielectric layer 5 fills the first trenches 12 and the second trenches 112, and no first dielectric layer 2 exists between the third dielectric layer 5 in the second trenches 112 and the second patterns 111, as shown in FIG. 8. Specifically, the third dielectric layer 5 in the first trenches 12 is in direct contact with the first dielectric layer 2, and third dielectric layer 5 in the second trenches 112 is in direct contact with the second patterns 111.

**[0061]** In some embodiments, the third dielectric layer 5 can be formed through a physical vapor deposition process, a chemical vapor deposition process, an atomic layer deposition process, a spin-coating process, or the like. A material of the third dielectric layer 5 can be same as the material of the first dielectric layer 2. In some cases, the material of the third dielectric layer 5 can be different from the material of the first dielectric layer 2. Specifically, the third dielectric layer 5 can be, but are not limited to, a silicon dioxide (SiO<sub>2</sub>) layer or a silicon nitride (SiN) layer. Finally, the third dielectric layer 5 and the first dielectric layer 2 can jointly serve as a shallow trench isolation structure.

**[0062]** The manufacturing process of the present invention is simple, has broad application prospects in the field of semiconductor manufacturing, can effectively overcome shortcomings of existing technologies, and has high industrial utilization value.

**[0063]** It should be understood that, although steps in flowcharts are shown in sequence as indicated by the arrows, these steps are not necessarily performed in sequence as indicated by the arrows. Unless expressly stated herein, these steps are not performed in a strict order and can be performed in another order. In addition, at least some of the steps in the flowcharts can include a plurality of steps or stages. These steps or stages are not necessarily performed at the same time, but can be performed at different times, and these steps or stages are not necessarily performed in sequence, but can be performed in turn or alternately with other steps or at least some of steps or stages in other steps.

**[0064]** The technical features in the previously described embodiments can be combined randomly. For simplicity of description, not all possible combinations of the technical features in the previously described embodiments are described. However, the combinations of these technical features should be considered to be within the scope of the present specification as long as they do not contradict each other.

**[0065]** The previously described embodiments represent merely a few embodiments of the present invention with specific and detailed descriptions, but are not construed as a limitation to the scope of the present invention. It should be noted that, variations and modifications that can further be made by a person skilled in the art

without departing from the concept of the present invention all fall within the protection scope of the present invention. Therefore, the protection scope of the present invention should be subject to the appended claims.

## Claims

1. A method for manufacturing a semiconductor structure, comprising:
  - providing a substrate having a plurality of first trenches, wherein a first pattern is formed between two adjacent first trenches;
  - forming a first dielectric layer, the first dielectric layer covering at least side walls of the first pattern;
  - forming a second dielectric layer, the second dielectric layer filling the first trenches;
  - severing the first pattern to form a second pattern; and
  - removing the second dielectric layer.
2. The method for manufacturing the semiconductor structure of claim 1, wherein forming the first dielectric layer, the first dielectric layer covering at least side walls of the first pattern comprises:
  - forming the first dielectric layer on the side walls of the first pattern and bottom surfaces of the first trenches.
3. The method for manufacturing the semiconductor structure of claim 1, wherein forming the first dielectric layer, the first dielectric layer covering at least side walls of the first pattern comprises:
  - forming the first dielectric layer on the side walls of the first pattern, bottom surfaces of the first trenches, and an upper surface of the first pattern.
4. The method for manufacturing the semiconductor structure of claim 2 or 3, further comprising:
  - removing the first dielectric layer located at the bottom surface of the first trenches after forming the first dielectric layer and prior to forming the second dielectric layer.
5. The method for manufacturing the semiconductor structure of claim 1, wherein a width of the first pattern is less than or equal to 20 nm.
6. The method for manufacturing the semiconductor structure of claim 5, wherein a distance between two adjacent first patterns is less than or equal to 30 nm.
7. The method for manufacturing the semiconductor structure of claim 1, wherein a hardness of the first dielectric layer is greater than a hardness of the second dielectric layer.

8. The method for manufacturing the semiconductor structure of claim 7, wherein the first dielectric layer comprises a silicon dioxide layer.
9. The method for manufacturing the semiconductor structure of claim 7, wherein the second dielectric layer comprises a spin-on carbon layer or a spin-on glass layer.
10. The method for manufacturing the semiconductor structure of claim 1, wherein severing the first pattern to form the second pattern comprises:  
forming a plurality of second trenches on each of first patterns to cut the first pattern into a plurality of second patterns.
11. The method for manufacturing the semiconductor structure of claim 10, further comprising: after removing the second dielectric layer,  
filling a third dielectric layer in the first trenches and the second trenches, wherein the third dielectric layer fills the first trenches and the second trenches and no first dielectric layer exists between the third dielectric layer in the second trenches and the second patterns.
12. The method for manufacturing the semiconductor structure of claim 11, wherein the third dielectric layer comprises a silicon dioxide layer.
13. The method for manufacturing the semiconductor structure of claim 10, wherein forming the plurality of second trenches on each of first patterns to cut the first pattern into the plurality of second patterns comprises:  
  
forming a mask layer on an upper surface of the substrate;  
patterning the mask layer to obtain a patterned mask layer, wherein the patterned mask layer comprises a plurality of opening patterns penetrating through the mask layer, and the plurality of opening patterns define positions and shapes of the second trenches; and  
etching the first patterns based on the patterned mask layer to form the plurality of second trenches on each of the first patterns to cut the first pattern into the plurality of second patterns.
14. The method for manufacturing the semiconductor structure of claim 10, wherein an extension direction of the first pattern obliquely intersects an arrangement direction of adjacent second trenches spaced apart by a shortest distance in different columns.
15. The method for manufacturing the semiconductor structure of claim 10, wherein a depth of the first trenches is greater than a depth of the second trenches.
16. The method for manufacturing the semiconductor structure of claim 10, wherein a width of the first trenches is less than a width of the second trenches.
17. The method for manufacturing the semiconductor structure of claim 10, wherein the second trenches only separate the first pattern without separating the first dielectric layer on the side walls of the first pattern.
18. The method for manufacturing the semiconductor structure of claim 17, wherein the first pattern is separated through an etching process with an etching selection ratio greater than 8 between the first pattern and the first dielectric layer.
19. The method for manufacturing the semiconductor structure of claim 13, wherein a size of the plurality of opening patterns is greater than a width of the first pattern.
20. The method for manufacturing the semiconductor structure of claim 19, wherein a size of the second trenches is less than 15 nm, a thickness of the first dielectric layer ranges from 1 nm to 5 nm, and the size of the plurality of opening patterns is less than 30 nm.

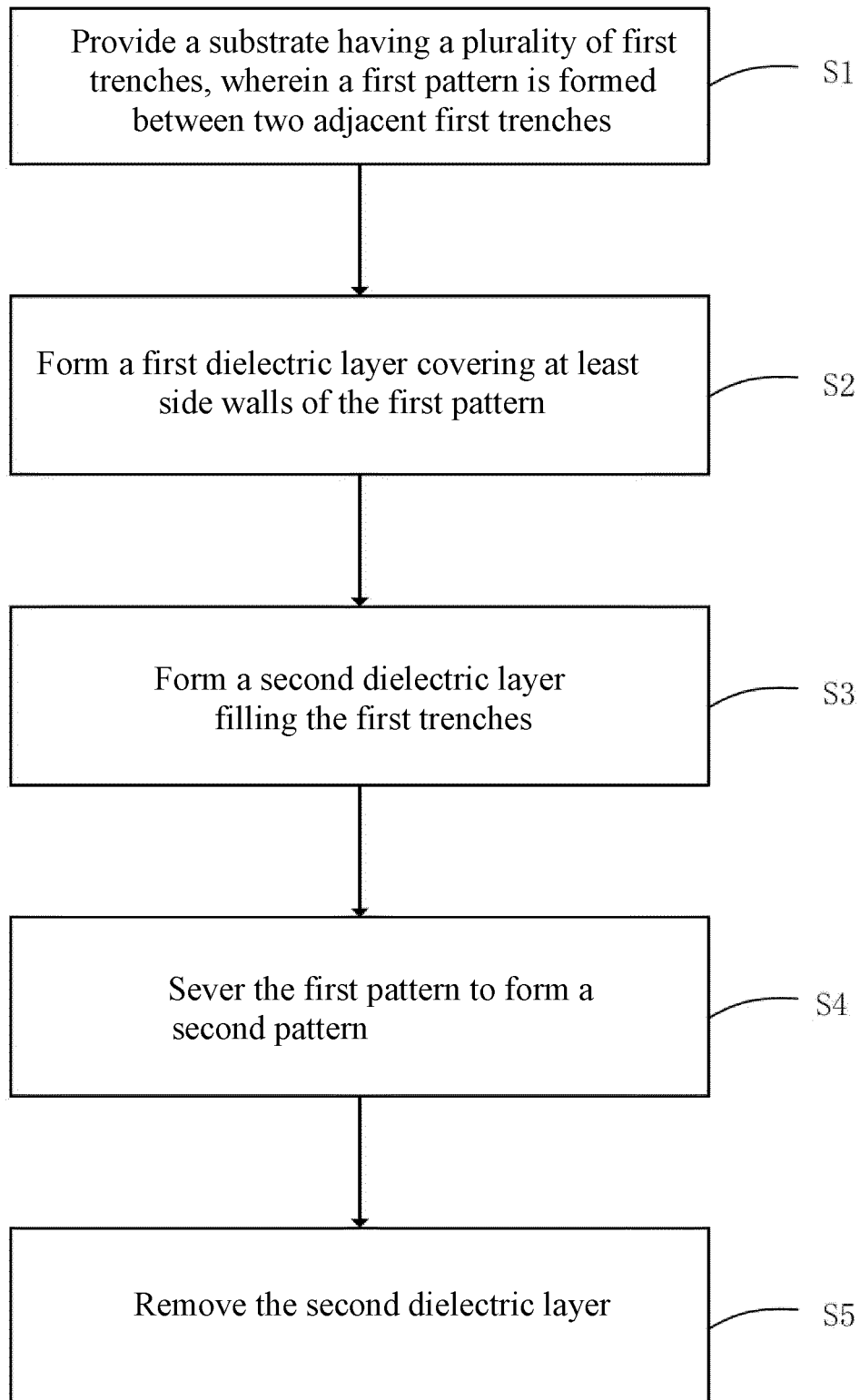


FIG. 1

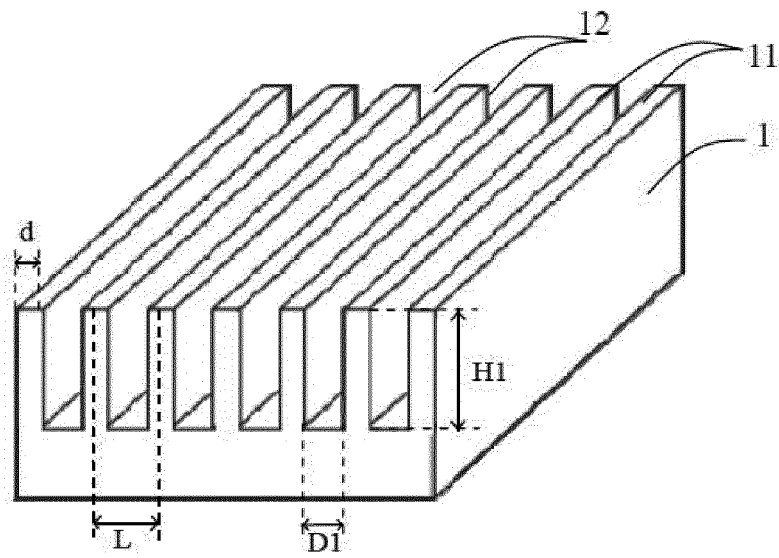


FIG. 2

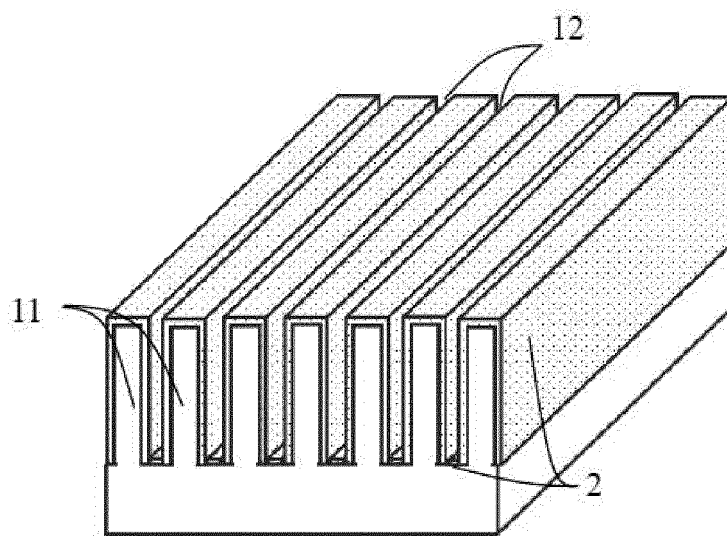


FIG. 3

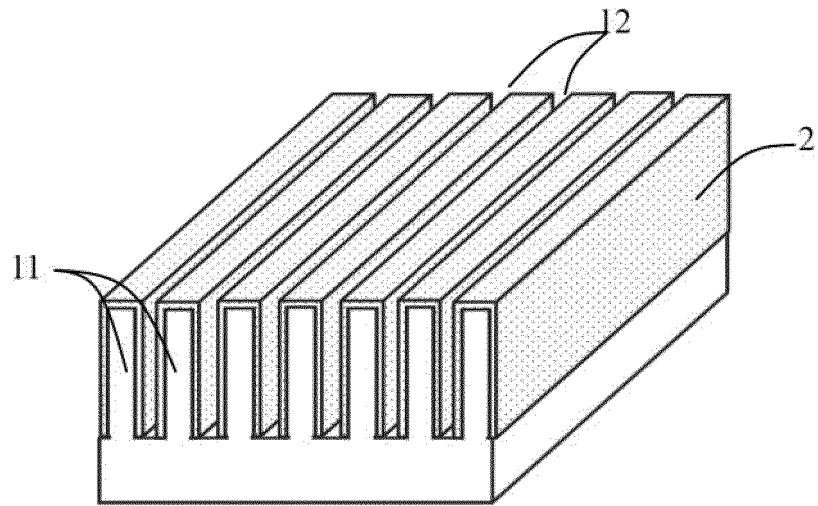


FIG. 4

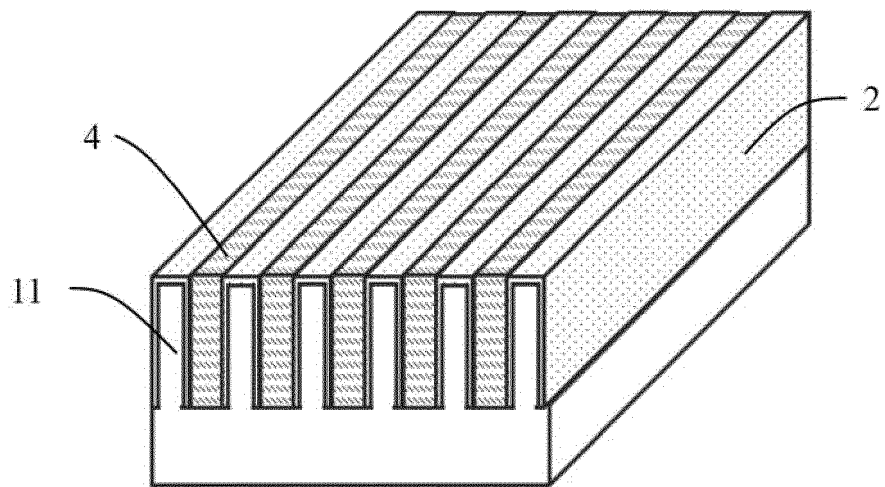


FIG. 5

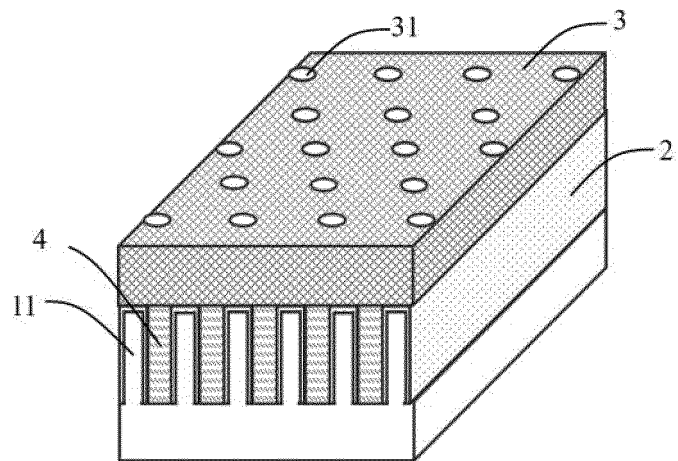


FIG. 6

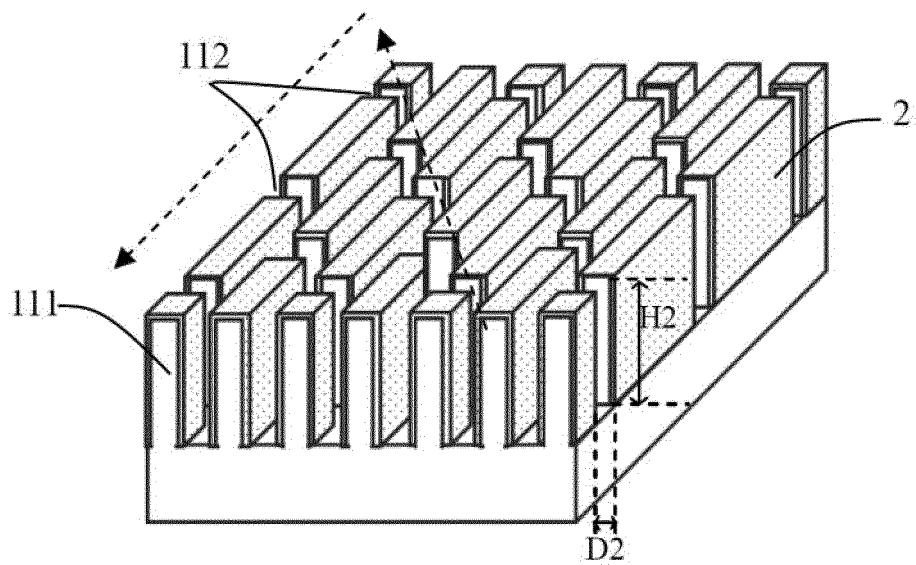


FIG. 7

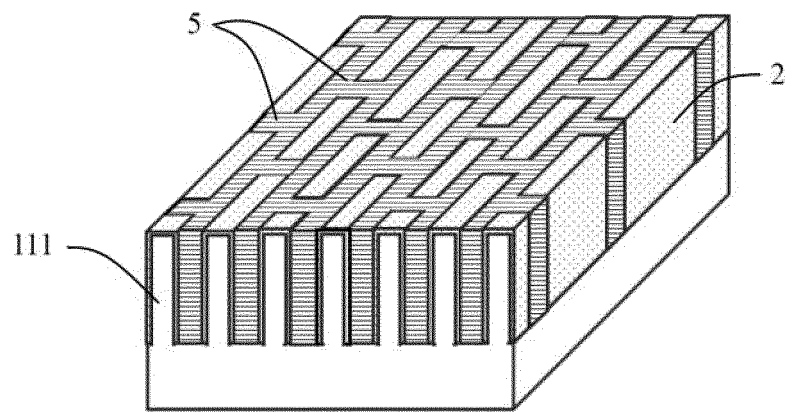


FIG. 8

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2021/083131

| 5         | <b>A. CLASSIFICATION OF SUBJECT MATTER</b><br>H01L 21/8242(2006.01)i<br>According to International Patent Classification (IPC) or to both national classification and IPC                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                       |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|--|-----------|------------------------------------------------------------------------------------|-----------------------|---|---------------------------------------------------------------------------------------------------------------------------------------------|-----|---|---------------------------------------------------------------------------------------------------------------------------------------------|-------|---|------------------------------------------------------------------------------------------|------|---|----------------------------------------------------------------------------------------------------------------------------------|------|
| 10        | <b>B. FIELDS SEARCHED</b><br>Minimum documentation searched (classification system followed by classification symbols)<br>H01L<br>Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                       |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
| 15        | Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)<br>CNABS, CNTXT, DWPI, SIPOABS, CNKI: 沟槽, 沟道, 有源, 填充, 介电, 介质, 保护, 刻蚀, 蚀刻, 存储, 密度, groove, channel, active, fill, dielectric, protect, etch+, memory, density                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                       |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
| 20        | <b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b> <table border="1"> <thead> <tr> <th>Category*</th> <th>Citation of document, with indication, where appropriate, of the relevant passages</th> <th>Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>CN 107275286 A (RUILI INTEGRATED CIRCUIT CO., LTD.) 20 October 2017 (2017-10-20)<br/>description, paragraphs [0119]-[0197], and figures 2-20</td> <td>1-9</td> </tr> <tr> <td>A</td> <td>CN 107275286 A (RUILI INTEGRATED CIRCUIT CO., LTD.) 20 October 2017 (2017-10-20)<br/>description, paragraphs [0119]-[0197], and figures 2-20</td> <td>10-20</td> </tr> <tr> <td>A</td> <td>US 10559568 B1 (NANYA TECHNOLOGY CORP.) 11 February 2020 (2020-02-11)<br/>entire document</td> <td>1-20</td> </tr> <tr> <td>A</td> <td>CN 101577242 A (SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORPORATION, BEIJING) 11 November 2009 (2009-11-11)<br/>entire document</td> <td>1-20</td> </tr> </tbody> </table>                                                                                                                                                                                                                                                                                                                                     |                       |  | Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. | X | CN 107275286 A (RUILI INTEGRATED CIRCUIT CO., LTD.) 20 October 2017 (2017-10-20)<br>description, paragraphs [0119]-[0197], and figures 2-20 | 1-9 | A | CN 107275286 A (RUILI INTEGRATED CIRCUIT CO., LTD.) 20 October 2017 (2017-10-20)<br>description, paragraphs [0119]-[0197], and figures 2-20 | 10-20 | A | US 10559568 B1 (NANYA TECHNOLOGY CORP.) 11 February 2020 (2020-02-11)<br>entire document | 1-20 | A | CN 101577242 A (SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORPORATION, BEIJING) 11 November 2009 (2009-11-11)<br>entire document | 1-20 |
| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Relevant to claim No. |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
| X         | CN 107275286 A (RUILI INTEGRATED CIRCUIT CO., LTD.) 20 October 2017 (2017-10-20)<br>description, paragraphs [0119]-[0197], and figures 2-20                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 1-9                   |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
| A         | CN 107275286 A (RUILI INTEGRATED CIRCUIT CO., LTD.) 20 October 2017 (2017-10-20)<br>description, paragraphs [0119]-[0197], and figures 2-20                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 10-20                 |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
| A         | US 10559568 B1 (NANYA TECHNOLOGY CORP.) 11 February 2020 (2020-02-11)<br>entire document                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | 1-20                  |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
| A         | CN 101577242 A (SEMICONDUCTOR MANUFACTURING INTERNATIONAL CORPORATION, BEIJING) 11 November 2009 (2009-11-11)<br>entire document                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 1-20                  |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
| 35        | <input type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                       |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
| 40        | * Special categories of cited documents:<br>“A” document defining the general state of the art which is not considered to be of particular relevance<br>“E” earlier application or patent but published on or after the international filing date<br>“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)<br>“O” document referring to an oral disclosure, use, exhibition or other means<br>“P” document published prior to the international filing date but later than the priority date claimed<br>“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention<br>“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone<br>“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art<br>“&” document member of the same patent family |                       |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
| 45        | Date of the actual completion of the international search<br><b>24 May 2021</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                       |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
| 50        | Date of mailing of the international search report<br><b>09 June 2021</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                       |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
| 55        | Name and mailing address of the ISA/CN<br><b>China National Intellectual Property Administration (ISA/CN)<br/> No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing 100088<br/> China</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                       |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |
|           | Authorized officer<br>Facsimile No. (86-10)62019451<br>Telephone No.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                       |  |           |                                                                                    |                       |   |                                                                                                                                             |     |   |                                                                                                                                             |       |   |                                                                                          |      |   |                                                                                                                                  |      |

INTERNATIONAL SEARCH REPORT  
Information on patent family members

International application No.

PCT/CN2021/083131

| Patent document<br>cited in search report | Publication date<br>(day/month/year) | Patent family member(s) | Publication date<br>(day/month/year) |
|-------------------------------------------|--------------------------------------|-------------------------|--------------------------------------|
| CN 107275286 A                            | 20 October 2017                      | CN 107230675 B          | 26 June 2018                         |
|                                           |                                      | CN 107230675 A          | 03 October 2017                      |
|                                           |                                      | CN 107275286 B          | 19 June 2018                         |
| US 10559568 B1                            | 11 February 2020                     | CN 110890342 A          | 17 March 2020                        |
|                                           |                                      | TW I688107 B            | 11 March 2020                        |
|                                           |                                      | TW 202011611 A          | 16 March 2020                        |
|                                           |                                      | US 2020126994 A1        | 23 April 2020                        |
| CN 101577242 A                            | 11 November 2009                     | CN 101577242 B          | 23 March 2011                        |

Form PCT/ISA/210 (patent family annex) (January 2015)

**REFERENCES CITED IN THE DESCRIPTION**

*This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.*

**Patent documents cited in the description**

- CN 202010428539 [0001]