(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 1 313 282 A1**

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
21.05.2003 Bulletin 2003/21

(51) Int Cl.[7]: **H04L 27/26**, H04L 25/02

(21) Application number: **02025271.4**

(22) Date of filing: **12.11.2002**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LU MC NL PT SE SK TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **15.11.2001 JP 2001349886**
12.07.2002 JP 2002203839

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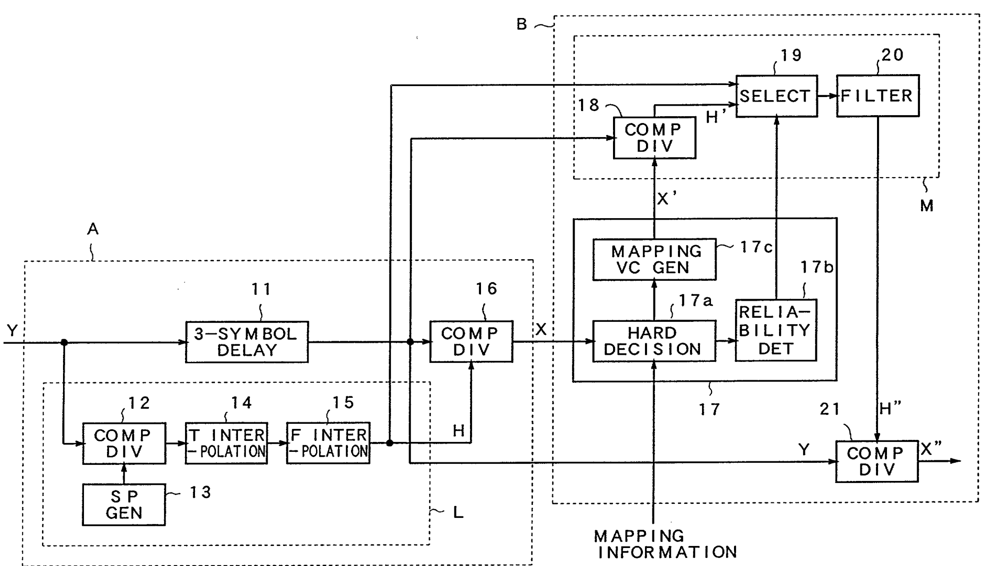
(54) **Method and apparatus for OFDM (orthogonal frequency division multiplexing) demodulation**

(57) At a first equalizer A, a scattered pilot signal is interpolated in time direction and frequency direction, thereby obtaining a channel characteristic H. By complex-dividing a received signal Y subjected to FFT by the channel characteristic, the respective signal is reconstituted. At a second equalizer B, a resultant signal is hard-decided, thereby obtaining a mapping vector X. Then, by dividing the received signal Y by X, a channel characteristic is calculated again. The calculated channel characteristic having reliability is substituted for the original channel characteristic. The substituted channel characteristic is filtered in frequency direction. In this way, a channel characteristic H' is calculated again and a signal point is reconstituted.

F I G. 1



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Description

[0001] The present invention relates to an orthogonal frequency division multiplex (OFDM) demodulation method and an OFDM demodulator used for digital broadcasting by an OFDM transmission system.

[0002] Recently, a ground digital television broadcasting system has been studied hard. In the United States of America, a VSB system is utilized. In European countries and Japan, an orthogonal frequency division multiplex (OFDM) system is utilized as a transmission system. In England and Singapore and the like, commercial service for such system has already started. The OFDM system divides a transmission signal into a large number of carriers that are orthogonal with each other, multiplexes the carriers and transmits the same.

[0003] An OFDM signal may have long symbol interval because of a large number of carriers being used. For this reason, an interval during which a part of signal is cyclicly copied and then transmitted, i.e., a so-called guard interval may be provided. A delayed wave within the guard interval does not occur an interference between symbols. Thus, an equalizer of OFDM demodulator can be simply structured.

[0004] In accordance with the OFDM system used in European countries and Japan, a channel characteristic is estimated at a receiving end. Thus, scattered pilot signals (SP signals) for modulating carriers periodically distributed in directions of symbol time and carrier frequency at specified phase and amplitude is provided at a transmitting end. Besides, continual pilot signals (CP signals), transmission parameter signals (TMCC signals), and ancillary information signals (AC signals) are placed at specified carrier positions and data signals are placed at other carrier positions.

[0005] Conventionally, at a receiving end, a scattered pilot signal is fetched and a fetched pilot signal is divided by known amplitude and phase. In this way, a channel characteristic at a position of the scattered pilot signal is obtained. A channel characteristic at each information carrier position is calculated by interpolating the scattered pilot signal in directions of symbol time and carrier frequency.

[0006] Conventionally in ground digital broadcasting, fixed receivers for receiving HDTV signal have been mainly considered. Under a fixed receiving environment, for interpolation in symbol direction, a zero order hold filter is utilized in order to reduce a scale of circuit.

[0007] Recently, receiving of mobile which is one of characteristics for ground digital broadcasting has attracted attention. Under an environment of receiving a mobile, a channel varies significantly. For this reason, there is a limit to conventionally estimate a channel for scattered pilot signal in symbol direction by using a zero order hold filter. Thus, it is considered that linear interpolation of scattered pilot signal in symbol time direction must be required. Nevertheless, only linear interpolation of scattered pilot signal is insufficient for characteristics under an environment of receiving a mobile. Thus, it has been studied to use diversity or the like simultaneously.

[0008] It is an object of the invention to provide an OFDM demodulation method and an OFDM demodulator used for improving receiving performance under an environment of receiving a mobile.

[0009] This object is achieved by the method of claim 1 and the demodulator of claim 10. Advantageous embodiments are characterized in the sub-claims.

[0010] The present invention provides a demodulation technique used for orthogonal frequency division multiplex (OFDM) transmission system which modulates a plurality of carriers with their frequencies being orthogonal with each other for each symbol period so as to transmit digital information.

[0011] When a scattered pilot signal and a continual pilot signal are modulated by specified amplitude and phase that are uniquely determined by a carrier number k of carrier in an overall transmission band, among a received signal Yn,1 subjected to FFT, a scattered pilot signal SPn,k is firstly fetched. Next, the scattered pilot signal is interpolated in time direction and frequency direction, thereby estimating a channel characteristic Hn,1. Yn,1 is complex-divided by the resultant channel characteristic Hn,1, whereby mapping vectors Xn,1 for transmission parameter signal, ancillary information signal and data signal placed at the various carrier positions are reconstituted.

[0012] By hard-deciding the reconstituted mapping vectors Xn,1, a primary mapping vector X'n,1 at each carrier position is calculated. Then, Yn,1 is complex-divided by the mapping vector X'n,1, thereby caluculating a primary channel characteristic H'n,1.

[0013] The resultant H'n,1 is filtered in frequency direction, thereby calculating a secondary channel characteristic H"n,1. By dividing Yn,1 by H"n,1, a secondary mapping vector X"n,1 is calculated.

[0014] By repeating such equalization process for several times, precision in estimation of channel characteristic can be improved especially under an environment of receiving a mobile while a receiving performance under the environment of receiving a mobile can be improved.

[0015] Embodiments of the invention are now described with reference to the drawings.

Fig. 1 is a block diagram showing an overall structure of an OFDM demodulator according to a first embodiment of the present invention;

Fig. 2 illustrates an arrangement of carriers for an OFDM signal;

Fig. 3 is mapping illustrations showing arrangements of a received signal used for the OFDM demodulator of the present invention;

Fig. 4 illustrates thresholds for mapping points used for calculating a channel characteristic in hard-decided data;

Figs. 5A to 5C illustrate arrangements of received signals obtained by a conventional decoding method and decoding methods of embodiments of the present invention;

Fig. 6 is a block diagram showing an overall structure of an OFDM demodulator according to a second embodiment of the present invention;

Fig. 7 is a block diagram showing structures of a first equalizer A and a second equalizer B of an OFDM demodulator according to a third embodiment of the present invention;

Fig. 8 is a block diagram showing a structure of a third equalizer C of the OFDM demodulator according to the third embodiment of the present invention;

Fig. 9 is a block diagram showing structures of a first equalizer A and a second equalizer B of an OFDM demodulator according to a fourth embodiment of the present invention;

Fig. 10 is a block diagram showing a structure of a third equalizer C of the OFDM demodulator according to the fourth embodiment of the present invention;

Fig. 11 is a block diagram showing structures of a first equalizer A and a second equalizer B of an OFDM demodulator according to a fifth embodiment of the present invention;

Fig. 12 is a block diagram showing a structure of a third equalizer D of the OFDM demodulator according to the fifth embodiment of the present invention;

Fig. 13 is a block diagram showing structures of a first equalizer A and a second equalizer B of an OFDM demodulator according to a sixth embodiment of the present invention;

Fig. 14 is a block diagram showing a structure of a third equalizer E of the OFDM demodulator according to the sixth embodiment of the present invention;

Fig. 15 is a block diagram showing structures of a first equalizer A and a second equalizer B of an OFDM demodulator according to a seventh embodiment of the present invention; and

Fig. 16 is a block diagram showing a structure of a third equalizer F of the OFDM demodulator accoridng to the seventh embodiment of the present invention.

Prior to the detail description of embodiments of the present invention, a basic principle of the present invention will be described by using mathematical expressions. A parameter n indicates a symbol number and a parameter k indicates a carrier number. Parameter Yn,k indicates a received OFDM signal after FFT processing. A channel characteristic is indicated by Hn,k. Parameter Xn,k indicates a received signal (also referred to as a mapping vector) at each carrier position. The received signal Xn,k is equalized by using the following formula (1):

$$Xn,k = Yn,k/Hn,k \qquad (1).$$

[0016] Calculation of the channel characteristic Hn,k is described in various references. This calculation is described in detail in the embodiments of the present invention. The channel characteristic is calculated by interpolating a scattered pilot signal in time direction and frequency direction. Under an environment of receiving a mobile, however, Hn, k calculated by the scattered pilot signal may not necessarily be a precisely estimated value for the channel characteristic.

[0017] In accordance with the present invention, a received signal Xn,k is firstly reconstituted by using a channel characteristic calculated by using a scattered pilot signal. Then, a hard decision is performed for Xn,k in accordance with mapping information at each carrier position. If a distance from an original mapping point is equal to or shorter than a threshold (Th), it is determined that Xn,k has reliability.

[0018] Next, the aforementioned formula (1) is transformed, thereby obtaining the following formula (2):

$$H'n,k = Yn,k/Xn,k \qquad (2).$$

[0019] If it is determined that Xn,k has reliability, a new channel characteristic H'n,k at a carrier position is calculated by using the formula (2) and a mapping vector subjected to hard decision at an original signal point. Since H'n,k calculated at the carrier position has more reliability than Hn,k at the same carrier position, Hn,k is replaced with H'n,k. A new channel characteristic is filtered in frequency direction. The newly calculated channel characteristic has more reliability because of the above-described process. Thus, more precise received data can be obtained by using again the formula (1). Such process can be repeated.

(First Embodiment)

[0020] Next, an OFDM demodulator according to a first embodiment will be described with reference to the drawings. Fig. 1 shows a structural view of an OFDM demodulator of the first embodiment. The OFDM demodulator is configured so as to hard-decide a demodulated received signal and then calculate again a channel characteristic. In a receiving system shown in Fig. 1, a received OFDM signal is subjected to FFT processing. Then, a resultant signal is inputted, as an OFDM signal, to a first equalizer A shown by broken lines. The first equalizer A is configured so as to include a first channel estimation block L, a three-symbol delay unit 11 and a second complex divider (COMP DIV) 16. The first equalizer A estimates a channel characteristic by linearly interpolating a scattered pilot signal, and then equalizes a received OFDM decoded signal.

[0021] Fig. 2 shows an example of an arrangement of an OFDM signal. Mod is a symbol indicating a residue operation and p indicates an integer number. As shown in Fig. 2, scattered pilot signals (SP signal) are distributed and arranged at specified carrier positions. Within a corresponding segment, each of specified position satisfies $k = 3 (n \bmod 4) + 12p$ for symbol with symbol number n, where k is a carrier number.

[0022] Referring to Fig. 1, a scattered pilot signal is fetched from an OFDM signal. Then, at a first complex divider 12, the scattered pilot signal is complex-divided by a reference SP signal outputted from an SP signal generator (SP GEN) 13. The scattered pilot signal is a signal which is modulated by specified amplitude and phase that are uniquely determined at a time of its transmission by a carrier number k in an overall transmission band for the corresponding carrier. By dividing the transmitted scattered pilot signal by the reference SP signal, the amplitude and the phase of the scattered pilot signal are aligned in a direction and a channel characteristic at the position of the scattered pilot signal can be calculated.

[0023] A time direction linear interpolation circuit (T INTERPOLATION) 14 interpolates a scattered pilot signal in symbol time direction. Thus, a channel characteristic at the position of the carrier number $k = 3p$ can be estimated. As linear interpolation is performed in symbol time direction, an OFDM signal subjected to FFT is delayed by three symbols at the three-symbol delay unit 11.

[0024] A frequency direction interpolation circuit 15 (F INTERPOLATION) is a filter for interpolating a channel characteristic in frequency direction. Thus, the channel characteristics at all carrier number positions can be estimated. In the first equalizer A, the SP signal generator 13, the first complex divider 12, the time direction linear interpolation circuit 14 and the frequency direction interpolation circuit 15 constitute a first channel estimation block L. A second complex divider 16 complex-divides an OFDM signal subjected to FFT by a channel characteristic so as to reconstitute a phase and an amplitude of the OFDM signal.

[0025] As described above, the phase and the amplitude of the conventional OFDM signal are processed by the first equalizer A shown in Fig. 1, and thus a data signal is decoded. As seen from a signal arrangement shown in Fig. 2, the number of scattered pilot signals is small. Thus, under an environment of receiving a mobile, a channel characteristic cannot sufficiently estimated only by the above-described process.

[0026] In accordance with the present embodiment, as shown in Fig. 1, a second equalizer B is provided. The second equalizer B performs hard decision process, on the basis of mapping information, for a signal whose amplitude and phase have been determined at the first equalizer A for each mapping.

[0027] Fig. 3 shows constellation diagrams showing the various mapping points. Euclidean distances between mapping points are different for each of mappings, i.e., for each of BPSK, QPSK, 16QAM and 64QAM. Fig. 4 illustrates thresholds (Th) of BPSK and QPSK utilized for the present invention for data subjected to hard decision. Although not shown in Fig. 4, thresholds are used for 16QAM and 64QAM, respectively. The shorter the distance between signal points of mapping, the smaller threshold may be used or may not be used. In accordance with the present embodiment, a threshold is provided for each mapping.

[0028] At a hard decision block 17 shown in Fig. 1, data which is subjected to hard decision at a hard decision unit 17a is supplied to a reliability detection block 17b. At the reliability detection block (RELIABILITY DET) 17b, reliability of the data is determined based on the aforementioned threshold. Further, the data which is subjected to hard decision at the hard decision unit 17a is supplied to a mapping vector generator (MAPPING VC GEN) 17c. At the mapping vector generator 17c, a mapping vector at a hard decision point is selected.

[0029] A third complex divider 18 divides a signal subjected to FFT by a mapping vector from the mapping vector generator 17c. A resultant signal obtained by division is a channel characteristic $H'_{n,1}$ at the carrier position. If it is determined at the reliability detection block 17b that the channel characteristic $H'_{n,1}$ has reliability, the channel characteristic $H'_{n,1}$ has higher reliability than the channel characteristic $H_{n,1}$ at the carrier position. Hence a selection circuit (SELECT) 19 substitutes the channel characteristic $H'_{n,1}$ at the carrier position obtained at the frequency direction interpolation circuit 15 for the channel characteristic $H_{n,1}$.

[0030] If it is determined at the reliability detection block 17b that the channel characteristic $H'_{n,1}$ does not have reliability, the selection circuit 19 selects the channel characteristic $H_{n,1}$ that is calculated by the frequency direction interpolation circuit 15. The channel characteristic selected by the selection circuit 19 is subjected to filter process at a frequency direction filter 20.

[0031] A fourth complex divider 21 divides a signal Yn,1 subjected to FFT by using a second channel characteristic H"n,1 calculated by the frequency direction filter 20 so as to obtain a signal with newly determined amplitude and phase. This signal is referred to as a second mapping vector X"n,1. The third complex divider 18, the hard decision block 17, the selection circuit 19 and the frequency direction filter 20 in the second equalizer B constitute a second channel estimation block M. Accordingly, the second equalizer B is formed of the second channel estimation block M, the hard decision block 17 and the fourth complex divider 21.

[0032] Figs. 5A to 5C show one example of signal points obtained by the present embodiment. Fig. 5A shows a distribution of signal outputted from the complex divider 16 of the equalizer A shown in Fig. 1. Fig. 5B shows a distribution of signal outputted from the complex divider 21 of the second equalizer B shown in Fig. 1. 16QAM is utilized in the present embodiment. As seen from the figures, a distribution range of constellation of Fig. 5B is smaller than that of Fig. 5A. In this way, reliability of decoded data is improved.

(Second Embodiment)

[0033] An OFDM demodulator according to a second embodiment of the present invention will be described. Fig. 6 is a structural view of the OFDM demodulator of the second embodiment. The OFDM demodulator is also configured so as to hard-decide a demodulated received signal and then calculate again a channel characteristic. As in the first embodiment, the first equalizer A includes a three-symbol delay unit 31, a first complex divider 32, an SP signal generator 33, a time direction linear interpolation circuit 34, a frequency direction interpolation circuit 35 and a second complex divider 36. The second equalizer B includes a hard decision block 37, a third complex divider 38, a selection circuit 39, a frequency direction filter 40 and a fourth complex divider 41. The hard decision block 37 includes a hard decision unit 37a, a reliability detection block 37b and a mapping vector generator 37c.

[0034] The second embodiment is different from the first embodiment in that: when it is determined by the reliability detection block 37b that low reliability is provided, then a stop signal is outputted and a complex dividing process is not performed by the complex divider 38. Namely, at the reliability detection block 37b, a predetermined threshold is provided for each type of mapping and it is determined whether or not a mapping vector Xn,1 is within a predetermined threshold. If the mapping vector is within the predetermined threshold, the selection circuit 39 selects the primary channel characteristic H'n,1. Other processes are the same as in the first embodiment and the same effects as those of the first embodiment can be obtained.

(Third Embodiment)

[0035] An OFDM demodulator according to a third embodiment of the present invention will be described. Figs. 7 and 8 are structural views of the OFDM demodulator according to the third embodiment. The OFDM demodulator is configured so as to include the first equalizer A and the second equalizer B shown in Fig. 1 and a third equalizer C shown in Fig. 8.

[0036] As in the first embodiment, the first equalizer A has a first channel estimation block L, a three-symbol delay unit 51 and a second complex divider 56. The first channel estimation block L is configured so as to include a first complex divider 52, an SP signal generator 53, a time direction linear interpolation circuit 54 and a frequency direction interpolation circuit 55.

[0037] The SP signal generator 53 generates a known SP signal. The first complex divider 52 complex-divides a scattered pilot signal SPn,k of the received signal Yn,1 subjected to FFT by an output of the SP signal generator 53. The time direction linear interpolation circuit 54 interpolates an output of the first complex divider 52 in time direction. The frequency direction interpolation circuit 55 interpolates an output of the time direction linear interpolation circuit 54 in frequency direction so as to output a channel characteristic Hn,1. The second complex divider 56 complex-divides Yn,1 by the channel characteristic Hn,1 and thus outputs a mapping vector Xn,1.

[0038] The second equalizer B has a second channel estimation block M, a first hard decision block 57 and a fourth complex divider 61. The second channel estimation block M is configured so as to include a third complex divider 58, a first selection circuit 59 and a first frequency direction filter 60. The third complex divider 58 complex-divides a received signal Yn,1 by a mapping vector X'n,1. The first selection circuit 59 selects an output H'n,1 of the third complex divider 58 or a channel characteristic Hn,1 depending on an output of the reliability detection block 57b. The first frequency direction filter 60 filters an output of the first selection circuit 59.

[0039] The first hard decision block 57 includes a first hard decision unit 57a, a first reliability detection block 57b and a first mapping vector generator 57c. The first hard decision unit 57a hard-decides an output Xn,1 of the first equalizer A. The first reliability detection block 57b detects reliability of result of hard decision. The first mapping vector generator 57c calculates a primary mapping vector X'n,1 on a basis of decision result of the first hard decision unit 57a. The fourth complex divider 61 calculates a secondary mapping vector X"n,1 by complex-dividing a received signal

Yn,1 by an output H"n,1 of the first frequency direction filter 60.

[0040] A third equalizer C shown in Fig. 8 has a third channel estimation block N, a second hard decision block 62 and a sixth complex divider 66. The third equalizer C repeats a process performed by the second equalizer B. The third channel estimation block N is configured so as to include a fifth complex divider 63, a second selection circuit 64 and a second frequency direction filter 65. The fifth complex divider 63 complex-divides a received signal Yn,1 by a mapping vector X"'n,1. The second selection circuit 64 selects an output H"'n,1 of the fifth complex divider 63 or a channel characteristic H"n,1 depending on an output of the second hard decision block 62. The second frequency direction filter 65 filters an output of the second selection circuit 64.

[0041] The second hard decision block 62 is configured so as to include a second hard decision unit 62a, a second reliability detection block 62b and a mapping vector generator 62c. The second hard decision unit 62a hard-decides an output X"n,1 of the second equalizer B. The second reliability detection block 62b detects reliability of result of hard decision. The second mapping vector generator 62c calculates a mapping vector X"'n,1 on the basis of decision result of the second hard decision unit 62a. The sixth complex divider 66 calculates a quaternary mapping vector X""n,1 by complex-dividing a received signal Yn,1 by an output H""n,1 of the second frequency direction filter 65.

[0042] The third equalizer C repeats the same process as in the second equalizer B. Thus, as shown in Fig. 5C, mapping points of received signal can be further converged into a central position of each of symbol points.

(Fourth Embodiment)

[0043] An OFDM demodulator according to a fourth embodiment of the present invention will be described. Figs. 9 and 10 are structural views of the OFDM demodulator of the fourth embodiment. The OFDM demodulator has a first equalizer A and a second equalizer B shown in Fig. 9 and a third equalizer C shown in Fig. 10.

[0044] The first equalizer A includes, as in the first to third embodiments, a three-symbol delay unit 71, a first complex divider 72, an SP signal generator 73, a time direction linear interpolation circuit 74, a frequency direction interpolation circuit 75, and a second complex divider 76.

[0045] The second equalizer B includes a first hard decision block 77, a third complex divider 78, a first selection circuit 79, a first frequency direction filter 80 and a fourth complex divider 81. The first hard decision block 77 is configured so as to include a first hard decision unit 77a, a first reliability detection block 77b and a first mapping vector generator 77c.

[0046] The third equalizer C repeats same process as performed by the second equalizer B. As shown in Fig. 10, the third equalizer C includes a second hard decision block 82, a fifth complex divider 83, a second selection circuit 84, a second frequency direction filter 85, and a sixth complex divider 86. The second hard decision block 82 includes a second hard decision unit 82a, a second reliability detection block 82b, and a second mapping vector generator 82c.

[0047] The present embodiment is different from the third embodiment only in that: a signal inputted to the selection circuit 84 is not an output of the frequency direction filter 80 but an output of the selection circuit 79. Namely, the second reliability detection block 82b applies a predetermined threshold to each type of mapping and determines whether or not a mapping vector X"n,1 is within a predetermined threshold. If it is determined that the mapping vector is within the predetermined threshold, the second selection circuit 84 selects H"'n,1. If it is determined that the mapping vector is outside the predetermined threshold, the second selection circuit 84 selects the output of the selection circuit 79. In accordance with the present embodiment, almost the same effects as in the OFDM demodulator of the third embodiment can be obtained.

(Fifth Embodiment)

[0048] Next, an OFDM demodulator according to a fifth embodiment of the present invention will be described. Figs. 11 and 12 are structural views of the OFDM demodulator of the fifth embodiment. The OFDM demodulator includes a first equalizer A and a second equalizer B shown in Fig. 11 and a third equalizer D shown in Fig. 12.

[0049] The first equalizer A includes an SP extraction unit 110, a three-symbol delay unit 111, a first channel estimation block L and a second complex divider 116. The SP extraction unit 110 extracts an SP signal from a received signal Yn,1 subjected to FFT. The first channel estimation block L includes an SP signal generator 113, a first complex divider 112, a time direction linear interpolation circuit 114, and a frequency direction interpolation circuit 115.

[0050] The SP signal generator 113 generates a known SP signal. The first complex divider 112 complex-divides a distributed split signal SPn,k of received signal Yn,1 subjected to FFT by an output of the SP signal generator 113. The time direction linear interpolation circuit 114 interpolates an output of the first time direction complex divider 112. The frequency direction interpolation circuit 115 interpolates an output of the time direction linear interpolation circuit 114 in frequency direction so as to calculate a channel characteristic Hn,1. The second complex divider 116 complex-divides the received signal Yn,1 by the channel characteristic Hn,1 and thus outputs a mapping vector Xn,1.

[0051] The second equalizer B includes a hard decision block 117 and a second channel estimation block M. The hard decision block 117 includes a hard decision unit 117a, a reliability detection block 117b, and a mapping vector generator 117c. The hard decision unit 117a hard-decides an output Xn,1 of the first equalizer A. The reliability detection block 117b detects reliability of result of hard decision. The mapping vector generator 117c calculates a mapping vector X'n,1 on the basis of result of decision of the hard decision unit 117a.

[0052] The second channel estimation block M is configured so as to include a third complex divider 118, a selection circuit 119, and a frequency direction filter 120. The third complex divider 118 complex-divides the received signal Yn, 1 by the mapping vector X'n,1. The selection circuit 119 selects an output H'n,1 of the third complex divider 118 or a channel characteristic Hn,1 depending on an output of the reliability detection block 117b. The frequency direction filter 120 filters an output of the selection circuit 119 and outputs a secondary channel characteristic H"n,1.

[0053] As shown in Fig. 12, the third equalizer D includes an SP extraction unit 121, a time direction linear interpolation circuit 122, an frequency direction interpolation circuit 123, a three-symbol delay unit 124, and a fourth complex divider 125. The SP extraction unit 121 extracts an SP signal at a scattered pilot signal position SPn,k by using the channel characteristic H"n,1 obtained by the second equalizer B. The time direction linear interpolation circuit 122 interpolates an output of the SP extraction unit 121 in time direction. The frequency direction interpolation circuit 123 interpolates an output of the time direction linear interpolation circuit 122 in frequency direction so as to calculate a tertiary channel characteristic H"'n,1. The fourth complex divider 125 complex-divides a received signal Yn,1 which is delayed by the three-symbol delay unit 124 by the channel characteristic H"'n,1.

[0054] Referring to Fig. 11, for the purpose of comparison of the third equalizer D to the first equalizer A, the SP extraction unit 110 is shown in the first equalizer A. However, the SP extraction unit 110 is not shown in the first to fourth embodiments.

[0055] In accordance with the fifth embodiment, same as the channel characteristic calculated in the first embodiment, a channel characteristic at an SP signal position is extracted from an output of the frequency direction filter 120 by the SP extraction unit 121. Then, the channel characteristic at the SP signal position is interpolated in time direction by the time direction linear interpolation circuit 122. In this way, a channel characteristic at a position of carrier number k = 3p (wherein p indicates an integer number) is estimated. Because linear interpolation is performed in a symbol direction, an OFDM signal subjected to FFT is further delayed by three symbols at the three-symbol delay unit 124. As compared to the channel characteristic at the complex divider 112 shown in Fig. 11, the channel characteristic extracted by the SP extraction unit 121 has a noise removed and high reliability. Subsequent time direction linear interpolation circuit 122 and frequency direction interpolation circuit 123 operate similarly to the interpolation circuit 114 and the interpolation circuit 115 in the first equalizer A.

[0056] An output of the three-symbol delay unit 124 is divided at the complex divider 125 by using a channel characteristic serving as an output of the frequency direction interpolation circuit 123 which is calculated again. As a result, a signal at each carrier position can be reconstituted with high precision.

(Sixth Embodiment)

[0057] Next, an OFDM demodulator of a sixth embodiment of the present invention will be described. Figs. 13 and 14 are structural views of the OFDM demodulator according to the sixth embodiment. The OFDM demodulator includes a first equalizer A and a second equalizer B shown in Fig. 13 and a third equalizer E shown in Fig. 14.

[0058] The first equalizer A includes a first channel estimation block L, a three-symbol delay unit 131 and a second complex divider 136. The first channel estimation block L includes an SP signal generator 133, a first complex divider 132, a time direction linear interpolation circuit 134, and a frequency direction interpolation circuit 135.

[0059] The SP signal generator 133 generates a known SP signal. The first complex divider 132 complex-divides a scattered pilot signal SPn,k of received signal Yn,1 subjected to FFT by an output of the SP signal generator 133. The time direction linear interpolation circuit 134 interpolates an output of the first complex divider 132 in time direction. The frequency direction interpolation circuit 135 interpolates an output of the time direction linear interpolation circuit 134 in frequency direction so as to calculate a channel characteristic Hn,1. The second complex divider 136 complex-divides the received signal Yn,1 by the channel characteristic Hn,1 so as to output a mapping vector Xn,1.

[0060] The second equalizer B includes a hard decision block 137 and a second channel estimation block M. The hard decision block 137 includes a hard decision unit 137a, a reliability detection block 137b, and a mapping vector generator 137c. The hard decision unit 137a hard-decides an output Xn,1 of the first equalizer A. The reliability detection block 137b detects reliability of result of hard decision. The mapping vector generator 137c calculates a mapping vector X'n,1 of output of the hard decision unit 137a.

[0061] The second channel estimation block M includes a third complex divider 138, a selection circuit 139, and a frequency direction filter 140. The third complex divider 138 complex-divides the received signal Yn,1 by the mapping vector X'n,1. The selection circuit 139 selects an output H'n,1 of the third complex divider 138 or a channel characteristic Hn,1 depending on an output of the reliability detection block 137b. The frequency direction filter 140 filters an output of the selection circuit 139 and outputs a secondary channel characteristic H"n,1.

[0062] The third equalizer E includes a two-symbol delay unit 141, a time direction filter 142, an one-symbol delay unit 143, and a fourth complex divider 144.

[0063] The two-symbol delay unit 141 delays the channel characteristic H"n,1 obtained by the second equalizer B by two symbols. The time direction filter 142 interpolates an output H"n-2,1 of the two-symbol delay unit 141 and the channel characteristic H"n,1 not subjected to symbol delay in time direction so as to obtain a tertiary channel characteristic H"'n-1,1. The one-symbol delay unit 143 delays a received signal Yn,1 obtained from the first equalizer A by one symbol. The fourth complex divider 144 complex-divides the signal Yn-1,1 which is delayed by one symbol by an output H"'n-1,1 of the time direction filter 142.

[0064] In accordance with the sixth embodiment, a channel characteristic outputted from the frequency direction filter 140 in the second equalizer B is delayed by two symbols at the two-symbol delay unit 141. The channel characteristic delayed by two symbols and the channel characteristic which is not delayed at the same carrier position are averaged by the time direction filter 142. Then, a channel characteristic at an intermediate symbol position is calculated by the following formula (3):

$$H\ (n-1,k) = [H\ (n,k) + H\ (n-2,k)]/2 \qquad (3).$$

[0065] The one-symbol delay unit 143 further delays a signal subjected to FFT by one symbol at in order to make this process correspond to a delay time.

(Seventh Embodiment)

[0066] Next, an OFDM demodulator according to a seventh embodiment of the present invention will be described. Figs. 15 and 16 are structural views of the OFDM demodulator of the seventh embodiment. The OFDM demodulator includes a first equalizer A and a second equalizer B shown in Fig. 15 and a third equalizer F shown in Fig. 16.

[0067] The first equalizer A includes a first channel estimation block L, a three-symbol delay unit 151, and a second complex divider 156. The first channel estimation block L includes a first complex divider 152, an SP signal generator 153, a time direction linear interpolation circuit 154, and a frequency direction interpolation circuit 155.

[0068] The SP signal generator 153 generates a known SP signal. The first complex divider 152 complex-divides a scattered pilot signal SPn,k of received signal Yn,1 subjected to FFT by an output of the SP signal generator 153. The time direction linear interpolation circuit 154 interpolates an output of the first complex divider 152 in time direction. The frequency direction interpolation circuit 155 interpolates an output of the time direction linear interpolation circuit 154 in frequency direction so as to calculate a channel characteristic Hn,1. The second complex divider 156 complex-divides the received signal Yn,1 by the channel characteristic Hn,1 and thus outputs a mapping vector Xn,1.

[0069] The second equalizer B includes a hard decision block 157 and a second channel estimation block M. The hard decision block 157 is configured so as to include a hard decision unit 157a, a reliability detection block 157b, and a mapping vector generator 157c. The hard decision unit 157a hard-decides an output Xn,1 of the first equalizer A. The reliability detection block 157b detects reliability of result of hard decision. The mapping vector generator 157c calculates a mapping vector X'n,1 on a basis of result of decision of the hard decision unit 157a.

[0070] The second channel estimation block M is configured so as to include a third complex divider 158, a selection circuit 159 and a frequency direction filter 160. The third complex divider 158 complex-divides the received signal Yn, 1 by the mapping vector X'n,1. The selection circuit 159 selects an output H'n,1 of the third complex divider 158 or the channel characteristic Hn,1 depending on an output of the reliability estimation block 157b. The frequency direction filter 160 filters an output of the selection circuit 159 and thus outputs a secondary channel characteristic H"n,1.

[0071] The third equalizer F includes one-symbol delay units 161 and 162 serving as cascade delay units, a time direction filter 163, an one-symbol delay unit 164, and a fourth complex divider 165. The cascade symbol delay units delay a channel characteristic H"n,1 obtained by the second equalizer B by one symbol and two symbols, respectively. The time direction filter 163 interpolates outputs H"n-2,1 and H"n-1,1 of the cascade symbol delay units and a channel characteristic H"n,1 not subjected to symbol delay in time direction and thus outputs a tertiary channel characteristic H"'n-1,1. The one-symbol delay unit 164 delays the received signal Yn,1 supplied from the first equalizer A by one symbol. The fourth complex divider 165 complex-divides a signal Yn-1,1 which is obtained by delaying a received signal by one symbol by an output H"'n-1,1 of the time direction filter 163.

[0072] In accordance with the present embodiment, the one-symbol delay units 161 and 162 delay the channel characteristic outputted from the frequency direction filter 160 in the second equalizer B by one symbol, respectively. Then, the time direction filter 163 calculates a channel characteristic at a symbol position again from channel characteristics of prior and subsequent symbols at the same carrier position and the channel characteristic at corresponding symbol position. In accordance with the present embodiment, a channel characteristic is calculated by using the following formula (4):

$$H(n-1,k) = [H(n-2,k) + 2H(n-1,k) + H(n,k)]/4 \quad (4).$$

[0073] A signal subjected to FFT is delayed by one symbol at the one-symbol delay unit 164 in order to make such process correspond to a delay time.

[0074] As described above, in accordance with the above-described embodiments, received data subjected to demodulation is hard-decided. Then, the received data subjected to FFT is divided by using a mapping vector subjected to hard decision. As a result, a channel characteristic can be newly calculated.

[0075] Further, in accordance with the above-described embodiments, the channel characteristic can be calculated by using all of the received data which are determined as reliable. Thus, as compared to conventional estimation of channel only by a scattered pilot signal, precision in estimation of channel characteristic is significantly improved especially in an environment of receiving a mobile.

[0076] Moreover, in accordance with the above-described embodiments, a threshold which is determined as reliable can be changed for each mapping. For this reason, even in a case of, e.g., single hierarchy of QPSK, it may be considered that a scattered pilot signal, a continual pilot signal, a transmission parameter signal, and an ancillary information signal are scattered in a QPSK signal. Thus, reliability of channel characteristic is higher as compared to a case that only QPSK is provided.

[0077] In Japanese ISDB-T system, signals of QPSK, 16QAM and 64QAM are frequency-interleaved as synchronous signals. In a case of 16QAM, as QPSK is frequency-interleaved. □Thereby at a time of decoding a signal, a pilot signal with high reliability of QPSK is considered to be included. Accordingly, reliability in estimation of channel is improved as compared to a case that only 16QAM is provided.

[0078] Similarly, in a case of 64QAM, pilot signals of 16QAM and QPSK are considered to be included. Accordingly, reliability in estimation of channel is improved as compared to a case that only 64QAM is provided.

[0079] Although the present invention exhibits sufficient effects in a case of single hierarchy, the present invention exhibits effects to improve a performance of 64QAM especially when a frequency interleaving is performed and various mappings exist.

[0080] It is to be understood that although the present invention has been described with regard to preferred embodiments thereof, various other embodiments and variants may occur to those skilled in the art, which are within the scope of the invention, and such other embodiments and variants are intended to be covered by the following claims.

Claims

1. An OFDM demodulation method used for an orthogonal frequency division multiplex (OFDM) transmission system which modulates a plurality of carriers with their frequencies being orthogonal with each other for each symbol period so as to transmit digital information, wherein

in case a symbol number is indicated by n, a residue operation is indicated by mod and an integer number is indicated by p, a scattered pilot signal SPn,k is placed at a carrier position that a carrier number k within a segment satisfies k = 3 * (n mod 4) + 12p for a symbol with symbol number n in OFDM signal for said transmission system;

continual pilot signals, transmission parameter signals and ancillary information signals are placed at specified carrier positions and data signals are placed at other carrier positions; and

said scattered pilot signal and said continual pilot signal are modulated by specified amplitude and phase that are uniquely determined by said carrier number k of said carrier in a transmission band;

said OFDM demodulation method comprises following steps of:

fetching said scattered pilot signal SPn,k from a received signal Yn,1 (wherein 1 is an integer number) subjected to FFT;

estimating a channel characteristic Hn,1 by interpolating said scattered pilot signal in time direction and frequency direction;

reconstituting mapping vectors Xn,1 of transmission parameter signal, ancillary information signal and data signal placed at the respective carrier positions by complex-dividing said received signal Yn,1 by the obtained channel characteristic Hn,1;

calculating a primary mapping vector X'n,1 at each carrier position by hard-deciding said reconstituted mapping vectors Xn,1;

deriving a primary channel characteristic H'n,1;

deriving a secondary channel characteristic H"n,1; and

deriving a final mapping vector by dividing said received signal Yn,1 or a signal derived therefrom, by said last mentioned channel characteristic, thereby decoding said data signal.

2. The method of claim 1, comprising the steps of:

fetching said scattered pilot signal SPn,k from a received signal Yn,1 (wherein 1 is an integer number) subjected to FFT;
estimating a channel characteristic Hn,1 by interpolating said scattered pilot signal in time direction and frequency direction;
reconstituting mapping vectors Xn,1 of transmission parameter signal, ancillary information signal and data signal placed at the respective carrier positions by complex-dividing said received signal Yn,1 by the obtained channel characteristic Hn,1;
calculating a primary mapping vector X'n,1 at each carrier position by hard-deciding said reconstituted mapping vectors Xn,1;
calculating a primary channel characteristic H'n,1 by complex-dividing said received signal Yn,1 by said primary mapping vector X'n,1;
calculating a secondary channel characteristic H"n,1 by filtering said primary channel characteristic H'n,1 in frequency direction; and
calculating a secondary mapping vector X"n,1 by dividing said received signal Yn,1 by said secondary channel characteristic H"n,1, thereby decoding said data signal.

3. The method of claim 1, comprising the steps of:

fetching said scattered pilot signal SPn,k from a received signal Yn,1 (wherein 1 is an integer number) subjected to FFT;
estimating a channel characteristic Hn,1 by interpolating said scattered pilot signal in time direction and frequency direction;
reconstituting mapping vectors Xn,1 of transmission parameter signal, ancillary information signal and data signal placed at the respective carrier positions by complex-dividing said received signal Yn,1 by the obtained channel characteristic Hn,1;
calculating a primary mapping vector X'n,1 at each carrier position by hard-deciding said reconstituted mapping vectors Xn,1;
providing a predetermined threshold for each type of mapping at a time of said hard decision, substituting a primary channel characteristic H'n,1 obtained by using signal points within the predetermined threshold for said channel characteristic Hn,1 at said carrier position, and filtering the resultant channel characteristic H'n, 1 in frequency direction, thereby calculating a secondary channel characteristic H"n,1; and
calculating a secondary mapping vector X"n,1 by dividing said received signal Yn,1 by said H"n,1, thereby decoding said data signal.

4. The method of claim 1, comprising the steps of:

fetching said scattered pilot signal SPn,k from a received signal Yn,1 (wherein 1 is an integer number) subjected to FFT;
estimating a channel characteristic Hn,1 by interpolating said scattered pilot signal in time direction and frequency direction;
reconstituting mapping vectors Xn,1 of transmission parameter signal, ancillary information signal and data signal placed at the respective carrier positions by complex-dividing said received signal Yn,1 by the obtained channel characteristic Hn,1;
calculating a primary mapping vector X'n,1 at each carrier position by hard-deciding said reconstituted mapping vectors Xn,1;
calculating a primary channel characteristic H'n,1 by complex-dividing said received signal Yn,1 by said mapping vector X'n,1;
calculating a secondary channel characteristic H"n,1 by filtering said primary channel characteristic H'n,1 in frequency direction;
reconstituting secondary mapping vectors X"n,1 of a transmission parameter signal, an ancillary information signal and a data signal placed at the respective carriers by dividing said received signal Yn,1 by secondary channel characteristic H"n,1;
calculating a tertiary mapping vector X'"n,1 at each carrier position by hard-deciding said mapping vector X"n,1;
calculating a tertiary channel characteristic H'"n,1 by complex-dividing said received signal Yn,1 by said map-

ping vector X'''n,1;
calculating a quaternary channel characteristic H''''n,1 by filtering said H'''n,1 in frequency direction; and
calculating a quaternary mapping vector X''''n,1 by dividing said received signal Yn,1 by said quaternary channel characteristic H''''n,1, thereby decoding said data signal.

5. The method of claim 1, comprising the steps of:

fetching said scattered pilot signal SPn,k from a received signal Yn,1 (wherein 1 is an integer number) subjected to FFT;
estimating a channel characteristic Hn,1 by interpolating said scattered pilot signal in time direction and frequency direction;
reconstituting mapping vectors Xn,1 of transmission parameter signal, ancillary information signal and data signal placed at the respective carrier positions by complex-dividing said received signal Yn,1 by the obtained channel characteristic Hn,1;
calculating a primary mapping vector X'n,1 at each carrier position by hard-deciding said reconstituted mapping vectors Xn,1;
providing a first predetermined threshold for each type of mapping at a time of said hard decision, substituting a primary channel characteristic H'n,1 obtained by using signal points within the predetermined threshold for said channel characteristic Hn,1 at said carrier position, and filtering said channel characteristic H'n,1 in frequency direction, thereby calculating a secondary channel characteristic H''n,1;
reconstituting secondary mapping vectors X''n,1 of a transmission parameter signal, an ancillary information signal and a data signal placed at the respective carrier positions by dividing said received signal Yn,1 by said channel characteristic H''n,1;
calculating a tertiary mapping vector X'''n,1 at each carrier position by hard-deciding said mapping vectors X''n,1;
providing a second predetermined threshold for each type of mapping at a time of said hard decision, and substituting a tertiary channel characteristic H'''n,1 obtained by using signal points within the predetermined threshold for said channel characteristic H''n,1 at said carrier position;
calculating a quaternary channel characteristic H''''n,1 by filtering said channel characteristic H'''n,1 in frequency direction; and
calculating a quaternary mapping vector X''''n,1 by dividing said received signal Yn,1 by said channel characteristic H''''n,1, thereby decoding said data signal.

6. The OFDM demodulation method according to any of claims 1 to 5, further comprising the following steps of:

obtaining a transmission parameter signal, an ancillary information signal and a data signal placed at the respective carrier positions by utilizing said channel characteristics;
obtaining mapping vectors by hard-deciding the resultant signals; and
repeating obtaining new channel characteristic by utilizing said mapping vectors, thereby decoding said data signal.

7. The method of claim 1, comprising the steps of:

fetching said scattered pilot signal SPn,k from a received signal Yn,1 (wherein 1 is an integer number) subjected to FFT;
estimating a channel characteristic Hn,1 by interpolating said scattered pilot signal in time direction and frequency direction;
reconstituting mapping vectors Xn,1 of transmission parameter signal, ancillary information signal and data signal placed at the respective carrier positions by complex-dividing said received signal Yn,1 by the obtained channel characteristic Hn,1;
calculating a primary mapping vector X'n,1 at each carrier position by hard-deciding said reconstituted mapping vectors Xn,1;
calculating a primary channel characteristic H'n,1 by complex-dividing said received signal Yn,1 by said mapping vector X'n,1;
calculating a secondary channel characteristic H''n,1 by filtering said primary channel characteristic H'n,1 in frequency direction;
extracting a channel characteristic of said scattered pilot signal SPn,k from said secondary channel characteristic H''n,1;

calculating a tertiary channel characteristic H"'n,1 by interpolating said extracted channel characteristic in time direction and frequency direction; and
calculating a mapping vector X"n,1 by dividing said received signal Yn,1 by said tertiary channel characteristic H"'n,1, thereby decoding said data signal.

8. The method of claim 1, comprising the steps of:

fetching said scattered pilot signal SPn,k from a received signal Yn,1 (wherein 1 is an integer number) subjected to FFT;
estimating a channel characteristic Hn,1 by interpolating said scattered pilot signal in time direction and frequency direction;
reconstituting mapping vectors Xn,1 of transmission parameter signal, ancillary information signal and data signal placed at the respective carrier positions by complex-dividing said received signal Yn,1 by the obtained channel characteristic Hn,1;
calculating a primary mapping vector X'n,1 at each carrier position by hard-deciding said reconstituted mapping vectors Xn,1;
calculating a primary channel characteristic H'n,1 by complex-dividing said received signal Yn,1 by said mapping vector X'n,1;
calculating a secondary channel characteristic H"n,1 by filtering said primary channel characteristic H'n,1 in frequency direction;
delaying said secondary channel characteristic H"n,1 by two symbols, and from a channel characteristic H"n-2,1 delayed by two symbols and a channel characteristic H"n,1 without symbol delay, calculating a tertiary channel characteristic H"'n,1 of symbol between such symbols; and
calculating a secondary mapping vector X"n-1,1 by dividing said received signal Yn-1,1 by said tertiary channel characteristic H"'n-1,1, thereby decoding said data signal.

9. The method of claim 1, comprising the steps of:

fetching said scattered pilot signal SPn,k from a received signal Yn,1 (wherein 1 is an integer number) subjected to FFT;
estimating a channel characteristic Hn,1 by interpolating said scattered pilot signal in time direction and frequency direction;
reconstituting mapping vectors Xn,1 of transmission parameter signal, ancillary information signal and data signal placed at the respective carrier positions by complex-dividing said received signal Yn,1 by the obtained channel characteristic Hn,1;
calculating a primary mapping vector X'n,1 at each carrier position by hard-deciding said reconstituted mapping vectors Xn,1;
calculating a primary channel characteristic H'n,1 by complex-dividing said received signal Yn,1 by said mapping vector X'n,1;
calculating a secondary channel characteristic H"n,1 by filtering said primary channel characteristic H'n,1 in frequency direction;
delaying said channel characteristic H"n,1 by one symbol and two symbols;
from said channel characteristic H"n-2,1 delayed by two symbols, said channel characteristic H"n-1,1 delayed by one symbol and a channel characteristic H"n,1 without symbol delay, calculating a tertiary channel characteristic H"'n-1,1 of symbol between such symbols; and
calculating a secondary mapping vector X"n-1,1 by dividing received signal Yn-1,1 obtained by delaying said received signal by one symbol by said H"'n-1,1, thereby decoding said data signal.

10. An OFDM demodulator for an orthogonal frequency division multiplex (OFDM) transmission system which modulates a plurality of carriers with their frequencies being orthogonal with each other for each symbol period so as to transmit digital information, wherein

when a symbol number is indicated by n, a residue operation is indicated by mod and an integer number is indicated by p, a scattered pilot signal SPn,k is placed at a carrier position that a carrier number k within a segment satisfies k = 3 * (n mod 4) + 12p for a symbol with symbol number n in an OFDM signal for said transmission system;
continual pilot signals, transmission parameter signals and ancillary information signals are placed at specified carrier positions and data signals are placed at other carrier positions; and

said scattered pilot signal and said continual pilot signal are modulated by specified amplitude and phase that are uniquely determined by the carrier number k of said carrier in a transmission band;
said OFDM demodulator comprises:

a first equalizer which equalizes a received OFDM signal Yn,1 (wherein 1 indicates an integer number) by using said scattered pilot signal SPn,k, and which calculates a channel characteristic Hn,1 and mapping vectors Xn,1 of signals placed at the respective carriers; and
a second equalizer which hard-decides the mapping vector Xn,1 obtained by said first equalizer A, which derives a primary channel characteristic H'n,1, which derives a secondary channel characteristic H"n,1, which re-equalizes said received signal Yn,1 by using said last mentioned channel characteristic, and which derives a final mapping vector.

11. The demodulator of claim 10 comprising:

a first equalizer which equalizes a received OFDM signal Yn,1 (wherein 1 indicates an integer number) by using said scattered pilot signal SPn,k, and which calculates a channel characteristic Hn,1 and mapping vectors Xn,1 of signals placed at the respective carriers; and
a second equalizer which hard-decides the mapping vector Xn,1 obtained by said first equalizer A, which calculates a primary channel characteristic H'n,1 by using a primary mapping vector X'n,1 obtained by said hard decision and said received signal Yn,1, which calculates a secondary channel characteristic H"n,1 by filtering said primary channel characteristic H'n,1 in frequency direction, which re-equalizes said received signal Yn,1 by using said secondary channel characteristic H"n,1, and which calculates a secondary mapping vector X"n,1.

12. The demodulator of claim 11, wherein said first equalizer comprises:

a first channel estimation block which has an SP signal generator which generates a known SP signal, a first complex divider which complex-divides said scattered pilot signal SPn,k of received signal Yn,1 subjected to FFT by an output of said SP signal generator, a time direction interpolation block and a frequency direction interpolation block that interpolate an output of said first complex divider in time direction and frequency direction, respectively, so as to calculate a channel characteristic Hn,1; and
a second complex divider which complex-divides said received signal Yn,1 by said channel characteristic Hn, 1 so as to output a mapping vector Xn,1, and
said second equalizer comprises:

a hard decision block which has a hard decision unit which hard-decides the output Xn,1 of said first equalizer, a mapping vector generator which calculates a mapping vector X'n,1 on the basis of decision result of said hard decision unit, and a reliability detection block which detects reliability of result of hard decision;
a second channel estimation block which has a third complex divider which complex-divides said received signal Yn,1 by said mapping vector X'n,1, a selection circuit which selects one of an output H'n,1 of said third complex divider and said channel characteristic Hn,1 depending on an output of said reliability detection block, and a frequency direction filter which filters an output of said selection circuit; and
a fourth complex divider which complex-divides said received signal Yn,1 by said secondary channel characteristic H"n,1 outputted from said frequency direction filter so as to calculate a secondary mapping vector X"n,1.

13. The demodulator of claim 11, wherein said reliability detection block applies a predetermined threshold to each type of mapping and determines whether or not the mapping vector Xn,1 is within a predetermined threshold; and
said selection circuit selects said primary channel characteristic H'n,1 in case said the mapping vector is within the predetermined threshold.

14. The demodulator of claim 10, comprising:

a first equalizer which equalizes a received OFDM signal Yn,1 (wherein 1 indicates an integer number) by using said scattered pilot signal SPn,k, and which calculates a channel characteristic Hn,1 and mapping vectors Xn,1 of signals placed at the respective carriers;
a second equalizer which hard-decides the mapping vector Xn,1 obtained by said first equalizer A, which

calculates a primary channel characteristic H'n,1 by using a primary mapping vector X'n,1 obtained by said hard decision and said received signal Yn,1, which calculates a secondary channel characteristic H"n,1 by filtering said primary channel characteristic H'n,1 in frequency direction, which re-equalizes said received signal Yn,1 by using said secondary channel characteristic H"n,1, and which calculates a secondary mapping vector X"n,1; and

a third equalizer which hard-decides a mapping vector X"n,1 obtained at said second equalizer, which calculates a tertiary channel characteristic H"'n,1 by using a tertiary mapping vector X"'n,1 obtained by hard decision and said received signal Yn,1, which calculates a quaternary channel characteristic H""n,1 by filtering said channel characteristic H"'n,1 in frequency direction, which re-equalizes said received signal Yn,1 by using said channel characteristic H""n,1, and which calculates a quaternary mapping vector X""n,1.

15. The demodulator of claim 14, wherein said first equalizer comprises:

a first channel estimation block which has an SP signal generator which generates a known SP signal, a first complex divider which complex-divides said scattered pilot signal SPn,k of received signal Yn,1 subjected to FFT by an output of said SP signal generator, a time direction interpolation block and a frequency direction interpolation block that interpolate an output of said first complex divider in time direction and frequency direction, respectively, so as to calculate a channel characteristic Hn,1; and

a second complex divider which complex-divides said received signal Yn,1 by said channel characteristic Hn, 1 so as to output a mapping vector Xn,1,

said second equalizer comprises:

a hard decision block which has a first hard decision unit which hard-decides an output Xn,1 of said first equalizer, a first mapping vector generator which calculates a mapping vector X'n,1 of the output of said first hard decision unit, and a first reliability detection block which detects reliability result of said first hard decision unit;

a second channel estimation block which has a third complex divider which complex-divides said received signal Yn,1 by said mapping vector X'n,1, a first selection circuit which selects an output H'n,1 of said third complex divider and said channel characteristic Hn,1 depending on an output of said reliability detection block, and a first frequency direction filter which filters an output of said first selection circuit; and

a fourth complex divider which calculates a secondary mapping vector X"n,1 by complex-dividing said received signal Yn,1 by said secondary channel characteristic H"n,1 outputted from said frequency direction first filter; and

said third equalizer comprises:

a second hard decision block which has a second hard decision unit which hard-decides an output X"n,1 of said second equalizer, a second mapping vector generator which calculates a mapping vector X"'n,1 of an output of said second hard decision unit, and a second reliability detection block which detects reliability of result of hard decision;

a third channel estimation block which has a fifth complex divider which complex-divides said received signal Yn,1 by said mapping vector X"'n,1, a second selection circuit which selects one of an output H"'n,1 of said fifth complex divider and said channel characteristic H"n,1 depending on an output of said second reliability detection block, and a second frequency direction filter which filters an output of said second selection circuit; and

a sixth complex divider which calculates a quaternary mapping vector X""n,1 by complex-dividing said received signal Yn,1 by an output H""n,1 of said second frequency direction filter.

16. The demodulator of claim 15, wherein said second reliability detection block applies a predetermined threshold to each type of mapping and determines whether or not a mapping vector is within a predetermined threshold, and

said second selection circuit selects H'n,1 or H"'n,1 in case mapping vector X"n,1 is within the predetermined threshold.

17. The demodulator of any one of the claims 11 to 16, wherein a plurality of equalizers are provided such that a transmission parameter signal, an ancillary information signal and a data signal that are placed at the respective carrier positions are obtained by utilizing said channel characteristic, the resultant signals are hard-decided so as to obtain mapping vectors, a new channel characteristic is obtained by using said mapping vectors and such process is repeated, and thereby said data signal is decoded.

18. The demodulator of claim 10, comprising:

a first equalizer which equalizes a received OFDM signal Yn,1 (wherein 1 indicates an integer number) by using said scattered pilot signal SPn,k, and which calculates a channel characteristic Hn,1 and mapping vectors Xn,1 of signals placed at the respective carriers;
a second equalizer which hard-decides the mapping vector Xn,1 obtained by said first equalizer A, which calculates a primary channel characteristic H'n,1 by using a primary mapping vector X'n,1 obtained by said hard decision and said received signal Yn,1, and which calculates a secondary channel characteristic H"n,1 by filtering said primary channel characteristic H'n,1 in frequency direction; and
a third equalizer which extracts a channel characteristic for said scattered pilot signal SPn,k from the channel characteristic H"n,1 obtained at said second equalizer, which interpolates said extracted channel characteristic in time and frequency directions, thereby calculating a tertiary channel characteristic H'"n,1, and which divides said received signal Yn,1 by said tertiary channel characteristic H'"n,1, thereby calculating a mapping vector X"n,1.

19. The OFDM demodulator according to claim 18, wherein said first equalizer comprises:

a first channel estimation block which has an SP signal generator which generates a known SP signal, a first complex divider which complex-divides said scattered pilot signal SPn,k of received signal Yn,1 subjected to FFT by an output of said SP signal generator, a time direction interpolation block and a frequency direction interpolation block that interpolate an output of said first complex divider in time direction and frequency direction, respectively, so as to calculate a channel characteristic Hn,1; and
a second complex divider which complex-divides said received signal Yn,1 by said channel characteristic Hn, 1 so as to output a mapping vector Xn,1, and
said second equalizer comprises:

a hard decision block which has a hard decision unit which hard-decides the output Xn,1 of said first equalizer, a mapping vector generator which calculates a mapping vector X'n,1 on the basis of decision result of said hard decision unit, and a reliability detection block which detects reliability of result of hard decision;
a second channel estimation block which has a third complex divider which complex-divides said received signal Yn,1 by said mapping vector X'n,1, a selection circuit which selects one of an output H'n,1 of said third complex divider and said channel characteristic Hn,1 depending on an output of said reliability detection block, and a frequency direction filter which filters an output of said selection circuit and outputs a secondary channel charistic H"n,1; and
said third equalizer comprises:

an SP extraction unit which extracts an SP signal at a position of scattered pilot signal SPn,k by using the channel characteristic H"n,1 obtained by said second equalizer;
interpolation blocks in time and frequency directions which interpolate an output of said SP signal extraction unit in time and frequency directions so as to calculate a tertiary channel characteristic H'"n,1; and
a fourth complex divider which complex-divides said received signal Yn,1 by said channel characteristic H'"n,1.

20. The demodulator of claim 10, comprising:

a first equalizer which equalizes a received OFDM signal Yn,1 (wherein 1 indicates an integer number) by using said scattered pilot signal SPn,k, and which calculates a channel characteristic Hn,1 and mapping vectors Xn,1 of signals placed at the respective carriers;
a second equalizer which hard-decides the mapping vector Xn,1 obtained by said first equalizer A, which calculates a primary channel characteristic H'n,1 by using a primary mapping vector X'n,1 obtained by said hard decision and said received signal Yn,1, which calculates a secondary channel characteristic H"n,1 by filtering said primary channel characteristic H'n,1 in frequency direction, so as to output a secondary channel characteristic H"n,1; and
a third equalizer which delays the channel characteristic H"n,1 obtained at said second equalizer by two symbols, which, from a channel characteristic H'"n-2,1 delayed by two symbols and the channel characteristic H'"n,1 without symbol delay, calculates a quaternary channel characteristic H""n-1,1 for symbol between such

symbols, and which divides said received signal Yn-1,1 by said channel characteristic H""n-1,1, thereby calculating a secondary mapping vector X"n-1,1.

21. The OFDM demodulator of claim 20, wherein said first equalizer comprises:

a first channel estimation block which has an SP signal generator which generates a known SP signal, a first complex divider which complex-divides said scattered pilot signal SPn,k of received signal Yn,1 subjected to FFT by an output of said SP signal generator, a time direction interpolation block and a frequency direction interpolation block that interpolate an output of said first complex divider in time direction and frequency direction, respectively, so as to calculate a channel characteristic Hn,1; and
a second complex divider which complex-divides said received signal Yn,1 by said channel characteristic Hn, 1 so as to output a mapping vector Xn,1;
said second equalizer comprises:

a hard decision block which has a hard decision unit which hard-decides an output Xn,1 of said first equalizer, a mapping vector generator which calculates a mapping vector X'n,1 based on an output of said hard decision unit, and a reliability detection block which detects reliability result of hard decision; and
a second channel estimation block which has a third complex divider which complex-divides said received signal Yn,1 by said mapping vector X'n,1, a selection circuit which selects one of an output H'n,1 of said third complex divider and said channel characteristic Hn,1 depending on an output of said reliability detection block, and a frequency direction filter which filters an output of said selection circuit so as to output a secondary channel characteristic H"n,1; and
said third equalizer comprises:

a two-symbol delay unit which delays the channel characteristic H"n,1 obtained by said second equalizer by two symbols;
a time direction filter block which interpolates in time direction an output H"n-2,1 of said two-symbol delay unit and the channel characteristic H"n,1 without symbol delay so as to obtain a tertiary channel characteristic H'"n-1,1; and
a fourth complex divider which complex-divides a signal Yn-1,1 which is obtained by delaying said received signal by one symbol by an output H'"n,1 of said time direction filter block.

22. The demodulator of claim 10, comprising:

a first equalizer which equalizes a received OFDM signal Yn,1 (wherein 1 indicates an integer number) by using said scattered pilot signal SPn,k, and which calculates a channel characteristic Hn,1 and mapping vectors Xn,1 of signals placed at the respective carriers;
a second equalizer which hard-decides the mapping vector Xn,1 obtained by said first equalizer A, which calculates a primary channel characteristic H'n,1 by using a primary mapping vector X'n,1 obtained by said hard decision and said received signal Yn,1, which calculates a secondary channel characteristic H"n,1 by filtering said primary channel characteristic H'n,1 in frequency direction; and
a third equalizer which delays said channel characteristic H"n,1 obtained by said second equalizer by one symbol and two symbols respectively, which, from a channel characteristic H"n-1,1 delayed by one symbol, a channel characteristic H"n-2,1 delayed by two symbols and said channel characteristic H"n,1 without symbol delay, calculates a H'"n-1,1 for symbol between such symbols, and which divides Yn-1,1 obtained by delaying said received signal by one symbol by a tertiary channel characteristic H'"n-1,1, thereby calculating a secondary mapping vector X"n-1,1.

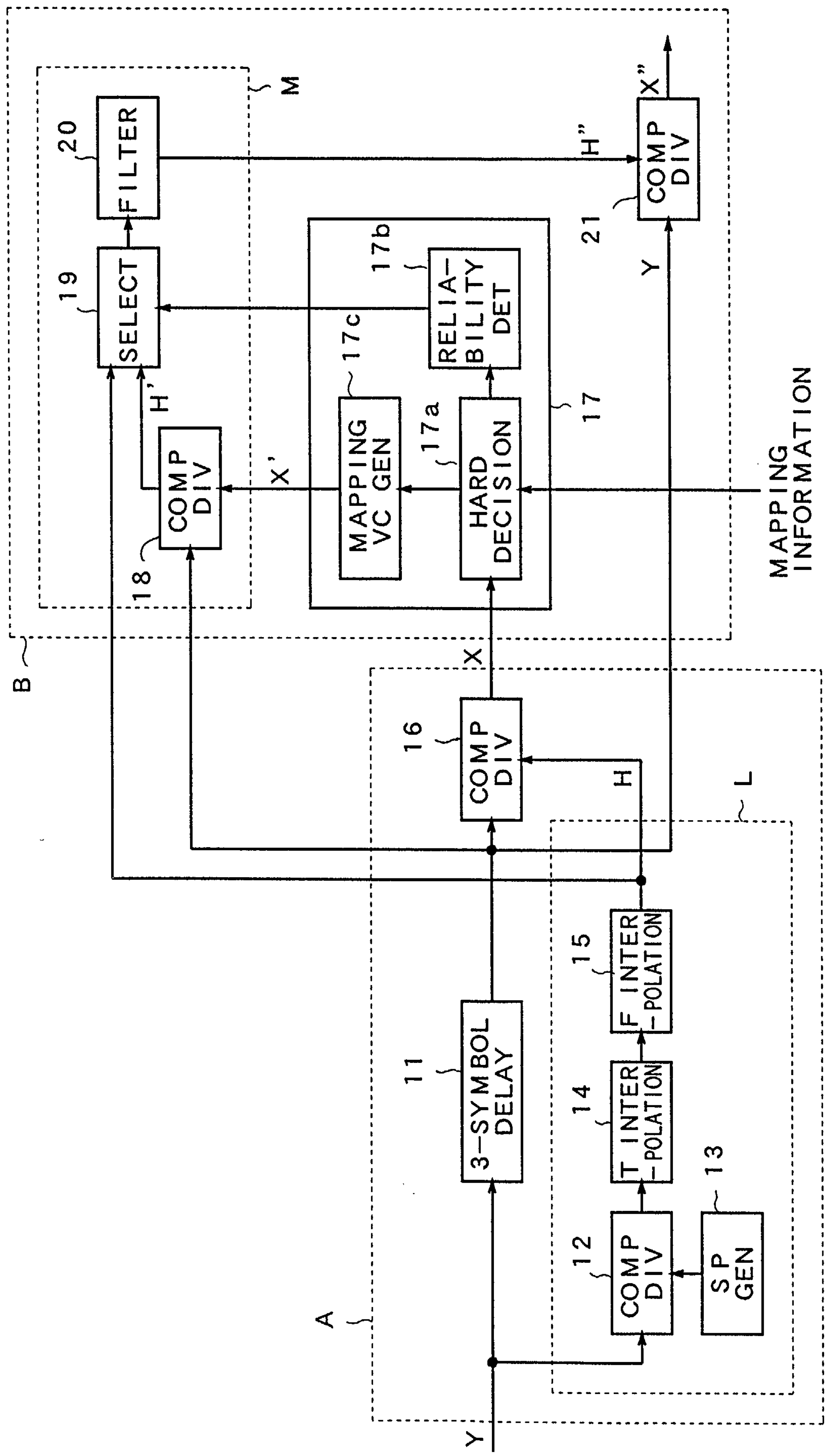
23. The demodulator of claim 22, wherein said first equalizer comprises:

a first channel estimation block which has an SP signal generator which generates a known SP signal, a first complex divider which complex-divides said scattered pilot signal SPn,k of received signal Yn,1 subjected to FFT by an output of said SP signal generator, a time direction interpolation block and a frequency direction interpolation block that interpolate an output of said first complex divider in time direction and frequency direction, respectively, so as to calculate a channel characteristic Hn,1; and
a second complex divider which complex-divides said received signal Yn,1 by said channel characteristic Hn, 1 so as to output a mapping vector Xn,1;
said second equalizer comprises:

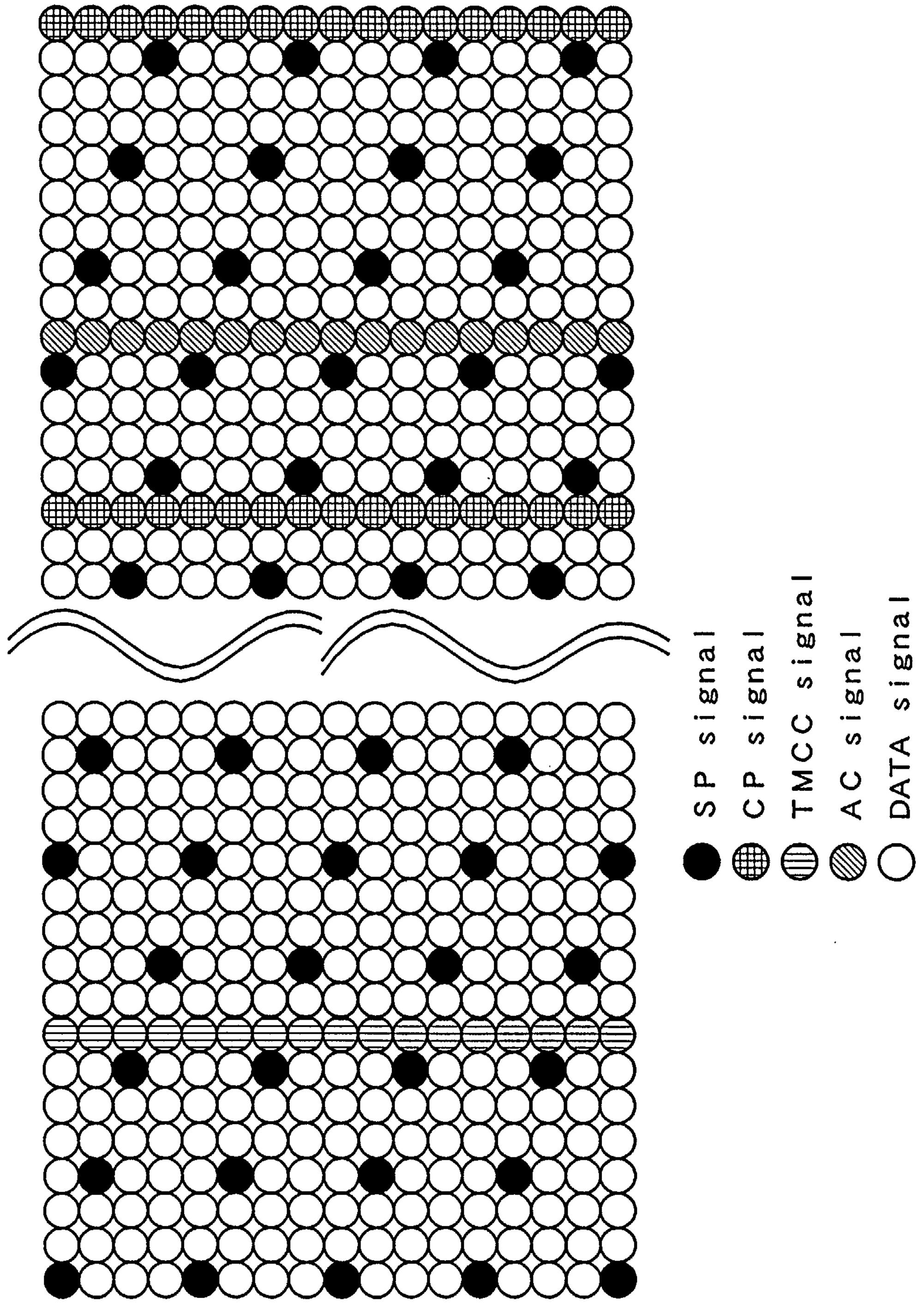
a hard decision block which has a hard decision unit which hard-decides an output Xn,1 of said first equalizer, a mapping vector generator which calculates a mapping vector X'n,1 based on an output of said hard decision unit, and a reliability detection block which detects reliability result of hard decision; and
a second channel estimation block which has a third complex divider which complex-divides said received signal Yn,1 by said mapping vector X'n,1, a selection circuit which selects one of an output H'n,1 of said third complex divider and said channel characteristic Hn,1 depending on an output of said reliability detection block, and a frequency direction filter which filters an output of said selection circuit so as to output a secondary channel characteristic H"n,1; and
said third equalizer comprises:

cascade symbol delay units which delay said secondary channel characteristic H"n,1 obtained by said second equalizer by one symbol and two symbols, respectively;
a time direction filter block which interpolates in time direction said channel characteristic H"n-2,1 and H"n-1,1 of said cascade symbol delay units and said channel characteristic H"n,1 without symbols delay so as to obtain a tertiary channel characteristic H"'n-1,1; and
a fourth complex divider which complex-divides a signal Yn-1,1 obtained by delaying said received signal by one symbol by said tertiary channel characteristic H"'n-1,1 outputted from of said time direction filter block.

FIG. 1


Y
A
11
3-SYMBOL DELAY
12
COMP DIV
13
SP GEN
14
T INTER-POLATION
15
F INTER-POLATION
L
H
16
COMP DIV
X
B
17
17a
HARD DECISION
17b
RELIA-BILITY DET
17c
MAPPING VC GEN
MAPPING INFORMATION
X'
18
COMP DIV
H'
19
SELECT
20
FILTER
M
H"
21
COMP DIV
Y
X"

F I G. 2



F I G. 3

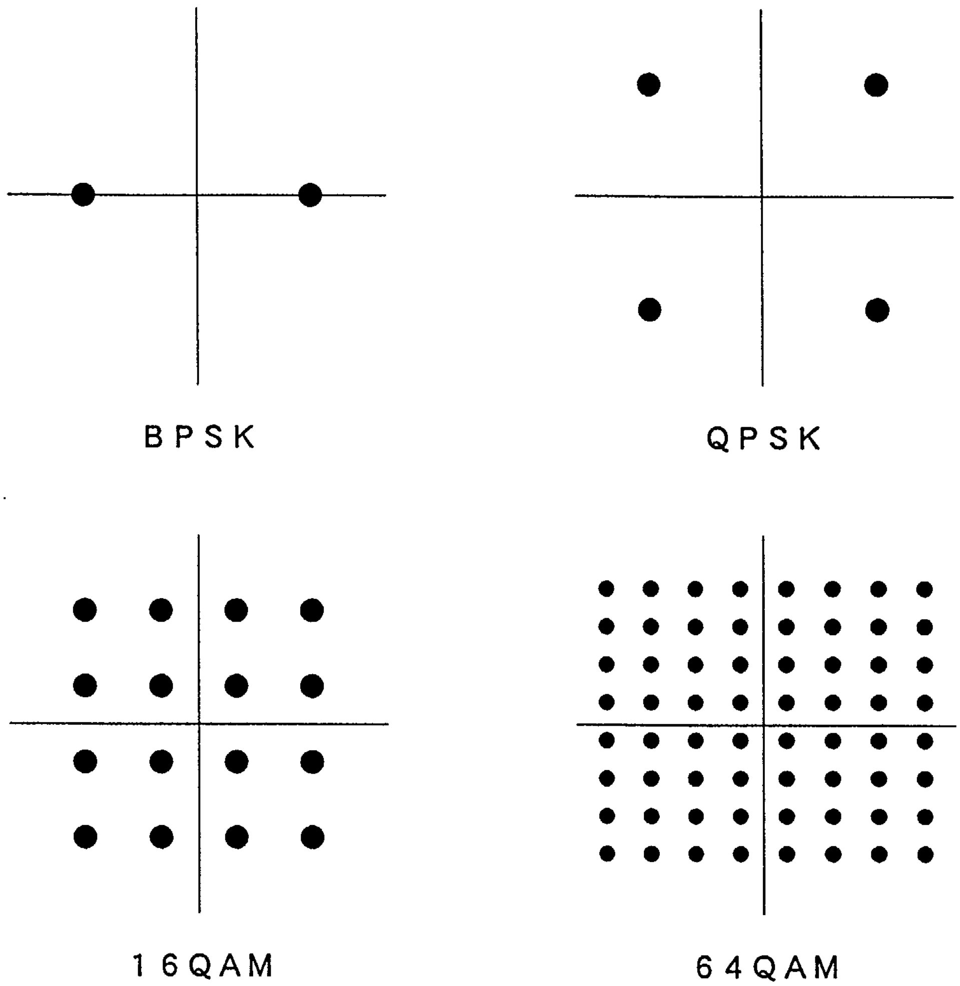


FIG. 4

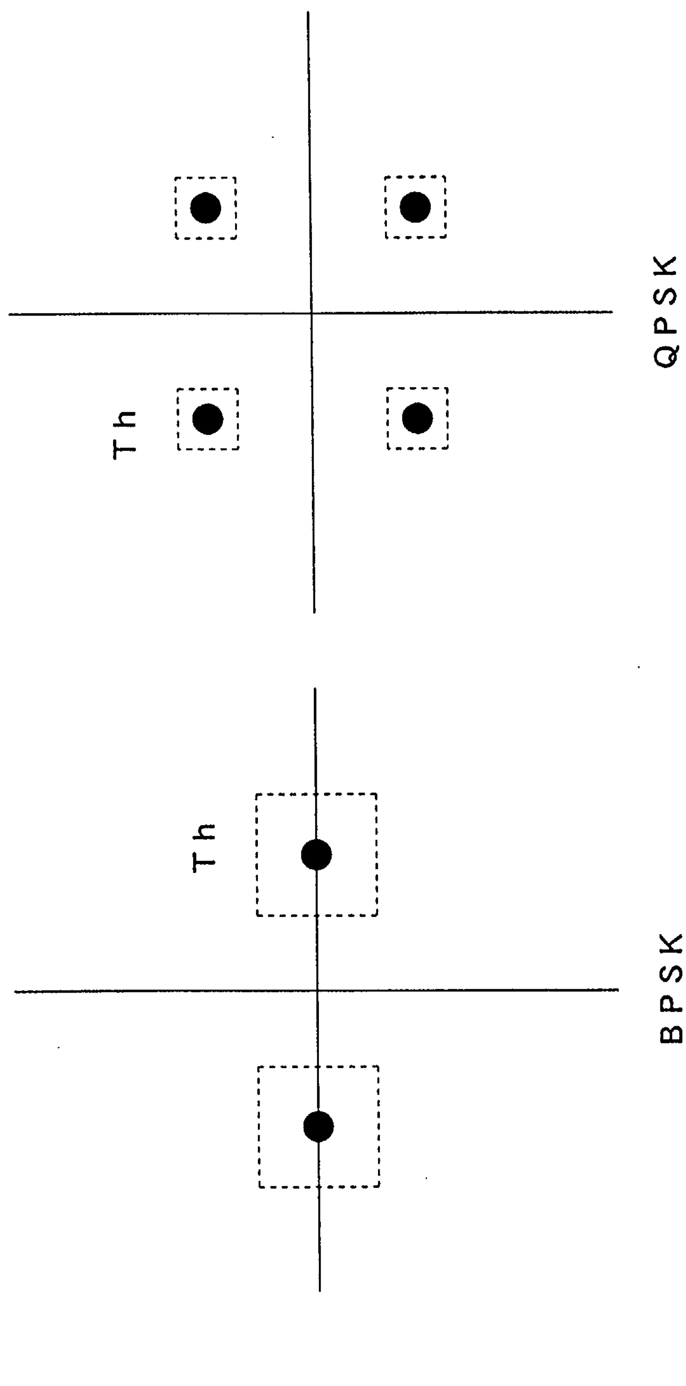
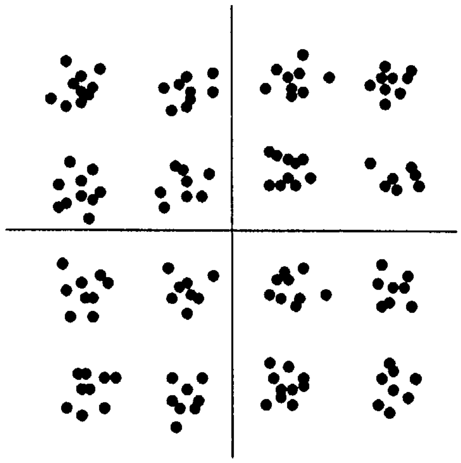
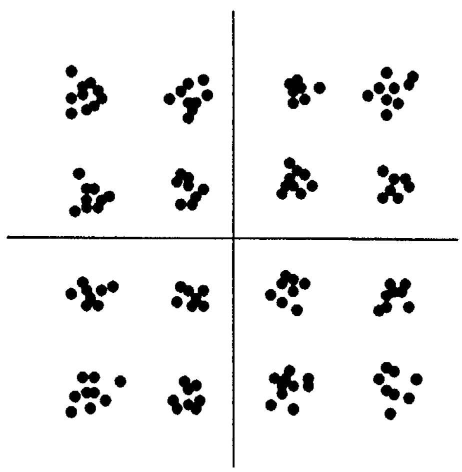


FIG. 5A



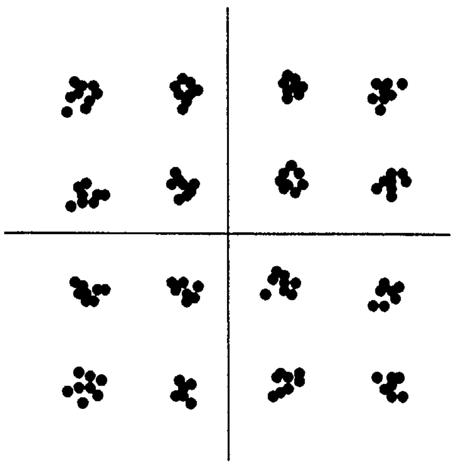
CONVENTIONAL
DECODING
METHOD

FIG. 5B



DECODING
METHOD OF
PRESENT INVENTION
(ONE PROCESS)

FIG. 5C



DECODING
METHOD OF
PRESENT INVENTION
(TWO PROCESS)

FIG. 6

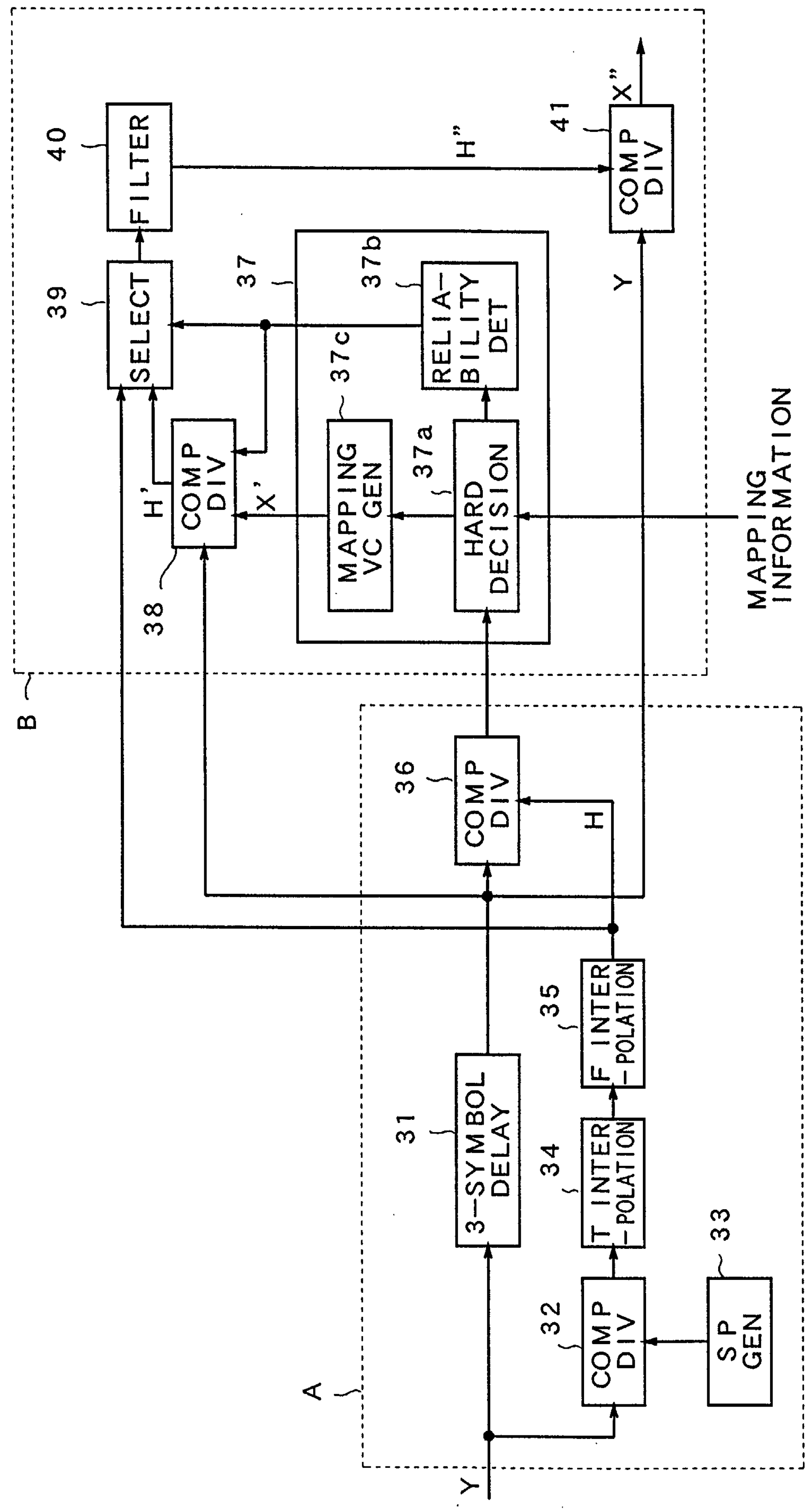
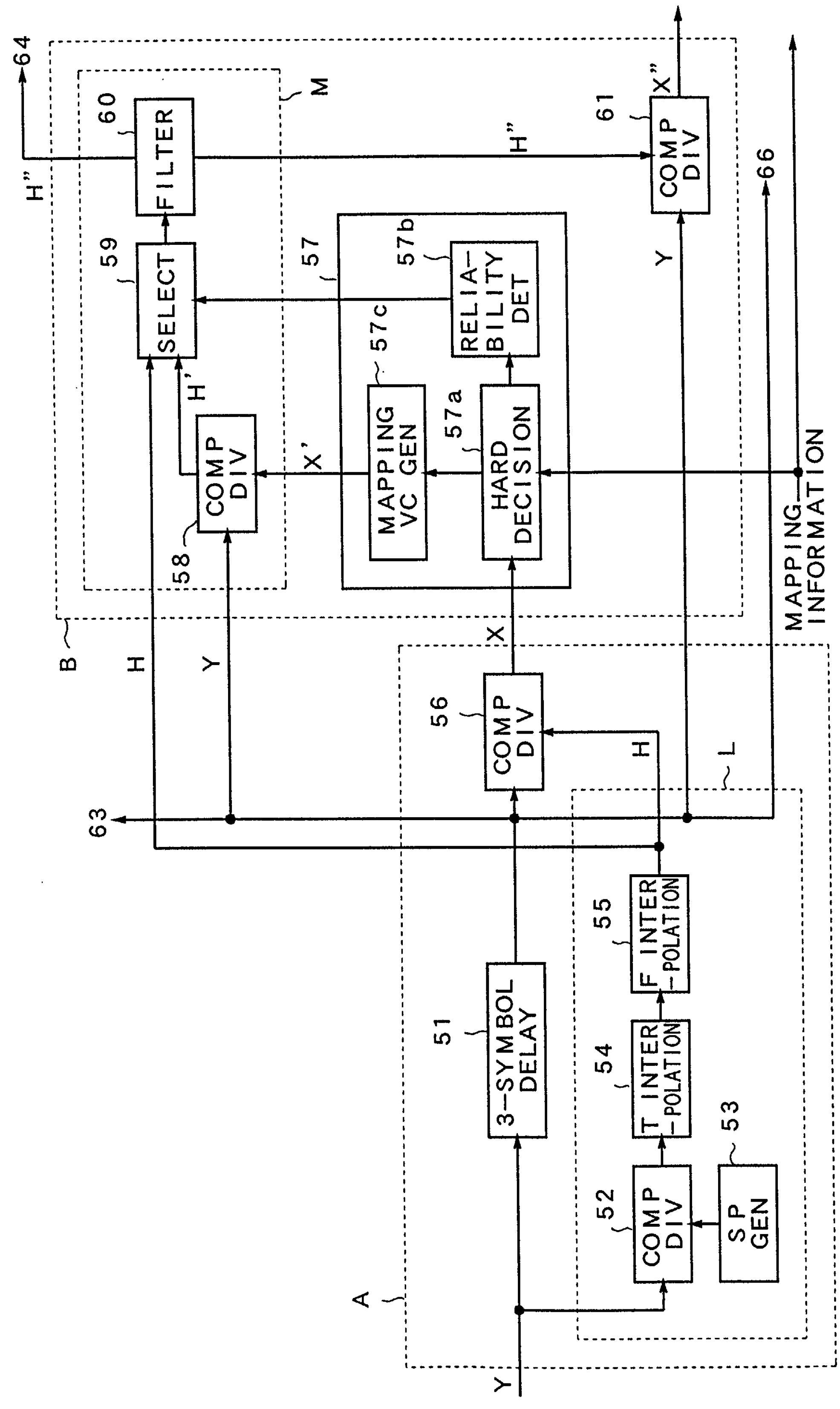

B
A
Y
3-SYMBOL DELAY
31
COMP DIV
32
SP GEN
33
T INTER-POLATION
34
F INTER-POLATION
35
COMP DIV
36
H
37
HARD DECISION
37a
RELIA-BILITY DET
37b
MAPPING VC GEN
37c
MAPPING INFORMATION
COMP DIV
38
X'
H'
SELECT
39
FILTER
40
H"
COMP DIV
41
Y
X"

FIG. 7


Y
A
3-SYMBOL DELAY
51
COMP DIV
52
SP GEN
53
T INTER-POLATION
54
F INTER-POLATION
55
L
H
COMP DIV
56
X
63
B
H
Y
COMP DIV
58
X'
H'
SELECT
59
FILTER
60
H''
64
M
57
MAPPING VC GEN
57c
HARD DECISION
57a
RELIA-BILITY DET
57b
H''
COMP DIV
61
X''
Y
66
MAPPING INFORMATION

F I G. 8

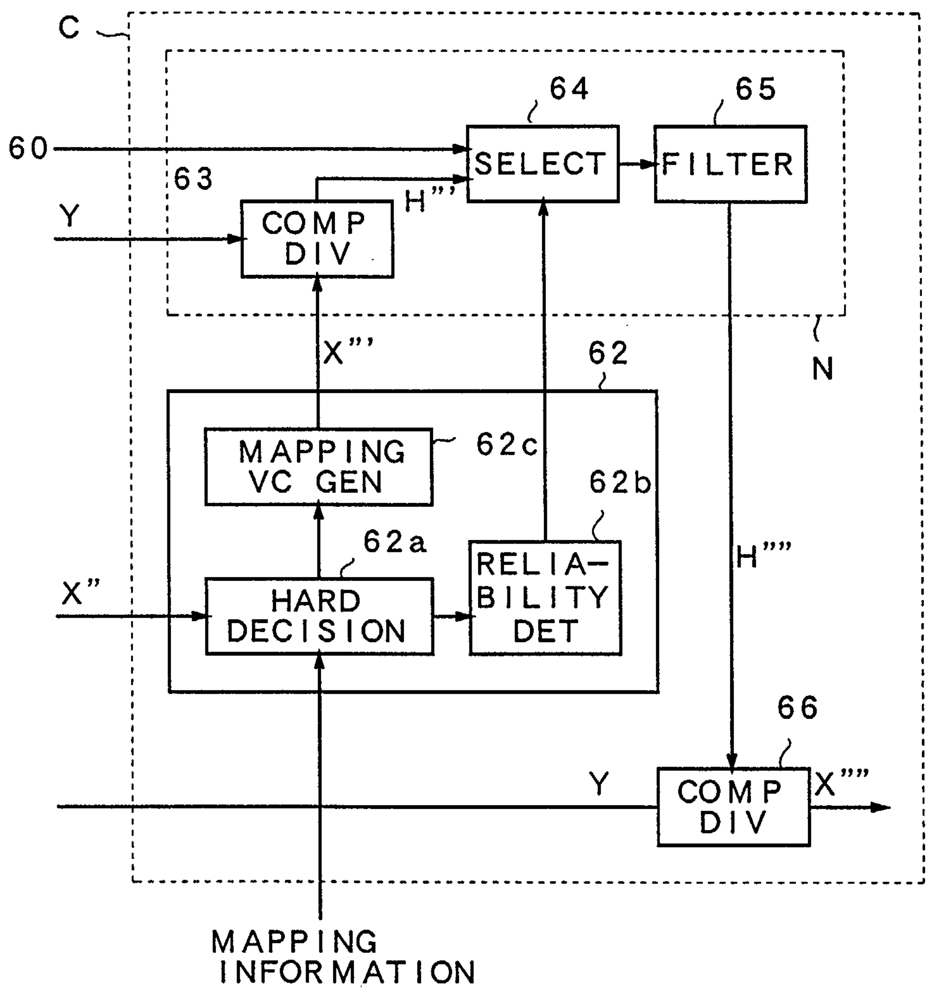
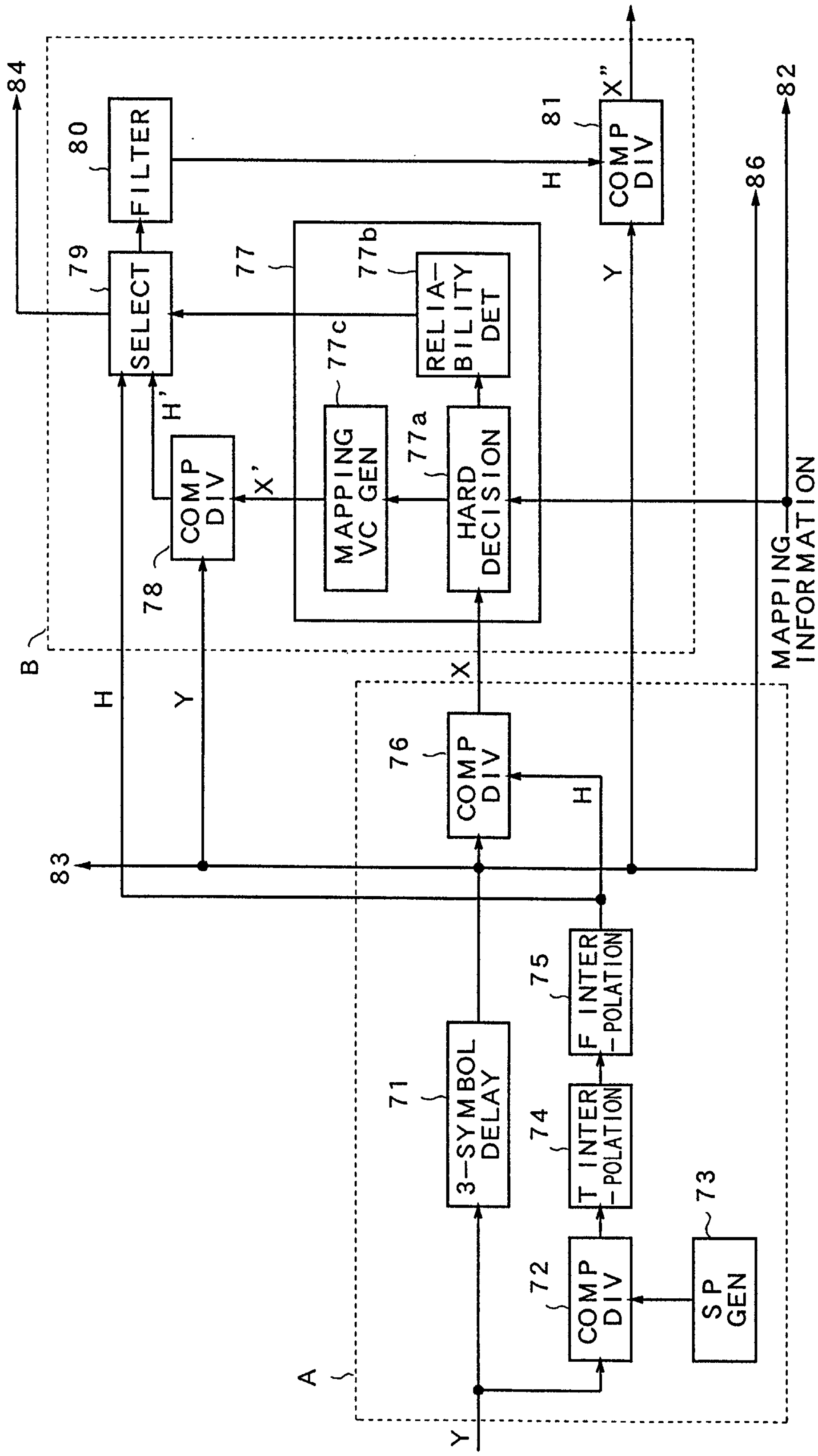

C
64
65
60
SELECT
FILTER
63
H"'
Y
COMP DIV
X"'
62
N
MAPPING VC GEN
62c
62b
62a
H""
X"
HARD DECISION
RELIA-BILITY DET
66
Y
COMP DIV
X""
MAPPING INFORMATION

FIG. 9


Y
A
71
3-SYMBOL DELAY
72
COMP DIV
73
SP GEN
74
T INTER -POLATION
75
F INTER -POLATION
76
COMP DIV
H
X
83
B
H
Y
77
77a
HARD DECISION
77b
RELIA-BILITY DET
77c
MAPPING VC GEN
78
COMP DIV
X'
H'
79
SELECT
84
80
FILTER
81
COMP DIV
H
Y
X"
86
82
MAPPING INFORMATION

F I G. 1 0

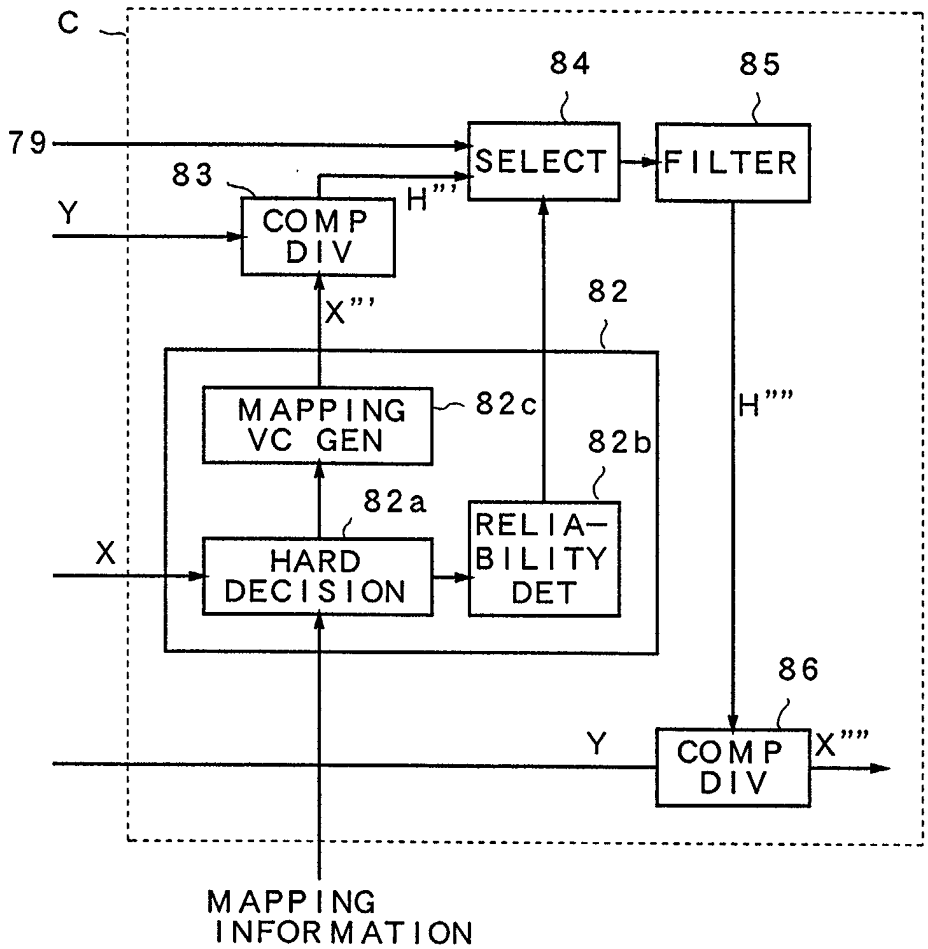
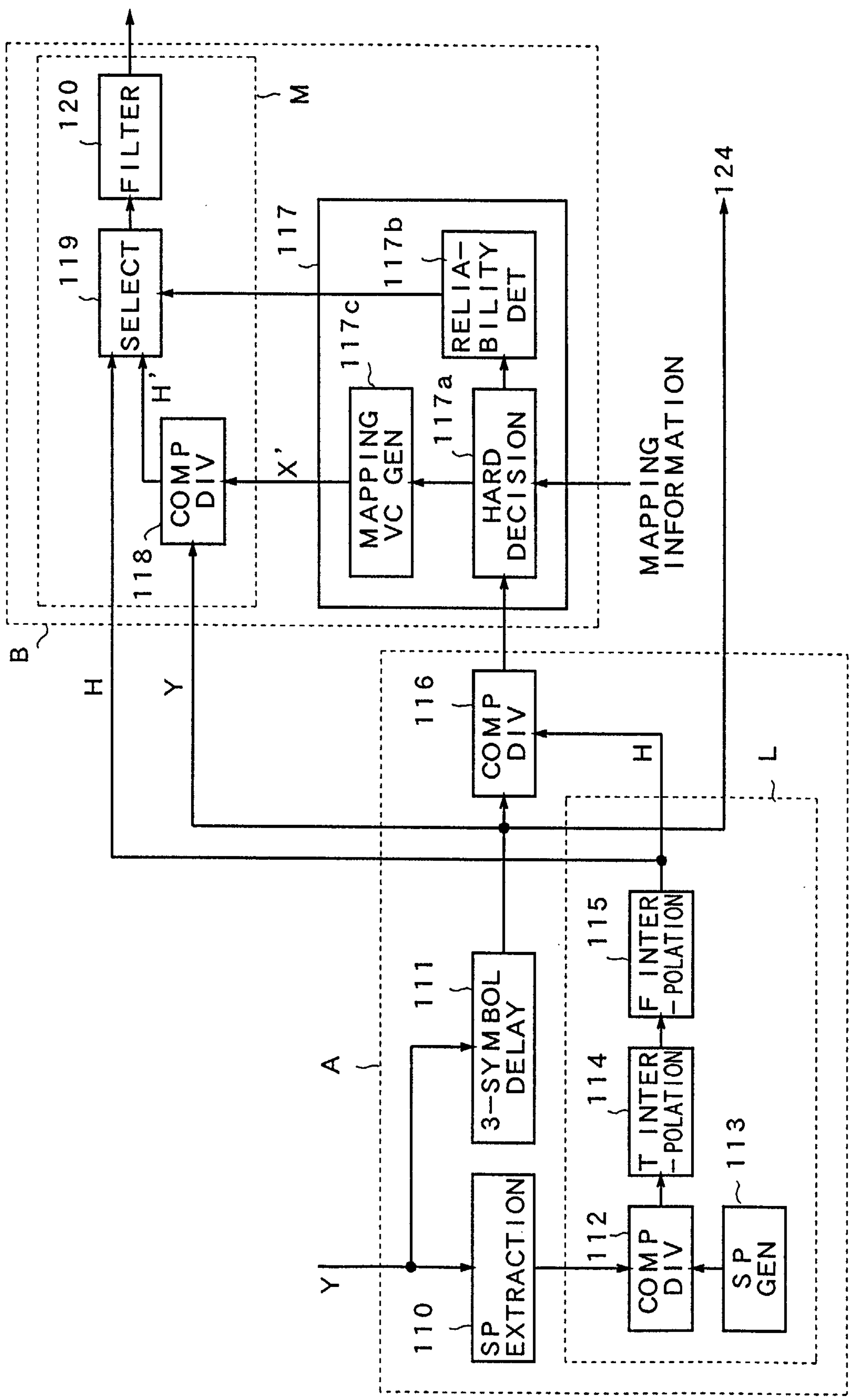

C
84
85
79
SELECT
FILTER
83
H"'
Y
COMP
DIV
X"'
82
H""
MAPPING
VC GEN
82c
82b
82a
RELIA-
BILITY
DET
X
HARD
DECISION
86
Y
COMP
DIV
X""
MAPPING
INFORMATION

FIG. 11



Y
110
SP EXTRACTION
111
3-SYMBOL DELAY
A
112
COMP DIV
113
SP GEN
114
T INTER -POLATION
115
F INTER -POLATION
L
116
COMP DIV
H
Y
H
124
B
117
117a
HARD DECISION
117b
RELIA-BILITY DET
117c
MAPPING VC GEN
MAPPING INFORMATION
X'
118
COMP DIV
H'
119
SELECT
120
FILTER
M

F I G. 1 2

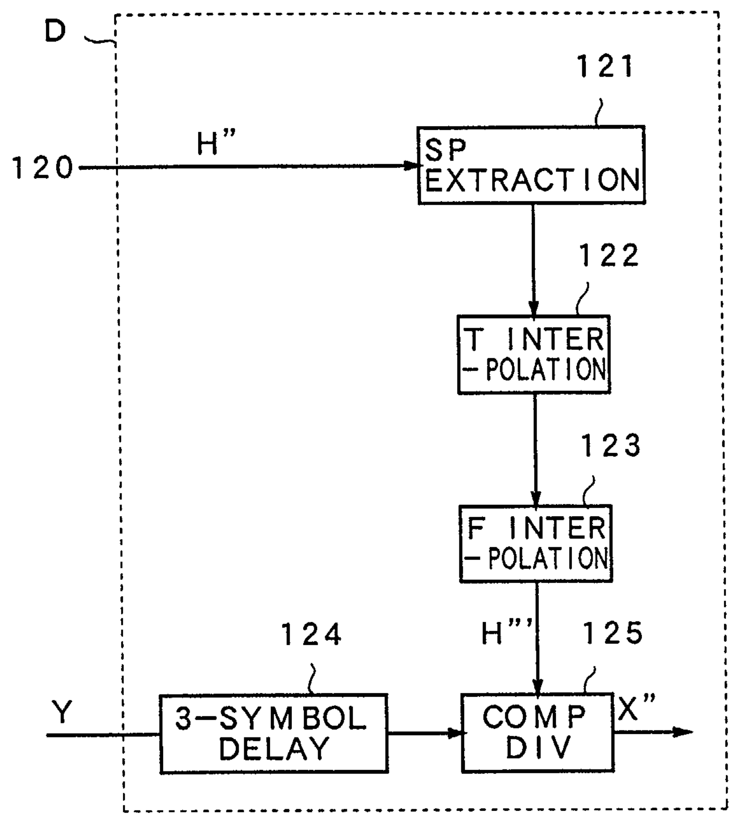
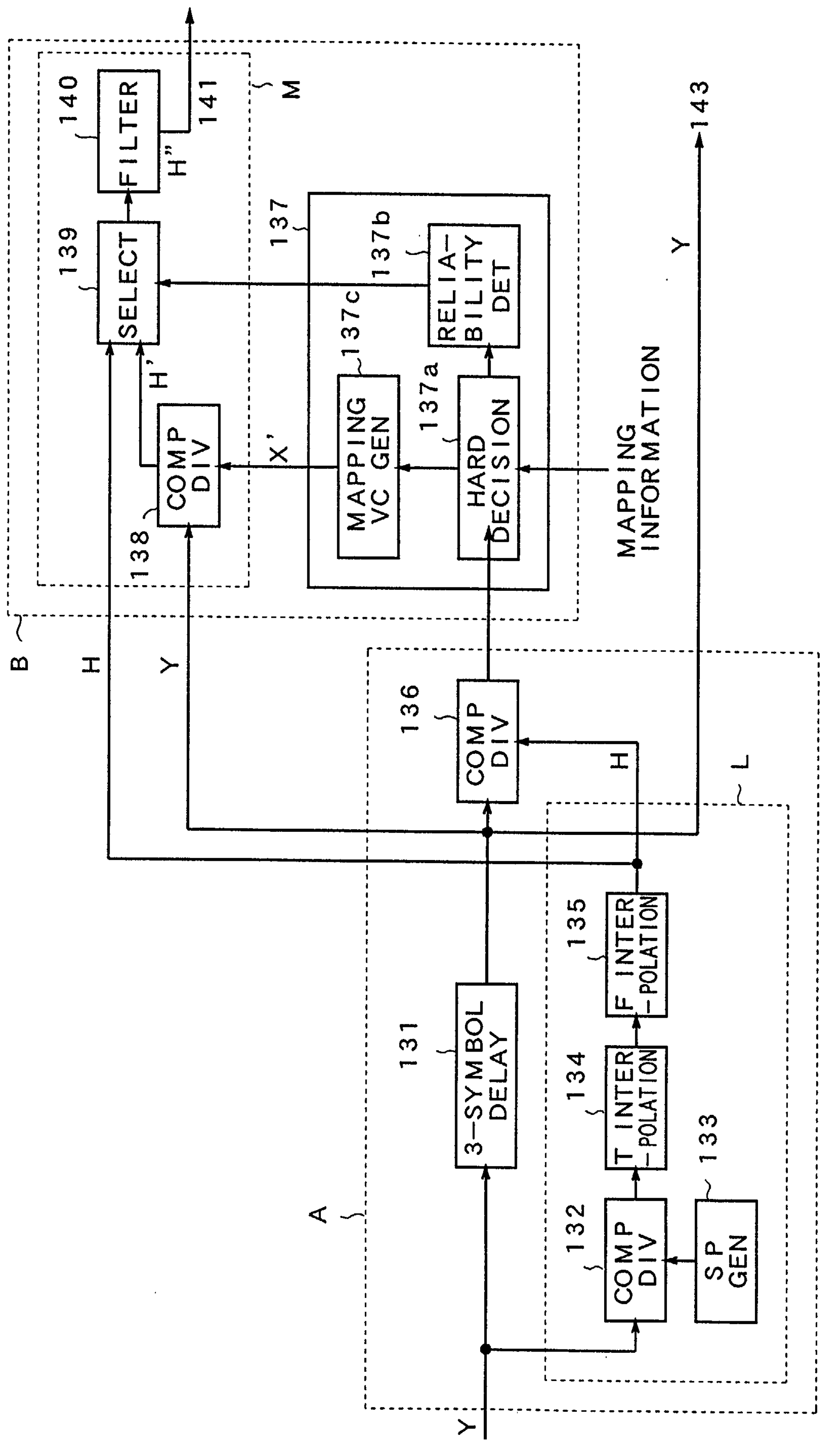
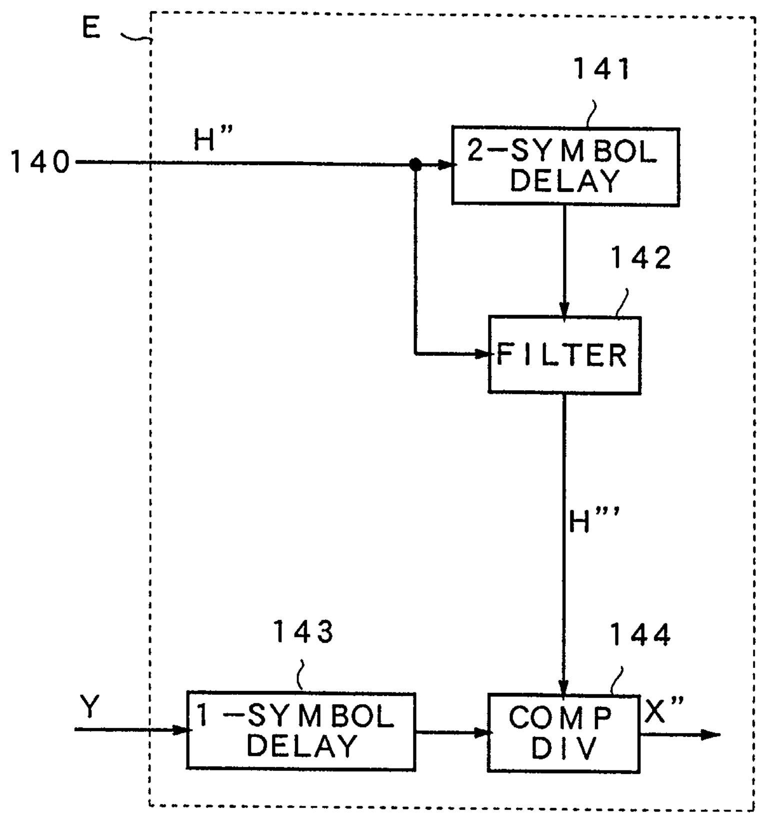

D
121
H"
120
SP EXTRACTION
122
T INTER-POLATION
123
F INTER-POLATION
124
H"'
125
Y
3-SYMBOL DELAY
COMP DIV
X"

FIG. 13


Y
A
131
3-SYMBOL DELAY
132
COMP DIV
133
SP GEN
134
T INTER -POLATION
135
F INTER -POLATION
L
H
136
COMP DIV
Y
143
B
H
Y
138
COMP DIV
X'
H'
139
SELECT
140
FILTER
H"
141
M
137
137a
HARD DECISION
137b
RELIA-BILITY DET
137c
MAPPING VC GEN
MAPPING INFORMATION

F I G. 1 4


E
141
140
H"
2-SYMBOL DELAY
142
FILTER
H"'
143
144
Y
1 -SYMBOL DELAY
COMP DIV
X"

F I G. 1 5

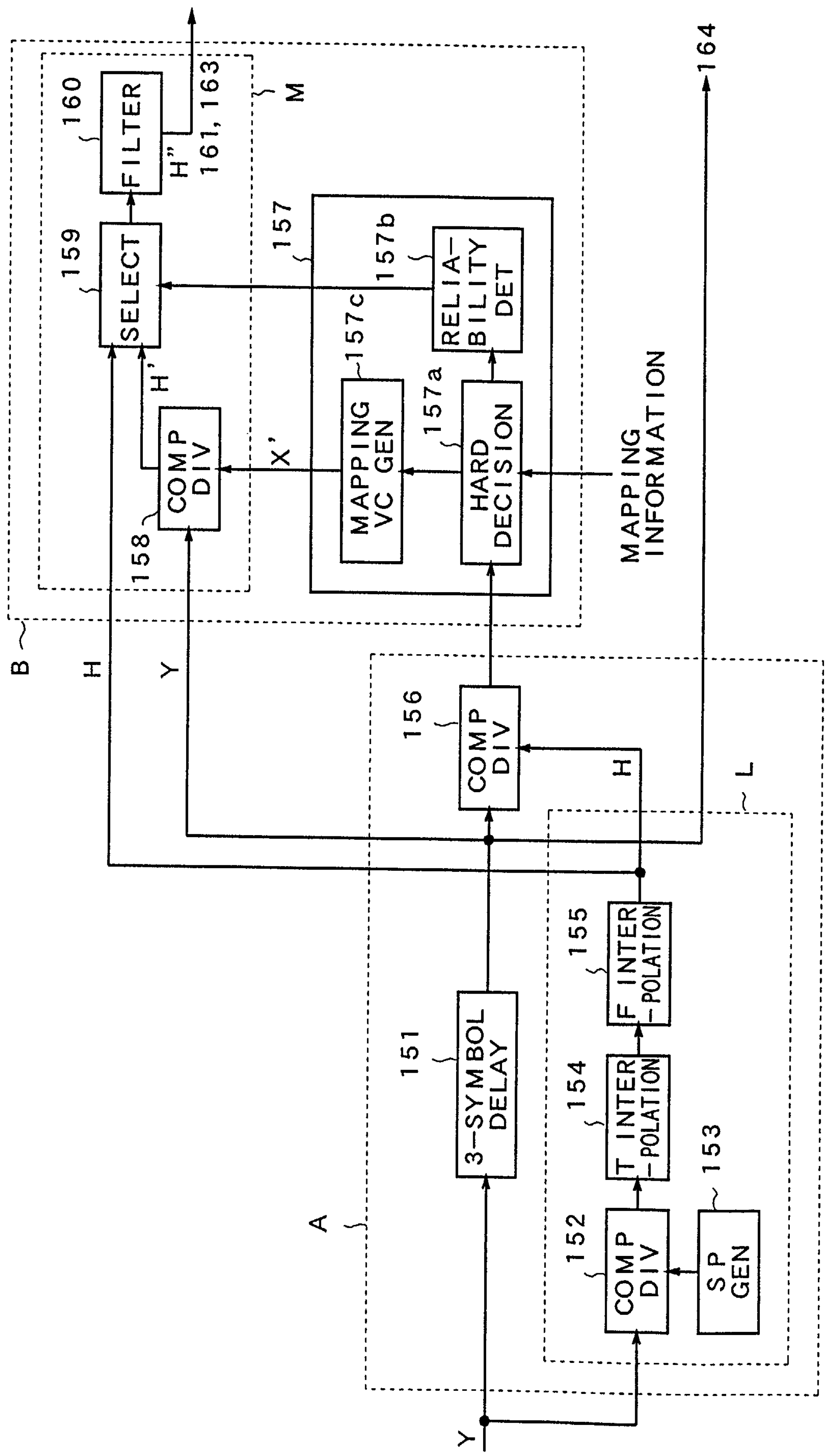
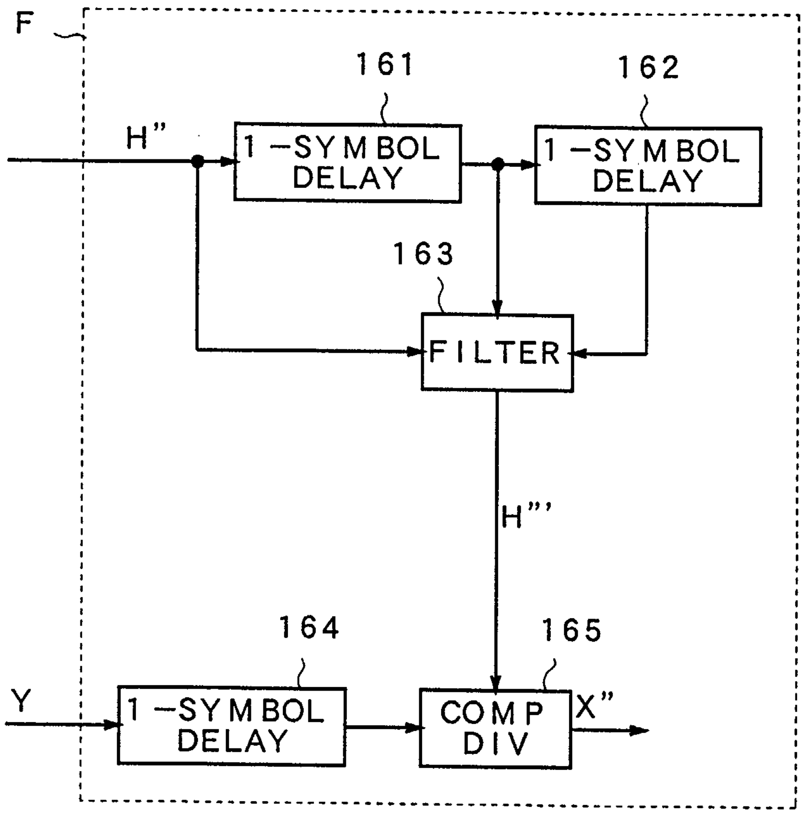

Y
3-SYMBOL DELAY
151
A
COMP DIV
152
SP GEN
153
T INTER -POLATION
154
F INTER -POLATION
155
L
H
COMP DIV
156
164
B
H
Y
HARD DECISION
157a
MAPPING VC GEN
157c
RELIA-BILITY DET
157b
157
MAPPING INFORMATION
X'
COMP DIV
158
H'
SELECT
159
FILTER
160
H"
161, 163
M

FIG. 16


F
161
162
H"
1 -SYMBOL DELAY
1 -SYMBOL DELAY
163
FILTER
H"'
164
165
Y
1 -SYMBOL DELAY
COMP DIV
X"

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 02 5271

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A		2-9, 11-23	
A	US 2001/015954 A1 (KUWABARA MASAHIRO ET AL) 23 August 2001 (2001-08-23) * abstract * * figure 1 * * claims *	1-23	
A	EP 0 998 068 A (SONY CORP) 3 May 2000 (2000-05-03) * abstract; figure 1 *	1-23	
A	EP 1 154 602 A (LUCENT TECHNOLOGIES INC) 14 November 2001 (2001-11-14) * abstract * * figure 4 *	1,10	

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H04L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10 February 2003	Koukourlis, S

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10-02-2003

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