March 8, 1966 J. W. LOEFFLER 3,239,138

ELECTRONIC ARTICLE COUNTING DEVICE

Filed Oct. 2, 1963 3 Sheets-Sheet 1

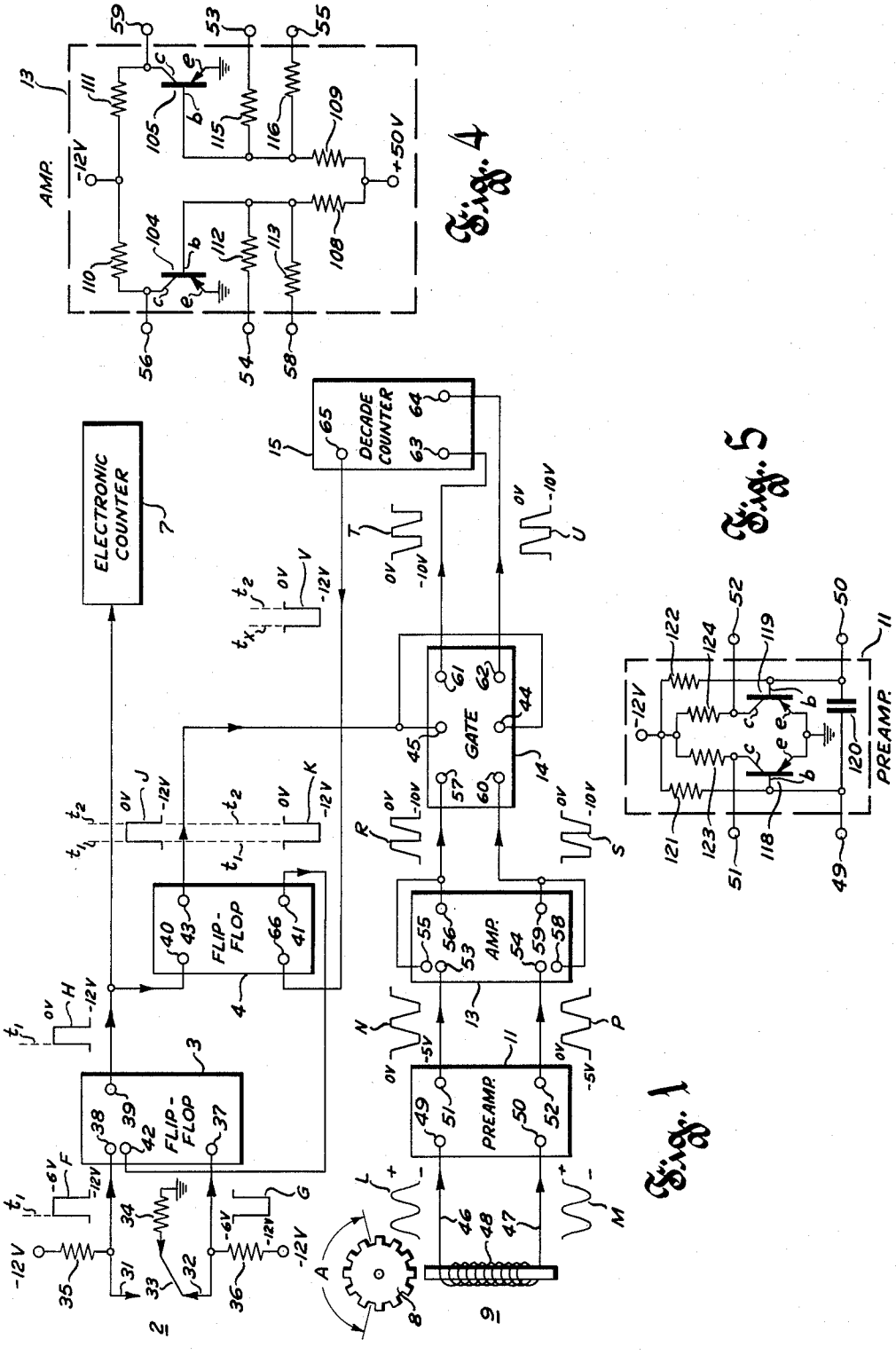


Fig. 1

Fig. 4

Fig. 5

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ELECTRONIC ARTICLE COUNTING DEVICE

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Fig. 2

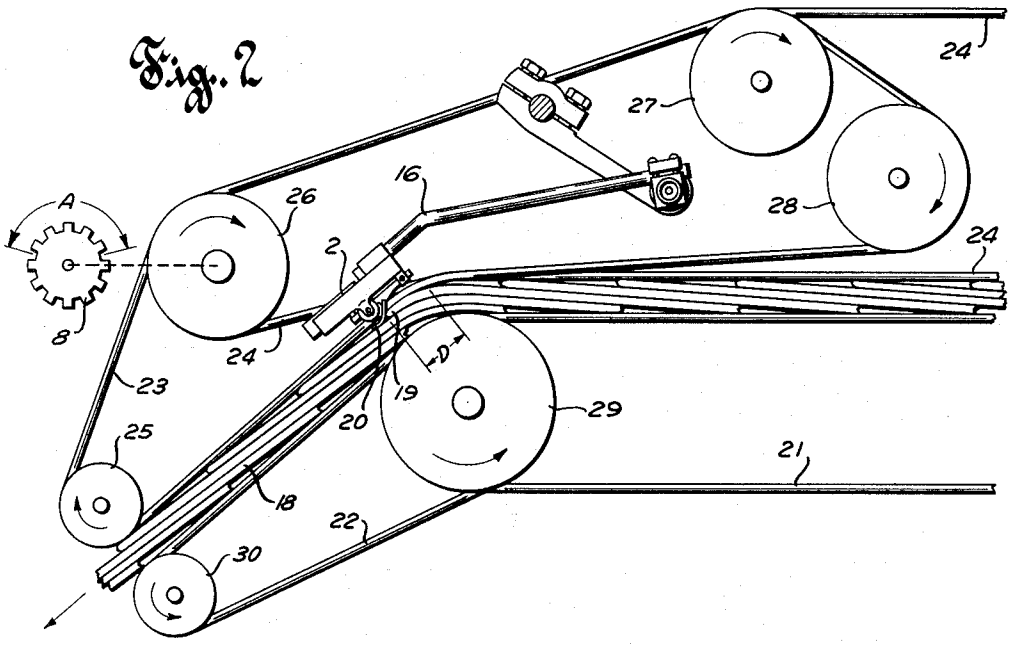
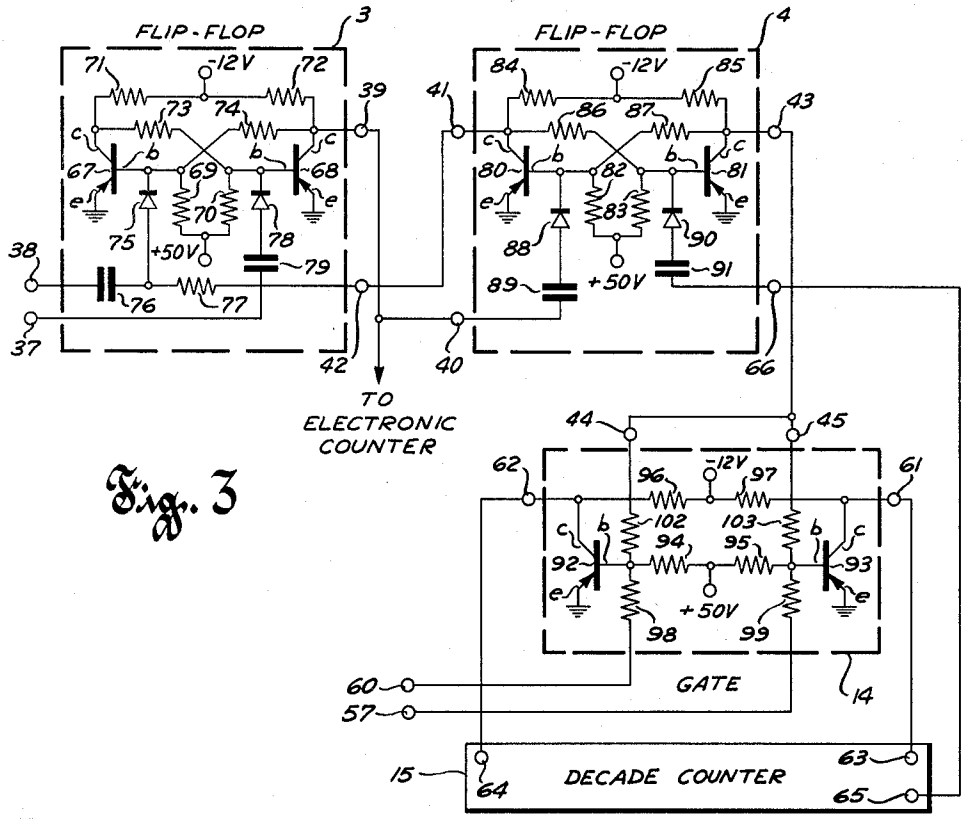


Fig. 3



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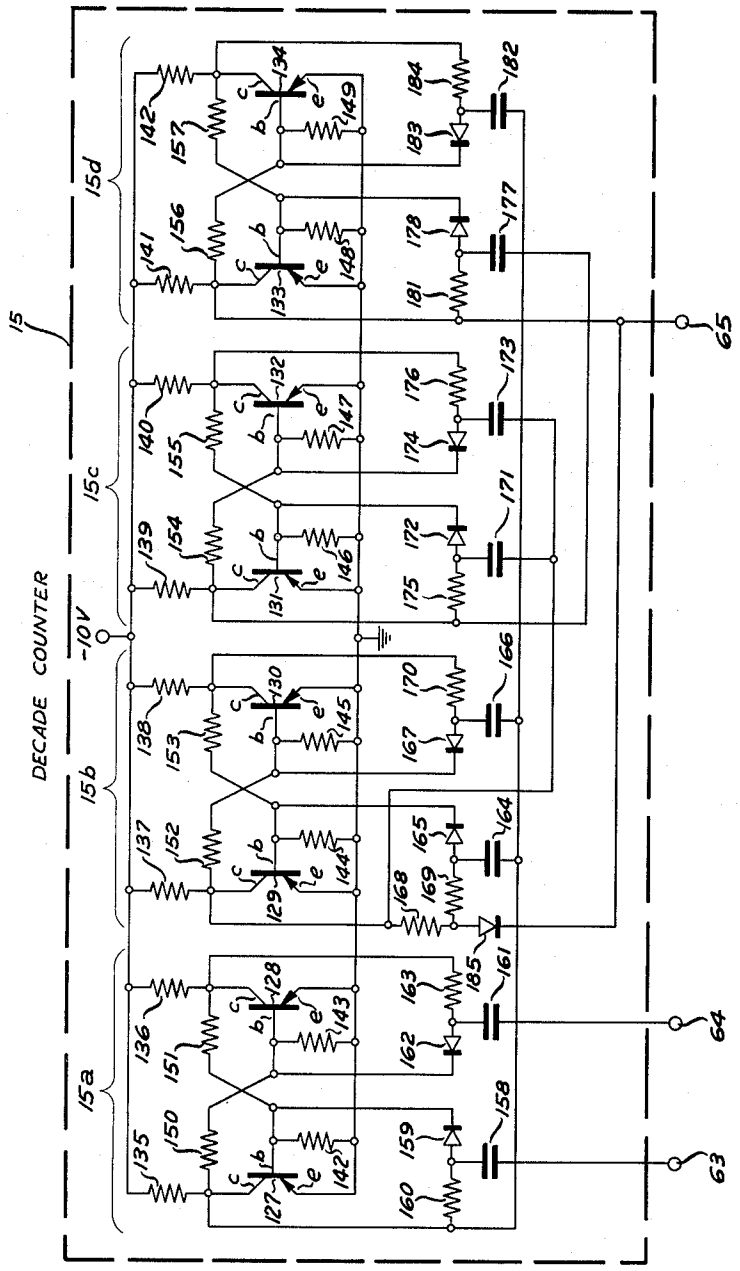


Fig. 6

United States Patent Office 3,239,138 Patented Mar. 8, 1966

3,239,138

ELECTRONIC ARTICLE COUNTING DEVICE

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Filed Oct. 2, 1963, Ser. No. 313,515
3 Claims. (Cl. 235—98)

This invention relates to article counting devices and more particularly to apparatus for counting newspapers conveyed in a lapped stream.

In the use of article counting devices, there often arises the problem of false counts which result from spurious actuations of the article sensing device. Common causes of false counting are excessive vibration of the sensing device, irregularities in the surface of the article counted, and contact bounce in electrical devices.

In the production of newpapers, the printed and folded product is normally conveyed from one operation to the next in a continuous stream between flexible belts and in a lapped relationship. The counting device is usually positioned to sense the leading edge of each of the moving newspapers in the stream. Such an arrangement is described in the F. E. Howdle et al. Patent No. 3,027,075, issued March 27, 1962, where the leading edge of each newspaper strikes the actuator of an electric switch which in turn provides a pulse to be counted by an electronic pulse counter.

Operating experience with such newspaper sensing devices at various conveyor speeds has shown that the occurrence of false counts is most frequent during that portion of newspaper travel immediately after the sensing device has contacted the leading edge to register the passing of the newspaper. While the leading edges of newspapers are commonly spaced about three inches apart and minimally spaced about two inches apart, false counts most often occur in approximately the first inch after the leading edge. This is the area where irregularities in thickness of the newspaper most often occur, and the probability of contact bounce and excessive vibration is highest. Similar phenomena can occur in the counting of other types of articles.

It is therefore an object of this invention to provide a counting apparatus for articles being conveyed which will minimize false counts and be effective and reliable at various conveyor speeds and counting rates.

It is a more specific object to provide a counting apparatus which is rendered insensitive to actuation of the article sensing device during that period in which false counts are most likely to occur.

Other objects and advantages will hereinafter appear.

While the device hereinafter described is adapted to fulfill the objects stated, it is to be understood that it is not intended that the invention be confined to the particular preferred embodiment disclosed since it is susceptible of various modifications without departing from the scope of the claims.

In the drawings:

FIGURE 1 is a diagrammatic illustration of a system which incorporates the principles of this invention;

FIG. 2 is a schematic drawing showing the relationship of the article sensing device to a lapped stream of newspapers;

FIG. 3 illustrates in greater detail the circuitry of several of the elements of FIG. 1;

FIG. 4 shows the details of the amplifier of FIG. 1;

FIG. 5 shows the detailed circuitry of the preamplifier element of FIG. 1; and

FIG. 6 illustrates the circuitry of a decade counter suitable for use in the system of FIG. 1.

The objects of this invention are accomplished by providing a counting apparatus for counting individual articles in a conveyed stream which is rendered insensitive by an electronic gate device for a period initiated by the actuation of the article counting device and lasting for a time inversely proportional to the speed of the conveyed stream. This period of time corresponds to that time and distance of article travel during which false counts are most likely to occur and is of a smaller duration than the minimum interval between the passage of individual articles.

FIG. 1 illustrates the overall relationship and electrical connection of elements of the present invention which include a counting switch **2**, two flip-flop circuits **3** and **4**, a pulse counter **7**, a magnetic pulse wheel **8**, a magnetic pickup **9**, a preamplifier **11**, an amplifier **13**, a gate circuit **14**, and a decade counter **15**. In FIG. 1, there are also included voltage pulse diagrams F, G, H, J, K, L, M, N, P, R, S, T, U and V which illustrate the form of pulses at various points in the system. These diagrams are of voltage versus time with the time scale of each diagram running from left to increased time at the right. The indicated voltages with the diagrams are illustrative of the maximum and minimum voltages of the pulses.

FIG. 2 illustrates the mechanical relationship of elements of the present invention. Counting switch **2** is supported by a pivoted arm **16** in a position to detect a passage of leading edges of individual newspapers in a lapped stream **18**. A leading edge **19** is shown as it makes contact with follower **20** which actuates counting switch **2**. The construction and operation of counting switch **2** is more completely described in Frederic E. Howdle and Edwin X. Schmidt Patent No. 3,027,075, issued March 27, 1962. The lapped stream **18** is supported and conveyed by flexible belts **21**, **22**, **23** and **24** which are in turn supported by rollers **25**, **26**, **27**, **28**, **29** and **30**. The gear toothed pulse wheel **8** is mechanically connected to roller **26** so that it will rotate at a speed proportional to the speed of the conveyed stream.

Returning to FIG. 1, counting switch **2** is shown to be of the single pole double throw variety with two stationary contacts **31** and **32** and a movable contact **33** which is biased to remain in contact with stationary contact **32** when in its normal unactuated position. Movable contact **33** is connected to ground through a resistor **34**. Stationary contacts **31** and **32** are connected, respectively, to a negative 12-volt source through resistors **35** and **36**. The magnitude of this voltage is not critical and, as are all of the voltages illustrated hereinafter, is chosen as an exemplary voltage for purposes of illustration.

Contacts **32** and **31** of counting switch **2** are connected, respectively, to input terminals **37** and **38** of flip-flop circuit **3**. Output terminal **39** of flip-flop circuit **3** is connected to the input of the electronic counter **7** and to an input terminal **40** of flip-flop circuit **4**. One of the output terminals **41** of flip-flop circuit **4** is connected to a third input terminal **42** of flip-flop circuit **3**, while the other output terminal **43** of flip-flop circuit **4** is connected to each of control input terminals **44** and **45** of gate circuit **14**.

A pair of leads **46** and **47** leading to coil **48** of magnetic pickup **9** are connected, respectively, to input terminals **49** and **50** of preamplifier **11**. The output terminals **51** and **52** of preamplifier **11** are respectively connected to input terminals **53** and **54** of amplifier **13**. Input terminal **55** and output terminal **56** of amplifier **13** are together connected to input terminal **57** of gate **14**. Similarly, input terminal **58** and output terminal **59** of amplifier **13** are connected to input terminal **60** of gate **14**.

The output of gate circuit **14** is carried from output terminal **61** to input terminal **63** of decade counter **15** and from output terminal **62** to input terminal **64** of dec-

ade counter 15. The output of decade counter 15 is carried from output terminal 65 to input terminal 66 of flip-flop circuit 4.

FIG. 3 shows the detailed circuitry of flip-flop circuit 3, flip-flop circuit 4, and gate circuit 14. Flip-flop circuit 3 is a resistance coupled flip-flop circuit which includes two transistors 67 and 68, each having a grounded emitter *e*, a base *b*, and a collector *c*. The collector of transistor 68 is connected to output terminal 39. A positive 50 volt source is connected to the base of transistors 67 and 68 through resistors 69 and 70, respectively. A negative 12-volt source is connected to the collectors of transistors 67 and 68 through resistors 71 and 72, respectively. A pair of resistors 73 and 74 cross-couple the base of transistor 67 to the collector of transistor 68, and the base of transistor 68 to the collector of transistor 67. A diode 75 permits input signals to be applied to the base of transistor 67 from either input terminal 38 through capacitor 76, or input terminal 42 through resistor 77. Similarly, diode 78 permits input signals to be applied to the base of transistor 68 from input terminal 37 through capacitor 79.

A closely similar circuit is shown for flip-flop circuit 4 which utilizes a transistor 80 with a grounded emitter *e*, a base *b*, and a collector *c* connected to output terminal 41 and a transistor 81 with a grounded emitter *e*, a base *b*, and a collector *c* connected to output terminal 43. A positive 50-volt source is connected to the base of transistor 80 and base of transistor 81 through resistors 82 and 83, respectively. A negative 12-volt source is connected to the collector of transistor 80 and the collector of transistor 81 through resistors 84 and 85, respectively. Resistors 86 and 87 cross-couple the base of transistor 80 to the collector of transistor 81 and the base of transistor 81 to the collector of transistor 80. Positive going pulse inputs are applied to the pase of transistor 80 through diode 88 and capacitor 89. Similarly, diode 90 and capacitor 91, in series, connect input terminal 66 to the base of transistor 81.

Gate circuit 14 comprises a transistor 92 having a grounded emitter *e*, a base *b*, and a collector *c* connected to output terminal 62; and a transistor 93 with a grounded emitter *e*, a base *b*, a collector *c* connected to output terminal 61. A positive 50-volt source is connected to the base of transistor 92 through a resistor 94 and to the base of transistor 93 through a resistor 95. A negative 12-volt source is connected to the collectors of each of transistors 92 and 93 through resistors 96 and 97, respectively. Input terminals 60 and 57 are connected to the base electrodes of each of transistors 92 and 93 by resistors 98 and 99, respectively. Control signals are applied to the base of transistor 92 from control input terminal 44 through resistor 102. Similarly, the base of transistor 93 receives control signals from control input terminal 45 through resistor 103.

FIG. 4 illustrates a dual amplifier 13 which is used for pulse amplification and formation. This circuit utilizes a transistor 104 with a grounded emittter *e*, a base *b*, and a collector *c* connected to output terminal 56, and a transistor 105 having a grounded emitter *e*, a base *b*, and a collector *c* connected to output terminal 59. A positive 50-volt source is connected to bases of transistors 104 and 105 through resistors 108 and 109, respectively. A negative 12-volt source is connected to the collectors of transistors 104 and 105 through resistors 110 and 111, respectively. A resistor 112 serves to carry input signals from input terminal 54 to the base of transistor 104. Resistor 113 connects input terminal 58 to the base of transistor 104. Similarly, resistor 115 connects input terminal 53 to the base of transistor 105 and resistor 116 connects input terminal 55 to the base of transistor 105.

FIG. 5 illustrates the circuitry of preamplifier 11 of FIG. 1. It is a dual preamplifier using transistors 118 and 119 and is designed to run saturated to increase stability. Transistor 118 has a grounded emitter *e*, a base *b* connected to input terminal 49, a collector *c* connected to output terminal 51. Similarly, transistor 119 has a grounded emitter *e*, a base *b* connected to input terminal 50, and a collector *c* connected to output terminal 52. A capacitor 120 is connected across inputs 49 and 50 to reduce any high frequency spikes or pickup which might occur. A negative 12-volt source is connected to the base of transistor 118 through resistor 121, to the base of transistor 119 through resistor 122, to the collector of transistor 118 through resistor 123, and to the collector of transistor 119 through resistor 124.

The system of FIG. 1 also includes a decade counter 15 which will count each of the positive going wave fronts applied alternately to input terminals 63 and 64, and upon the occurrence of each tenth count, will produce a positive going pulse at output terminal 65. The operation of a preferred form of such a counter will now be explained with reference to FIG. 6.

Counter 15 is a four-bit counter adapted for decade counting and consists of four resistance coupled flip-flops 15*a*, 15*b*, 15*c* and 15*d*, which are connected for binary counting. The first flip-flop circuit 15*a* includes transistors 127 and 128. The second flip-flop 15*b* includes transistors 129 and 130. The third flip-flop 15*c* includes transistors 131 and 132. And the fourth flip-flop 15*d* includes transistors 133 and 134. Each transistor has a grounded emitter *e*, a base *b* and a collector *c*.

A negative 10-volt source is connected to the collector of each transistor through resistors 135, 136, 137, 138, 139, 140, 141 and 142. Between the emitter of each transistor and their respective bases there are placed resistors 142, 143, 144, 145, 146, 147, 148 and 149. Within each flip-flop circuit the base of each transistor is cross-coupled to the collector of the opposite transistor by resistors 150, 151, 152, 153, 154, 155, 156 and 157.

Input terminal 63 is connected to the base of transistor 127 by capacitor 158 in series with diode 159. A resistor 160 connects the collector of transistor 127 to a point between capacitor 158 and diode 159. Similarly, capacitor 161, in series with diode 162 connects input terminal 64 to the base of transistor 128, and resistor 163 connects the collector of transistor 128 to the common connection of capacitor 161 and diode 162. A coupling capacitor 164 and diode 165, in series, connect the collector of transistor 127 to the base of transistor 129 in the second flip-flop circuit 15*b*. Similarly, capacitor 166 and diode 167 couples the collector of transistor 127 with the base of transistor 130. Between the collector of transistor 129 and the common connection point of capacitor 164 and diode 165, there are, in series, two resistors 168 and 169. Between capacitor 166 and the collector of transistor 130, there is a resistor 170. The collector of transistor 129 in the second flip-flop circuit 15*b* is coupled to the third flip-flop circuit through capacitor 171 and diode 172 in series, to the base of transistor 131, and through capacitor 173 and diode 174, in series, to the base of transistor 132. A resistor 175 is connected between capacitor 171 and the collector of transistor 131 and resistor 176 is connected between capacitor 173 and the collector of transistor 132. The collector of transistor 131 in the third flip-flop circuit is coupled to the base of transistor 133 in the fourth flip-flop circuit 15*d* through capacitor 177 and diode 178 in series. A resistor 181 is connected between capacitor 177 and the collector of transistor 133. Capacitor 182 and diode 183, in series, serve to couple the collector of transistor 127 in the first flip-flop circuit 15*a* to the base of transistor 134 in the fourth flip-flop circuit 15*d*. A resistor 184 is connected between capacitor 182 and the collector of transistor 134. The adaptation for decade counting is completed by the connection of diode 185 between the juncture of resistors 168 and 169 in the second flip-flop circuit 15*b* and the collector of transistor 133 in the fourth flip-flop circuit 15*d*. Output terminal 65 is also connected to the collector of transistor 133.

The values of the resistors in each of the four flip-flop circuits are chosen so that, upon the initial application of power to decade counter **15**, the left-hand transistor in each flip-flop circuit becomes conductive while its opposite becomes nonconductive. It therefore may be assumed that the initial state of the counter is such that each of transistors **127**, **129**, **131** and **133** are conductive while transistors **128**, **130**, **132** and **134** are nonconductive.

In the initial state of the counter, since transistor **128** is nonconductive, the base of transistor **127** is at a potential which is significantly negative with respect to ground and transistor **127** conducts at saturation. The collector of transistor **127**, therefore, is very close to zero or ground voltage. Further, the base of transistor **128** is held close to zero volts and transistor **128** remains in a substantially nonconducting state. The appearance of a sharply positive going voltage at input terminal **63** causes a current to flow through capacitor **158** and diode **159**, and the base of transistor **127** becomes positive to turn off transistor **127**. The turning off of transistor **127** causes the collector of transistor **127** and the base of transistor **128** to become negative. Transistor **128** thereupon becomes conductive at saturation and a substantially zero or ground voltage appears at the collector of transistor **127**. The base of transistor **127** is thereby held at a voltage close to zero and transistor **127** remains substantially nonconductive. This completes the "one" count and the decade counter **15** is then ready to accept the next sharply positive going signal which will appear at input terminal **64** to cause the "two" count.

The appearance of a sharply positive going voltage at input terminal **64** causes a current to flow through capacitor **161** and diode **162** to cause the base of transistor **128** to become positive to turn off transistor **128**. The collector of transistor **128** and the base of transistor **127** then become more negative to turn on transistor **127**. The collector of transistor **127** is then suddenly raised close to ground potential to hold transistor **128** in a substantially nonconductive state. The sharp rise in voltage of the collector of transistor **127** also causes a current flow through capacitor **164**. The current flow through capacitor **164** and diode **165** causes the second flip-flop circuit **15***b* to flip by turning off transistor **129**. The voltage rise to capacitors **166** and **182** at this point has no effect, since the transistors **130** and **134** to which they lead are already turned off and the negative voltages at their respective collectors block, through resistors **163** and **184**, the pulses at their respective capacitor-diode gates consisting of diode **162** and capacitor **161**, and diode **183** and capacitor **182**. This completes the "two" count.

The third positive going input signal will appear at input terminal **63** to cause the "three" count. This third positive going voltage causes the first flip-flop **15***a* to flip by turning off transistor **127**. The fourth positive going input signal which will appear at input terminal **64** will cause the first flip-flop **15***a* to flop by turning off transistor **128** and will cause the second flip-flop circuit **15***b* to flop, since the positive going voltage, which appears at the collector of transistor **127**, will cause a current flow through capacitor **166** and diode **167** to cause the base of transistor **130** to go positive and turn off transistor **130**. Further, as a consequence of the fourth positive going input signal at input terminal **64**, the third flip-flop circuit **15***c* will flip, since the collector of transistor **129** will go sharply from a negative voltage to ground to cause a current to flow through capacitor **171** and diode **172** to turn off transistor **131**.

This procedure continues through the "seven" count after which transistors **128**, **130**, **132** and **133** are conductive. The eighth positive going input signal, which will appear at input terminal **64**, causes the first three flip-flop circuits **15***a*, **15***b* and **15***c* to flop and the fourth flip-flop circuit **15***d* to flip. Transistor **133** in the fourth flip-flop circuit **15***d* is turned off as a consequence of the sharply positive going voltage at the collector of transistor **131** when transistor **131** becomes conductive. At this point represented by time *tx* on pulse diagram V of FIG. 1 the collector of transistor **133** becomes negative. The collector of transistor **133** is connected to diode **185** which permits the negative voltage to be impressed between resistors **168** and **169** in the second flip-flop circuit **15***b*. Since capacitor **164** and diode **165** form a capacitor-diode gate the negative voltage applied at their juncture will prevent the charging of capacitor **164** and will therefore suppress the positive going voltage which would otherwise be applied to the gate of transistor **129** when the first flip-flop circuit **15***a* flops at the "ten" count and the collector of transistor **127** returns to ground voltage. Flip-flop circuit **15***b* will therefore remain unaffected by the "ten" count. The ninth positive going input signal which will appear at input terminal **63**, will cause the first flip-flop circuit **15***a* to flip to complete the "nine" count. At this point transistors **128**, **129**, **131** and **134** are conductive and decade counter **15** is ready for the "ten" count. The tenth positive going input, which appears at input terminal **64**, turns off transistor **128**, and transistor **127** becomes conductive. The collector of transistor **127** goes suddenly from a negative voltage to ground, and this sharply positive going voltage change causes a current flow through capacitor **182** and diode **183** to turn off transistor **134** in the fourth flip-flop circuit **15***d*. The second flip-flop **15***b* is not affected by this sharply positive going voltage since, as has been explained, current flow to base of **129** is suppressed. The "ten" count therefore causes decade counter **15** to return to its initial state in which transistors **127**, **129**, **131** and **133** are conductive. Further, as transistor **133** in the fourth flip-flop circuit **15***d* is turned on, its collector goes sharply from a negative voltage to near ground voltage at time t_2 to cause a sharply going voltage change at output terminal **65**. (See pulse diagram V of FIG. 1.)

The operation of the entire system will now be described.

The input signals to the system consist of pulse counts from counter switch **2** and a signal from magnetic pickup **9** which indicates the distance traveled by newspaper stream **18**. Referring to FIG. 2, paper stream **18** travels from right to left. The actuator **20** of counter switch **2** is shown as it contacts the leading edge **19** of a newspaper to cause operation of switch **2**. Distance D represents the distance following the leading edge in which unwanted false counts are most likely to occur. Pulse wheel **8** is connected to roller **26** so that pulse wheel **8** rotates through arc A during the time paper stream **18** travels through distance D. Therefore, five teeth of gear toothed pulse wheel **8** (FIG. 1) will pass the magnetic pickup **9** from the time actuator **20** of counter switch **2** contacts leading edge **19** until actuator **20** is distance D behind leading edge **19**.

As shown in FIG. 1, the movable contact **33** of counting switch **2** is normally in contact with stationary contact **32**. While counter switch **2** remains unactuated, terminal **37** of flip-flop **3** therefore receives an input voltage of negative 6-volts as shown by diagram G, if resistors **36** and **34** are chosen to be of equal value. At the same time terminal **38** receives the initial negative 12-volt signal as shown by diagram F.

As the leading edge **19** presses against actuator **20** to operate counter switch **2** at time t_1, movable contact **33** moves to break contact with contact **32** and makes contact with contact **31**. The signal to terminal **37** thereupon goes sharply to negative 12-volts as shown by diagram G at time t_1 and the signal to terminal **38** goes sharply to negative 6-volts as shown by diagram F. After leading edge **19** passes, the bias applied to movable contact **33** returns it to its original position. As a result, the signal to terminal **38** returns sharply to negative 12-volts and the signal to terminal **37** returns to negative 6-volts. Diagrams F and G illustrate the complete pulse forms produced by the passage of the single leading edge

19. The counter switch may then be actuated by another leading edge.

The pulses of diagrams F and G applied to terminals 38 and 37 serve to activate flip-flop 3. It is assumed that flip-flop state is initially in the state where transistor 127 is conductive and transistor 68 is nonconductive. Consequently terminal 39 is initially at negative 12-volts as shown by diagram H.

The positive going leading edge of the pulse of diagram F causes a current to flow through capacitor 76 and diode 75 to cause the base of transistor 67 to become positive. Transistor 67 consequently becomes nonconductive and flip-flop circuit 3 flips. Terminal 39 goes sharply to ground voltage as shown by diagram H. This change occurs so shortly after actuation of switch 2 that these two events may be considered to happen at the same time t_1. The positive going trailing edge of the pulse of diagram G causes flip-flop 3 to flop to its original state by applying a positive voltage to the base of transistor 68 by way of capacitor 79 and diode 78. As flip-flop 3 flops the voltage of terminal 39 returns to negative 12-volts to complete the pulse of diagram H.

The pulse of diagram H causes the number of newspapers totalized by electronic counter 7 to increase by one. The pulse of diagram H is also applied to terminal 40 of flip-flop 4 which is assumed to be initially in the state where transistor 80 is conductive.

The positive going leading edge of the pulse of diagram H causes current to flow through capacitor 89 and diode 88 to cause the base of transistor 80 to become positive and turn off transistor 80. Flip-flop 4 thereupon flips at time t_1 causing terminal 41 to become negative as shown by diagram K and terminal 43 to change from negative 12-volts to zero or ground voltage as shown by diagram J. The negative 12-volts of terminal 41 causes a negative voltage to be applied through terminal 42 and resistor 77 to the juncture of capacitor 76 and diode 75. Capacitor 76 and diode 75 form a capacitor-diode gate and the negative voltage at their juncture suppresses any further positive pulses to the base of transistor 67 resulting from positive going transients applied to terminal 38. Flip-flop 3 therefore cannot be changed from its initial state after time t_1 by spurious counter pulses and no pulses can be produced at terminal 39 to operate electronic counter 7 until flip-flop 4 returns to its original state and the negative voltage is removed from terminal 42 at time t_2.

Simultaneously, at time t_1, the zero voltage of terminal 43 is applied to terminals 44 and 45 of gate 14 to allow pulses which originate at magnetic pickup 9 to be delivered to decade counter 15.

Each pulse produced by magnetic pickup 9 corresponds to a given increment of distance of travel of paper stream 18, since pulse wheel 8 is coupled to roller 26 in the stream conveyor system. The pulses produced in coil 48 and delivered by leads 46 and 47 are in the form of an alternating current as shown by diagrams L and M of FIG. 1. As each tooth of pulse wheel 8 passes magnetic pickup 9 one pulse or cycle is produced. Each of diagrams L and M illustrate two pulses or cycles which correspond to the passage of two teeth of pulse wheel 8.

The pulses of diagrams L and M are neither of the form nor strength to be usable in the decade counter 15 and, therefore, are amplified and formed by preamplifier 11 and amplifier 13.

Preamplifier 11 is a dual amplifier which accepts input signals at terminals 49 and 50 and delivers balanced amplified output pulses at terminals 51 and 52. The output pulses which are 180° out of phase and of the form shown in diagrams N and P of FIG. 1. These pulses are delivered to input terminals 53 and 54 of amplifier 13. The output terminals 56 and 59 of amplifier 13 are connected to input terminals 55 and 58 to cross-couple transistors 104 and 105 through resistors 113 and 116. Amplifier 13 is driven very hard to produce rapidly negative going waveforms at the output terminals 56 and 59 as shown by diagrams R and S. These output pulses of amplifier 13 constitute the input to gate circuit 14.

Gate circuit 14 includes two amplifying transistors 92 and 93 which, when operated in their normal unsaturated operating range, function to produce at their cathodes a signal which is of inverse waveform with respect to the input signals delivered to their bases. When the bases of these transistors 92 and 93 are held at relatively high negative voltages they conduct at saturation and their cathodes remain at near ground voltage regardless of the input to terminals 60 and 57, and will then not deliver pulse outputs to terminals 62 and 61. Therefore, before time t_1, the pulses which originate at magnetic pickup 9 will not pass through gate 14 to decade counter 15, because the input terminals 45 and 44 of gate 14 are held at negative 12 volts by the output at terminal 43 of flip-flop 4. At time t_1, the output of flip-flop 4 at terminal 43 goes to zero volts and the bases of transistors 92 and 93 are biased into the normal operating range of transistors 92 and 93. The variations in base voltage caused by the pulses of diagram R at terminal 57 and the pulses of diagram S at terminal 60 are then amplified and inverted to appear at output terminals 61 and 62, respectively.

The output pulses of gate 14 are of the form shown in diagrams T and U with the sharply positive going waveforms necessary to operate decade counter 15.

As previously explained decade counter 15 counts each of the sharply positive going transients which will appear alternately at input terminals 63 and 64. At time t_1, the time of the newspaper count by counter switch 2, pulses will begin to be delivered to decade counter 15 through gate 14. Decade counter then counts ten of the alternately delivered pulses and, upon counting the "ten" count, produces an output pulse at terminal 65 of the form shown in diagram V. The counting of ten pulses corresponds to the passage of five teeth of pulse wheel past magnetic pickup 9, since each tooth produces two sharply positive going waveforms at the input terminals 63 and 64 of decade counter 15. The counting of ten pulses therefore also corresponds to the movement of newspaper stream 18 through distance D (FIG. 2). The sharply positive going leading edge of the pulse of curve V therefore occurs at a time t_2 which is the end of the period during which false counts by counter switch 2 are most likely to occur.

The sharply positive going leading edge of the pulse of diagram V is delivered to input terminal 66 of flip-flop 4. This positive going transient causes a positive voltage to be applied to the base of transistor 81. Transistor 81 is thereby turned off and flip-flop 4 flops to its original state. The voltage at output terminal 43 as shown by diagram J thereupon returns to negative 12-volts at time t_2 to "close" gate circuit 14 and stop the counting by decade counter 15. Simultaneously, the voltage at output terminal 41 of flip-flop 4 goes rapidly from negative 12-volts to ground voltage. Upon the removal of the negative voltage from terminal 42 of flip-flop 3 of the capacitor-diode gate consisting of capacitor 76 and diode 75 will again permit the activation of flip-flop 4 by pulses from counter switch 2 impressed on terminal 38. Counter pulses may thereupon again be sent to electronic counter 7 and, after time t_2, the system is in its original state and ready to count the next newspaper.

The aforedescribed cycle of operation will repeat following the counting of each newspaper in the lapped stream 18.

I claim:

1. An article counting system comprising:

means for conveying articles to be counted;

means for sensing the passage of articles conveyed and having an electrical output indicative thereof;

an article counter operated by the output of said sensing means;

pulsing means for producing electrical pulses indicative of given increments of travel of articles conveyed;

pulse counter means rendered operative by the counting of an article for counting a selected number of pulses produced by said pulsing means and for subsequently producing an output signal; and

gating means for interrupting the output of said sensing means to said article counter upon the occurrence of an article count and allowing the passage of said output of said sensing means to said article counter upon the occurrence of an output signal from said pulse counter means, whereby the occurrence of false counts due to spurious operation of said sensing means is prevented for a selected distance of travel of said articles following the counting of an article.

2. An article counting system comprising:

article sensing means for producing an electrical pulse output indicative of the passage of each conveyed article;

first pulse counter means operated by said output of said article sensing means;

pulsing means for producing electrical pulses indicative of given increments of travel of articles conveyed;

second pulse counter means for counting a selected number of pulses produced by said pulsing means and for subsequent producing an output signal;

first gating means for allowing passage of pulse from said pulsing means to said second pulse counter means upon the counting of an article by said sensing means and for interrupting the pulses from said pulsing means to said second pulse counter means as a consequence of the output signal of said second pulse counter means; and

second gating means for interrupting the output of said sensing means to said first pulse counter means upon the occurrence of a pulse output from said sensing means to said first pulse counter means and

allowing the passage of the output of said sensing means to said first pulse counter means upon the occurrence of said output signal of said second pulse counter means;

whereby the output of said sensing means is interrupted to prevent false counts due to spurious operation of said sensing means during a selected distance of travel of conveyed articles following the counting of an article.

3. An article counting system comprising, in combination:

article sensing means for producing an output indicative of the passage of each of a plurality of conveyed articles to be counted;

means operated by the output of said sensing means for counting the number of articles;

means for measuring the rate of travel of said articles and having an output indicative of the time required for a given distance of article travel; and

means for interrupting the output of said sensing means after the counting of an article for the time required for a given distance of article travel as measured by said rate of travel measuring means which given distance of article travel is less than the space interval of said articles, to thereby prevent the occurrence of false counts following the counting of an article while said article travels through said given distance.

References Cited by the Examiner

UNITED STATES PATENTS

2,126,967	8/1938	Lyons	235—92
2,278,087	3/1942	McLaughlin et al.	235—98.4
2,730,301	1/1956	Beamish	235—98.4
2,730,302	1/1956	Roberts	93—93.3
2,910,231	10/1959	Hechler.	
3,027,817	4/1962	Loeffler	93—88.3

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