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(54) METHOD FOR IMPROVING A PHYSICAL PROPERTY DEFECT VALUE OF A GATE DIELECTRIC

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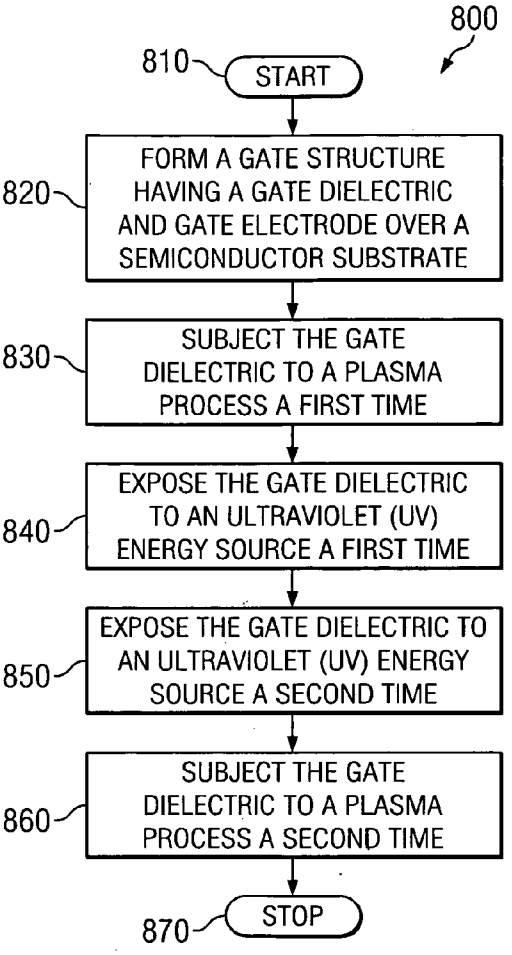
(57) **ABSTRACT**

The present invention provides a method for improving a physical property of a substrate, a method for manufacturing an integrated circuit, and an integrated circuit manufactured using the aforementioned method. In one aspect of the invention, the method for improving a physical property of a substrate includes subjecting the substrate to effects of a plasma process **830**, wherein the substrate has a physical property defect value associated therewith subsequent to the plasma process. The method further includes exposing the substrate to an ultraviolet (UV) energy source **840** to improve the physical property defect value.



100

FIG. 1

ELEMENT		K(eV)	L-I	L-II	L-III	M-I	M-II	M-III	M-IV	M-V	N-I	N-II	N-III
		1s	2s	2p1/2	2p3/2	3s	3p1/2	3p3/2	3d3/2	3d5/2	4s	4p1/2	4p3/2
1	H	13.6											
2	He	24.6*											
3	Li	54.7*											
4	Be	111.5*											
5	Be	188*											
6	C	284.2*											
7	N	409.9*	37.3*										
8	O	543.1*	41.6*										
9	F	696.7*											
10	Ne	870.2*	48.5*	21.7*	21.6*								
11	Na	1070.8+	63.5+	30.65	30.81								
12	Mg	1303+	88.7	49.78	49.5								
13	Al	1559.6	117.8*	72.95	72.55								
14	Si	1839	149.7*	99.82	99.42								

INITIAL SLOT	FINAL SLOT	ID	ORDER OF PROCESSING	WAFER TEMP (C)	EXPOSURE TIME (MIN)
1	1	41EMB06MSWA6	1	240	8
2	2	4SL2C04JSWH1	2	240	8
3	3	4SL2C04CSWG7	3	240	8
4	4	4SL2C04FSWE7	4	240	8
5	5	4SL2C048SWE3	5	240	8
6	6	4SL2C049SWB2	6	240	8
7	7	4SL2C041SWE1	CONTROL	CONTROL	CONTROL

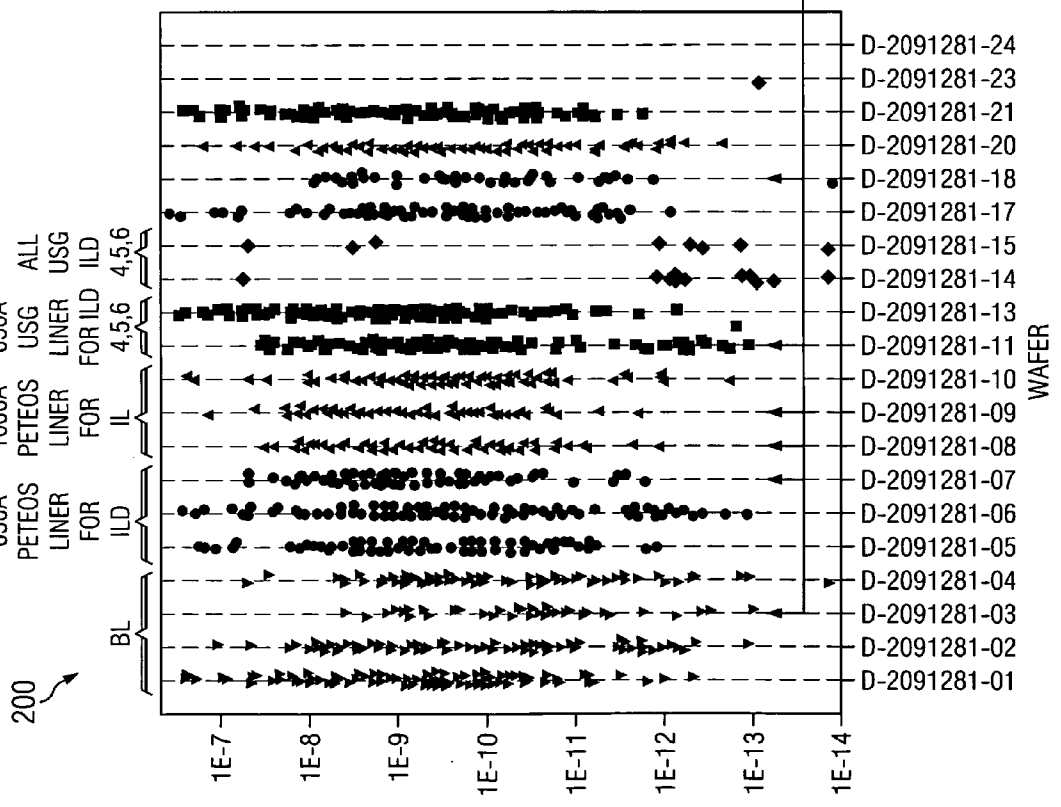


FIG. 2

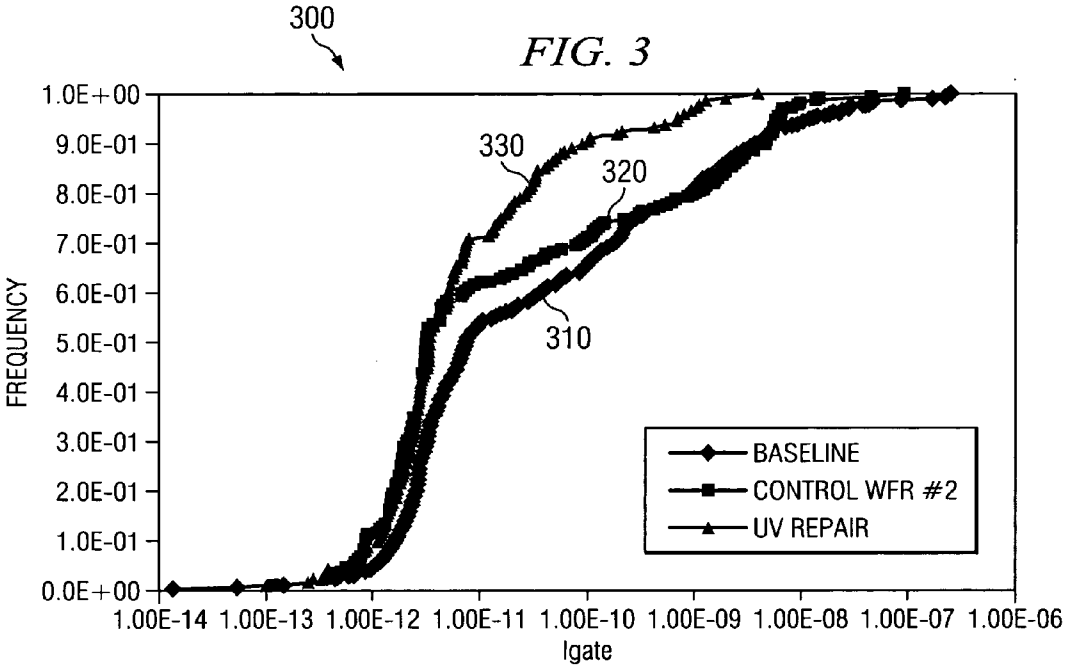
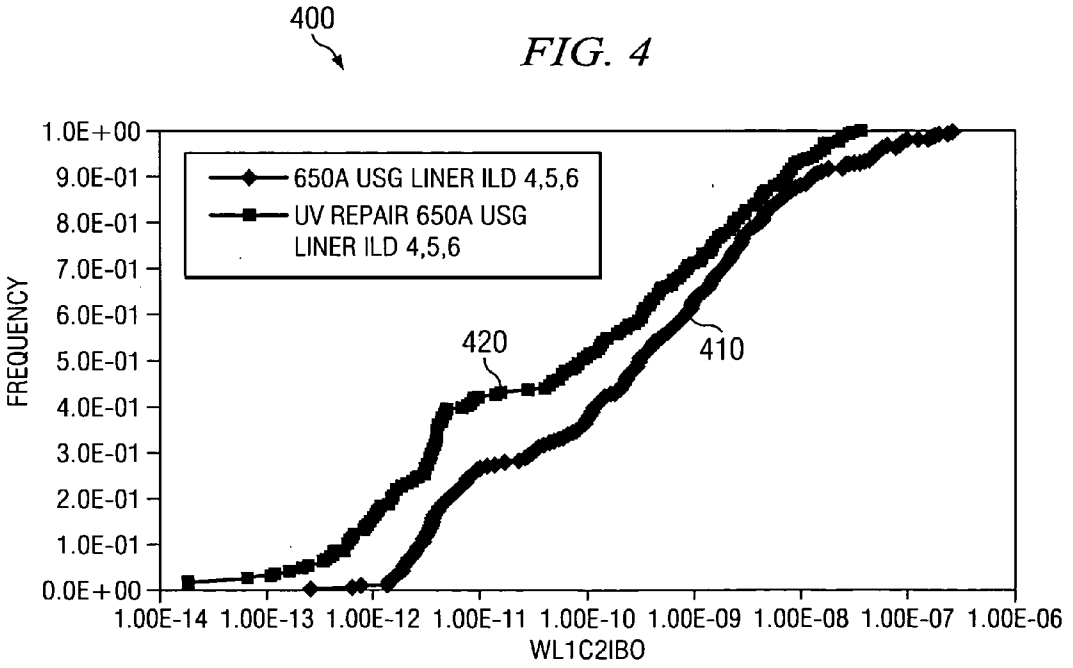

300
330
320
310
FREQUENCY
1.0E+00
9.0E-01
8.0E-01
7.0E-01
6.0E-01
5.0E-01
4.0E-01
3.0E-01
2.0E-01
1.0E-01
0.0E+00
1.00E-14 1.00E-13 1.00E-12 1.00E-11 1.00E-10 1.00E-09 1.00E-08 1.00E-07 1.00E-06
Igate
BASELINE
CONTROL WFR #2
UV REPAIR

FIG. 3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420
410
FREQUENCY
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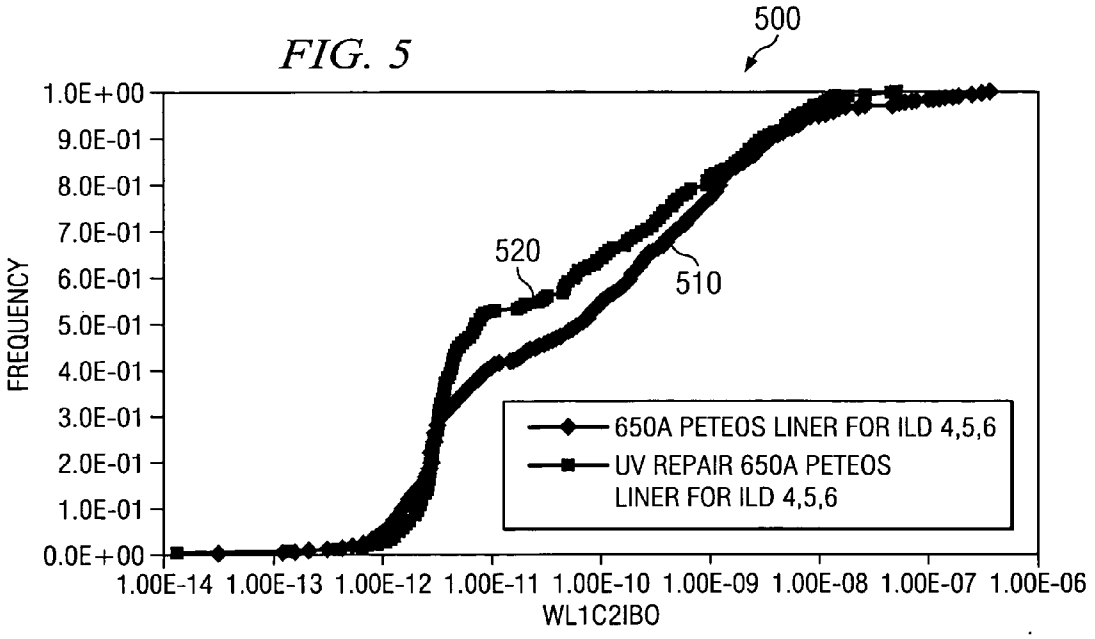
6.0E-01
5.0E-01
4.0E-01
3.0E-01
2.0E-01
1.0E-01
0.0E+00
1.00E-14 1.00E-13 1.00E-12 1.00E-11 1.00E-10 1.00E-09 1.00E-08 1.00E-07 1.00E-06
WL1C2IBO
650A USG LINER ILD 4,5,6
UV REPAIR 650A USG LINER ILD 4,5,6

FIG. 4

FIG. 5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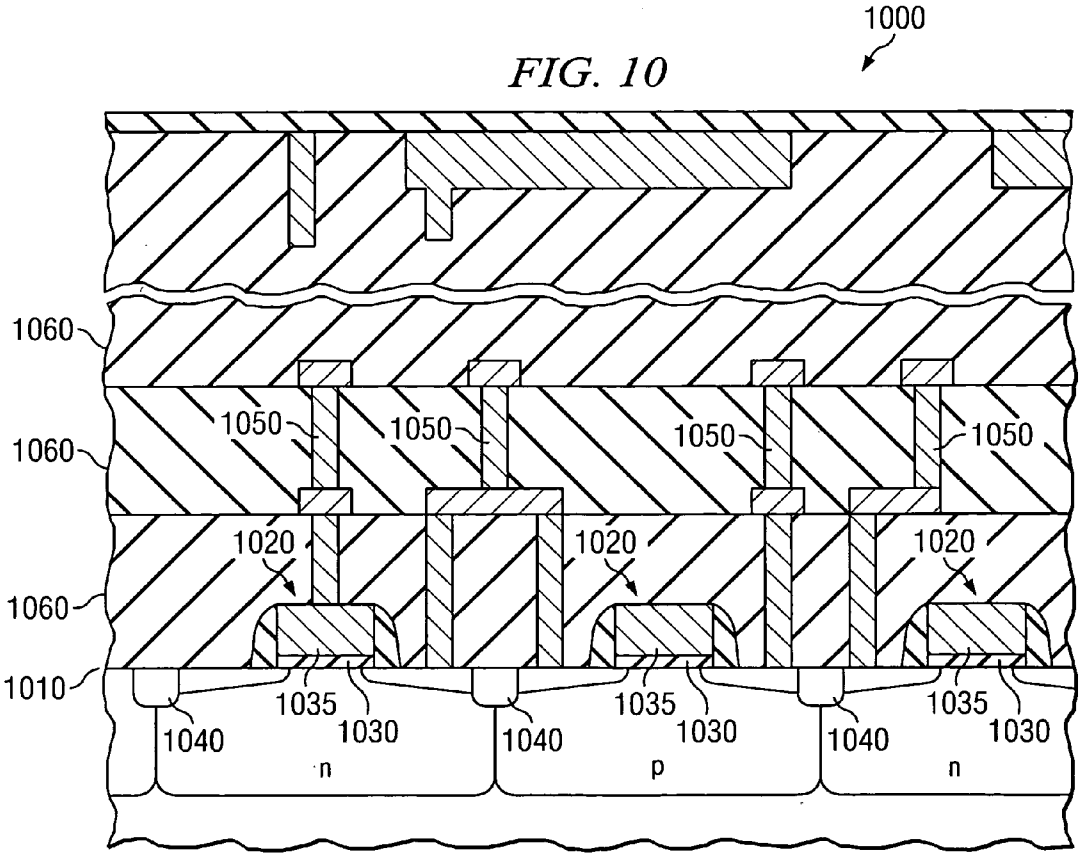
9.0E-01
8.0E-01
7.0E-01
6.0E-01
5.0E-01
4.0E-01
3.0E-01
2.0E-01
1.0E-01
0.0E+00
FREQUENCY
520
510
650A PETEOS LINER FOR ILD 4,5,6
UV REPAIR 650A PETEOS LINER FOR ILD 4,5,6
1.00E-14 1.00E-13 1.00E-12 1.00E-11 1.00E-10 1.00E-09 1.00E-08 1.00E-07 1.00E-06
WL1C2IBO

FIG. 10


1000
1060
1060
1060
1010
1050
1050
1050
1050
1020
1020
1020
1035
1030
1040
1035
1030
1040
1035
1030
1040
n
p
n

LOT	WAFER	GOI_3NTB _Delta	GOI_3NTF _Delta	GOI_3NTM _Delta	GOI_3PTB _Delta	GOI_3PTF _Delta	GOI_3PTM _Delta	TEMP (DEG C)	TIME (MIN)	
9968919	D-9968919-03	0.22	0.45	-0.30	0.11	-0.02	-0.05	50	4	Average Delta
9968919	D-9968919-03	-0.33	-0.18	0.41	-0.20	0.07	0.08	50	4	Std Dev Delta
9968919	D-9968919-05	-0.14	0.47	-0.13	0.03	-0.04	-0.01	50	8	Average Delta
9968919	D-9968919-05	-0.09	-0.34	0.47	0.06	0.09	0.02	50	8	Std Dev Delta
9968919	D-9968919-06	0.17	-0.22	0.32	0.00	0.01	-0.04	50	4	Average Delta
9968919	D-9968919-06	-0.65	-0.10	-0.92	-0.05	0.01	-0.05	50	4	Std Dev Delta
9968919	D-9968919-15	0.22	0.70	-0.34	-0.03	0.08	0.05	50	8	Average Delta
9968919	D-9968919-15	-0.08	-0.13	0.79	0.02	-0.13	-0.02	50	8	Std Dev Delta
9968919	D-9968919-16	0.03	0.46	0.33	-0.03	-0.04	0.07	240	4	Average Delta
9968919	D-9968919-16	-0.52	0.27	-0.54	0.04	0.04	-0.01	240	4	Std Dev Delta
9968919	D-9968919-17	0.21	-0.07	-0.33	0.02	-0.01	0.05	240	8	Average Delta
9968919	D-9968919-17	-0.81	-0.03	0.55	-0.01	0.01	-0.07	240	8	Std Dev Delta
9968919	D-9968919-18	0.08	-0.54	0.13	0.07	0.07	-0.04	240	4	Average Delta
9968919	D-9968919-18	-0.18	0.40	-0.32	-0.09	-0.09	-0.09	240	4	Std Dev Delta
9968919	D-9968919-21	0.06	0.20	0.61	0.08	-0.04	-0.10	240	8	Average Delta
9968919	D-9968919-21	-0.16	-0.11	-1.05	-0.04	0.01	0.02	240	8	Std Dev Delta
9968919	D-9968919-23	0.16	0.95	0.14	-0.10	0.01	0.03	Control	Control	Average Delta
9968919	D-9968919-23	-0.55	-0.17	-0.40	0.01	-0.02	0.00	Control	Control	Std Dev Delta
TEMP (DEG C)	TIME (MIN)									
50	4	0.20	0.12	0.01	0.05	-0.01	-0.05	Average Delta		
		-0.49	-0.14	-0.25	-0.12	0.04	0.01	Std Dev Delta		
50	8	0.04	0.59	-0.24	0.00	0.02	0.02	Average Delta		
		-0.08	-0.24	0.63	0.04	-0.02	0.00	Std Dev Delta		
240	4	0.05	-0.04	0.23	0.02	0.01	0.01	Average Delta		
		-0.35	0.34	-0.43	-0.03	-0.03	-0.05	Std Dev Delta		
240	8	0.13	0.07	0.14	0.05	-0.02	-0.02	Average Delta		
		-0.48	-0.07	-0.25	-0.03	0.01	-0.02	Std Dev Delta		
	GOI key:									
	GOI_3NTB									

600

FIG. 6

SPLIT	TECHNOLOGY	EOL SHIFT
CONDITION A	1.1 V PMOS CORE	93.08
CONDITION A	1.1 V PMOS CORE	155.32
CONDITION B	1.1 V PMOS CORE	176.26
CONDITION B	1.1 V PMOS CORE	118.75
CONDITION C	1.1 V PMOS CORE	93.15
CONDITION C	1.1 V PMOS CORE	96.60
DIELECTRIC 1	1.1 V PMOS CORE	110.61
DIELECTRIC 1, 8 MIN UV	1.1 V PMOS CORE	68.00
DIELECTRIC 1, 16 MIN UV	1.1 V PMOS CORE	57.00
DIELECTRIC 2	1.1 V PMOS CORE	133.02
DIELECTRIC 2, 8 MIN UV	1.1 V PMOS CORE	98.00
DIELECTRIC 2, 16 MIN UV	1.1 V PMOS CORE	104.00

FIG. 7A

720

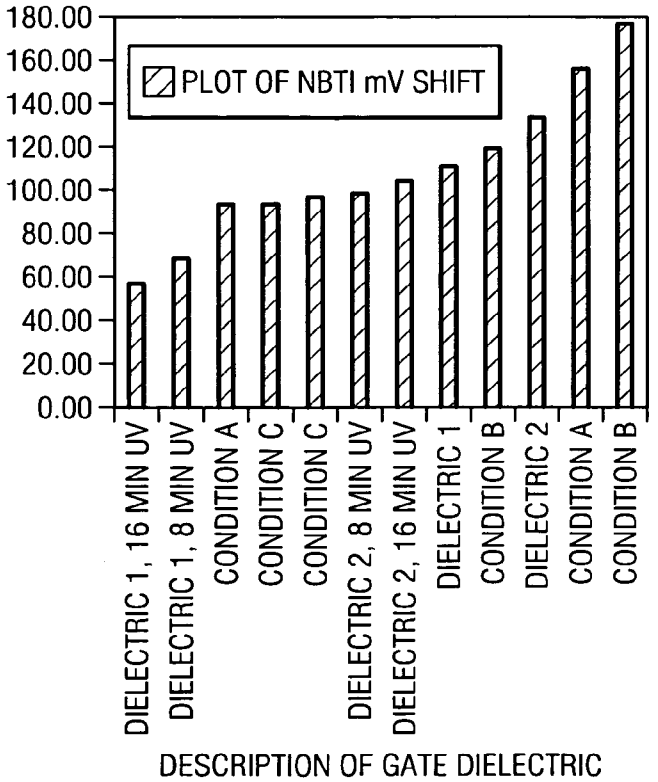


FIG. 7B

710

FIG. 8

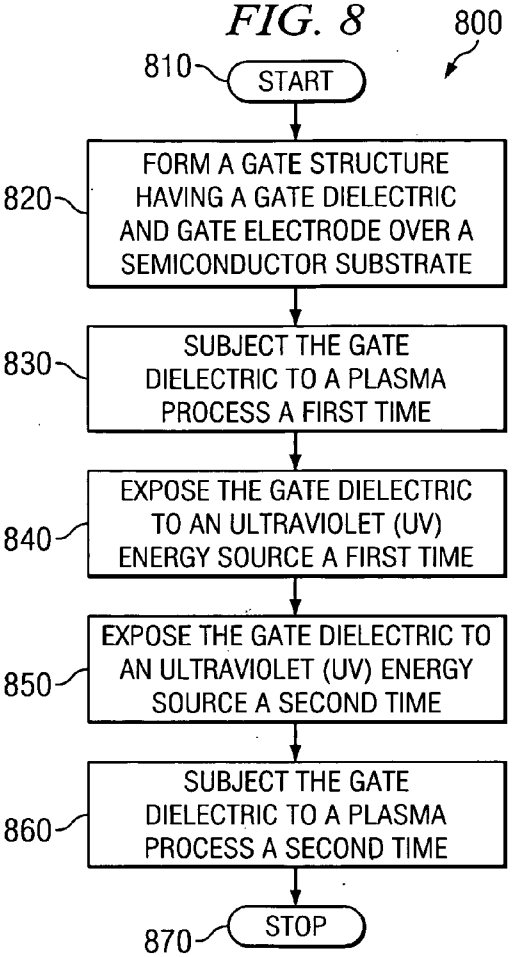
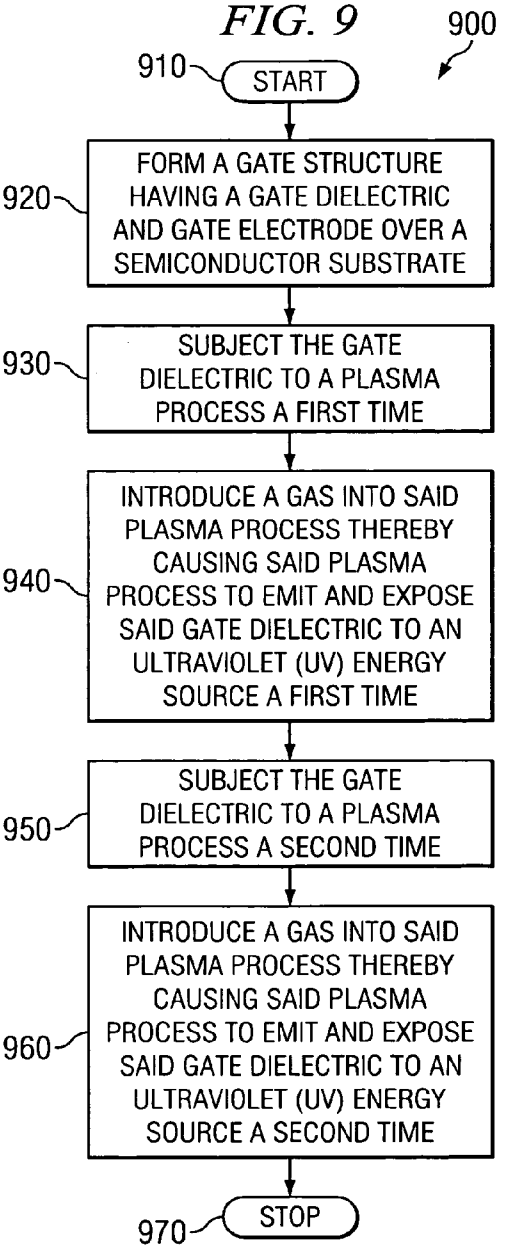

800
810
START
820
FORM A GATE STRUCTURE HAVING A GATE DIELECTRIC AND GATE ELECTRODE OVER A SEMICONDUCTOR SUBSTRATE
830
SUBJECT THE GATE DIELECTRIC TO A PLASMA PROCESS A FIRST TIME
840
EXPOSE THE GATE DIELECTRIC TO AN ULTRAVIOLET (UV) ENERGY SOURCE A FIRST TIME
850
EXPOSE THE GATE DIELECTRIC TO AN ULTRAVIOLET (UV) ENERGY SOURCE A SECOND TIME
860
SUBJECT THE GATE DIELECTRIC TO A PLASMA PROCESS A SECOND TIME
870
STOP

FIG. 9


900
910
START
920
FORM A GATE STRUCTURE HAVING A GATE DIELECTRIC AND GATE ELECTRODE OVER A SEMICONDUCTOR SUBSTRATE
930
SUBJECT THE GATE DIELECTRIC TO A PLASMA PROCESS A FIRST TIME
940
INTRODUCE A GAS INTO SAID PLASMA PROCESS THEREBY CAUSING SAID PLASMA PROCESS TO EMIT AND EXPOSE SAID GATE DIELECTRIC TO AN ULTRAVIOLET (UV) ENERGY SOURCE A FIRST TIME
950
SUBJECT THE GATE DIELECTRIC TO A PLASMA PROCESS A SECOND TIME
960
INTRODUCE A GAS INTO SAID PLASMA PROCESS THEREBY CAUSING SAID PLASMA PROCESS TO EMIT AND EXPOSE SAID GATE DIELECTRIC TO AN ULTRAVIOLET (UV) ENERGY SOURCE A SECOND TIME
970
STOP

METHOD FOR IMPROVING A PHYSICAL PROPERTY DEFECT VALUE OF A GATE DIELECTRIC

CROSS-REFERENCE TO PROVISIONAL APPLICATION

[0001] This application claims the benefit of U.S. Provisional Application No. 60/402,592 entitled "HEALING PLASMA DAMAGE USING ULTRA-VIOLET RADIATION," to Kirkpatrick, et al., filed on Aug. 9, 2002 and U.S. Provisional Application No. 60/406,839 entitled "HEALING PLASMA DAMAGE USING ULTRA-VIOLET RADIATION," to Kirkpatrick, et al., filed on Aug. 29, 2002, which are both commonly assigned with the present invention and incorporated herein by reference as if reproduced herein in their entirety.

TECHNICAL FIELD OF THE INVENTION

[0002] The present invention is directed, in general, to a method for manufacturing a substrate or an integrated circuit and, more specifically, to a method for improving a physical property defect value of a substrate in an integrated circuit, and an integrated circuit manufactured using the method.

BACKGROUND OF THE INVENTION

[0003] As the semiconductor industry continues to improve its process technologies, meeting circuit reliability metrics is becoming increasingly difficult. One circuit reliability metric that has experienced growing concern is that of the Gate Oxide Integrity (GOI).

[0004] GOI can be degraded by many factors. Currently, one of the most significant factors in degrading GOI is plasma damage to the gate dielectric. This plasma damage often results from any one of the numerous process steps that presently use plasma. For example, plasma processes can induce damage in the gate dielectrics, resulting in degradation of MOS characteristics due to a buildup of silicon-oxide interface states or oxide traps, or lead to early oxide breakdown. Since the number of process steps using plasma is increasing as the industry attempts to improve its process technologies, the degree to which the industry can control, limit or repair plasma damage, directly correlates to the ability to meet reliability requirements.

[0005] Currently there are two major approaches to reducing plasma damage in integrated circuits. The first approach includes eliminating plasma damage at its source by optimizing process and hardware parameters on the plasma tools. Unfortunately, the industry has optimized the process and hardware parameters about as much as it can. The other approach includes mitigating the severity of the plasma damage after it has already occurred by terminating the broken bonds using hydrogen or deuterium gas. Often this damage can likely reappear during the device's operating life, or show up during electrical or thermal stresses, which result in depassivation of the hydrogen. Another approach includes adding additional anneals to the manufacturing process. This approach, however, comes at the cost of additional thermal cycles and increased hydrogen concentration in the chips. Unfortunately, increased hydrogen concentrations have been linked to film delamination problems.

[0006] Accordingly, what is needed in the art is an integrated circuit or method of manufacturing an integrated circuit that does not experience the extent of plasma damage experienced in the prior art integrated circuits and methods of manufacture therefor.

SUMMARY OF THE INVENTION

[0007] To address the above-discussed deficiencies of the prior art, the present invention provides a method for improving a physical property of a substrate, a method for manufacturing an integrated circuit, and an integrated circuit manufactured using the aforementioned method. In one aspect of the invention, the method for improving a physical property of a substrate includes subjecting the substrate to effects of a plasma process, wherein the substrate has a physical property defect value associated therewith subsequent to the plasma process. The method further includes exposing the substrate to an ultraviolet (UV) energy source to improve the physical property defect value.

[0008] An alternative aspect of the present invention provides a method for manufacturing an integrated circuit. The method for manufacturing the integrated circuit includes forming a gate dielectric over a semiconductor substrate and then subjecting the gate dielectric to effects of a plasma process. In this instance, the gate dielectric has a physical property defect value associated therewith subsequent to the plasma process. Then, the gate dielectric is exposed to an ultraviolet (UV) energy source to improve the physical property defect value.

[0009] The present invention also provides an integrated circuit. The integrated circuit includes a semiconductor substrate having gate structures located thereover, as well as at least one plasma dielectric located over the semiconductor substrate, wherein the integrated circuit has a negative bias temperature instability (NBTI) shift of less than about 20% for a given operating voltage of 1.8 volts or less.

[0010] The foregoing has outlined preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] For a more complete understanding of the present invention, reference is now made to the following detailed description taken in conjunction with the accompanying FIGUREs. It is emphasized that various features may not be drawn to scale. In fact, the dimensions of various features may be arbitrarily increased or reduced for clarity of discussion. In addition, it is emphasized that some circuit components may not be illustrated for clarity of discussion. Reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0012] **FIG. 1** illustrates a table depicting binding energies for many of the common elements found within integrated circuits;

[0013] **FIG. 2** illustrates a graph depicting the benefits that may be obtained by exposing the gate dielectric to a UV energy source to improve the physical property defect value in accordance with the principles of the present invention;

[0014] **FIG. 3** illustrates a graph comparing measured leakage current values at different frequencies for a baseline wafer, a control wafer and a wafer exposed to the UV energy source;

[0015] **FIG. 4** illustrates a graph comparing measured leakage current values at different frequencies for a baseline wafer, a control wafer and a wafer exposed to the UV energy source, two of which are taken through a 650 Å USG liner plasma deposited as interlevel dielectric layers **4**, **5**, and **6**;

[0016] **FIG. 5** illustrates a graph comparing measured leakage current values at different frequencies for a baseline wafer, a control wafer and a wafer exposed to the UV energy source, two of which are taken through a 650 Å PETEOS liner plasma deposited as interlevel dielectric layers **4**, **5**, and **6**;

[0017] **FIG. 6** illustrates a table illustrating the GOI level benefits that may be obtained by exposing the gate dielectric to the UV energy source;

[0018] **FIG. 7** illustrates a graph and a table illustrating the NBTI level benefits that may be obtained by exposing the gate dielectric to the UV energy source in accordance with the principles of the present invention;

[0019] **FIG. 8** illustrates a flow diagram illustrating one method by which a physical property of a gate dielectric, and more specifically a physical property defect value of a gate dielectric may be improved;

[0020] **FIG. 9** illustrates a flow diagram illustrating an alternative method by which a physical property of a gate dielectric, and more specifically a physical property defect value of a gate dielectric may be improved; and

[0021] **FIG. 10** illustrates a cross-sectional view of an integrated circuit that might be manufactured according to the principles of the present invention.

DETAILED DESCRIPTION

[0022] The present invention addresses the need for accurately and consistently attaining the desired circuit reliability metrics required by today's integrated circuits. As discussed in the background of the invention above, plasma damage induced by any of the plasma processes used in the fabrication of integrated circuits currently has a major impact on the aforementioned circuit reliability metrics. In addition to the plasma damage having a degrading effect on an integrated circuit's Gate Oxide Integrity (GOI) value, it is also believed that the plasma damage has a degrading effect on the integrated circuit's antenna gate leakage value, threshold voltage drift value and the V_{min} value (i.e., the minimum voltage, with maximum frequency, at which the address circuit functions correctly). Additionally, it is theorized that the plasma damage has a degrading effect on the integrated circuit's negative bias temperature instability (NBTI) value.

[0023] In contrast to that previously known by those skilled in the art, the present invention encompasses the recognition that an ultraviolet (UV) energy source may be used to fix, patch or heal at least a portion of the damage caused by the aforementioned plasma process. Particularly, the present invention is focused on the previously unrecognized fact that the UV energy source may improve the affected integrated circuit's reliability metrics, or in other words physical property defect values, including its NBTI, GOI, antenna gate leakage, threshold voltage shift and V_{min} values.

[0024] The mechanism by which the UV energy source improves the NBTI, GOI, antenna gate leakage, threshold voltage shift and V_{min} values is not fully known. It is theorized that the UV energy source provides the additional energy required to locally excite the electrons proximate the dangling bonds and/or silicon-hydrogen bonds in the gate dielectric material of the integrated circuit. It is believed that once the electrons are sufficiently excited, the electrons will lower their energy by either cascade discharging to a stable energy state or by reestablishing covalent bonds with the surrounding atoms that were previously broken by the plasma damage.

[0025] Turning briefly to **FIG. 1**, illustrated is a table **100** depicting binding energies for many of the common elements found within integrated circuits. As those skilled in the art are aware, the binding energies are quoted relative to the vacuum level for rare gases and H_2, N_2, O_2, F_2, and Cl_2 molecules, relative to the Fermi level for metals, and relative to the top of the valence band for semiconductors. As discussed above, and supported by the table **100**, hydrogen is of concern because its low bond energy allows the bond to break when the integrated circuit is placed under stress. For example, comparing the outer orbital binding energies for hydrogen to the outer orbital binding energies of other favorable elements, such as nitrogen, oxygen and silicon, it is apparent that hydrogen is the weakest of the bonds.

[0026] Accordingly, if one were able to break the silicon-hydrogen bonds, and replace those bonds with stronger silicon-nitrogen, silicon-oxygen or silicon-silicon bonds, for example using the UV energy source, the integrated circuit's NBTI, GOI, antenna gate leakage, threshold voltage shift and V_{min} values should improve. Unfortunately, until now no methodology existed for replacing the weaker bonds with stronger bonds without causing other undesirable effects.

[0027] Turning now to **FIG. 2**, illustrated is a graph **200** depicting the benefits that may be obtained by exposing a gate dielectric to a UV energy source to improve the physical property defect value in accordance with the principles of the present invention. The graph **200** of **FIG. 2** plots the various leakage current values for a number of wafers, including certain wafers that have undergone the exposure to the UV energy source as well as certain wafers that have not. Notice the tighter distribution of leakage current values for those wafers that have undergone the exposure to the UV energy source.

[0028] Turning now to **FIG. 3**, illustrated is a graph **300** comparing measured leakage current values at different frequencies for a baseline wafer **310**, a control wafer **320** and a wafer exposed to the UV energy source **330**. The baseline wafer **310** is a standard wafer not having been subjected to the UV energy source. Similarly, the control wafer **320** is a wafer not having been subjected to the UV energy source and that has endured the same handling as the wafer exposed to the UV energy source **330**. Notice how the wafer exposed to the UV energy source **330** shows a tighter

distribution of sites with low leakage, which corresponds to less damage to the gate dielectric, than both the baseline wafer **310** and control wafer **320**.

[**0029**] Turning now to **FIG. 4**, illustrated is a graph **400** comparing measured leakage current values at different frequencies for a non UV treated wafer **410** and a wafer exposed to the UV energy source **420**. These measurements were taken after a 650 Å USG liner was plasma deposited as interlevel dielectric layers **4**, **5**, and **6**. Notice how the wafer exposed to the UV energy source **420** shows reduced leakage as compared to the non UV treated wafer **410**, indicating some level of repair.

[**0030**] Turning now to **FIG. 5**, illustrated is a graph **500** comparing measured leakage current values at different frequencies for a non UV treated wafer **510** and a wafer exposed to the UV energy source **520**. These measurements were taken after a **650**Å PETEOS liner was plasma deposited as interlevel dielectric layers **4**, **5**, and **6**. The wafer exposed to the UV energy source **520** shows dramatically reduced leakage as compared to the non UV treated wafer **510**, indicating a substantial level of repair. Thus, a substantial portion, if not all, of the damage caused by the plasma processes was repaired.

[**0031**] Turning now to **FIG. 6**, illustrated is a table **600** illustrating the GOI level benefits that may be obtained by exposing the gate dielectric to the UV energy source. Table **600** compares wafers pre and post UV exposure over a number of different exposure conditions. For example, the exposure conditions include 50° C. and 4 minutes, 50° C. and 8 minutes, 240° C. and 4 minutes, and 240° C. and 8 minutes. What results are ramped voltage breakdown values from the wafer averages. A positive average delta (Average Delta) indicates an improvement in GOI, and a negative Standard Deviation (Std Dev Delta) indicates an improvement in distribution. Notice that in almost all instances the wafers experienced improved GOI and distribution values. Again, table **600** further supports the idea that exposing a gate dielectric to a UV energy source improves the gate dielectric's physical property defect values.

[**0032**] Turning now to **FIG. 7**, illustrated is a graph **710** and a table **720** illustrating the NBTI level benefits that may be obtained by exposing the gate dielectric to the UV energy source in accordance with the principles of the present invention. As is illustrated, table **720** compares two dielectrics' (dielectric **1** and dielectric **2**) NBTI values for two different UV exposure times. Notice the elevated NBTI values for those examples not having experienced the UV exposure. In comparison, however, the NBTI values decrease dramatically with UV exposure. For example, in dielectric **1** the shift in NBTI is reduced by about 50% after only 16 minutes of UV exposure. Similarly, in dielectric **2** the shift in NBTI is reduced by about 25% after only 8 minutes of UV exposure. It is believed that the difference in improvement between dielectric **1** and dielectric **2** is a function of the method used to form the gate dielectric. Graph **710** and table **720**, again, establish one of the many benefits that may be achieved by using a UV treatment in accordance with the principles of the present invention.

[**0033**] Turning now to **FIG. 8**, illustrated is a flow diagram **800** illustrating one method by which a physical property of a gate dielectric, and more specifically a physical property defect value of a gate dielectric may be improved. The flow diagram **800** begins in a start step **810**. Thereafter, in a step **820**, at least one gate structure having a gate dielectric and a gate electrode is formed over a semiconductor substrate. Often, at this stage of the manufacturing process the gate dielectric has very few, if any, undesirable dangling bonds or silicon-hydrogen bonds.

[**0034**] Thereafter, in a step **830**, as is often the case, the gate dielectric is subjected to one or more plasma processes. As discussed above, this plasma process, which may be any plasma process used in the manufacture of integrated circuits, including any plasma deposition or etch process, often causes plasma damage in the gate dielectric. More often than not the plasma damage is located proximate the interface between the gate dielectric and the semiconductor substrate.

[**0035**] The plasma damage may show up in the form of dangling bonds, or if passivated with hydrogen, may show up in the form of weak silicon-hydrogen bonds. Unfortunately, neither the dangling bonds nor the weak silicon-hydrogen bonds are desired in today's integrated circuits, as they cause the gate dielectric to have a sub-par physical property defect value. In other words, the plasma damage causes the gate dielectric's circuit reliability metrics, such as NBTI, GOI, antenna gate leakage, threshold voltage shift and V_{min} values to degrade.

[**0036**] Accordingly, in a step **840**, the gate dielectric is exposed to a UV energy source. Unbeknownst to those skilled in the art, and as established above, the UV energy source improves the physical property defect value of the gate dielectric. The UV energy source may be supplied by a number of different techniques, however, in one particularly advantageous embodiment the UV energy source is supplied by a UV bulb. For example, commercially available equipment built for FLASH EEPROM erasure or UV light stabilization of photoresist, each having a UV bulb, could be used to expose the gate dielectric. One known FLASH EEPROM erasure tool may be purchased from Axcelis Technologies, located at 55 Cherry Hill Drive, Beverly, Mass. 01915-1053.

[**0037**] Certain embodiments of the present invention have the UV energy source supplying individual wavelengths ranging from about 138 nm to about 400 nm, and more specifically 190 nm and about 400 nm. These wavelengths are particularly advantageous because they provide superior physical property defect values with minimal damage to the gate dielectric than other wavelengths within the broad UV range. Other embodiments of the invention, however, have the UV energy source supplying a broad spectrum of wavelengths ranging from about 190 nm to about 400 nm. In one advantageous embodiment, the broad spectrum of wavelengths ranging from about 190 nm to about 240 nm provides over about 50% of an energy supplied by the aforementioned broad spectrum. While certain wavelength values for the UV energy source have been listed, other UV wavelength values are equally applicable.

[**0038**] The gate dielectric may also be exposed to the UV energy source for a wide range of different time periods. For example, it is believed that time periods ranging from about 2 minutes to about 20 minutes are sufficient to see dramatic improvements in the physical property defect values discussed above. It is further believed, however, that the narrower time period ranging from about 8 minutes to about 16 minutes provides equally impressive results. While an

optimum time period may exist, that time period would most likely be tailored to the-amount of plasma damage, the number of layers of material the UV energy source must penetrate, and so on.

[0039] Similarly, the gate dielectric material may be positioned within a heated environment while it is exposed to the UV energy source. The heated environment generally allows the time period upon which the gate dielectric is exposed to the UV energy source to be reduced. For example, it has been observed that temperatures ranging from about 50° C. to about 400° C., and more particularly, temperatures ranging from about 180° C. to about 400° C., are helpful in reducing the exposure time.

[0040] After exposing the gate dielectric to the UV energy source, and in an optional step **850**, the gate dielectric may be subjected to a plasma process a second time. Thereafter, in an optional step **860**, the gate dielectric might be exposed to the UV energy source a second time to correct any damage caused by the optional step **850**, or any untreated damage from prior processes. The theory is that the process flow for manufacturing an integrated circuit often includes a number of plasma processes, each having a negative impact on the physical property defect values thereof. Accordingly, multiple exposure steps may be required to correct the plasma damage. It can be envisioned where up to about 10 UV exposure steps, and more likely from about 2 to about 6 exposure steps, might be required or desired to correct the damage caused by the plasma processes.

[0041] It can be envisioned where the UV exposure occurs through a number of different layers formed over the gate dielectric. For example, it can be envisioned where the final exposure occurs after the integrated circuit device is almost complete. This does not pose a problem for the present invention as the UV energy is capable of penetrating or diffracting around all of these layers and still contacting the gate dielectric.

[0042] Sometime after the final exposure step has been completed, the process ends in a stop step **870**. While only seven steps were disclosed in the aforementioned flow diagram **800**, those skilled in the art understand that a number of other steps could, and most probably would, be interposed between any of the listed steps.

[0043] The advantages of using the present invention are almost limitless. First, the UV exposure process of the present invention can be performed at any point in the process flow. Further, it does not result in increased levels of hydrogen. Similarly, it does not result in the addition of added thermal cycles that would result in dopant redistribution. Also, it does not significantly increase the thermal stress, which limits the possibilities for film delamination or copper migration.

[0044] Turning now to **FIG. 9**, illustrated is a flow diagram **900** illustrating an alternative method by which a physical property of a gate dielectric, and more specifically a physical property defect value of a gate dielectric may be improved. The flow diagram **900** begins in a start step **910**. Thereafter, in a step **920**, at least one gate structure having a gate dielectric and a gate electrode is formed over a semiconductor substrate.

[0045] Thereafter, in a step **930**, as is often the case, the gate dielectric is subjected to one or more plasma processes. As discussed above, this plasma process, which may be any plasma process used in the manufacture of integrated circuits, often causes plasma damage in the gate dielectric. To correct this damage, and in a step **940**, a gas is introduced into the plasma process thereby causing the plasma process to emit an ultraviolet (UV) energy source. The ultraviolet energy source, as disclosed above, then improves the physical property defect value of the gate dielectric. The gas, which may include gases such as helium, neon, argon, krypton, xenon, and other similar gasses, preferably produces wavelengths ranging from about 138 nm to about 400 nm.

[0046] After exposing the gate dielectric to the UV energy source, and in an optional step **950**, the gate dielectric may be subjected to a plasma process a second time. Thereafter, in an optional step **960**, the gas may be introduced into the second plasma process, again causing the plasma process to emit an ultraviolet (UV) energy source. This process could then terminate with a stop step **970**.

[0047] Some advantages of this embodiment of the invention include the ability to expose the gate dielectric to the UV energy source without removing it from the plasma process chamber. Additionally, it allows companies to use their existing plasma processing equipment to expose their wafers to the desired W energy source. This alone, is a large cost savings over the other embodiment discussed with respect to **FIG. 8**.

[0048] While **FIGS. 8 and 9** illustrate two different processes for providing the UV energy source, those skilled in the art understand that such processes may be combined, and stay within the scope of the present invention. For example, those skilled in the art understand that a UV bulb could be placed within the plasma chamber, thus allowing the combination of the UV bulb and the gas introduced within the plasma chamber to provide the UV energy source. Such a combination could be very useful.

[0049] Turning now to **FIG. 10**, illustrated is a cross-sectional view of an integrated circuit **1000** that might be manufactured according to the principles of the present invention. The integrated circuit **1000** of **FIG. 10** includes a number of gate structures **1020**, each having a gate oxide **1030** and gate electrode **1035**, located over a substrate **1010**. As shown, field oxide structures **1040** may be located along the surface of the substrate **1010**, electrically isolating the various gate structures **1020** from one another. Also shown in **FIG. 10** are interconnect structures **1050** located in dielectric layers **1060**, wherein the interconnect structures **1050** connect the gate structures **1020** to other areas of the integrated circuit **1000** creating an operative integrated circuit. At least one layer included within the integrated circuit **1000** must be a plasma dielectric. That is, at least one layer within the integrated circuit must be a dielectric layer formed using a plasma process. In the embodiment shown in **FIG. 10**, one of the dielectric layers **1060** is a plasma dielectric layer. For example, some known examples of plasma dielectric layers include fluorosilicate glass (FSG), organosilicate glass (OSG), phosphosilicate glass (PSG), undopedsilicate glass (USG), PETEOS, PENitride, and others.

[0050] In direct contrast to the prior art structures, however, the integrated circuit **1000** has a negative bias temperature instability (NBTI) shift of less than about 20% for

a given operating voltage of 1.8 volts or less. Similarly, in one exemplary embodiment, the integrated circuit **1000** has a negative bias temperature instability (NBTI) shift of less than about 10% for the given operating voltage of 1.8 volts or less. In another exemplary embodiment, however, the integrated circuit has a negative bias temperature instability (NBTI) shift of less than about 10% for a given operating voltage of 1.5 volts or less.

[**0051**] Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.

1-30. (canceled)

31. An integrated circuit, comprising:

a semiconductor substrate having gate structures located thereover; and

at least one plasma dielectric layer located over said semiconductor substrate, wherein said integrated circuit has a negative bias temperature instability (NBTI) shift of less than about 20% for a given operating voltage of 1.8 volts or less.

32. The integrated circuit as recited in claim 31 wherein said integrated circuit has a negative bias temperature instability (NBTI) shift of less than about 10% for a given operating voltage of 1.8 volts or less.

33. The integrated circuit as recited in claim 32 wherein said integrated circuit has a negative bias temperature instability (NBTI) shift of less than about 10% for a given operating voltage of 1.5 volts or less.

34. The integrated circuit as recited in claim **30** wherein said at least one plasma dielectric layer comprises a material selected from the group of materials consisting of:

fluorosilicate glass (FSG),

organosilicate glass (OSG),

phosphosilicate glass (PSG),

undopedsilicate glass (USG),

PETEOS, and

PENitride.

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