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(54) **BARRIER PROCESS/STRUCTURE FOR TRANSISTOR TRENCH CONTACT APPLICATIONS**

(76) Inventors: **Vinay Chikarmane**, Portland, OR (US); **Kevin Fischer**, Hillsboro, OR (US); **Brennan Peterson**, Portland, OR (US)

Correspondence Address:
LEE & HAYES, PLLC
c/o Intellevate, LLC
P.O. BOX 52050
MINNEAPOLIS, MN 55402 (US)

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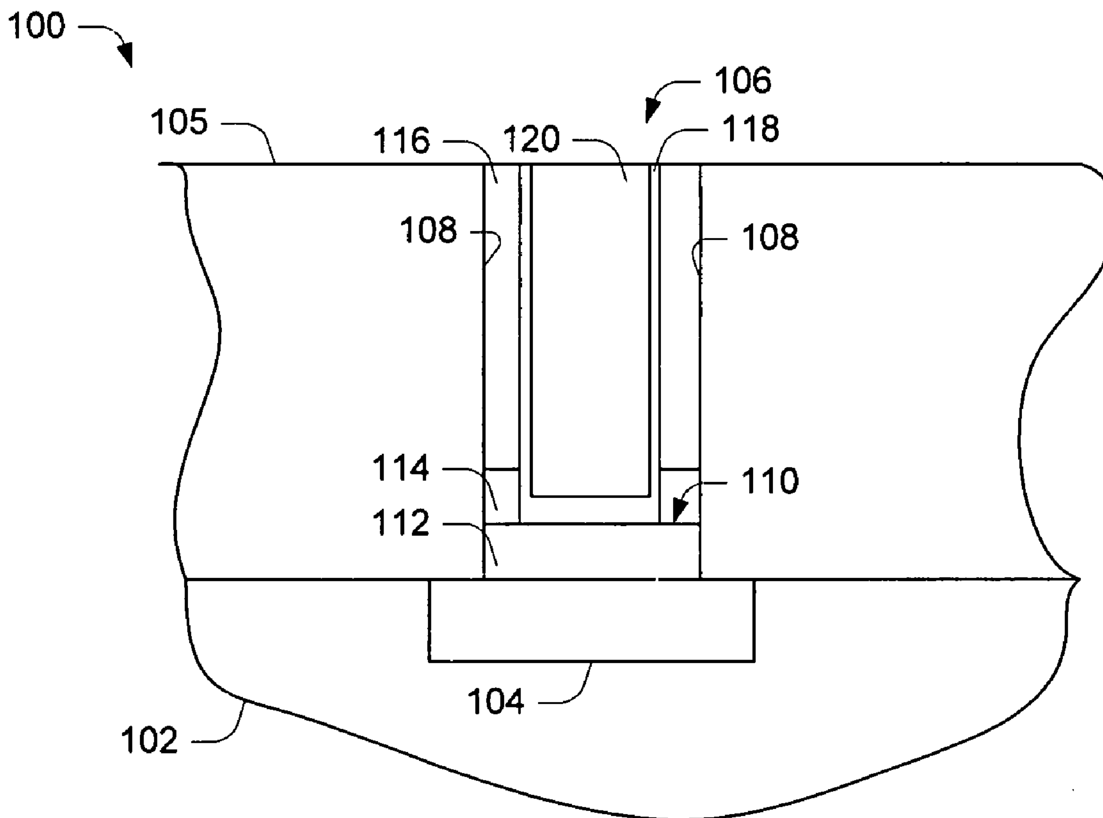
(57) **ABSTRACT**

A barrier architecture is provided that includes different materials that are selected to be employed in connection with copper contact applications. Some of the barrier material is formed over trench contact sidewalls, and other different barrier material is formed over trench contact bottoms. By selecting the appropriate barrier materials, electromigration can be improved while, at the same time, interconnect and contact resistances can be kept low and array leakage can be mitigated.



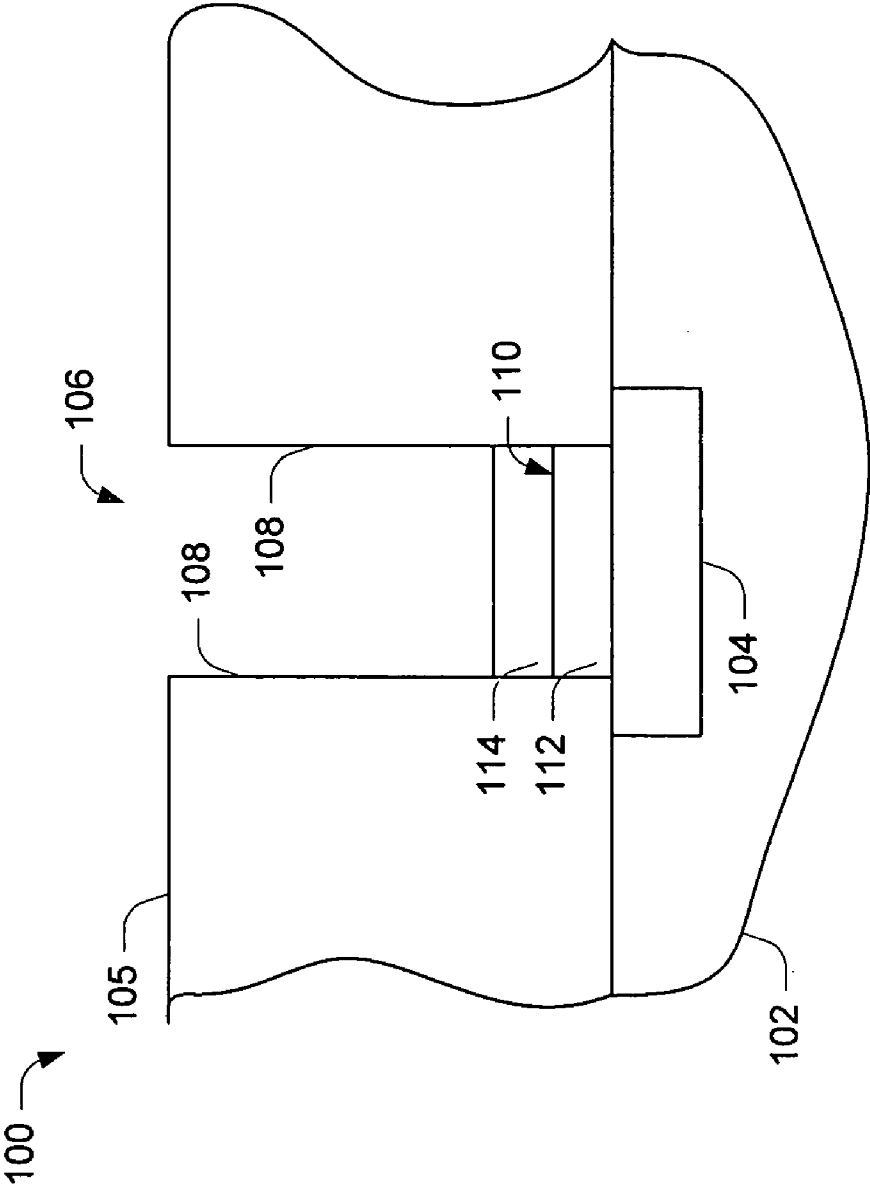


Fig. 1

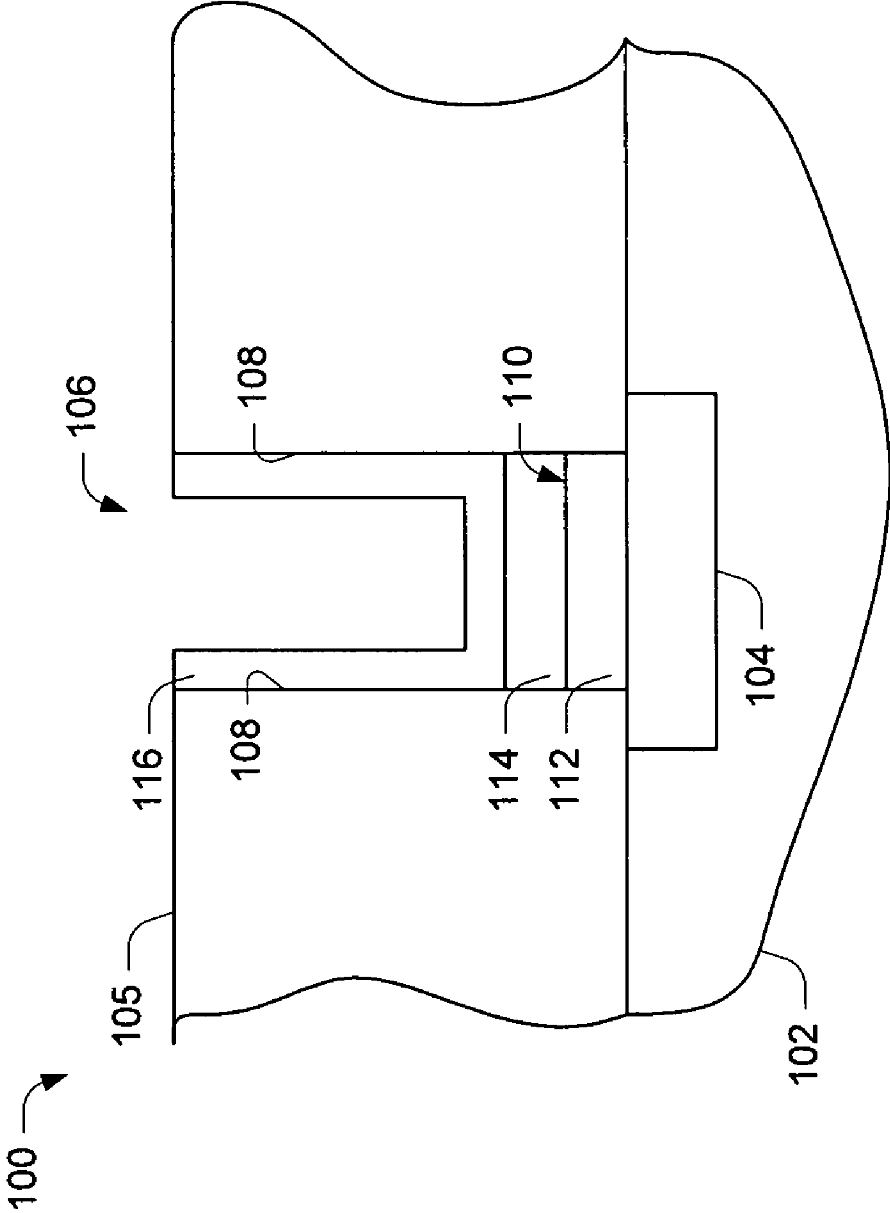


Fig. 2

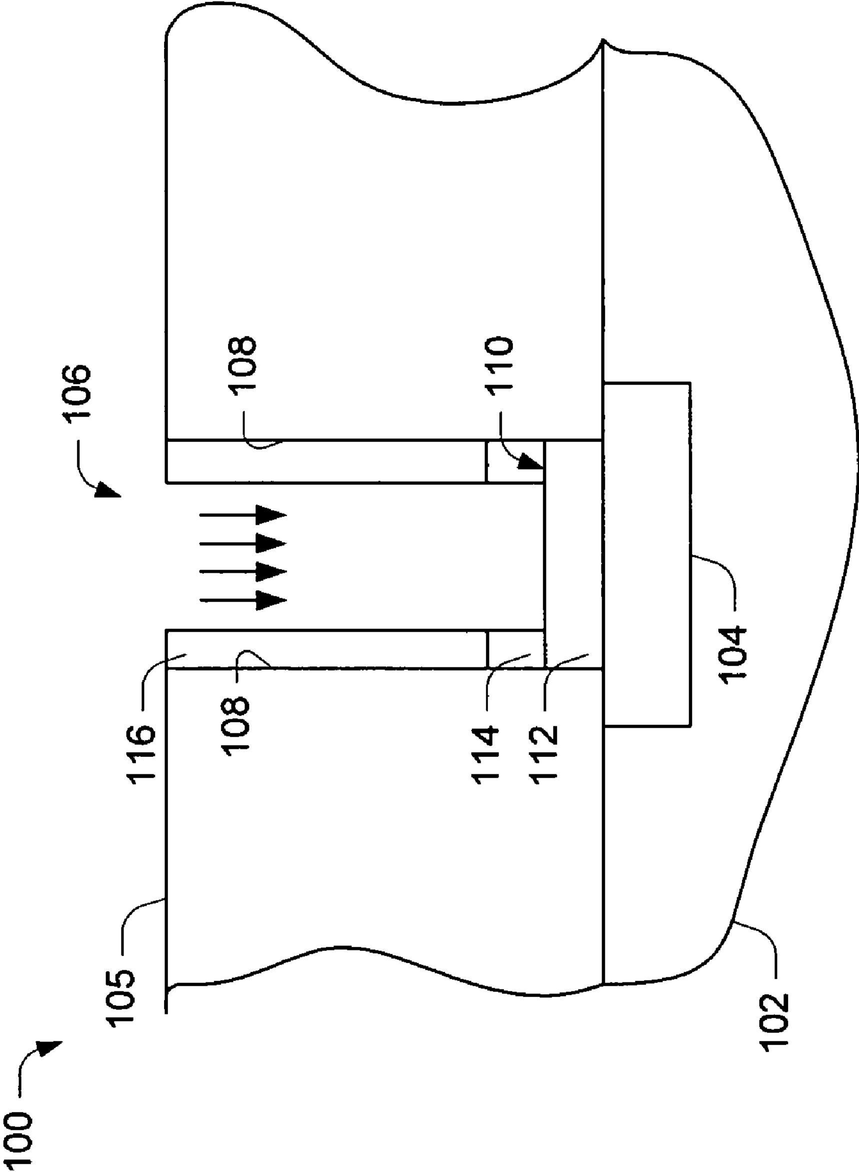


Fig. 3

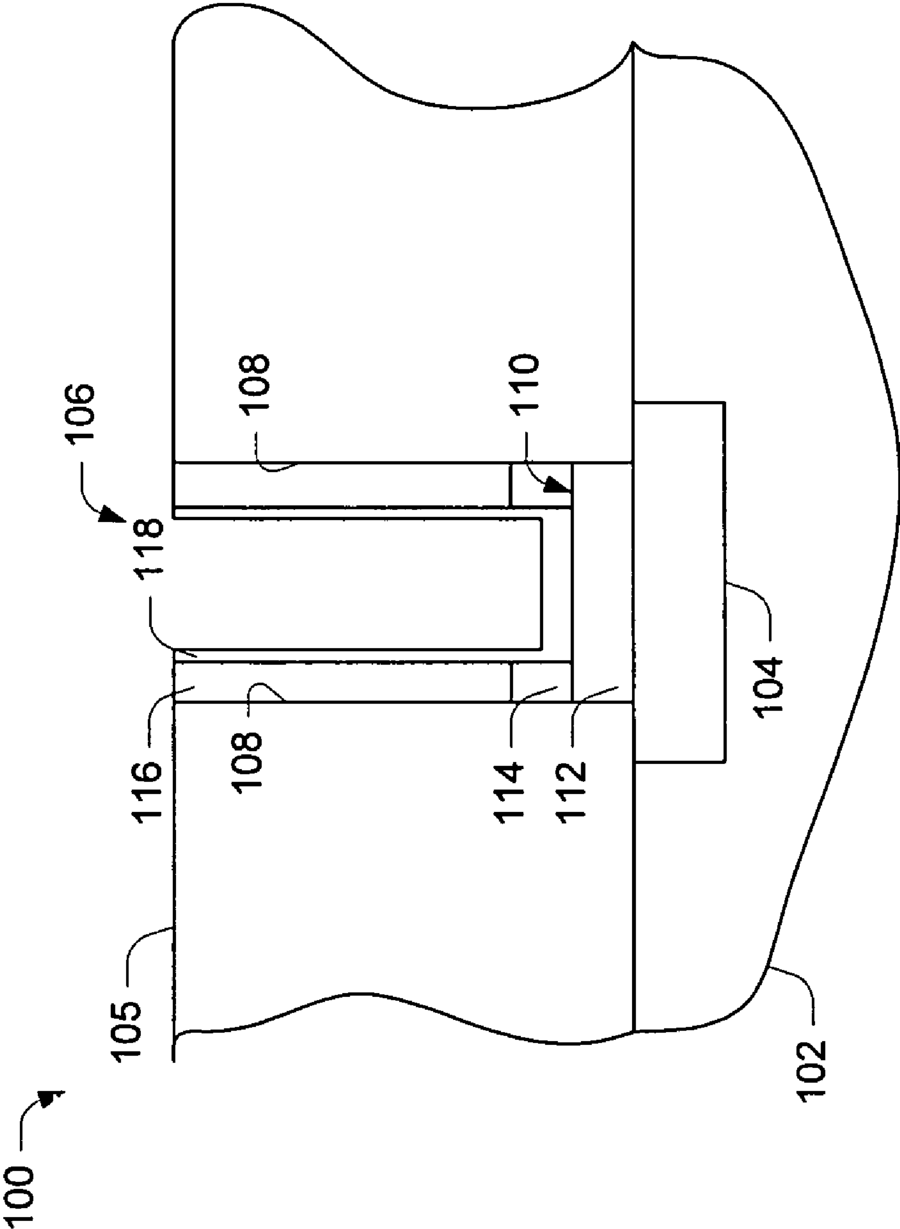


Fig. 4

100
105
102
106
118
108
110
120
116
108
114
112
104

Fig. 5

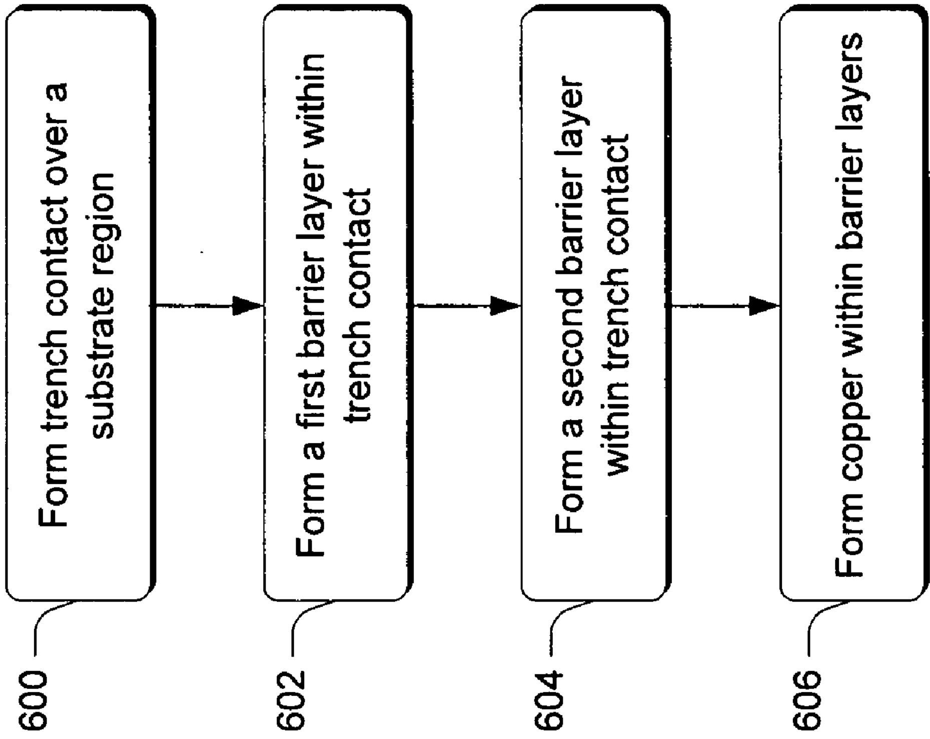


Fig. 6

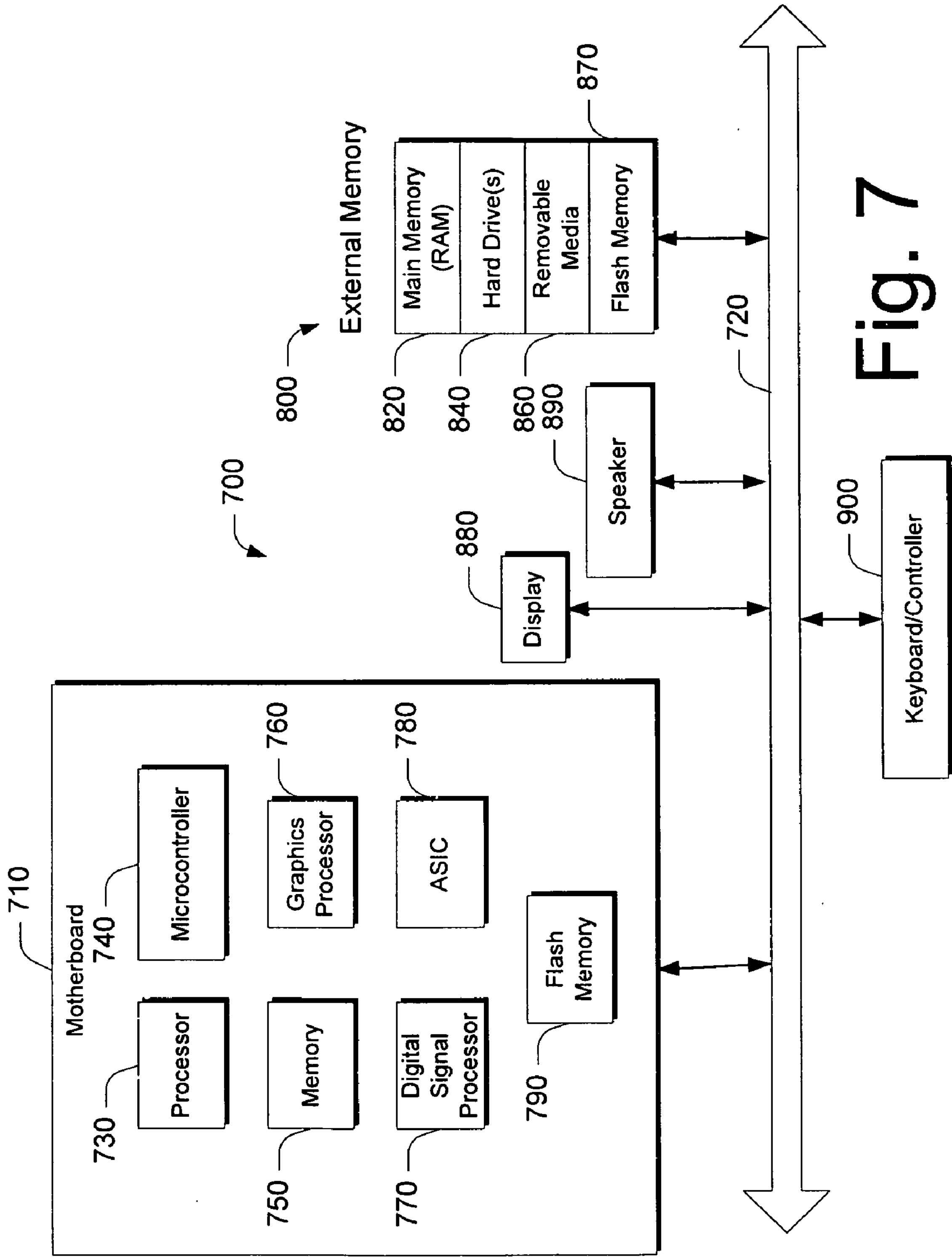


Fig. 7

BARRIER PROCESS/STRUCTURE FOR TRANSISTOR TRENCH CONTACT APPLICATIONS

[0001] This application is a divisional of prior pending U.S. patent application Ser. No. 11/496,291 filed on Jul. 31, 2006, which is herein incorporated by reference in its entirety, and priority is claimed to this application. Any disclaimer that may have occurred during the prosecution of the above-referenced application is hereby expressly rescinded, and reconsideration of all relevant art is respectfully requested.

BACKGROUND

[0002] Using copper for interconnections for transistor source/drain and gate regions can present some design challenges. For example, copper that is formed within typical trench contacts should be well contained to avoid issues associated with what is known as array leakage. Array leakage occurs when the copper within the trench contact leaks into or extrudes into underlying substrate regions. This can and typically does compromise a device.

[0003] One way to contain the copper is to provide a barrier layer within the trench contact. Typically, a common approach is to form a relatively strong barrier having a metallurgical consistency that is the same along both the sidewalls and the bottom of the trench contact. This, however, is not the best approach as it can lead to compromise of the line and contact resistances. That is, in the interest of having a robust barrier to address array leakage, line and contact resistances can be compromised.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. **1** is a diagrammatic side sectional view of a semiconductive substrate in process in accordance with one embodiment.

[0005] FIG. **2** is a diagrammatic side sectional view of the FIG. **1** substrate at a processing step subsequent to that shown in FIG. **1**, in accordance with one embodiment.

[0006] FIG. **3** is a diagrammatic side sectional view of the FIG. **2** substrate at a processing step subsequent to that shown in FIG. **2**, in accordance with one embodiment.

[0007] FIG. **4** is a diagrammatic side sectional view of the FIG. **3** substrate at a processing step subsequent to that shown in FIG. **3**, in accordance with one embodiment.

[0008] FIG. **5** is a diagrammatic side sectional view of the FIG. **4** substrate at a processing step subsequent to that shown in FIG. **4**, in accordance with one embodiment.

[0009] FIG. **6** is a flow diagram that illustrates acts in accordance with one embodiment.

[0010] FIG. **7** is a diagram that illustrates an exemplary system in which transistors formed in accordance with the embodiments described herein can be used, in accordance with one embodiment.

DETAILED DESCRIPTION

[0011] In the embodiments described below, a barrier is formed within a trench contact and contains copper that makes an electrical connection with a desired substrate region. In the illustrated and described embodiments, the barrier's metallurgical consistency is different over the trench contact's sidewalls from its metallurgical consistency over the bottom of the trench contact.

[0012] In at least some embodiments, the barrier is formed by first forming a first barrier layer within the trench contact and over the sidewalls and bottom of the contact. First barrier layer material is then removed from over the contact bottom and then a second barrier layer, different from the first barrier layer, is formed over the contact sidewalls and the substrate region with which electrical connection is desired. Following this, copper is formed within the trench contact to be in electrical communication with the desired substrate region. The desired substrate region can comprise any suitable region such as a source region, drain region, gate region and the like.

[0013] In the discussion that follows, a specific implementation example is provided under the heading "Implementation Example". It is to be appreciated and understood that such implementation example is not to be used to limit application of the claimed subject matter to only this example. Rather, changes and modifications can be made without departing from the spirit and scope of the claimed subject matter.

Implementation Example

[0014] Referring to FIG. **1**, a semiconductive substrate in process is shown generally at **100**. Substrate **100** can comprise any suitable substrate material and can have any suitable number of layers through which one or more trench contacts, as described below, can be formed. In this particular example, substrate **100** comprises a bulk monocrystalline silicon substrate **102** having a region **104** with which electrical connection is desired. As noted above, substrate region **104** can comprise any suitable region with which electrical connection is desired. Such regions can include, by way of example and not limitation, source regions, drain regions, gate regions and the like.

[0015] In the illustrated and described embodiment, an insulative material **105** is formed over the substrate and a trench contact **106** is formed in the insulative material. Any suitable material can be utilized as insulative material, with SiO_2 serving as but one non-limiting example. In addition, the trench contact can be formed using any suitable technique, such as a masked etch.

[0016] In this particular example, trench contact **106** is defined by a pair of sidewalls **108** which extend toward the substrate and terminate at or adjacent a contact bottom **110**. In this particular example, contact bottom **110** is defined by the upper surface of a salicide layer **112**, which is in electrical communication with substrate region **104**. In addition, in this particular example, salicide layer **112** is overlaid by an oxide layer **114**. It is to be appreciated and understood that the contact bottom can be defined by other materials, such as the upper surface of region **104**.

[0017] Referring to FIG. **2**, a first barrier layer **116** is formed within trench contact **106**. Layer **116** is designed to meet electromigration requirements while maintain a low RC to aid in transistor switching speed. As formed, the first barrier layer overlays sidewalls **108** and the bottom of the trench contact. Any suitable technique can be utilized to form first barrier layer **116**. In one embodiment, layer **116** is deposited using a high bias resputter process. Any suitable materials can be utilized for layer **116**. In at least some embodiments, layer **116** comprises a metal and/or a nitrogen-containing material, such as any suitable metal nitride, such as tantalum nitride, titanium nitride and the like.

[0018] Referring to FIG. **3**, material from over contact bottom **110** is removed to expose the contact bottom. Any suit-

able technique can be used to remove the material overlying the contact bottom. In this particular example, a sputter etch is employed to remove not only material of layer **116** that overlays the contact bottom, but also material of the oxide layer **114** that overlays the contact bottom. In at least some embodiments, the sputter etch is an Argon sputter etch. In this particular example, material of layer **116** that is not removed serves as a hardmask for underlying material. By serving as a hardmask, the material of layer **116** can reduce or eliminate feature flaring, as will be appreciated by the skilled artisan.

[0019] Referring to FIG. **4**, a second barrier layer **118** is formed within trench contact **106** and over contact bottom **110**. In this particular example, layer **118** is formed over first barrier layer **116**. In the illustrated and described embodiment, layer **118** is deposited using a low bias resputter ratio which effectively provides a desired thickness over the contact bottom **110**. Additionally, the low bias resputter process reduces the thickness of layer **118** over sidewalls **108**, as compared with the layer's thickness over contact bottom **110**. In one embodiment, the thickness of layer **118** over the sidewall is about 15% of the thickness of the layer over the contact bottom. Layer **118** is designed to provide low contact resistance to the contact to achieve high drive currents and block array leakage.

[0020] In the illustrated and described embodiment, the metallurgical consistency of layer **118** is different from the metallurgical consistency of layer **116**. In at least some embodiments, layer **118** is formed from a metal material examples of which include, by way of example and not limitation, tantalum, titanium and the like. In addition, the metallurgy and thickness of layer **118** can be selected to achieve a desirably low contact resistance while, at the same time, contain copper that is to be formed in the trench contact.

[0021] Referring to FIG. **5**, copper **120** is formed in trench contact **106** and in electrical communication with substrate region **104**. Any suitable technique can be utilized to provide copper into the trench contact.

[0022] As formed, the barrier that contains the copper comprises a first material that is formed adjacent the sidewalls **108** of trench contact **106**. The material that is selected for use in this layer can be selected with an appreciation of the materials that it is to separate which, in this example, comprise SiO_2 and copper. In other embodiments where such materials are different from those described above, the material selected for the first material may be different from those described above.

[0023] In addition, the barrier that contains the copper comprises a second material that is different from the first material and which is formed over the contact bottom **110** of trench contact **106**. The material that is selected for use in this layer can be selected with an appreciation of the materials that it is to separate which, in this example, comprise silicon or a silicon-containing contact material and copper. In other embodiments where such materials are different from those described above, the material selected for the second material may be different from those described above.

[0024] Further, in the specific example illustrated above, the barrier comprises multiple different layers that are formed at different times. Each of the layers is formed to overlie portions of the trench contact sidewalls and contact bottom. It is possible, however, to have a barrier architecture that is different from that specifically described above without departing from the spirit and scope of the claimed subject matter. For example, some barrier architectures might be designed to provide only a negligible amount of layer **118** material, if any, over the sidewalls of the trench contact.

[0025] Exemplary Method

[0026] FIG. **6** is a flow diagram that illustrates acts in a process in accordance with one embodiment. Act **600** forms one or more trench contacts over a substrate region with which electrical connection is desired. Any suitable techniques can be utilized to form the trench contact(s). Act **602** forms a first barrier layer within the trench contact. Any suitable techniques can be utilized to form the first barrier layer, non-limiting examples of which are given above. Act **604** forms a second barrier layer within the trench contact(s). Any suitable techniques can be utilized to form the second barrier layer, non-limiting examples of which are given above. Act **606** forms copper within the barrier layers and in electrical contact with the substrate region. Any suitable techniques can be utilized to form the second barrier layer, non-limiting examples of which are given above.

[0027] Exemplary System

[0028] Referring to FIG. **7**, a block diagram of an exemplary electronic system that can include transistors fabricated with copper interconnects, such as those described above is shown generally at **700**. Such electronic system can comprise a computer system that includes a motherboard **710** which is electrically coupled to various components in electronic system **700** via a system bus **720**. System bus **720** may be a single bus or any combination of busses.

[0029] Motherboard **710** can include, among other components, one or more processors **730**, a microcontroller **740**, memory **750**, a graphics processor **760** or a digital signal processor **770**, and/or a custom circuit or an application-specific integrated circuit **780**, such as a communications circuit for use in wireless devices such as cellular telephones, pagers, portable computers, two-way radios, and similar electronic systems and a flash memory device **790**.

[0030] The electronic system **700** may also include an external memory **800** that in turn includes one or more memory elements suitable to the particular application, such as a main memory **820** in the form of random access memory (RAM), one or more hard drives **840**, and/or one or more drives that handle removable media **860**, such as floppy diskettes, compact disks (CDs) and digital video disks (DVDs). In addition, such external memory may also include a flash memory device **870**. The electronic system **700** may also include a display device **880**, a speaker **890**, and a controller **900**, such as a keyboard, mouse, trackball, game controller, microphone, voice-recognition device, or any other device that inputs information into the electronic system **700**.

CONCLUSION

[0031] In the embodiments described above, a barrier architecture is provided that includes different materials that are selected to be employed in connection with copper contact applications. Some of the barrier material is formed over trench contact sidewalls, and other different barrier material is formed over trench contact bottoms. By selecting the appropriate barrier materials, contact resistances can be improved while, at the same time, concerns associated with array leakage can be mitigated.

[0032] Although the embodiments have been described in language specific to structural features and/or methodological acts, it is to be understood that the subject matter defined in the appended claims is not necessarily limited to the spe-

cific features or acts described. Rather, the specific features and acts are disclosed as exemplary forms of implementing the claimed subject matter.

What is claimed is:

1. A method comprising:

forming a trench contact over a substrate region with which electrical connection is desired;

forming a first barrier layer from a first barrier layer material within the trench contact;

forming a second barrier layer from a second barrier layer material within the trench contact; and

forming copper within the trench contact and in electrical communication with the substrate region.

2. The method of claim **1**, wherein the first and second barrier layer materials are different materials.

3. The method of claim **1**, wherein the first and second barrier layer materials have different metallurgical consistencies.

4. The method of claim **1**, wherein the act of forming the first barrier layer comprises:

forming the first barrier layer over trench contact sidewalls and a trench contact bottom; and

removing first barrier layer material from over the trench contact bottom.

5. The method of claim **4**, wherein the act of forming the first barrier layer comprises depositing the first barrier layer using a high bias resputter process, wherein the first barrier layer comprises a metal and/or nitrogen containing material.

6. The method of claim **5**, wherein the act of removing the first barrier layer material comprises employing a sputter etch to remove the first barrier layer material.

7. The method of claim **6**, wherein the act of forming the second barrier layer comprises using a low bias resputter process.

8. The method of claim **7**, wherein the second barrier layer material comprises a metal material.

9. The method of claim **4**, wherein the first barrier layer material comprises a metal nitride.

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