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(54) **Raster scan digital display system with a multiple memory device comparator facility.**

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US-A-4 070 710

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Description

The present invention relates to a raster scan digital display system with a multiple memory device comparator facility. In such a system, bit maps, in which data for display is stored in a bit pattern corresponding to the picture element pattern of the display and from which the pattern is read sequentially in correspondence with the display scanning to generate display drive signals, are used and the present invention is directed towards the problem of efficiently finding a required bit pattern distributed across the bit maps.

Bit mapped digital display systems are well known. An example of such a system is described in an article entitled 'Computer Graphics in Colour' by P. B. Denes in the Bell Laboratories Record, May 1974, at pages 139 through 146. In that article, it is stated that the computer stores the codes for successive points in successive locations in a buffer memory, and a suitable scan interface circuit reads the buffer memory and generates a video signal. It is also mentioned that a colour picture is produced by generating three separate colour signals for each single video signal.

Another example of a bit mapped digital display system is shown in U.S. Patent US—A—4070710 (Sukonick). The system described therein is essentially designed for a monochrome display, using a single bit map. There is, however, an arrangement described in which two bit maps are read together to produce colour signals.

In certain applications, it is desirable to compare a stored colour code or a multi-bit monochrome code with a reference code. One example is in a colour display system in which a figure, such as a circle, is to be displayed in one colour on a background of another colour and then filled with a solid colour. In order to do this, the digital signals for each scan line must be compared with the colour of the figure firstly as the scan lines enters the figure, and then as it leaves it. From this information, of course, the position and length of the portion of the scan line to be filled can be determined. This comparing operation clearly has other uses, such as in automatic image recognition in which particular patterns on a display are compared with known patterns.

In a bit mapped display system using multiple memories which are only accessible in byte-wide portions, the central processing unit (CPU) coupled to a display system is normally required to read a data byte from each memory and use bit manipulation instructions or individual bit testing to find data groups of four bits (when four memories are used) each from a different memory. As CPU's normally operate on data of at least one byte length, these bit manipulation or individual bit testing operations are excessively time consuming.

It is, therefore, an object of the invention to provide, in a raster scan display system, means for comparing sets of picture element (pel) data with a reference data set without using separate bit manipulation or individual bit testing techniques.

The present invention provides a raster scan digital display system including a number, n, of bit map memories, means for retrieving data from corresponding locations from each of the bit map memories in parallel groups of m bits, means for serialising the groups to form serial streams of parallel n-bit picture element (pel) defining groups, and a compare facility for comparing said retrieved data with an n-bit compare data group to detect equality between each bit of the compare group and corresponding bits of the retrieved data groups defining individual pels, characterised in that said compare facility comprises, for the, or each, pair of bit map stores, an individual comparing circuit arranged to compare each bit of each parallel m-bit group from the pair of maps with an associated one of a pair of the n bits of the compare data to provide, on each of 2m first output lines, corresponding to the 2m bits of the parallel input groups, a signal indicating where the input group bits coincide in value with the corresponding compare data bits, and means for combining the signals on the first output lines to provide, on m second output lines, signals indicating correspondence between the corresponding bits in both input groups and the corresponding compare data bits.

In other words, the invention incorporates, into a multiple memory device raster display system, a hardware comparator arrangement for comparing n-bit pel data witb n-bit reference data. The n-bit pel data is received by the comparator as groups of m×n bits, where m may be, for example an eight bit byte. The comparator is operable to effect a comparison on the corresponding n bits in each group of m and to provide an indication of equality or inequality between any one of the n-bit groups and the n-bit reference data.

The present invention will be described further with reference to an embodiment of the invention as illustrated in the accompanying drawings, in which:—

Figure 1 is a simplified block diagram of a multiplane bit mapped digital raster scan display system;

Figure 2 is a logic diagram of a comparator employed in the Figure 1 system;

Figure 3 shows a modification of the logic of Figure 2;

Figure 1 is a block diagram of a digital raster scan display system, the diagram being limited in detail, for simplicity, to the major components and the major data flow paths of the system. The system couples to a host CPU, for example a microprocessor, by an address bus 2, a control bus 7 and data bus 4. Four memories, MAP0 through MAP3, are provided, which may be, for example, dynamic random access memories, and which are addressed for read, write and refresh operations by an address unit 1. The capacity of

each memory is, for example, 64K bytes, and each memory is coupled to one of two graphics controllers 5 and 6 by one of data input/output busses 8, 9, 10 and 11. The graphics controllers control data flow between the memories and the CPU via CPU data bus 4. They also effect data manipulation operations, including the compare operation to be described later, on data written into, or read from the memories. Each memory is arranged to store a bit map comprising one component of each pel to be displayed. This data is accessed in bytes each representing one component of eight consecutive pels. The stored data is laid out such that adjacent locations are addressed in sequence to provide the data for sequentially scanned pels. To provide the display signals, corresponding location in each of the memories are accessed together to apply four bytes of data, one from each memory, to C.R.T. drive circuit 12. In drive circuit 12, the bytes are serialised to provide sequential sets of four parallel bits, one from each byte. Each set of four bits defines the characteristic of a displayed pel. For example, MAP0 may contain red, MAP1 green, MAP2 blue, and MAP3 attribute component data for each pel. From this data, The C.R.T. drive signals are developed on output lines 13. It is, of course, clear that the system may be used for a monochrome display, with the memory data representing, in the four bit combinations, different intensity levels for the display.

Figure 2 shows a colour compare system which forms a part of the graphics controllers 5 and 6 of Figure 1. It should be noted that the term 'colour compare' is used herein for convenience, it being clear that if the system is used for monochrome display, the comparison is made between intensity-representing data. The object of the colour compare system is to compare colour data from the CPU, received over bus 4 with colour data from MAP0 through MAP3. It will be remembered that, though the memory data is retrieved in bytes, the actual colour information for each displayed pel comprises 4 bits, one from each byte from the memories. Thus, any direct byte-by-byte comparison with CPU data is meaningless. However, to ensure minimum delay, byte transfer and manipulation is highly desirable.

In Figure 2, block 20 is in graphics controller 5, and block 21, whose components are identical to those of block 20 and are, therefore not shown, is in graphics controller 6. Let us assume that a byte of data is read from each of the memories MAP0 through MAP3. These are passed over busses 8 through 11 to respective registers 34 and 35 in block 20 and equivalent registers in block 21. Previously a byte of data, including the data to be compared with the memory data, has been passed by the CPU over bus 4 to a multiplexer 24 in box 20 and similar multiplexer in box 21. This byte of data represents 4 bits of colour information for four maps with 4 unused bits, which would be used if six or eight maps are employed. Each of the multiplexers is designed to select only two bits at any one time and pass these bits to a register, shown as register 25 in box 20. These two bits for multiplexer 24 are bits 0 and 1, selected by a signal on a POS1 line from the CPU, and for the other multiplexer, bits 2 and 3, selected by a signal on a POS2 line. Thus, the multiplexers select and pass on to their respective registers bits 0, 1, 2 and 3 of the CPU compare byte. Bit 0 is now to be compared with the bits in the byte from MAP0, bit 1 with those from MAP1, bit 2 with those from MAP2 and bit 3 with those from MAP3.

Referring now to box 20 in detail, each of eight lines 38—39 from the respective stages of register 34 are coupled as an input to a respective one of eight exclusive NOR circuits 26—27. These compare respective bits of the MAP0 byte from register 34 with the 0 position bit from register 25, the output of which is coupled in common to the XNOR circuits 26—27 through line 43. Similarly eight XNOR circuits 28—29 are coupled to register 35 through lines 40 and to register 25 through common line 42 to compare the 1 position bit from register 25 with the byte read from MAP1 to register 25. As is well known, an XNOR circuit provides a '1' output when its inputs are equal and a '0' output when they are not. Consequently, any correspondence between a bit in register 34 and the 0 position bit in register 25 raises the corresponding one of eight lines 44—45. Similarly, one or more of eight lines 46—47 are raised with correspondence between the bits in register 35 with the 1 position bit in register 25. Eight AND circuits 30—31 each receive the outputs of a corresponding pair of XNOR circuits over the lines 44—45 and 46—47 as shown. On receipt of an enable signal from the C.P.U. over line 48, each of these AND circuits provides an output on its corresponding one of eight lines 49—50. A raised output on one of lines 49—50 indicates correspondence between an associated pair of correspondingly ordered bits from MAP0 to MAP1 and the two colour compare bits in register 25. Similarly one or more of eight lines 51—52 are raised in accordance with the MAP2 and MAP3 data and the remaining two colour compare bits.

To complete the colour compare function, corresponding lines of the two sets 49—50 and 51—52 provide respective inputs to eight AND circuits 32—33 as shown. It should be noted that with open collector outputs from AND circuits 30—31, the AND circuits 32—33 may be simple dot-AND connections rather than transistor logic circuits. AND circuits 32—33 have eight output lines 54—55, and an output on any one of these lines indicates equality between all four bits of the colour compare data and a corresponding four-bit pel data group within the eight such groups received as a byte from each of MAP0 through MAP3. Thus, if lines 54 is activated, the first group (bit 0 of the bytes from MAP0 through MAP3) equal the colour compare data, and if line 55 is activated the last group (bit 7 of the bytes

from the maps) equals the colour compare data. The eight lines 54—55 are coupled back to the CPU to provide the indications of equality.

Though a system employing four bit maps has been described, it is evident that a similar system using two bit maps may be constructed by using only the components in box 20, so that the outputs of AND gates 30—31 provide the output signals without the use of AND gates 32—33. Similarly, the system could be expanded to operate on six or eight bit maps by adding a circuit of the type in box 20 for each additional pair of maps used, and suitably modifying the output circuits from the boxes to the output lines. By using identical logic to service each pair of maps, the number of distinct LSI designs required to service different number of these maps is clearly decreased.

Figure 3 is a logic diagram showing a modification of the arrangement shown in Figure 2. Figure 3 shows certain components of block 20 in Figure 3, all of which have the same reference numerals in both figures. In Figure 3, the Figure 2 circuit is modified by the inclusion of eight OR circuits 60—61 in the output lines 44—45 of XNOR circuits 26—27 and a further eight OR circuits 62—63 in the output lines 46—47 of XNOR circuits 28—29. Each of the OR circuits 60—61 also receives an input in common from one stage of a register 66 over a line 64. Similarly each of the OR circuits 62—63 receives an input in common from the other stage of register 66 over a line 65. It should be noted that block 21, in Figure 2, includes a similar arrangement of a two stage register coupled to OR circuits.

The purpose of the modified arrangement is to permit the comparison of data from only a selected one, or ones, of the maps with the colour compare data. This is achieved by defining the map or maps which will not figure in the comparison operation. Register 66 and its equivalent in block 21 (Figure 2) are loaded from the CPU. The upper stage of register 66 is associated with the data from MAP0 and its lower stage with the MAP1 data A '1' bit in the upper stage results in a '1' bit output from all of the eight OR circuits 60—61 irrespective of the outputs of XNOR circuits 26—27. Similarly a '1' bit in the lower stage provides '1' bit outputs on lines 46—47 irrespective of the outputs from XNOR circuits 28—29. Thus, whenever a '1' bit appears in a stage of register 66 and its equivalent in block 21 (Figure 2), then the logic system provides outputs, in response to inputs from the corresponding maps, which always indicate equality with the corresponding colour compare bits. Thus, by appropriately loading these registers to indicate 'don't care' status, the colour compare operation can be made between the data from any one, two, three or all of the maps and the colour compare data.

In summary, what has been described is a colour compare system in which groups of n bits pel data are compared with an n bit colour compare group. The groups of pels are derived from n bit-mapped memories, each of which supplies m parallel bits representing one order of the n bit pel data for m consecutive pels. The system effects comparison of the m×n bits with the colour compare group in one operation.

Claims

1. A raster scan digital display system including a number, n, of bit map memories (MAP0 to MAP3), means (1, 5, 6) for retrieving data from corresponding locations from each of the bit map memories in parallel groups of m bits, means (12) for serialising the groups to form serial streams of parallel n-bit picture element (pel) defining groups, and a compare facility for comparing said retrieved data with an n-bit compare data group to detect equality between each bit of the compare group and corresponding bits of the retrieved data groups defining individual pels, characterised in that said compare facility comprises, for the, or each, pair of bit map stores, an individual comparing circuit (26, 27, 28, 29) arranged to compare each bit of each parallel m-bit group from the pair of maps with an associated one of a pair of the n bits of the compare data to provide, on each of 2m first output lines (44, 45, 46, 47), corresponding to the 2m bits of the parallel input groups, a signal indicating where the input group bits coincide in value with the corresponding compare data bits, and means (30, 31) for combining the signals on the first output lines to provide, on m second output lines (49, 50, 51, 52), signals indicating correspondence between the corresponding bits in both input groups and the corresponding compare data bits.

2. A raster scan digital display system as claimed in claim 1, in which n is greater than 2, including means (32, 33) for combining the signals on corresponding ones of the second output lines of each comparing circuit to provide, on m third output lines (54, 55), signals indicating correspondence between corresponding bits of all of the parallel input groups and the associated bits of compare data group.

3. A raster scan digital display system as claimed in claim 2 including, in each comparing circuit, means (24) for selecting, from a complete compare data bit group, the pair of bits associated with the comparing system.

4. A raster scan digital display system as claimed in claim 1 in which the, or each, comparing circuit includes a first register (25) for registering the pair of bits of the compare data associated with the comparing circuit, second and third registers (34, 35) for registering the retrieved groups of m bits from the associated bit map memories, first and second sets of m exclusive NOR circuits (26, 27, 28, 29), each coupled to receive an output of an associated stage of one of the second and third registers and an associated output of the first register, and a set of m AND circuits (30, 31), each coupled to receive the outputs of one exclusive NOR circuit in each set.

5. A raster scan display circuit as claimed in claim 4, in which n equals 4, including a further

set of m AND circuits (32, 33), each coupled to receive outputs from the corresponding AND circuits of each of the two comparing circuits.

6. A raster scan display circuit as claimed in any preceding claim, adapted selectively to compare the data from fewer than said n memories with said n-bit compare data group, including means (66) for indicating the memories from which data is not to be compared with the compare data, and logic means (60, 61, 62, 63), responsive to the indicating means to provide said signal on each of the m first output lines corresponding to the indicated memories irrespective of the data received from the indicated memories.

7. A raster scan display circuit as claimed in claim 6 in which the indicating means comprises n stage register means, of which each stage corresponds to an associated memory, and a plurality of OR circuits each coupled in an associated one of the said first output lines, each stage of the register means being coupled to gate an associated m of the OR circuits whereby, when that stage is in a '1' binary stage, all of the coupled OR circuits provide said signal irrespective of the outputs of the associated comparing circuits.

Patentansprüche

1. Rasteranzeigeeinrichtung mit einer Zahl n von Bitmusterspeichern (MAP bis MAP3), mit Mitteln (1, 5, 6) zum Abrufen der Daten von den entsprechenden Plätzen in jedem der Bitmusterspeicher in parallelen Gruppen von m Bits, Mitteln (12) für die Umwandlung der Gruppen in serielle Ströme paralleler Gruppen, die ein n-Bit-Bildelement (Pel) definieren, und einer Vergleichseinrichtung zum Vergleichen der abgerufenen Daten mit einer Vergleichsdatengruppe mit n Bit, um die Gleichheit zwischen jedem Bit der Vergleichsgruppe und den entsprechenden Bits der aufgerufenen Datengruppe festzustellen, die einzelne Pels bilden, dadurch gekennzeichnet, das besagter Vergleicher für ein oder alle Paare der Bitkartenspeicher eine einzelne Vergleichsschaltung (26, 27, 28, 29) enthält, angeordnet, um jedes Bit jeder parallelen m-Bit Gruppe von dem Kartenpaar mit einem zugeordneten Paar der n Bits der zu liefernden Vergleichsdaten zu vergleichen, auf jeder von 2m ersten Ausgangsleitungen (44, 45, 46, 47), den 2m Bits der parallelen Eingabegruppen entsprechend, wobei ein Signal anzeigt, wo die Bits der Eingabegruppen wertmäßig mit den entsprechenden Vergleichsdatenbits zusammenfallen, und Mittel (30, 31) für die Kombination der Signale auf den ersten Ausgangsleitungen, um auf m zweiten Ausgangsleitungen (49, 50, 51, 52) Signale zu liefern, die die Entsprechung zwischen den zugehörigen Bits in den Eingangsgruppen und den zugehörigen Vergleichsdatenbits anzeigen.

2. Rasteranzeigeeinrichtung gemäß Anspruch 1, in den n größer als 2 ist, mit Mitteln (32, 33) zum Kombinieren der Signale auf den entsprechenden zweiten Ausgangsleitungen einer jeden Vergleicherschaltung, um auf m dritten Ausgangsleitungen (54, 55) Signale bereitzustellen, die die Entsprechung zwischen den Bits aller paralleler Eingabegruppen und der zugehörigen Bits der Vergleichsdatengruppen anzeigen.

3. Rasteranzeigeeinrichtung gemäß Anspruch 2 mit Mitteln (24) in jedem Vergleicherkreis, um in einer kompletten Vergleichsdaten-Bitgruppe das Bitpaar auszuwählen, das dem dem Vergleichssystem zugeordnet ist.

4. Rasteranzeigeeinrichtung gemäß Anspruch 1, in dem der oder die Vergleichserschaltungen ein erstes Register (25) enthalten, um das Bitpaar der Vergleichsdaten mit dem zugehörigen Vergleicherkreis aufzuzeichnen, sowie zweite und dritte Register (34, 35) um die aufgerufenen Gruppen von m Bits von den zugeordneten Bitmusterspeichern und erste und zweite Sätze von m ausschließenden NOR-Verknüpfungen (26, 27, 28, 29) aufzuzeichnen, die jeweils gekoppelt sind, um einen Ausgang von einer zugeordneten Stufe eines der zweiten und dritten Register und einen Satz vom m AND-Verknüpfungen (30, 31) zum empfangen, von denen jede gekoppelt ist, um die Ausgänge einer ausschließenden NOR-Verknüpfung in jedem Satz zu empfangen.

5. Rasteranzeigeeinrichtung gemäß Anspruch 4, in der n gleich 4, mit einem weiteren Satz von m AND-Verknüpfungen (32, 33), jede gekoppelt, um Ausgaben von den entsprechenden AND-Verknüpfungen von jedem der beiden Vergleicher zu empfangen.

6. Rasteranzeigeeinrichtung gemäß einem der vorangehenden Ansprüche, selektiv angepaßt, um die Daten von weniger als besagten n Speichern mit der besagten n-Bit Vergleichsdatengruppe zu vergleichen, mit Mitteln (66), um die Speicher anzuzeigen, von denen Daten nicht mit den Vergleichsdaten verglichen werden sollen, und logischen Mitteln (60, 61, 62, 63), die auf die besagten Anzeigemittel ansprechen, um besagtes Signal auf jeder der m ersten Ausgangsleitungen zu liefern, die den angezeigten Speichern entspricht, ohne Berücksichtigung der von den angezeigten Speichern empfangenen Daten.

7. Rasteranzeigeeinrichtung gemäß Anspruch 6, in der die Anzeigemittel n Stufenregistermittel enthalten, von denen jede Stufe einem zugeordneten Speicher entspricht, und eine Mehrzahl von OR-Verknüpfungen, von denen jede mit einer zugeordneten der besagten ersten Ausgangsleitungen gekoppelt ist, um ein zugeordnetes m der OR-Verknüpfungen zu verknüpfen, wenn diese Stufe in einem binären Zustand '1' ist, und alle der besagten OR-Verknüpfungen besagtes Signal liefern, ohne Rücksicht auf die Ausgänge der zugehörigen Vergleicherschaltungen.

Revendications

1. Un système d'affichage numérique à balayage de trame comprenant un certain nombre n de mémoires de mappes de bits (MAP0 à MAP3), des moyens (1, 5, 6) pour récupérer des données dans des emplacements correspondants de chacune des mémoires de mappes de bits en

groupes parallèles de m bits, des moyens (12) pour sérialiser les groupes pour former des coulants en série de groupes de définition d'éléments images (pel) de n bits et un dispositif de comparaison pour comparer lesdites données récupérées à un groupe de données de comparaison de n bits afin de détecter l'égalité entre chaque bit du groupe de comparaison et les bits correspondants des groupes de données récuperées définissant des éléments pel individuels, caractérisé en ce que ledit dispositif de comparaison comprend pour les mémoires de mappes de bits ou chaque paire de celles ci, un circuit de comparaison individuel (26, 27, 28, 29) agencé pour comparer chaque bit de chaque groupe de m bits parallèles de la paire de mappes à un bit d'une paire des n bits des données de comparaison pour délivrer sur chacune des 2m premières lignes de sortie (44, 45, 46, 47) correspondant aux 2 m bits des groupes d'entrée parallèles, un signal indiquant où les bits des groupes d'entrée coïncident en valeur avec les bits de données de comparaison correspondants, et des moyens (30, 31) pour combiner les signaux sur les premières lignes de sortie afin de délivrer sur les m secondes lignes de sortie (49, 50, 51, 52), des signaux indiquant une correspondance entre les bits correspondants dans les deux groupes d'entrée et les bits de données de comparaison correspondants.

2. Un système d'affichage numérique à balayage de trame tel que revendiqué à la revendication 1 dans lequel n est plus grand que 2, comprenant des moyens (32, 33) pour combiner les signaux sur des lignes correspondantes des secondes lignes de sortie de chaque circuit de comparaison afin de délivrer sur m troisièmes lignes de sortie (54, 55), des signaux indiquant la correspondance entre des bits correspondants de tous les groupes d'entrée parallèles et les bits associés du groupe de données de comparaison.

3. Un système d'affichage numérique à balayage de trame tel que revendiqué à la revendication 2, comprenant dans chaque circuit de comparaison, des moyens (24) pour sélectionner depuis un groupe complet de bits de données de comparaison, la paire de bits associée au système de comparaison.

4. Un système d'affichage numérique à balayage de trame tel que revendiqué à la revendication 1 dans lequel le ou chaque circuit de comparaison comprend un premier registre (25) pour enregistrer la paire de bits des données de comparaison associées au circuit de comparaison, des deuxième et troisième registres (34, 35) pour enregistrer les groupes récuperés de m bits à partir des mémoires de mappes de bits associées, des premier et second ensembles de m circuits OU NEGATIF EXCLUSIF (26, 27, 28, 29), chacun de ces circuits étant connecté pour recevoir une sortie d'un étage associé de l'un des deuxième et troisième registres et une sortie associée du premier registre, et un ensemble de m circuits ET (30, 31), chacun de ces circuits étant connecté pour recevoir les sorties d'un circuit OU NEGATIF EXCLUSIF dans chaque ensemble.

5. Un circuit d'affichage à balayage de trame tel que revendiqué à la revendication 4 dans lequel n est égal à 4, comprenant un autre ensemble de m circuits ET (32, 33), chacun étant connecté pour recevoir des sorties des circuits ET correspondants de chacun des deux circuits de comparaison.

6. Un circuit d'affichage à balayage de trame tel que revendiqué à l'une quelconque des revendications précédentes, sélectivement prévu pour comparer les données issues de moins desdits n mémoires audit groupe de données de comparaison de n bits, comprenant des moyens (66) pour indiquer les mémoires depuis lesquelles des données ne sont pas à comparer aux données de comparaison et des moyens logiques (60, 61, 62, 63) repondant à des moyens indicateurs pour délivrer ledit signal sur chacune des m premières lignes de sortie correspondant aux mémoires indiquées indépendamment des données reçues des mémoires indiquées.

7. Un circuit d'affichage à balayage de trame tel que revendiqué à la revendication 6 dans lequels les moyens indicateurs comprennent des moyens à registre à n étages dont chaque étage correspond à une mémoire associée et une pluralité de circuits OU dont chacun est connecté à une ligne associée desdites premières lignes de sortie, chaque étage des registres étant connecté pour conditionner un nombre m des circuits OU associés, ce qui fait que lorsque cet étage est dans un état "1" binaire, tous les circuits OU connectés délivrent ledit signal indépendamment des sorties des circuits des comparaison associés.

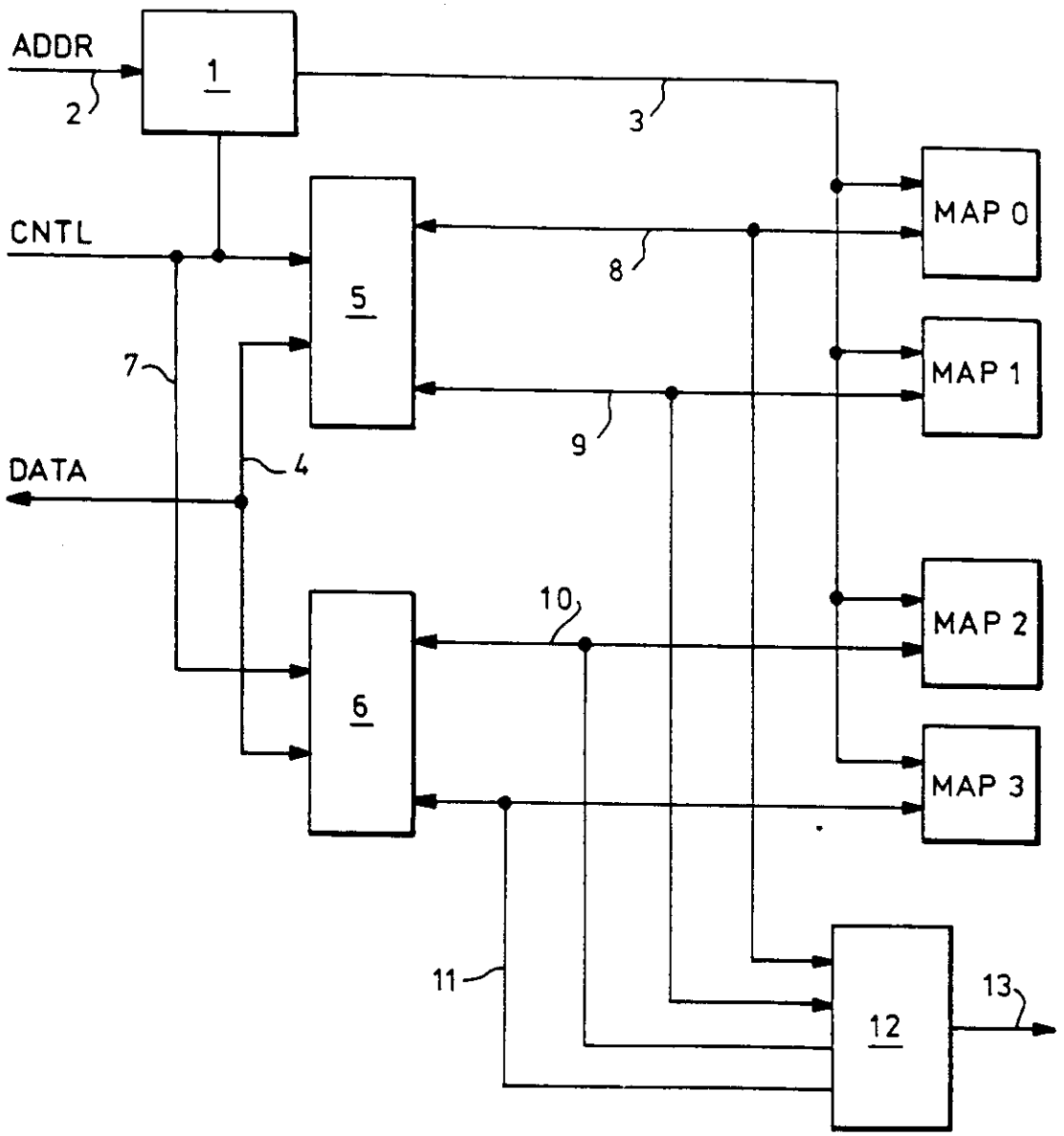

FIG. 1

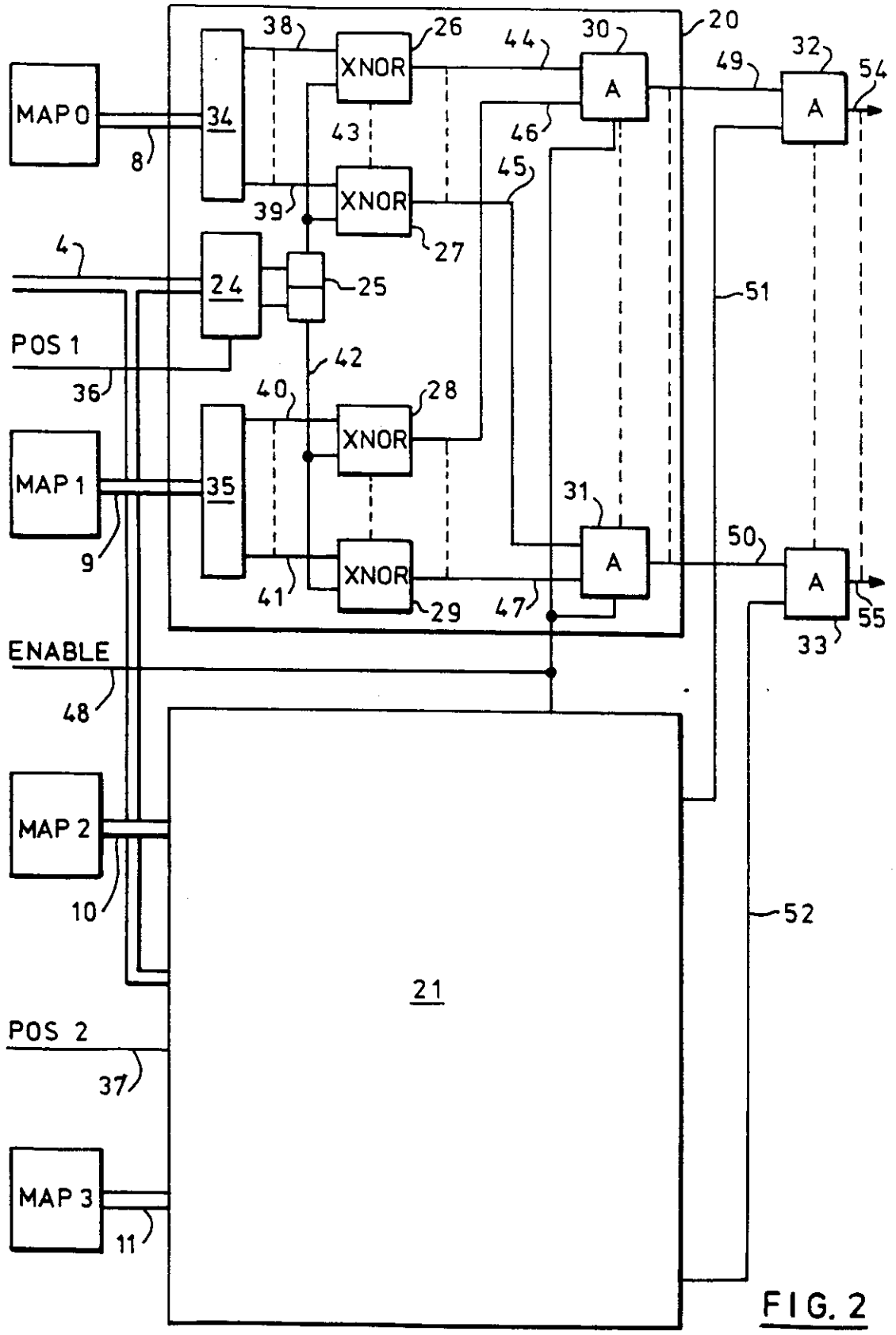
MAP 0
8
34
38
XNOR
26
44
30
20
49
32
54
A
43
46
39
XNOR
45
27
4
24
25
51
POS 1
36
42
40
28
XNOR
MAP 1
9
35
31
50
A
41
XNOR
29
47
55
33
ENABLE
48
MAP 2
10
52
21
POS 2
37
MAP 3
11

FIG. 2

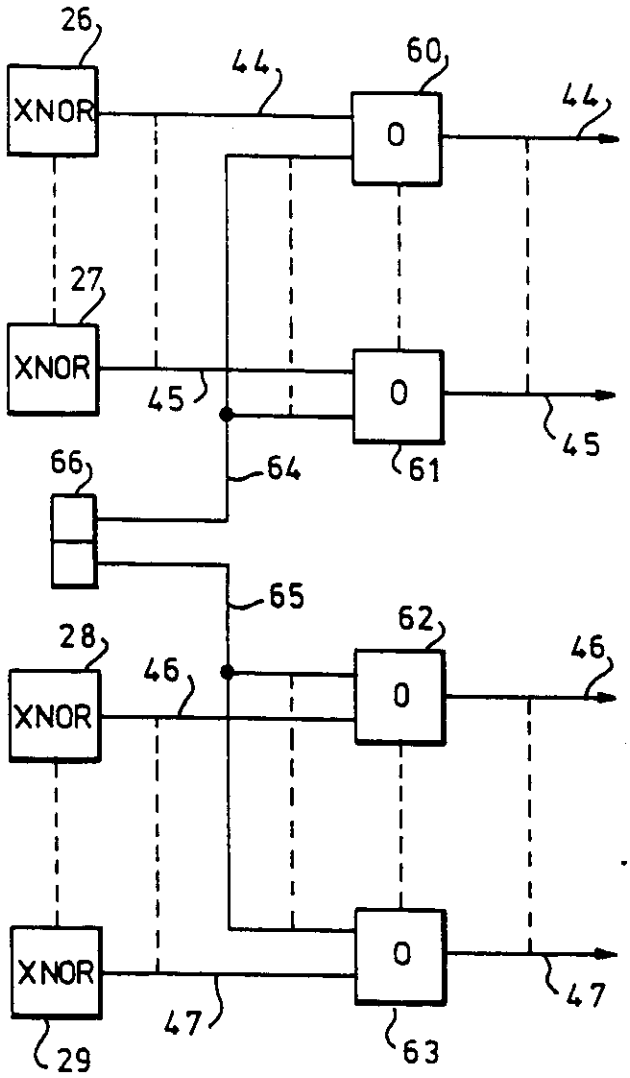
26
XNOR
44
60
O
44
27
XNOR
45
O
45
66
64
61
65
28
XNOR
46
62
O
46
XNOR
47
O
47
29
63

FIG. 3

REGISTER ENTRY FOR EP0139094

European Application No EP84107799.3 filing date 05.07.1984

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Title RASTER SCAN DIGITAL DISPLAY SYSTEM WITH A MULTIPLE MEMORY DEVICE COMPARATOR FACILITY

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