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(54) **Digital transmission systems**

(57) A digital data transmission system in which successive non-overlapping groups of four binary bits in a serial binary input stream are translated into corresponding six-bit binary groups at a higher speed in which all the six-bit groups have a digital sum of 3, giving zero d.c. content in the line with accurate error detection capability and preserved MARK parity.

Translation from 4-bit groups to 6-bit groups is readily accomplished by four input circuits (11A - 11D) providing for each 4-bit group sight logic conditions representing the true (A, B, C, D) and inverted ($\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$) respectively and applying these logic conditions to a logic network comprising AND gates (12A - 12D) and OR gates (13A - 13D, 14, 15A - 15D) in accordance with a translation table (Figure 1).

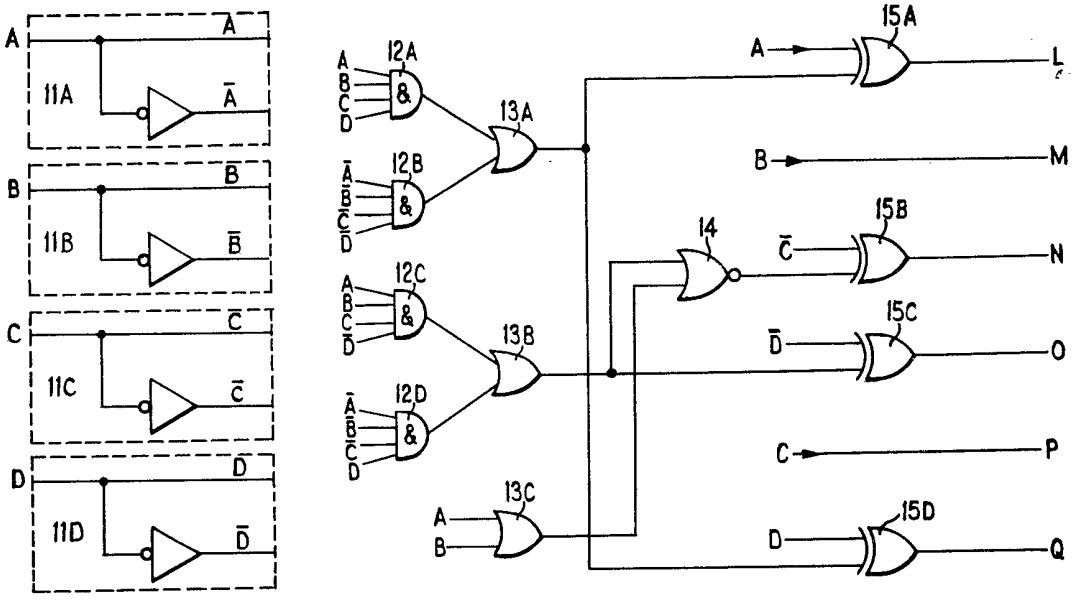

FIG. 2

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FIG.1

TRAFFIC BINARY WORDS		LINE CODE WORDS
0000	A	100101
1000	B	101100
0100	C	011100
1100	D	110100
0010	E	001110
1010	F	100110
0110	G	010110
1110	H	110010
0001	$\underline{H}$	001101
1001	$\underline{G}$	101001
0101	$\underline{F}$	011001
1101	$\underline{E}$	110001
0011	$\underline{D}$	001011
1011	$\underline{C}$	100011
0111	$\underline{B}$	010011
1111	A	011010

111XXX
000XXX
XXX000
XXX111
} ARE PROHIBITED WORDS

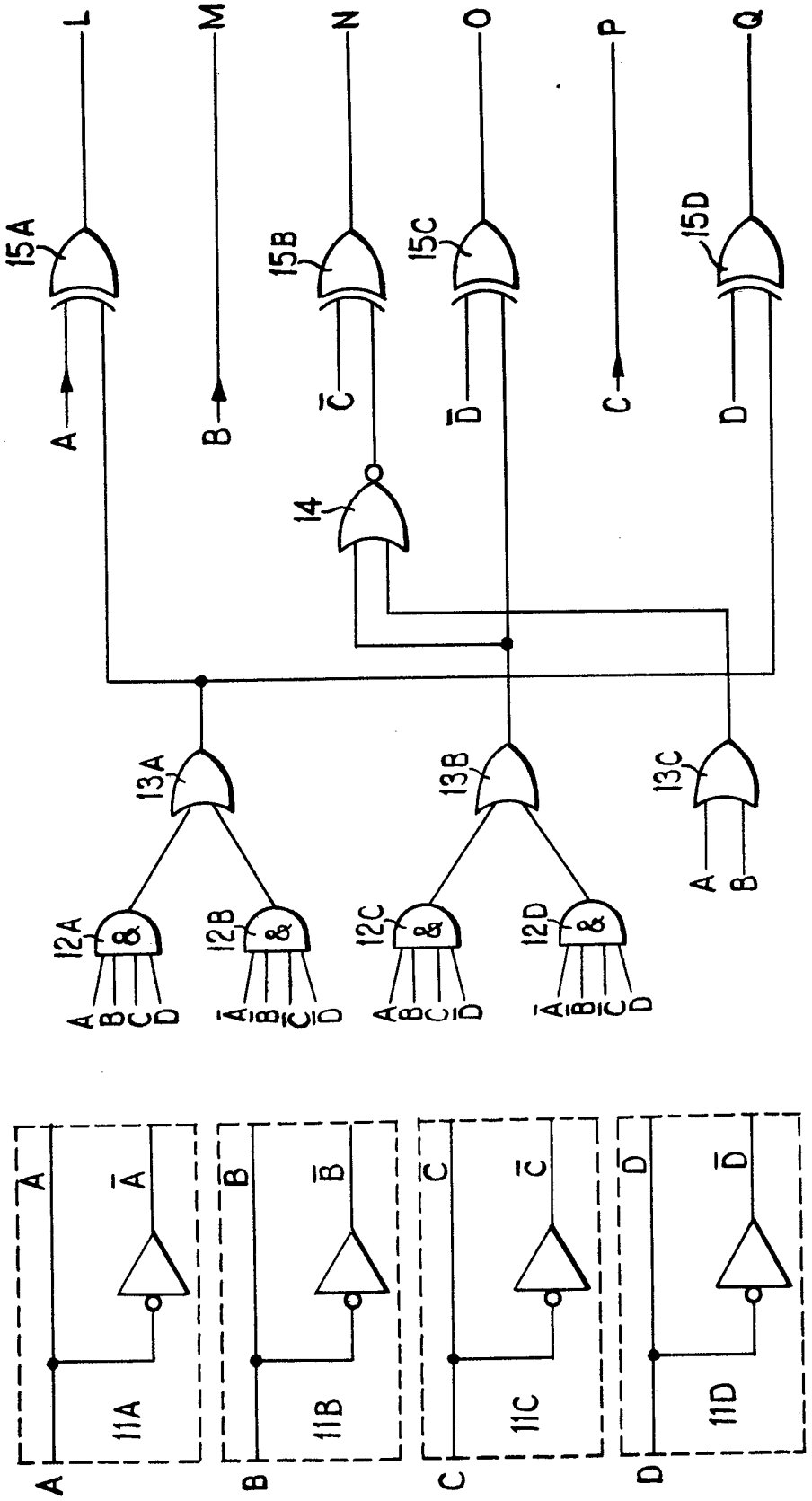
L
M
N
O
P
Q
15A
15B
15C
15D
A
B
C̄
D̄
C
D
14
13A
13B
13C
12A
12B
12C
12D
A B C D
Ā B C D
A B C D
Ā B C D
A B
A
Ā
11A
B
B̄
11B
C
C̄
11C
D
D̄
11D

FIG.2

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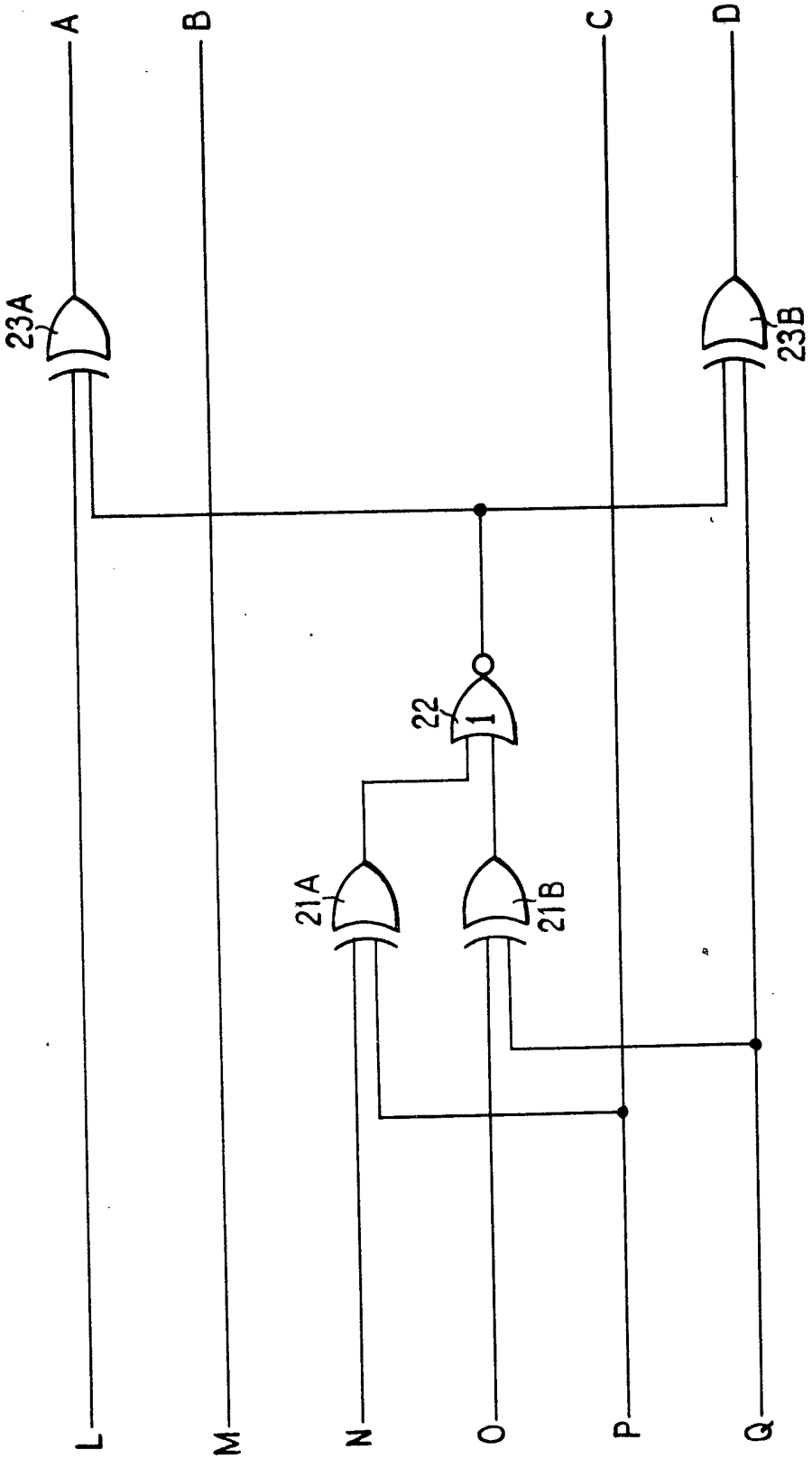

FIG.3

001111	0011
010111	0110
011011	0111
011101	0101
011110	0110
100111	1010
101011	1011
101101	1001
101110	1010
110011	1111
110101	1100
110110	1110
111001	1101
111010	1110
111100	1100

110000	1100
101000	1000
100100	1000
100010	1010
100001	1001
011000	0101
010100	0100
010010	1110
010001	0101
001100	0000
001010	0011
001001	0001
000110	0010
000101	0001
000011	0011

FIG.4

SPECIFICATION

Digital transmission systems

This invention relates to pulse code modulation transmission systems.

Over the years considerable effort has been expended in the development of transmission line codes for pcm systems, particularly as transmission speeds have risen. Many line codes have been derived in which an *m*-bit binary code is translated into an *n*-bit ternary code, see for example British Patent No. 1 156 279 (D.B. Waters - 1), or a *p*-bit binary code, such as described in the paper "Binary Coding in Fibre Optic Digital Transmission with respect to Timing Extraction and Error Monitoring" by E. Balicco and G. Ludicello, 23rd International Congress on Electronics, Rome, Italy, 22nd - 24th March, 1976. In the ternary code case *n* is less than *m* and in the binary code case *p* is greater than *m*.

One of the desirable properties of any high speed line code is that it should have minimal, preferably zero, d.c. content. Other desiderata are parity checking facilities, accurate error detection possibilities, good timing properties, simple translation logic.

According to the present invention there is provided a digital data transmission system including a transmitter to which binary encoded digital signals at a first bit rate are applied serially, the transmitter including means for selecting successive non-overlapping groups of four binary bits in the incoming signal, logic means to which the groups are applied in sequence, the logic means being adapted to translate each four-bit binary group into a corresponding six-bit binary group wherein all the six-bit binary groups have an equal number of MARKS and SPACES and no group has the first three or the last three bits all MARKS or all SPACES, and means for transmitting the six-bit binary groups through the system at a second higher bit rate, and a receiver at which the six-bit groups are received, the receiver including logic means adapted to re-translate the six-bit groups into the corresponding four-bit groups, and means for delivering at an output the four-bit groups in their original sequence at the first bit rate.

An embodiment of the invention will now be described with reference to the accompanying drawings, in which:-

Figure 1 is a code translation table,

Figure 2 illustrates the transmitter translation logic for the translation table of Figure 1,

Figure 3 illustrates the receiver retranslation logic, and

Figure 4 is a table showing additional retranslation allocations required in the receiver to provide an extended error correction facility.

The line code is based on the fact that there are twenty possible 6 bit binary words with a digital sum of 3 (i.e. that are d c balanced) which may be allocated a 4 bit binary equivalent. It is therefore possible to prohibit the use of words 000111 and 111000, with the consequent advantages described later. Figure 1 is a table of one possible set of translations from four-bit binary words to six-bit binary words.

The points to note about the table in Figure 1 are:

a) All line words have a digital sum of 3 (and are therefore d c balance) giving the code the following properties.

i) Zero d c content in the line signals

ii) Accurate error detection possible

iii) Misalignment will cause high rate of words with a digital sum not equal to 3.

iv) Mark parity is preserved after every two words.

b) 000XXX
111XXX are prohibited words
XXX000 which means that
XXX111

i) 000 or $\overline{111}$ should never occur in the first or second half of a received word. This may be used for alignment purposes.

ii) The maximum number of consecutive ones or zeroes is 4 ensuring good timing properties.

c) Using the retranslation logic shown in Figure 3 the worst case error multiplication is 3.

The average error multiplication factor is $\frac{92}{96} = 0.958$.

If a programmable read-only memory (PROM) were used for retranslation, the binary (4 bit) equivalent of each unused 6 bit line word could be chosen to reduce both the maximum and average error multiplication factors.

d) In an 8 M bits/s transmission system the word translation rate is a 2.112 MHz (473 nS) allowing the use of LP Schottky TTL logic circuitry.

Figure 2 shows a single translation logic for the table shown in Figure 1. The four bits of a 4-bit binary word for translation are applied to four input circuits 11A - 11D each of which includes an inverter so that for each bit a true and an inverted logic condition is obtained. Thus if a '1' input is applied to circuit 11A two outputs A and $\overline{A}$ are obtained being '1' '0' respectively. If an '0' input is applied then A and $\overline{A}$ are respectively '0' and '1'. The eight outputs from 11A - 11D are then applied different combinations of four at a time to four AND gates 12A - 12D, the combinations being respectively ABCD, $\overline{A}\overline{B}\overline{C}\overline{D}$, $AB\overline{C}D$ and $\overline{A}\overline{B}C\overline{D}$. The outputs of AND gates 12A and 12B are applied to OR gate 13A, the outputs of 12C and 12D being applied to a similar OR gate 13B. Outputs A and B from 11A and 11B are applied to an EXCLUSIVE OR gate 13C. The output from OR gate 13A is applied to an EXCLUSIVE OR gate 15A together with output A from 11A, and the EXCLUSIVE OR gate 15D together with D from 11D. The output of 13B is applied to OR gate 14 together with the output of 13C, gate 14 having an inverted output. The output gate 14 is applied to EXCLUSIVE OR gate 15B together with $\overline{C}$ from 11C. The output of 13B is also applied to EXCLUSIVE OR gate 15C together with $\overline{D}$ from 11D. The outputs of 15A - 15D provide four outputs LNOQ, which together with the outputs B and C from 11B and 11C make up six outputs LMNOPQ providing the 6-bit binary translation of the 4-bit input word.

At the receiver the retranslation logic required is shown in Figure 3. Two of the six inputs, namely M and P, remain unchanged (compare this with the

arrangement shown in Figure 2) and provide bit B and C. Inputs N and P are applied to EXCLUSIVE OR gate 21A, and O and Q are applied to 21B. The outputs of 21A and 21B are applied to EXCLUSIVE OR gate 22, which has an inverted output. The output of 22 is applied to EXCLUSIVE OR gate 23A together with input A, and to 23B together with input Q. The outputs of 23A & 23B provide bits A & D respectively of the retranslated 4-bit binary word.

The translation shown in Figure 3 is the simplest form of logic. If additional logic can be tolerated it is possible to extend the error correcting capability of the receiver. Thus, if required, the receiver can cope with single errors per word as shown in the table of Figure 4. Using this retranslation table the maximum error multiplication factor is reduced to 2 and the average is 0.79, i.e. 20% of line signal errors are corrected. When the system becomes misaligned errors will be indicated at a rate of approximately every four words, or 1 error in every 24 bits in the received signals. The additional logic required to implement the table shown in Figure 4 whilst not shown can readily be designed by those skilled in the art.

CLAIMS

1. A digital data transmission system including a transmitter to which binary encoded digital signals at a first bit rate are applied serially, the transmitter including means for selecting successive non-overlapping groups of four binary bits in the incoming signal, logic means to which the groups are applied in sequence, the logic means being adapted to translate each four-bit binary group into a corresponding six-bit binary group wherein all the six-bit binary groups have an equal number of MARKS and SPACES and no group has the first three or the last three bits all MARKS or all SPACES, and means for transmitting the six-bit binary groups through the system at a second higher bit rate, and a receiver at which the six-bit groups are received, the receiver including logic means adapted to re-translate the six-bit groups into the corresponding four-bit groups, and means for delivering at an output the four-bit groups in their original sequence at the first bit rate.

2. A system according to claim 1 wherein the selecting means includes four input circuits, one for each of the four binary bits in a selected group, each input circuit including an inverter whereby each input circuit produces two output signals corresponding to the true and inverted logic conditions respectively of the corresponding binary bit in the selected group, the logic means including four 4-input AND gates to each of which outputs the input circuits are applied in four different predetermined combinations, and a network of OR gates to which the outputs of the AND gates are applied together with some of the binary bits in the selected four-bit group to provide four of the bits of the six-bit binary group, the remaining two bits of the six-bit group being two of the bits of the four-bit group.

3. A digital data transmission system substantially as described with reference to the accompanying drawings.

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