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(54) Title: TRENCH MOSFET HAVING LOW GATE CHARGE

**(57) Abstract:** A trench MOSFET device comprising: (a) a silicon substrate (200) of a first conductivity type (preferably N-type conductivity); (b) a silicon epitaxial layer (202) of the first conductivity type over the substrate, the epitaxial layer having a lower majority carrier concentration than the substrate; (c) a body region (204) of a second conductivity type (preferably P-type conductivity) within an upper portion of the epitaxial layer; (d) a trench (206) having trench sidewalls and a trench bottom, which extends into the epitaxial layer from an upper surface of the epitaxial layer and through the body region of the device; (f) an oxide region (210t) lining the trench, which comprises a lower segment (210d) covering at least the trench bottom and upper segments covering at least upper regions of the trench sidewalls; (g) a conductive region (211g) within the trench adjacent the oxide region; and (h) a source region (212) of the first conductivity type within an upper portion of the body region and adjacent the trench. The lower segment (210d) of the oxide region is thicker than the upper segments of the oxide region in this embodiment.

WO 03/044865 A1

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

# TRENCH MOSFET HAVING LOW GATE CHARGE

## FIELD OF THE INVENTION

**[0001]** The present invention relates to microelectronic circuits, and more particularly to trench MOSFET devices having low gate charge.

## BACKGROUND OF THE INVENTION

**[0002]** Metal oxide semiconductor field effect transistor (MOSFET) devices that use trench gates provide low turn-on resistance. In such trench MOSFET devices, the channels are arranged in a vertical manner, instead of horizontally as in most planar configurations. Such transistors provide high current per unit area where low forward voltage drops are required.

**[0003]** FIG. 1 shows a partial cross-sectional view of a trench MOSFET device containing an N+ substrate 1, an N- epitaxial layer 2, P body regions 3, and N+ regions 11. Typically, the P body regions 3 are diffused into the N- epitaxial layer 2, which is disposed on the N+ substrate 1, and the N+ regions 11 are in turn diffused in the body regions 3. Due to the use of these two diffusion steps, a transistor of this type is commonly referred to as a double-diffused metal oxide semiconductor field effect transistor with trench gating or, in brief, a "trench DMOS".

**[0004]** The trench MOSFET device shown in Fig. 1 also includes a trench 8 filled with conductive material 10, which is separated from regions 2, 3, 11 by an oxide region 15, 16. As arranged, the conductive and insulating materials 10 and 16 in the trench 8 form the gate and gate oxide layer, respectively, of the trench MOSFET. The N+ regions 11 form the sources for the device, and the epitaxial layer 2 and N+ substrate 1 together form the drain of the trench MOSFET device. When a potential difference is applied across the P body 3 and the gate 10, charges are capacitively induced within the body region 3, resulting in the formation of a channel within the P body region 3 of the trench MOSFET device adjacent the trench 8. When another potential difference is applied

across the sources 11 and the drain 1,2, a current flows from the source metal 14 to the drain 1,2 through the channel, and the trench MOSFET device is said to be in the power-on state.

**[0005]** Examples of trench MOSFET transistors are disclosed, for example, in U.S. Patent Nos. 5,907,776, 5,072,266, 5,541,425, and 5,866,931, the entire disclosures of which are hereby incorporated by reference.

**[0006]** A typical MOSFET device includes numerous individual MOSFET transistor cells that are fabricated in parallel within a single chip (i.e., a section of a semiconductor wafer). Hence, a chip like that shown in Fig. 1 typically contains numerous cells. Square-shaped and hexagonal cell configurations are common. In a design like that shown in Fig. 1, the substrate region 1 acts as a common drain contact for all of the individual MOSFET transistor cells. All the sources 11 for the MOSFET cells are typically shorted together via a metal source contact 14 that is disposed on top of the N+ source regions 11. An insulating region 12, such as borophosphosilicate glass, is typically placed between the conductive material 10 in the trenches 8 and the metal source contact 14 to prevent the gates 10 from being shorted with the source regions 11. Consequently, to make contact with the gates 10, the conductive material within the trenches is typically extended into a termination region beyond the MOSFET cells, where a metal gate contact is provided. Since the conductive regions are interconnected with one another via the trenches, this arrangement provides a single gate contact for all the gate regions of the device. As a result of this scheme, even though the chip contains a matrix of individual transistor cells, these cells behave as a single large transistor.

**[0007]** Demand persists for trench MOSFET devices having ever-lower on-resistance. The simplest way to reduce on-resistance is to increase cell density. Unfortunately, the gate charges associated with trench MOSFET devices increase when cell density is increased. The device of Fig. 1 is disclosed in JP05335582 to Omron Corp. and entitled "Vertical MOSFET device and Manufacture thereof", the complete disclosure of which is hereby incorporated by reference. This device takes advantage of the fact that oxide film at the trench sidewall forms the channel within the P-body region

3, while oxide film at the bottom of the trench does not contribute significantly to channel formation, but nonetheless contributes to gate charges. In response, the oxide film 15 at the bottom of the trench 8 can be thickened substantially relative to the oxide film 16 at the sidewall to reduce gate charges. According to the JP05335582 abstract, the thick gate oxide film 15 is formed at the bottom of the groove by stacking oxide films by decompressed CVD until the trench 8 flattens, and etching back this oxide film to form the thick oxide film 15 at the bottom of the trench 8. Subsequently the thinner gate oxide film 16 is formed at the sidewall of the trench 8 by thermal oxidation.

## SUMMARY OF THE INVENTION

**[0008]** Unfortunately, a gate oxide formed by CVD, such as that described in the JP05335582 abstract, creates a high state charge at the interface between the CVD gate oxide and the silicon. This and other disadvantages of the devices of the prior art are addressed by the design and manufacture of the trench MOSFET devices of the present invention.

**[0009]** According to an embodiment of the invention, a trench MOSFET device is provided, which comprises: (a) a silicon substrate of a first conductivity type (preferably N-type conductivity); (b) a silicon epitaxial layer of the first conductivity type over the substrate, the epitaxial layer having a lower majority carrier concentration than the substrate; (c) a body region of a second conductivity type (preferably P-type conductivity) within an upper portion of the epitaxial layer; (d) a trench having trench sidewalls and a trench bottom, which extends into the epitaxial layer from an upper surface of the epitaxial layer and through the body region of the device; (f) an oxide region lining the trench, which comprises a lower segment covering at least the trench lower and upper segments covering at least upper regions of the trench sidewalls; (g) a conductive region within the trench adjacent the oxide region; and (h) a source region of the first conductivity type within an upper portion of the body region and adjacent the trench. The lower segment of the oxide region is thicker than the upper segments of the oxide region

in this embodiment. Moreover, those portions of the oxide region that form interfaces with the silicon are thermally grown.

**[0010]** According another embodiment of the invention, a trench MOSFET device is provided which comprises: (a) a silicon substrate of a first conductivity type (preferably N-type conductivity); (b) a silicon epitaxial layer of the first conductivity type over the substrate, the epitaxial layer having a lower majority carrier concentration than the substrate; (c) a body region of a second conductivity type (preferably P-type conductivity) within an upper portion of the epitaxial layer; (d) a trench having trench sidewalls and a trench bottom, which extends into the epitaxial layer from an upper surface of the epitaxial layer and extends through the body region; (e) an oxide region lining the trench, which comprises a lower segment covering at least the trench bottom and upper segments covering at least upper regions of the trench sidewalls; (f) a conductive region within the trench adjacent the oxide region; and (g) a source region of the first conductivity type within an upper portion of the body region and adjacent the trench. In this embodiment, the lower segment of the oxide region is thicker than the upper segments of the oxide region, establishing shoulders in the oxide region that are adjacent the conductive region along the trench sidewalls.

**[0011]** In some embodiments, the lower segment of the oxide region includes a thermally grown portion (which can range, for example, from 500 to 2000 Angstroms in thickness) adjacent the trench and a deposited oxide portion (which can also range, for example, from 500 to 2000 Angstroms in thickness) adjacent the conductive region, while the upper segments of the oxide region consist of thermally grown oxide (which can range, for example, from 100 to 1000 Angstroms in thickness). The deposited oxide portion is preferably densified TEOS.

**[0012]** In other embodiments, the lower segment of the oxide region is a thick thermally grown oxide region (which can range, for example, from 500 to 2000 Angstroms in thickness), while the upper segments of the oxide region are thin thermally grown oxide regions (which can range, for example, from 100 to 1000 Angstroms in thickness).

[0013] Preferably, the conductive region of the device comprises polycrystalline silicon. In some embodiments, the conductive region comprises a polycrystalline silicon portion and a portion selected from a refractory metal and a refractory metal alloy (for example, a tungsten portion or a titanium-tungsten alloy portion). In other embodiments, the conductive region comprises a polycrystalline silicon portion and a refractory metal silicide portion (e.g., a titanium silicide portion).

[0014] According another embodiment of the invention, a trench MOSFET device is provided which comprises: (a) a silicon substrate of first conductivity type (preferably N-type conductivity); (b) a silicon epitaxial layer of the first conductivity type over the substrate, the epitaxial layer having a lower majority carrier concentration than the substrate; (c) a body region of second conductivity type (preferably P-type conductivity) within an upper portion of the epitaxial layer; (d) a trench having trench sidewalls and a trench bottom, which extends into the epitaxial layer from an upper surface of the epitaxial layer and extends through the body region; (e) an oxide region lining the trench, the oxide region comprising (i) a u-shaped lower segment covering the trench bottom and lower regions of the trench sidewalls and (ii) upper segments covering at least upper regions of the trench sidewalls; (f) a conductive region within the trench adjacent the oxide region; and (g) a source region of the first conductivity type within an upper portion of the body region and adjacent the trench. In this embodiment, the u-shaped lower segment of the oxide region is thicker than the upper segments of the oxide region.

[0015] According to yet another embodiment of the invention, a method of forming a trench MOSFET device is provided which comprises: (a) providing a silicon substrate of a first conductivity type; (b) providing a silicon epitaxial layer of the first conductivity type over the substrate, the epitaxial layer having a lower majority carrier concentration than the substrate; (c) forming a body region of a second conductivity type within an upper portion of the epitaxial layer; (d) etching a trench extending into the epitaxial layer from an upper surface of the epitaxial layer, the trench extending through the body region and the trench having trench sidewalls and a trench bottom; (f) forming an oxide region lining the trench, the oxide region comprising a lower segment covering at least the

trench bottom and upper segments covering at least upper regions of the trench sidewalls; (g) depositing a conductive region within the trench adjacent the oxide region; and (h) forming a source region of the first conductivity type within an upper portion of the body region and adjacent the trench. The lower segment of the oxide region formed in this embodiment is thicker than the upper segments of the oxide region, such that shoulders are established in the oxide region adjacent the conductive region along the trench sidewalls.

[0016] In some embodiments, the oxide region lining the trench is formed by a process comprising: (a) forming a thermal oxide layer within the trench; (b) providing a deposited oxide layer over the thermal oxide layer; (c) forming an etch resistant region (for example, a photoresist region or a polysilicon region) in the trench bottom over the deposited oxide layer; and (d) etching the deposited oxide layer where not covered by the etch resistant region. A thermal oxidation step is preferably carried out after the deposited oxide-etching step.

[0017] In other embodiments, the oxide region lining the trench is formed by a process comprising: (a) forming a thick thermal oxide layer within the trench; (b) forming an etch resistant region (for example, a photoresist region or a polysilicon region) in the trench bottom over the thick thermal oxide layer; and (c) etching the thermal oxide layer where not covered by the etch resistant region. A thermal oxidation step is preferably carried out after the thermal oxide etching step.

[0018] One advantage of the present invention is that an improved trench MOSFET device can be provided which has a high cell density, and hence low on resistance, while at the same time providing an acceptably low gate charge.

[0019] Another advantage of the present invention is that a trench MOSFET device having a thick layer of oxide at the trench bottom can be provided without simultaneously creating undesirably high state charge levels at the oxide/semiconductor interface.

[0020] Another advantage of the present invention is that a trench MOSFET device can be provided in which an interface between a CVD oxide and silicon is avoided, reducing the state charge levels associated with interfaces of this nature.

[0021] Another advantage of the present invention is that a trench MOSFET device can be provided in which a high quality oxide/silicon interface, typically formed by thermal oxidation, can be provided within the gate trenches, providing an acceptably low level of interfacial state charges.

[0022] These and other embodiments and advantages of the present invention will become immediately apparent to those of ordinary skill in the art upon review of the Detailed Description and Claims to follow.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] Fig. 1 is a schematic partial cross-sectional view of a trench MOSFET transistor device of the prior art.

[0024] Fig. 2 is a schematic partial cross-sectional view of a trench MOSFET transistor device in accordance with an embodiment of the invention.

[0025] Fig. 3 is a schematic partial cross-sectional view of a trench MOSFET transistor device in accordance with another embodiment of the invention.

[0026] Fig. 4 is a schematic partial cross-sectional view of a trench MOSFET transistor device in accordance with another embodiment of the invention.

[0027] Fig. 5 is a schematic partial cross-sectional view of a trench MOSFET transistor device in accordance with another embodiment of the invention.

[0028] Fig. 6 is a schematic partial cross-sectional view of a trench MOSFET transistor device in accordance with yet another embodiment of the invention.

[0029] Fig. 7 is a schematic partial cross-sectional view of a trench MOSFET transistor device in accordance with still another embodiment of the invention.

[0030] Fig. 8A through Fig. 8G are schematic partial cross-sectional views illustrating a process for manufacturing the trench MOSFET transistor device like that of Fig. 2.

[0031] Fig. 9A through Fig. 9G are schematic partial cross-sectional views illustrating another process for manufacturing the trench MOSFET transistor device like that of Fig. 2.

[0032] Fig. 10A through Fig. 10H are schematic partial cross-sectional views illustrating a process for manufacturing the trench MOSFET transistor device like that of Fig. 3.

[0033] Fig. 11A through Fig. 11C are schematic partial cross-sectional views illustrating a process for manufacturing the trench MOSFET transistor devices like those of Fig. 4 and Fig. 5.

[0034] Fig. 12A through Fig. 12C are schematic partial cross-sectional views illustrating a process for manufacturing the trench MOSFET transistor devices like those of Fig. 6 and Fig. 7.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[0035] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the present invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein.

[0036] One embodiment of a trench MOSFET of the present invention is shown in partial cross section in Fig. 2. The trench MOSFET shown contains an N-type epitaxial layer 202, which is provided on an N+ substrate 200. The N+ substrate 200 is typically a silicon substrate having a thickness ranging, for example, from 10 to 25 mils and a resistivity ranging, for example, from 0.005 to 0.01 Ohm-cm. The N-type epitaxial layer 202 is also typically silicon having a thickness ranging from, for example, 5 to 6 microns and a resistivity ranging, for example, from 0.18 to 0.25 Ohm-cm.

[0037] Trenches 206 formed within the epitaxial layer are lined with thermally grown oxide regions 210t and also contain deposited oxide regions 210d at the trench bottom. Note that the trench bottom can have a variety of configurations including v-shaped, rounded u-shaped, and square u-shaped configurations. The trench sidewalls are substantially vertical, typically having angles ranging from 75 degrees (tapered) to 90 degrees (vertical) to 100 degrees (reentrant), more preferably from 85 to 90 degrees. The

trenches 206 are further filled with polysilicon regions 211g. The polysilicon regions 211g typically have a resistivity ranging from 15 to 25 Ohm/sq. The trenches 206 typically have a depth of 1.0 to 2.0 microns and a width of 0.2 to 2 microns. The regions between the trenches are frequently referred to as mesas or trench mesas, based on their shapes, and are typically 0.2 to 1.0 microns in width.

**[0038]** The thermally grown oxide regions 210t typically range from 100 to 1000 Angstroms in thickness, while the deposited oxide regions 210d typically range from 500 to 2000 Angstroms in thickness. In constructing a composite oxide region in this fashion, the trench MOSFET device can be provided with a very high cell density (e.g., 20M to 500M/in.sq.). The gate charges associated with this high cell density are held in check by providing thick oxide regions at the trench bottom, consisting of both thermally grown oxide regions 210t and deposited oxide regions 210d. As previously noted, the portions of the oxide regions at the trench bottoms 210d, 210t are not significantly involved in channel formation during operation and hence can be of considerable thickness, reducing gate charges. On the other hand, portions of the thermally grown gate oxide region 210t along the trench sidewalls above the deposited oxide regions 210d are sufficiently thin to effectively form a channel region within the adjacent P-body regions 204 during operation. Moreover, thermally grown oxide regions 210t, rather than deposited oxide regions 210d, are adjacent the silicon. As a result, the high state charge that is found at the interface between the silicon and the deposited oxide in prior art structures (e.g., the structure disclosed in the abstract of JP05335582) is avoided.

**[0039]** Within the epitaxial layer are P-body regions 204. Resistivities ranging from 0.1 to 1.0 Ohm-cm and depths of 1 to 2 microns from the surface of the epitaxial layer are typical of such structures. The trench MOSFET device of Fig. 2 also contains N+ source regions 212, which typically extend to a depth of 0.3 to 0.45 microns from the epitaxial layer surface and typically have resistivities of 0.001 to 0.003 Ohm-cm.

**[0040]** In the embodiment shown, P-body upper regions (p+ regions) 215 are provided between the n+ source regions 212 for purposes of forming good ohmic contact with the electrode 218. These regions 215 are shown as extending to approximately the

same depth as the n+ source regions 212, but other depths are clearly possible. Resistivities of 0.002 to 0.005 Ohm-cm are typical.

[0041] Electrical contact is made with the n+ source regions 212 via metal source contact 218. Insulating regions 216, typically BPSG (borophosphosilicate glass), prevent the polysilicon regions 211g associated with the gate electrodes from being shorted to the n+ source regions 212 through source contact 218. A separate metal gate contact (not shown) is typically connected to the gate runner portion of the polysilicon that is located outside of the region of the trench MOSFET cells. A metal drain contact (not shown) is also typically provided in electrical connection with the N+ substrate 200.

[0042] Another embodiment of the invention is shown in Fig. 3. Fig. 3 is essentially the same as Fig. 2, except for the configuration of the oxide regions lining the trenches. Specifically, whereas Fig. 2 contains oxide regions that are a combination of thermally grown oxide regions 210t and deposited oxide regions 210d, the oxide regions of Fig. 3 are entirely formed from thermally grown oxide 210t. Nonetheless, as in Fig. 2, the oxide regions 210t within the trenches 206 are thicker at the trench bottoms (typically 500 to 2000 Angstroms in thickness) than they are along the upper portions of the trench sidewalls (typically 100 to 1000 Angstroms). In this way, gate function is maintained, while reducing the gate charges associated with the device. Moreover, high interface state charges are avoided, because thermally grown oxide regions 210t, rather deposited oxide regions, are placed adjacent the silicon.

[0043] Other embodiments of the invention are shown in Fig. 4 and Fig. 5. Fig. 4 and Fig. 5 are essentially the same as Fig. 2 and Fig. 3, respectively. However, the polysilicon gate regions 211g of Figs. 2 and 3 are replaced by composite gate regions consisting of both polysilicon gate regions 211g and tungsten metal regions 211m. These embodiments provide lower gate resistance relative to a device containing only polysilicon gate regions, improving switching frequency. In alternative embodiments, the tungsten metal is replaced by other refractory metals and metal alloys, such as titanium-tungsten alloys.

[0044] Still other related embodiments of the invention are shown in Fig. 6 and Fig.

7. Fig. 6 and Fig. 7 are essentially the same as Fig. 2 and Fig. 3, respectively, except that the polysilicon gate regions 211g of Figs. 2 and 3 are replaced by composite gate regions. In Figs. 6 and 7, these regions consist of both polysilicon gate regions 211g and refractory metal silicide regions 211ms such as titanium silicide (typically $TiSi_2$). Refractory metals that readily form silicides include titanium, tungsten, tantalum, and molybdenum.

**[0045]** An embodiment of a process for the manufacture of a device like that of Fig. 2 will now be described in connection with Figs. 8A to 8G. In these figures, an N doped epitaxial layer 202 is initially grown on an N+ doped substrate 200. For example, epitaxial layer 202 can be 6.0 microns thick and have an n-type doping concentration of bout $3.4 \times 10^{16}$ $cm^{-3}$, while N+ doped substrate 200 can be 250 microns thick and have n-type doping concentration of about $5 \times 10^{19}$ $cm^{-3}$. A P-type layer 204 is then formed in the epitaxial layer 202 by implantation and diffusion. For example, the epitaxial layer 202 may be implanted with boron at 40 keV with a dosage of $6 \times 10^{13}$ $cm^{-2}$, followed by diffusion to a depth of 1.8 microns at 150° C.

**[0046]** A mask oxide layer (not shown) is then deposited, for example by chemical vapor deposition, and covered with a patterned trench mask (not shown). The mask oxide layer is then etched, for example, by buffered HF, forming a patterned mask oxide layer (not shown). Trenches 206 are subsequently etched through apertures in the patterned mask oxide layer, typically by reactive ion etching. Trench depths can be, for example, about 2.0 μm. Discrete P-body regions 204 are established as a result of this trench-forming step. A sacrificial oxide (not shown) is then grown, typically by dry oxidation to improve the quality of the silicon surface. This oxide is then removed, typically by buffered HF, forming the structure illustrated in Fig. 8A.

**[0047]** A thermal gate oxide layer 210t is grown over the entire device, for example, by dry oxidation at 900 to 1150 °C. A thickness in the range of 100 to 1000 Angstroms is preferred for the thermal gate oxide layer 210. Then, a TEOS (i.e., tetraethylorthosilicate or $Si(OC_2H_5)_4$) layer 210 is deposited, for example, by PECVD (plasma enhanced chemical vapor deposition) at temperatures between 500 and 600 °C, to provide the

structure of Fig. 8B. The TEOS layer 210 typically ranges from 400 to 1000 Angstroms in thickness.

**[0048]** The surface of the structure is then covered, and the trenches are filled, with a photoresist layer 207 to provide the structure of Fig. 8C. The resist layer is then etched, for example, by reactive ion etching, until all of the photoresist is removed except for resist portions 207 at the bottom of the trenches, providing the structure of Fig. 8D. The TEOS layer 210 is then etched, for example, by buffered HF to produce the structure of Fig. 8E.

**[0049]** The remaining resist 207 is removed, for example, by sulfuric acid. Subsequently, the TEOS regions 210 are densified, for example, by annealing at 950°C in $N_2$ to provide high-density deposited silicon dioxide regions 210d. The structure then undergoes an additional thermal oxidation step, for example, 10 to 20 minutes at 950 to 1150 C, to ensure that those portions of the gate oxide layer 210t not covered by deposited oxide 210d are of sufficient thickness. Thicknesses ranging from 10 to 1000 Angstroms are typical.

**[0050]** The surface of the structure is then covered, and the trenches are filled, with a polysilicon layer, typically using CVD. The polysilicon is typically doped N-type to reduce its resistivity, generally on order of 20 Ω/sq. N-type doping can be carried out, for example, during CVD with phosphorous chloride or by implantation with arsenic or phosphorous. As is typical, a patterned masking layer (not shown) is provided to preserve polysilicon in the gate runner region, and the unmasked portions of the polysilicon layer are etched, for example, by reactive ion etching. The polysilicon layer within the trench segments is slightly over-etched due to etching uniformity concerns, and the thus-formed polysilicon gate regions 211g typically have top surfaces that are 0.1 to 0.2 microns below the adjacent surface of the epitaxial layer 204. The resulting structure is shown in Fig. 8F.

**[0051]** The oxide layer 210t is then wet etched to a thickness of 100 Angstroms to form an implant oxide (not shown). The implant oxide avoids implant-channeling effects, implant damage, and heavy metal contamination during subsequent formation of source

regions. Source regions 212 are formed within upper portions of the P-body regions 204 via an implantation and diffusion process, using a patterned masking layer (not shown). For example, the source regions 212 may be implanted with arsenic at a dosage of 1 x $10^{16}$ $cm^{-2}$ and diffused to a depth of 0.4 microns at a temperature of 950°C. An additional mask (not shown) is then formed, followed by implantation and diffusion of boron to form P-body upper portions 215 (p+ regions) between n+ regions 212. For example, the P-body upper portions 215 may be implanted with boron at a dosage of 1.5e14 $cm^{-2}$ and diffused to a depth of .3-.6 microns.

**[0052]** A BPSG (borophosphosilicate glass) layer is then formed over the entire structure, for example, by PECVD, and provided with a patterned photoresist layer (not shown). The structure is etched, typically by reactive ion etching, to remove the BPSG and oxide over at least a portion of each source region 212, leaving behind BPSG regions 216. After removing the photoresist layer, the structure is provided with a metal contact layer 218 (aluminum in this example), which acts as a source electrode. The resulting cross-sectional views of this structure are shown in Fig. 8G. In the same step, a separate metal contact is typically connected to the gate runner, which is located outside the cells. Another metal contact is typically provided in connection with the substrate 200, which acts as a drain electrode.

**[0053]** An alternate method for producing a trench MOSFET structure like that shown in Fig. 2 is illustrated in Figs. 9A through 9G. The process for producing the structure of Fig. 9A is the same as that set forth above in connection with Fig. 8A. The process for producing Fig. 9B is the same as Fig. 8B, except that the TEOS layer 210 is densified in Fig. 9B following deposition to provide a high-density silicon dioxide layer 210d. As will become more apparent below, in contrast to the above procedure of Figs. 8A through 8G, densification is performed at this earlier stage, because portions of the layer 210d are permanently covered by polysilicon in the following step.

**[0054]** The surface of the structure is then covered, and the trenches are filled, with a doped polysilicon layer 211g in a manner like that described in Fig. 8F above, resulting in the structure of Fig. 9C. The polysilicon layer is then etched, for example, by reactive ion

etching, until only the bottoms of the trenches are filled with the polysilicon 211g. The resulting structure is shown in Fig. 9D.

[0055] The densified silicon dioxide layer 210d is then etched, for example by reactive ion etching, removing all of silicon dioxide layer 210d, except where protected by the polysilicon 211g coving the trench bottoms. The resulting structure is shown in Fig. 9E. As in Fig. 8F above, the structure then undergoes an additional thermal oxidation step to ensure that those portions of the gate oxide layer 210t not covered by the deposited oxide 210d are of sufficient thickness. An additional layer of polysilicon is then provided, covering the surface and filling the trenches of the device. As previously discussed, also in connection with Fig. 8F, a patterned masking layer is provided to preserve polysilicon in the gate runner region, and the polysilicon layer is slightly over-etched, creating final polysilicon gate regions 211g within the trenches. The resulting structure is shown in Fig. 9F. Finally, the steps described above in connection with Fig. 8G are preformed, producing the device shown in Fig. 9G.

[0056] A method of producing a trench MOSFET structure like that shown in Fig. 3 will now be described in connection with Figs. 10A through 10H.

[0057] As in the process of Fig. 8A, an N doped epitaxial layer 202 is initially grown on an N+ doped substrate 200. A P-type layer 204 is then formed in the epitaxial layer 202 by implantation and diffusion. A mask oxide layer is then deposited, and covered with a patterned trench mask (not shown). The mask oxide layer is then etched forming a patterned mask oxide layer 210. Trenches 206 are subsequently etched through apertures in the patterned mask oxide layer 210, establishing discrete P-body regions 204. The resulting structure is shown in Fig. 10A.

[0058] At this point, a thick oxide layer is grown over the entire structure, forming layer 210t (which also includes the patterned mask oxide layer 210 from the prior step). The resulting structure is shown in Fig. 10B. The thick oxide layer is grown by thermal oxidation, for example, by either wet or dry oxidation at 950 to 1150°C for a period of 10 to 120 minutes. After oxidation, the thick oxide layer is preferably 500 to 2000 microns in thickness.

[0059] The surface of the structure is then covered, and the trenches are filled, with a photoresist layer 207 to provide the structure of Fig. 10C. The resist layer is then etched, for example, by reactive ion etching, until all of the photoresist is removed except photoresist portions 207 at the bottom of the trenches, providing the structure of Fig. 10D.

[0060] The oxide layer 210t is then etched, for example by reactive ion etching, removing all of thick oxide layer, except where it is protected by the photoresist covering the trench bottoms, resulting in distinct, thick thermally grown oxide regions 210t as shown in Fig. 10E.

[0061] The remaining photoresist 207 is then removed, for example, by sulfuric acid. Subsequently, a thin gate oxide layer is formed on the exposed silicon surfaces of the structure, for example, by dry oxidation at 950 to 1150 °C. This thin gate oxide layer is typically 100 to 1000 Angstroms in thickness. As shown in Fig. 10F, this oxidation step results in a thermally grown oxide layer 210t having thick regions at the trench bottoms and thin regions on upper portions of the trench sidewalls (as well as on top of the structure).

[0062] A layer of polysilicon 211g for the gate region is provided over the entire structure, covering the surface and filling the trenches of the device as shown in Fig. 10G. The device is completed from this point as discussed above in connection with Figs. 8F and 8G, producing the structure of Fig. 10H.

[0063] A method of producing a trench MOSFET structure like that shown in Fig. 4 will now be described in connection with Fig. 11A and Fig. 11B.

[0064] This process is the same as that discussed above in connection with Figs. 8A through Fig. 8E. At this point, the remaining resist is removed, the TEOS layer is densified to provide a high-density silicon dioxide layer 210d, and the gate oxide layer 211t is thickened as in Fig. 8F above. However, a substantially thinner polysilicon layer 211g is provided over the surface of the device and in the trenches, such that the trenches are not filled by the polysilicon 211g. Instead, trench filling is completed by depositing a metal layer 211m of either tungsten (W) or a titanium-tungsten alloy (TiW) (or Tungsten

Silicide (WSi), if desired) using techniques known in the art such as CVD. The resulting structure is shown in Fig. 11A

**[0065]** As above, a patterned masking layer is provided to preserve the polysilicon, as well as the W/TiW, in the gate runner region, and the layers of polysilicon 211g and W/TiW 211m are slightly over-etched, producing composite gate regions consisting of polysilicon 211g and W/TiW 211m. Finally, the steps described above in connection with Fig. 8G are preformed, producing the device of Fig. 11B.

**[0066]** A method of producing a trench MOSFET structure like that shown in Fig. 5 is now described in connection with Fig. 11C. This process is the same as that of Fig. 10A through 10F. At this point, however, the trenches are not filled with polysilicon. Instead, a relatively thin polysilicon layer 211g is provided over the surface of the device and in the trenches. The trenches are then filled by depositing a metal layer 211m of either tungsten (W) or a titanium-tungsten alloy (TiW) (or Tungsten Silicide (WSi), if desired) and the structure is completed as discussed in connection with Fig. 11B. The completed structure is shown in Fig. 11C.

**[0067]** A method of producing a trench MOSFET structure like that shown in Fig. 6 is described in connection with Fig. 12A and Fig. 12B. The method is essentially the same as that discussed above in connection with Figs. 8A through 8F, except that the polysilicon layer within the trench segment is more heavily over-etched, such that the polysilicon gate regions 211g within the trenches typically have top surfaces that are 0.1 to 0.5 microns below the adjacent surface of the epitaxial layer 204. The patterned masking layer, which served to preserve polysilicon in the gate runner region, is removed and a refractory metal layer 211m such as a titanium layer is deposited, for example, by sputtering, to produce the structure of Fig. 12A. The refractory metal is then alloyed with polysilicon in the trench by rapid thermal anneal, forming refractory metal silicide regions 211ms (in this case titanium silicide ($TiSi_2$)). The non reacted Ti portion on the oxide layer is removed after $TiSi_2$ is formed in trench region. The steps described above in connection with Fig. 8G are then preformed, producing the device of Fig. 12B.

**[0068]** A method of producing a trench MOSFET structure like that shown in Fig. 7

is described in connection with Fig. 12C. The method is essentially the same as that discussed above in connection with Fig. 10A through Fig.10G. After applying the patterned masking layer to preserve polysilicon in the gate runner region, the procedures discussed in connection with Fig. 12A and Fig. 12B above are followed, producing the structure of Fig. 12C.

[0069] Although various embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and are within the purview of the appended claims without departing from the spirit and intended scope of the invention. As one example, the method of the present invention may be used to form a structure in which the conductivities of the various semiconductor regions are reversed from those described herein.

CLAIMS:

1. A trench MOSFET device comprising:

a silicon substrate of a first conductivity type;

a silicon epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

a body region of a second conductivity type within an upper portion of said epitaxial layer;

a trench extending into said epitaxial layer from an upper surface of said epitaxial layer, said trench extending through said body region, and said trench having trench sidewalls and a trench bottom;

an oxide region lining said trench, said oxide region comprising a lower segment covering at least the trench bottom and upper segments covering at least upper regions of said trench sidewalls;

a conductive region within said trench adjacent said oxide region; and

a source region of said first conductivity type within an upper portion of said body region and adjacent said trench,

wherein said lower segment of said oxide region is thicker than said upper segments of said oxide region such that shoulders are established in said oxide region adjacent said conductive region along said trench sidewalls.

2. The trench MOSFET device of claim 1, wherein said lower segment of said oxide region consists of a thermally grown portion adjacent said trench and a deposited oxide portion adjacent said conductive region, and wherein said upper segments of said oxide region consists of thermally grown oxide.

3. The trench MOSFET device of claim 2, wherein said deposited oxide portion is densified TEOS.

4. The trench MOSFET device of claim 2, wherein said thermally grown portion ranges from 500 to 2000 Angstroms in thickness.

5. The trench MOSFET device of claim 2, wherein said deposited oxide portion ranges from 500 to 2000 Angstroms in thickness.

6. The trench MOSFET device of claim 2, wherein said upper segment of said oxide region ranges from 100 to 1000 Angstroms in thickness.

7. The trench MOSFET device of claim 1, wherein said lower segment of said oxide region is a thick thermally grown oxide region, and wherein said upper segments of said oxide region are thin thermally grown oxide regions.

8. The trench MOSFET device of claim 7, wherein said thick thermally grown oxide region ranges from 500 to 2000 Angstroms in thickness.

9. The trench MOSFET device of claim 7, wherein said thin thermally grown oxide region ranges from 100 to 1000 Angstroms in thickness.

10. The trench MOSFET device of claim 1, wherein the conductive region comprises polycrystalline silicon.

11. The trench MOSFET device of claim 1, wherein the conductive region comprises a polycrystalline silicon portion and a portion selected from a refractory metal and a refractory metal alloy.

12. The trench MOSFET device of claim 11, wherein the conductive region comprises a polycrystalline silicon portion and a tungsten portion.

13. The trench MOSFET device of claim 11, wherein the conductive region comprises a polycrystalline silicon portion and a titanium-tungsten alloy portion.

14. The trench MOSFET device of claim 1, wherein the conductive region comprises a polycrystalline silicon portion and a refractory metal silicide portion.

15. The trench MOSFET device of claim 14, wherein the conductive region comprises a polycrystalline silicon portion and a titanium silicide portion.

16. The trench MOSFET device of claim 1, wherein said first conductivity type is N-type conductivity and said second conductivity type is P-type conductivity.

17. A method of forming a trench MOSFET device comprising:

providing a silicon substrate of a first conductivity type;

depositing a silicon epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

forming a body region of a second conductivity type within an upper portion of said epitaxial layer;

etching a trench extending into said epitaxial layer from an upper surface of said epitaxial layer, said trench extending through said body region and said trench having trench sidewalls and a trench bottom;

forming an oxide region lining said trench, said oxide region comprising a lower segment covering at least the trench bottom and upper segments covering at least upper regions of said trench sidewalls;

depositing a conductive region within said trench adjacent said oxide region; and

forming a source region of said first conductivity type within an upper portion of said body region and adjacent said trench,

wherein said lower segment of said oxide region is thicker than said upper segments of said oxide region such that shoulders are established in said oxide region adjacent said conductive region along said trench sidewalls.

18. The method of claim 17, wherein said oxide region lining said trench is formed by a process comprising:

forming a thermal oxide layer within said trench;

providing a deposited oxide layer over said thermal oxide layer;

forming an etch resistant region in the trench bottom over said deposited oxide layer; and

etching said deposited oxide layer where not covered by said etch resistant region.

19. The method of claim 18, wherein said etch resistant region is a photoresist region.

20. The method of claim 18, wherein said etch resistant region is a polysilicon region.

21. The method of claim 18, wherein a thermal oxidation step is carried out after said deposited oxide-etching step.

22. The method of claim 17, wherein said oxide region lining said trench is formed by a process comprising:

forming a thick thermal oxide layer within said trench;

forming an etch resistant region in the trench bottom over said thick thermal oxide layer; and

etching said thermal oxide layer where not covered by said etch resistant region.

23. The method of claim 22, wherein said etch resistant region is a photoresist region.

24. The method of claim 22, wherein said etch resistant region is a polysilicon region.

25. The method of claim 22, wherein a thermal oxidation step is carried out after said thermal oxide etching step.

26. A trench MOSFET device comprising:

a silicon substrate of a first conductivity type;

a silicon epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

a body region of a second conductivity type within an upper portion of said epitaxial layer;

a trench extending into said epitaxial layer from an upper surface of said epitaxial layer, said trench extending through said body region, and said trench having trench sidewalls and a trench bottom;

an oxide region lining said trench, said oxide region comprising a lower segment covering at least the trench bottom and upper segments covering at least upper regions of said trench sidewalls, wherein said lower segment is substantially thicker than said upper segments;

a conductive region within said trench adjacent said oxide region; and

a source region of said first conductivity type within an upper portion of said body region and adjacent said trench,

wherein those portions of said oxide region that form interfaces with said silicon are thermally grown.

27. A trench MOSFET device comprising:

a silicon substrate of a first conductivity type;

a silicon epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

a body region of a second conductivity type within an upper portion of said epitaxial layer;

a trench extending into said epitaxial layer from an upper surface of said epitaxial layer, said trench extending through said body region, and said trench having trench sidewalls and a trench bottom;

an oxide region lining said trench, said oxide region comprising a u-shaped lower segment covering the trench bottom and lower regions of said trench sidewalls and upper segments covering upper regions of said trench sidewalls, wherein said lower segment of said oxide region is thicker than said upper segments;

a conductive region within said trench adjacent said oxide region; and
a source region of said first conductivity type within an upper portion of said body region and adjacent said trench.

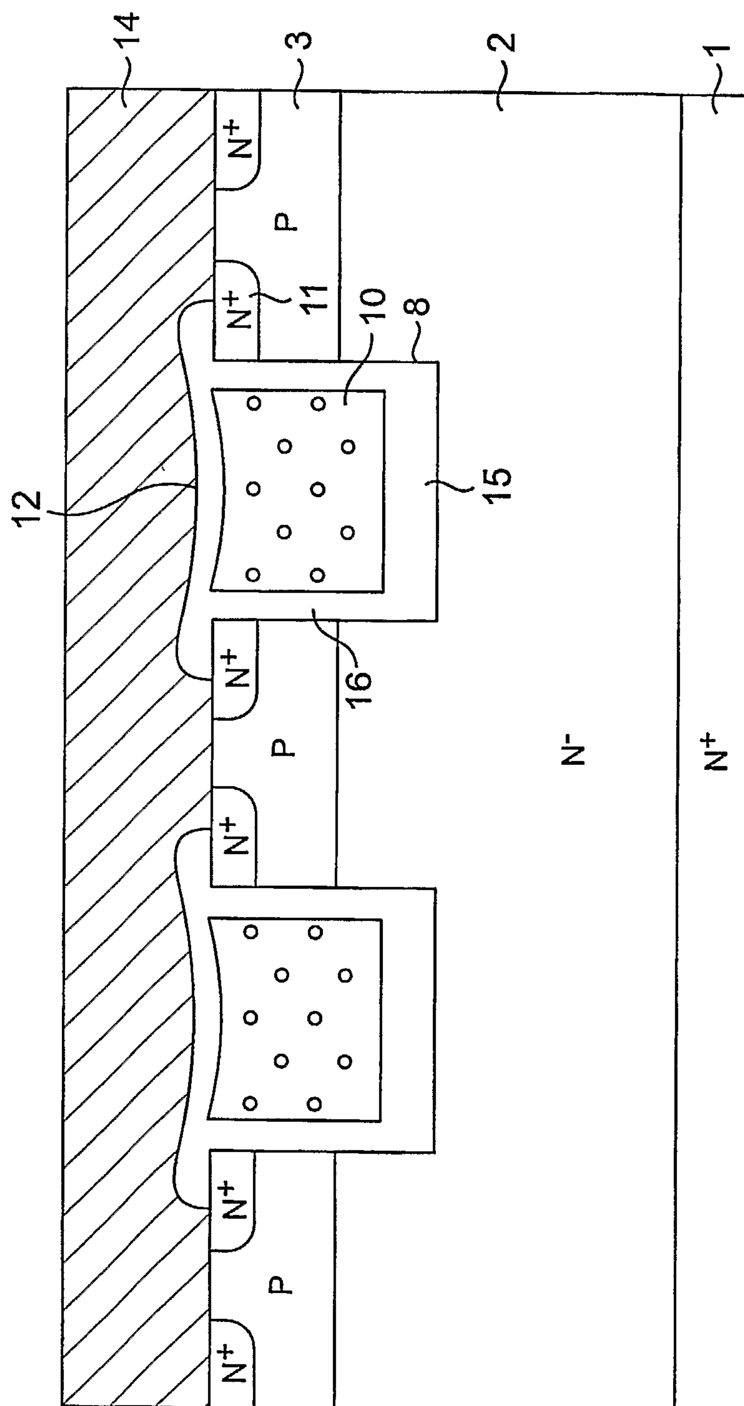


**FIG. 1**
**(PRIOR ART)**

FIG. 2

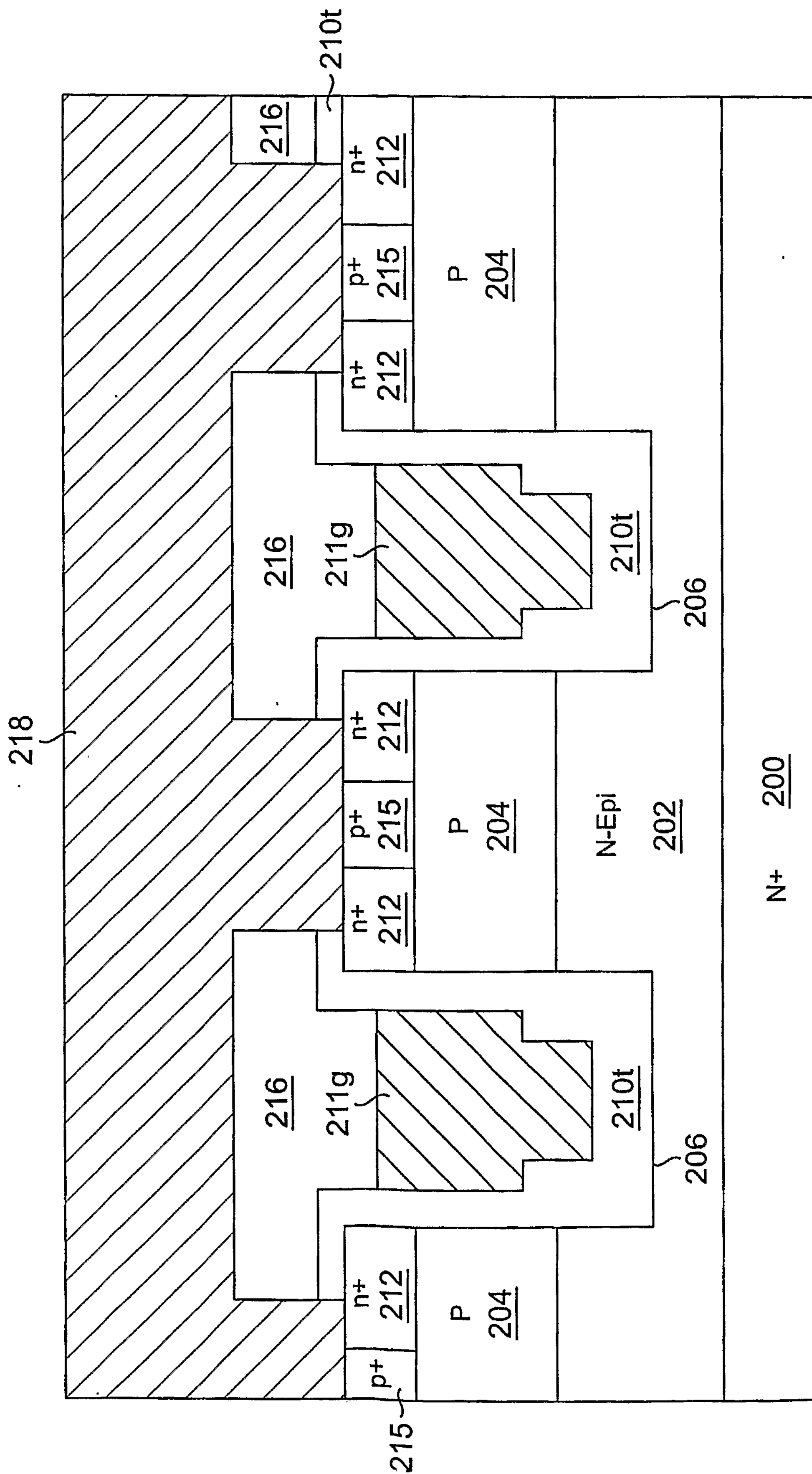


FIG. 3

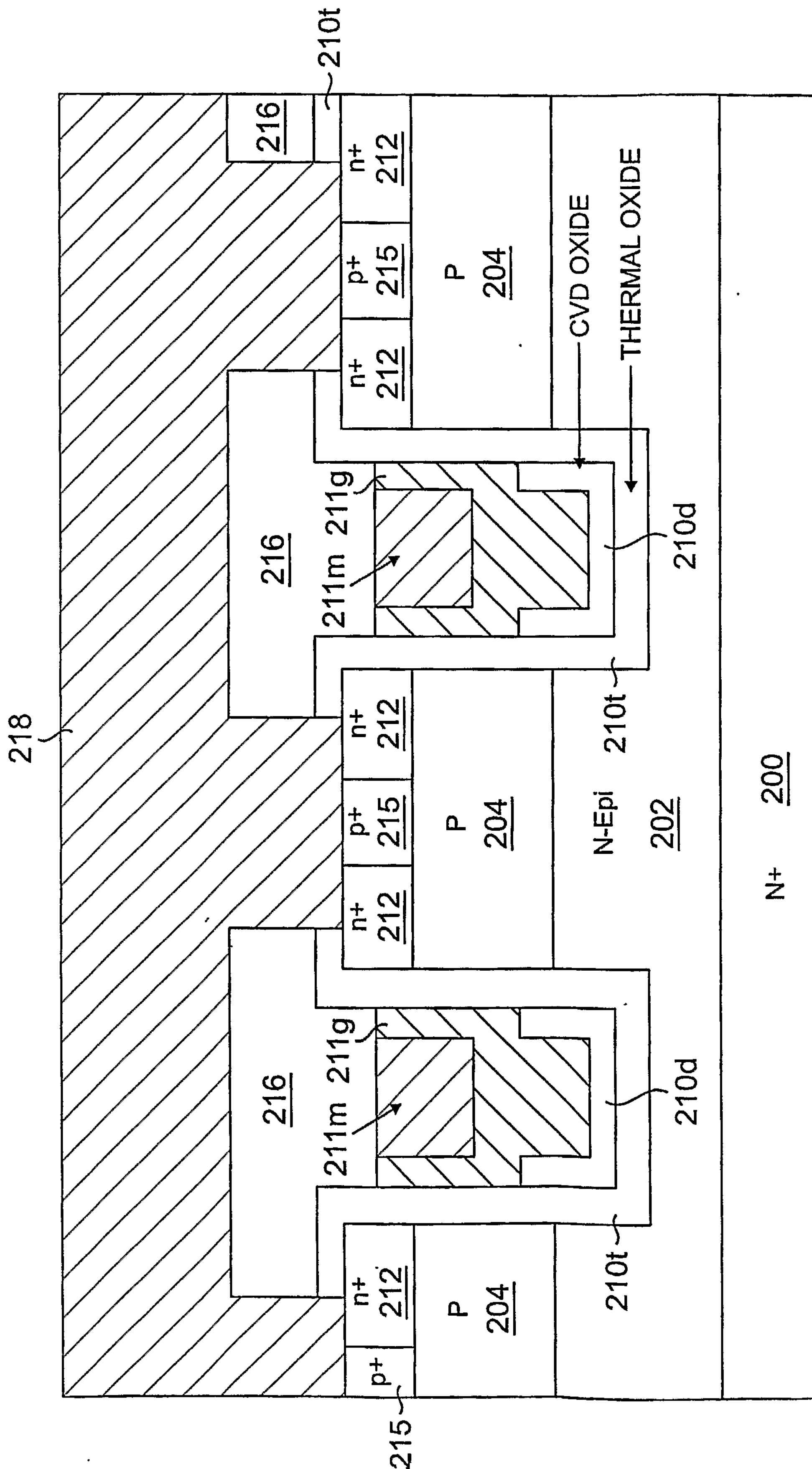


FIG. 4

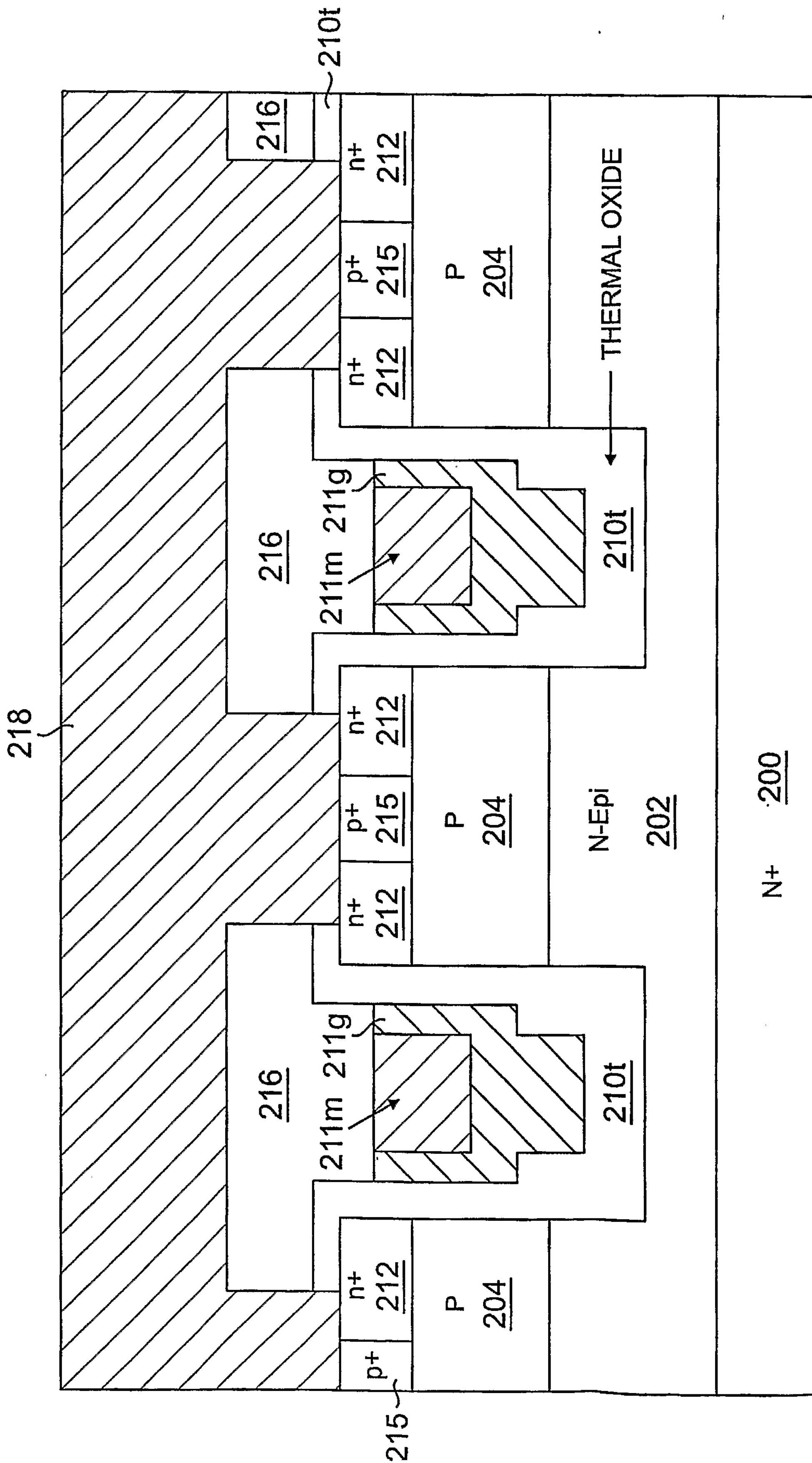


FIG. 5

FIG. 6

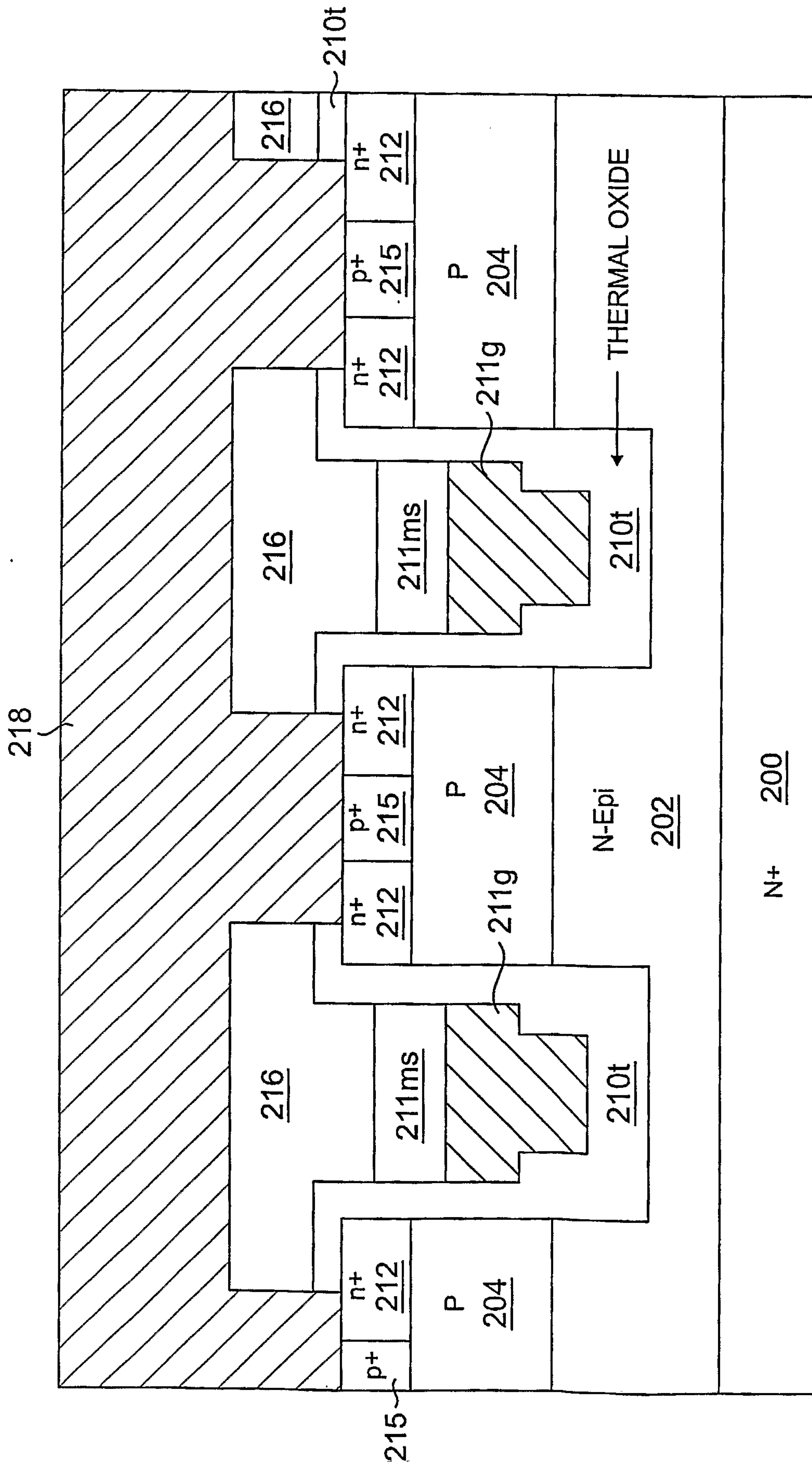


FIG. 7

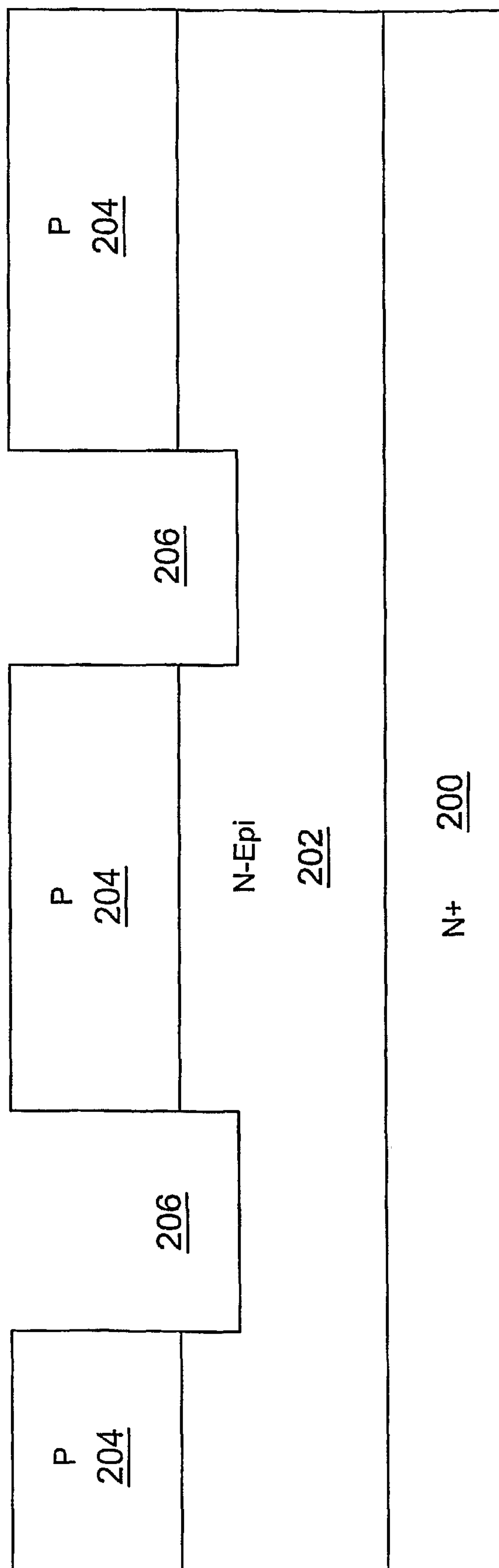


FIG. 8A

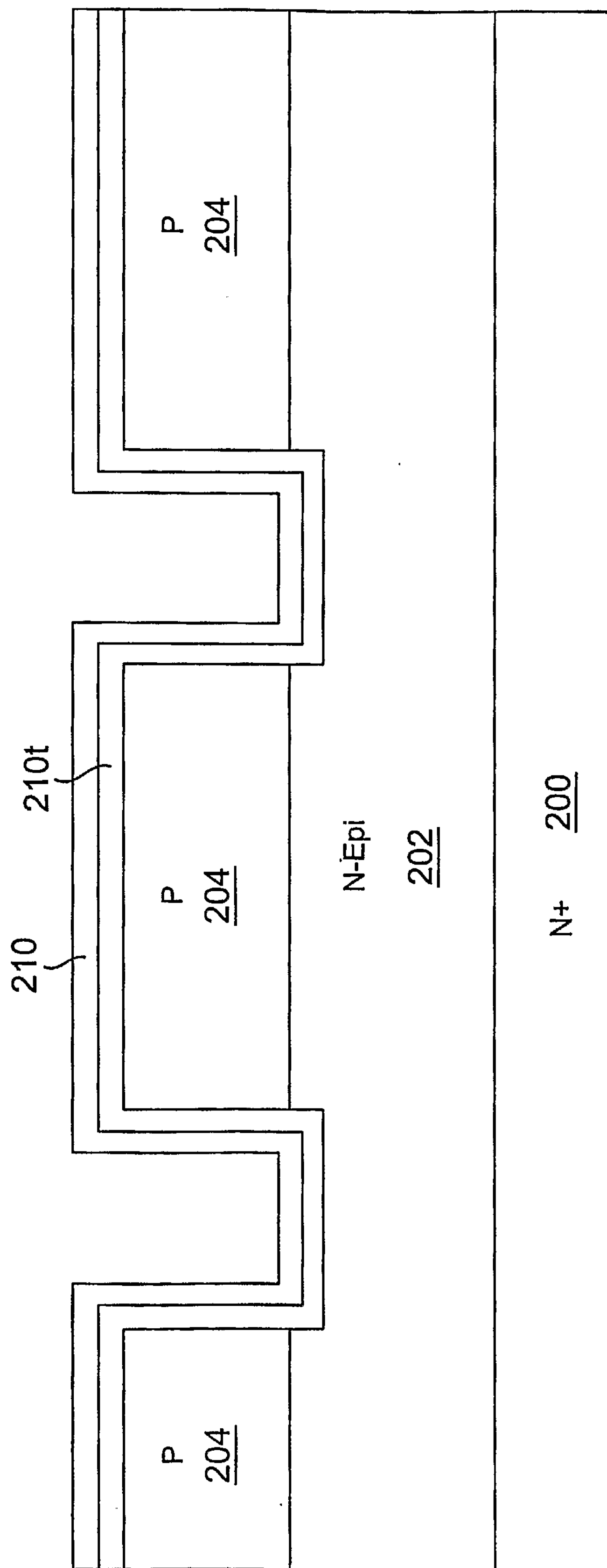


FIG. 8B

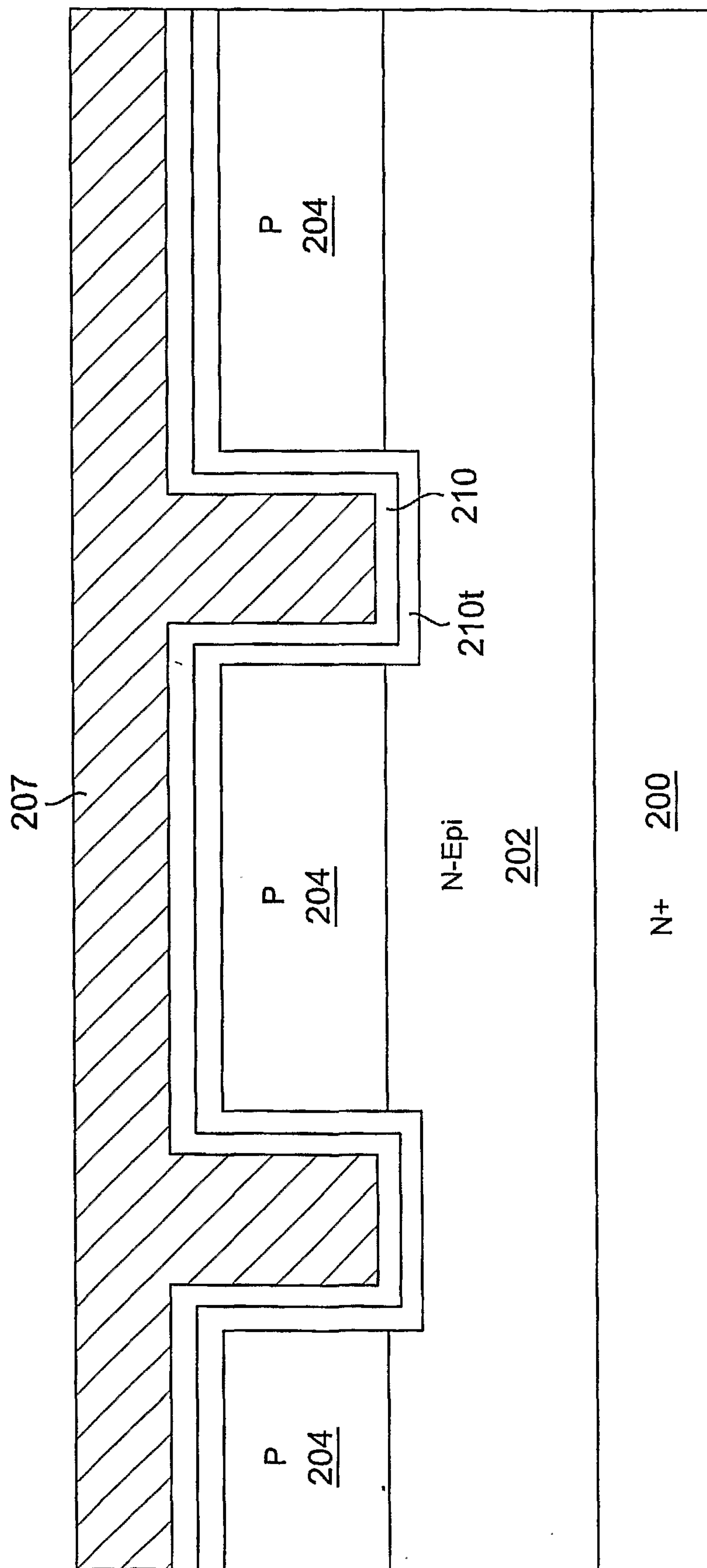


FIG. 8C

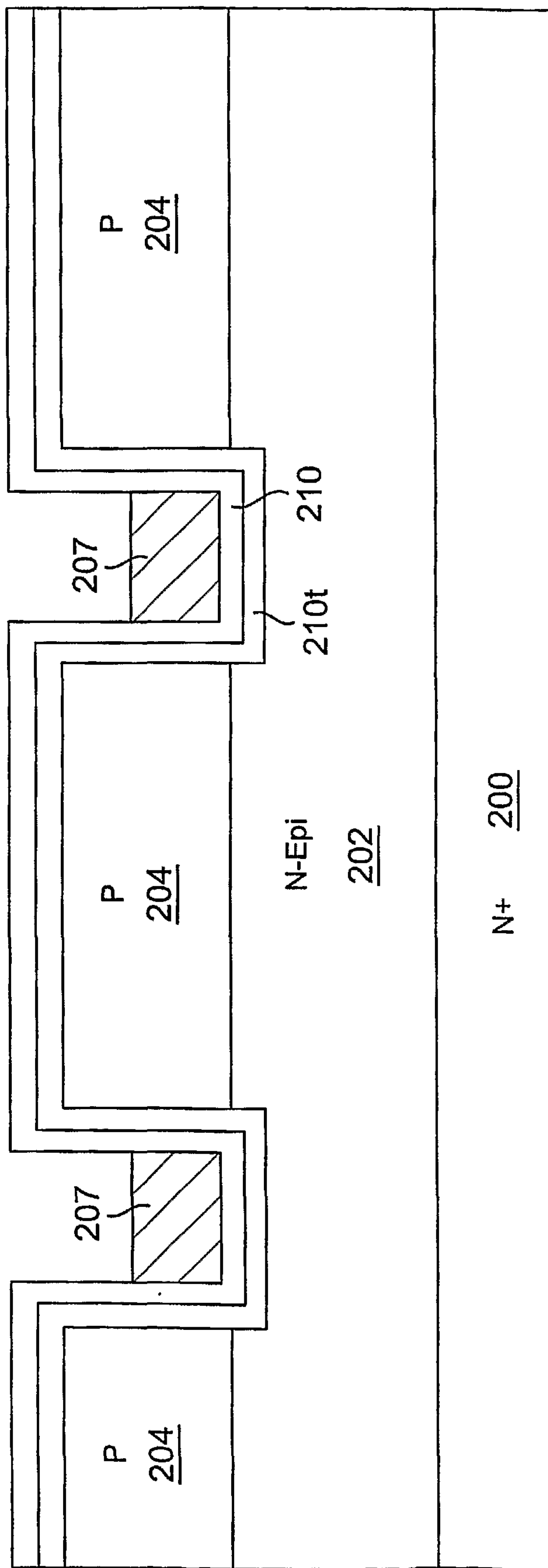


FIG. 8D

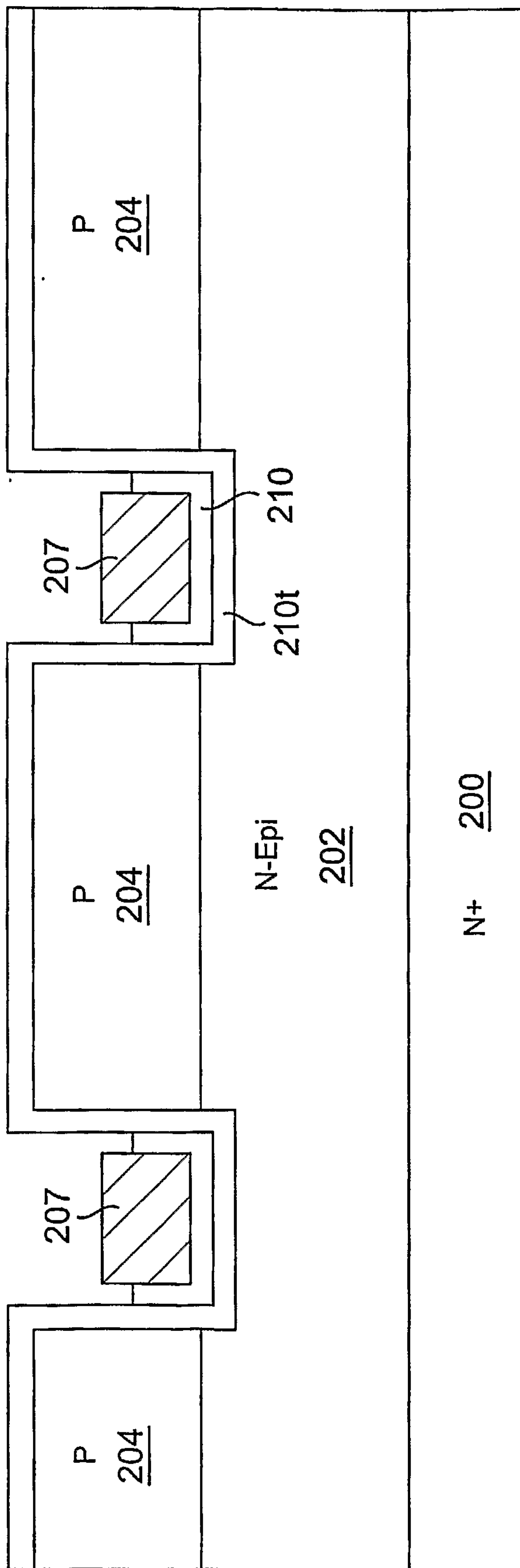


FIG. 8E

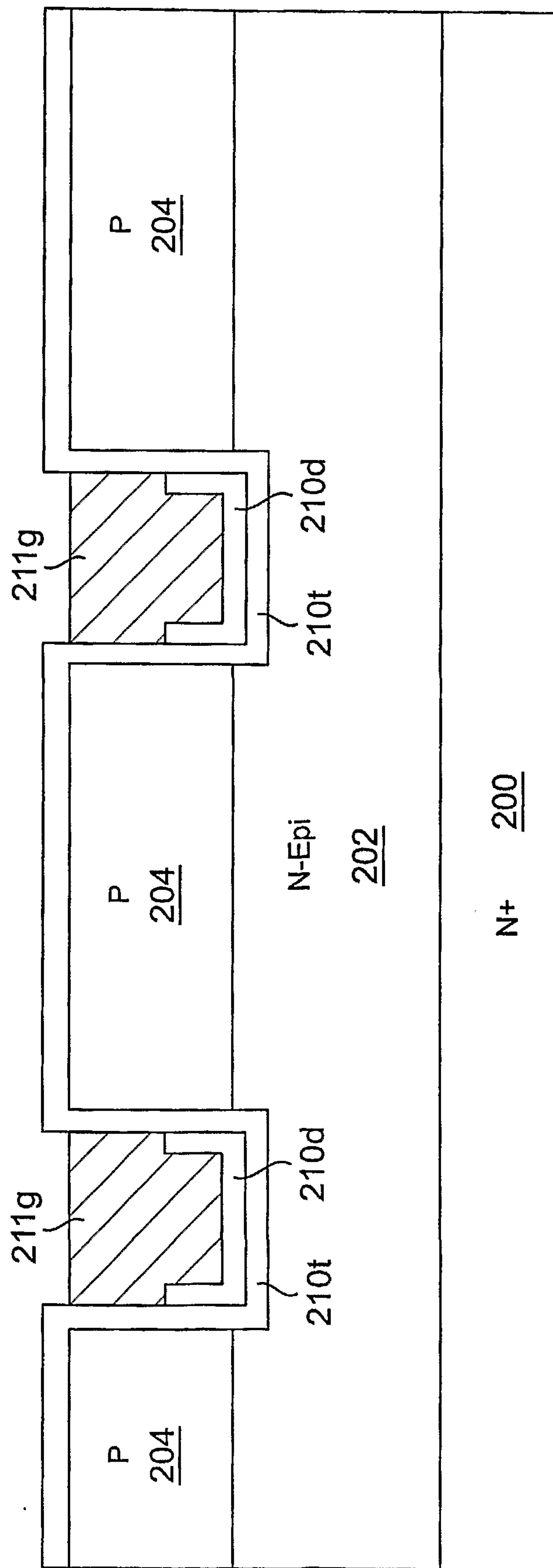


FIG. 8F

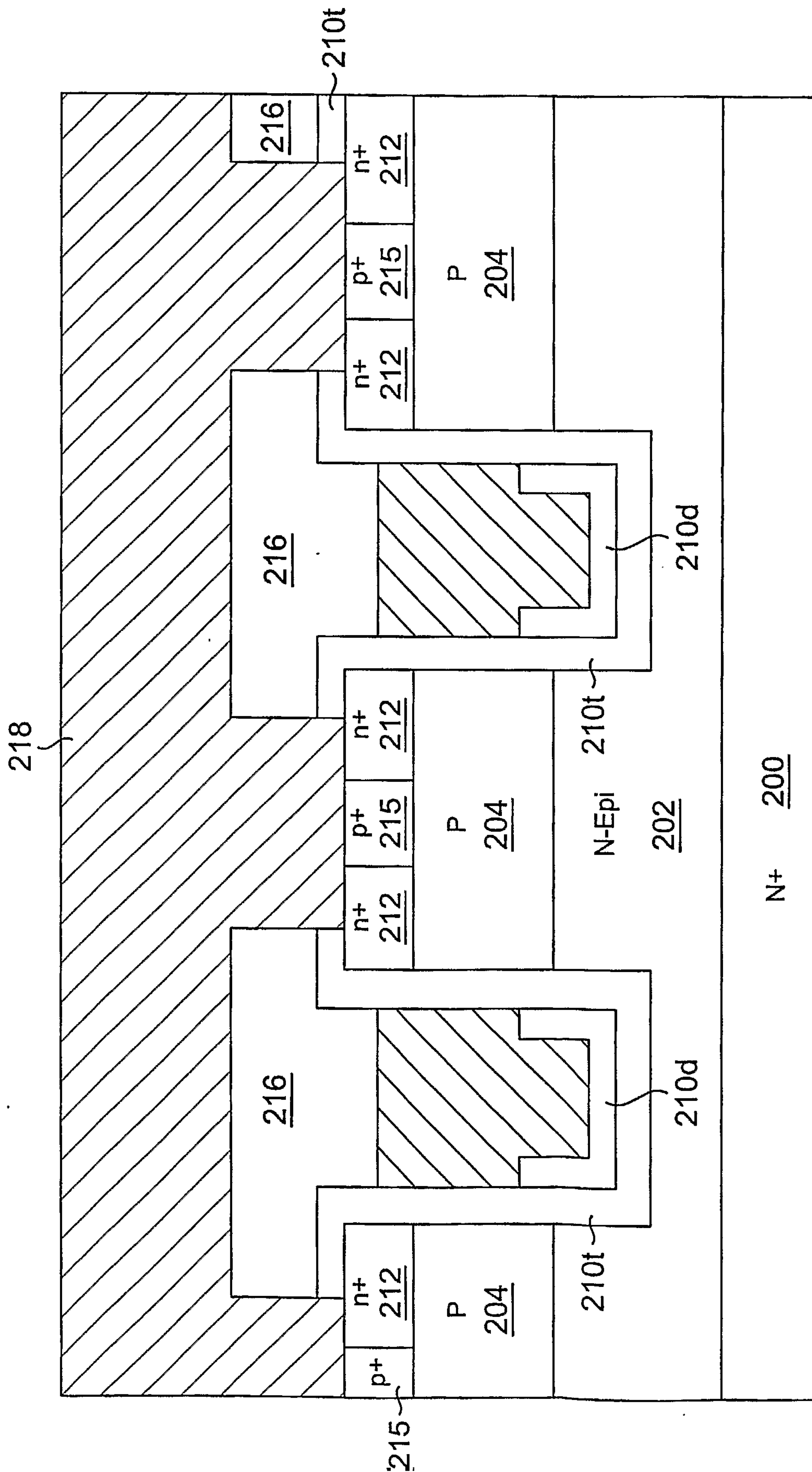


FIG. 8G

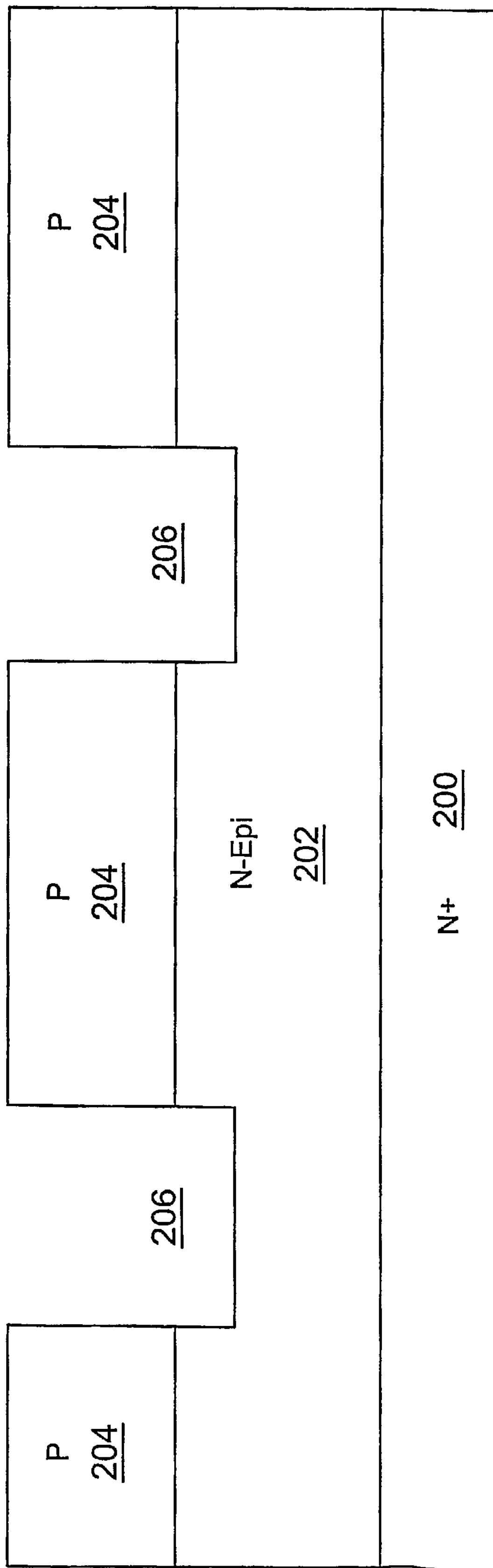


FIG. 9A

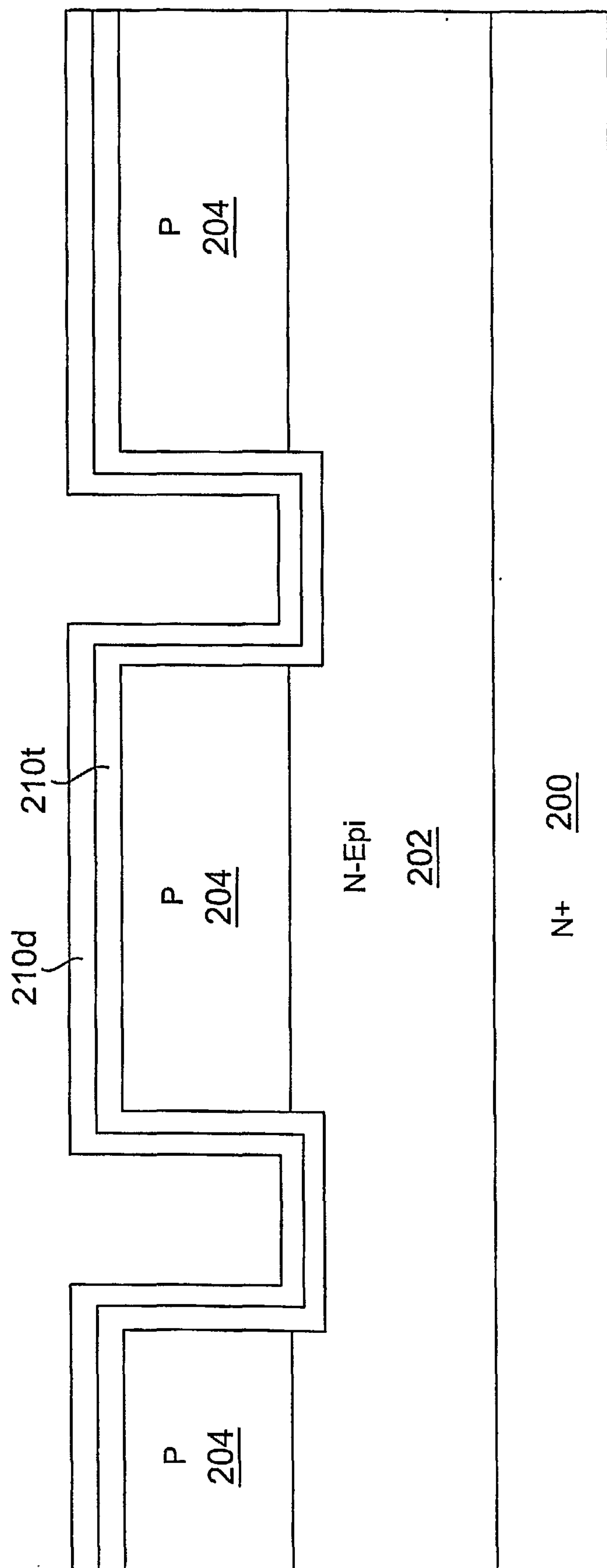


FIG. 9B

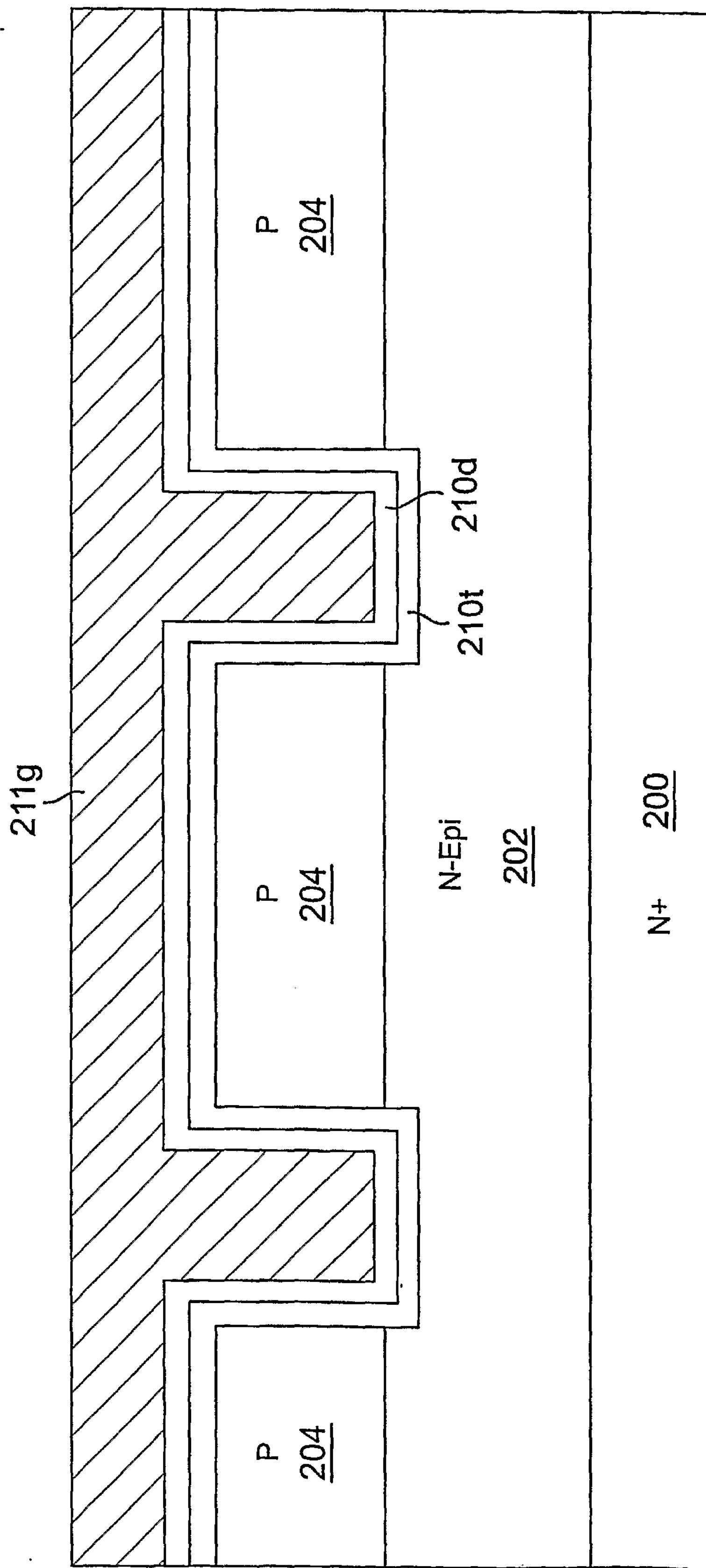


FIG. 9C

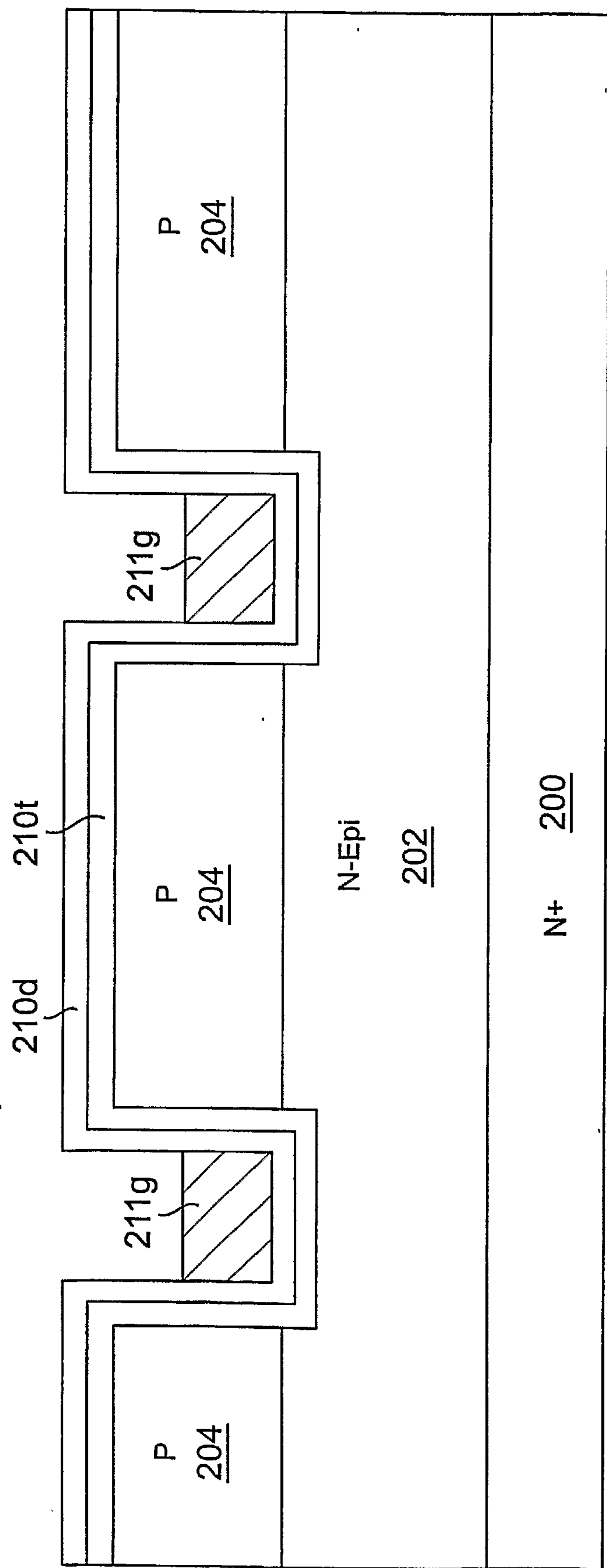


FIG. 9D

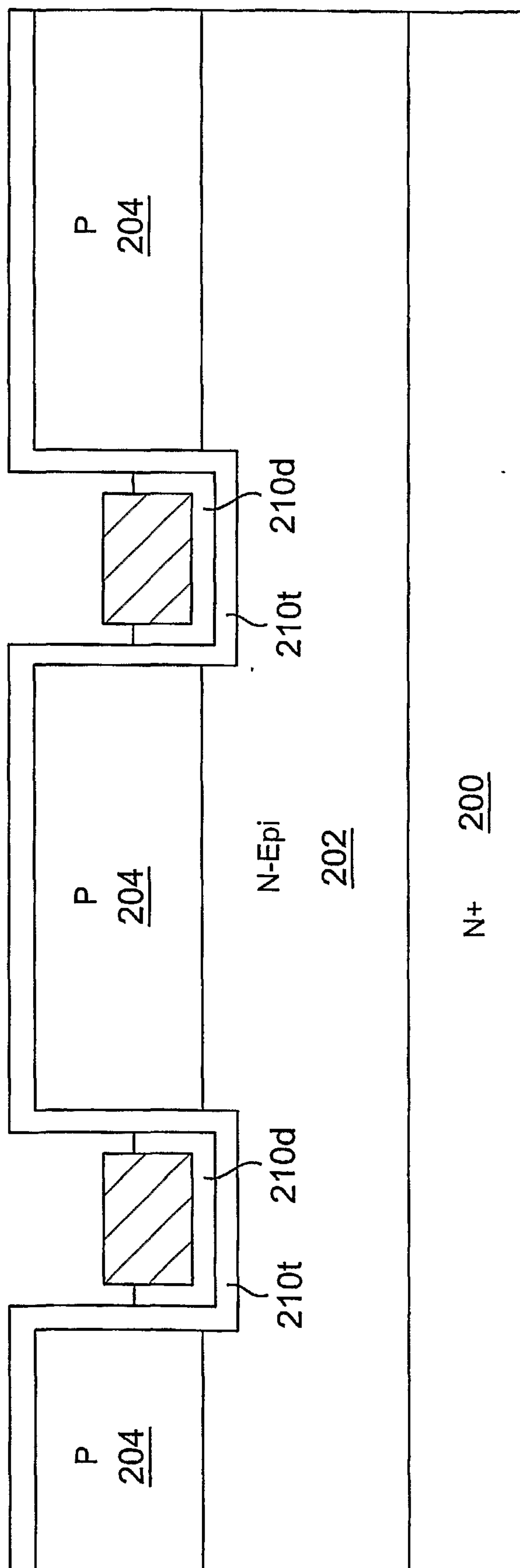


FIG. 9E

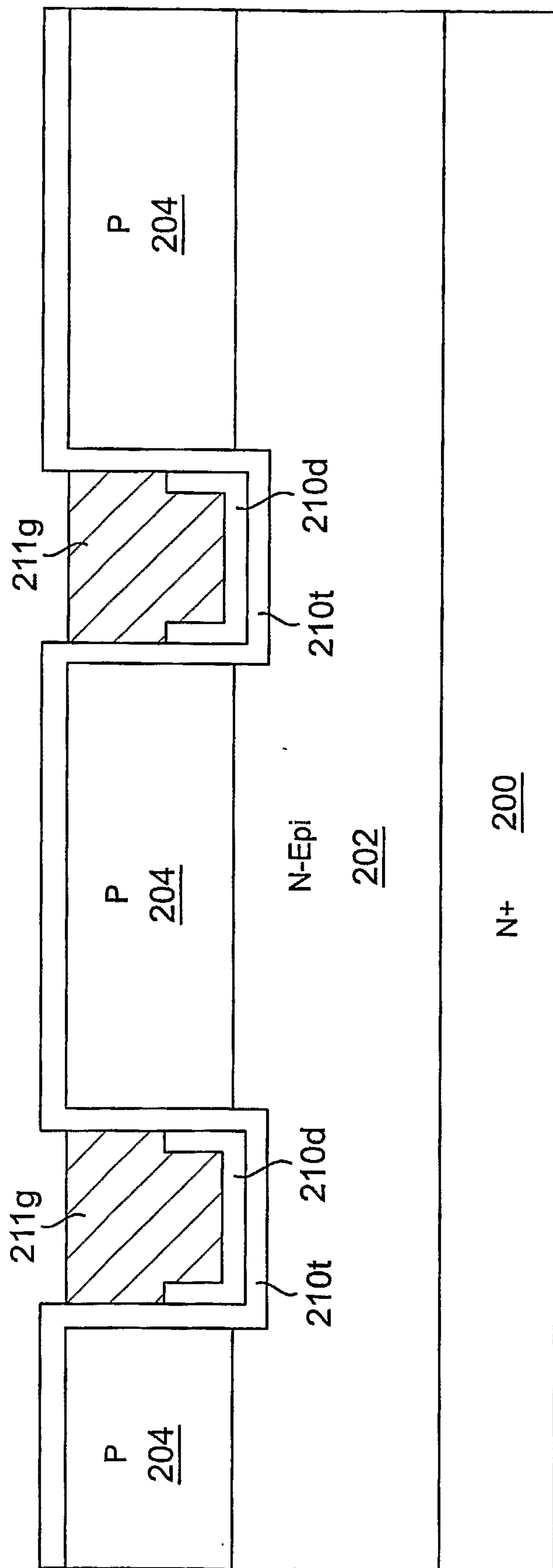


FIG. 9F

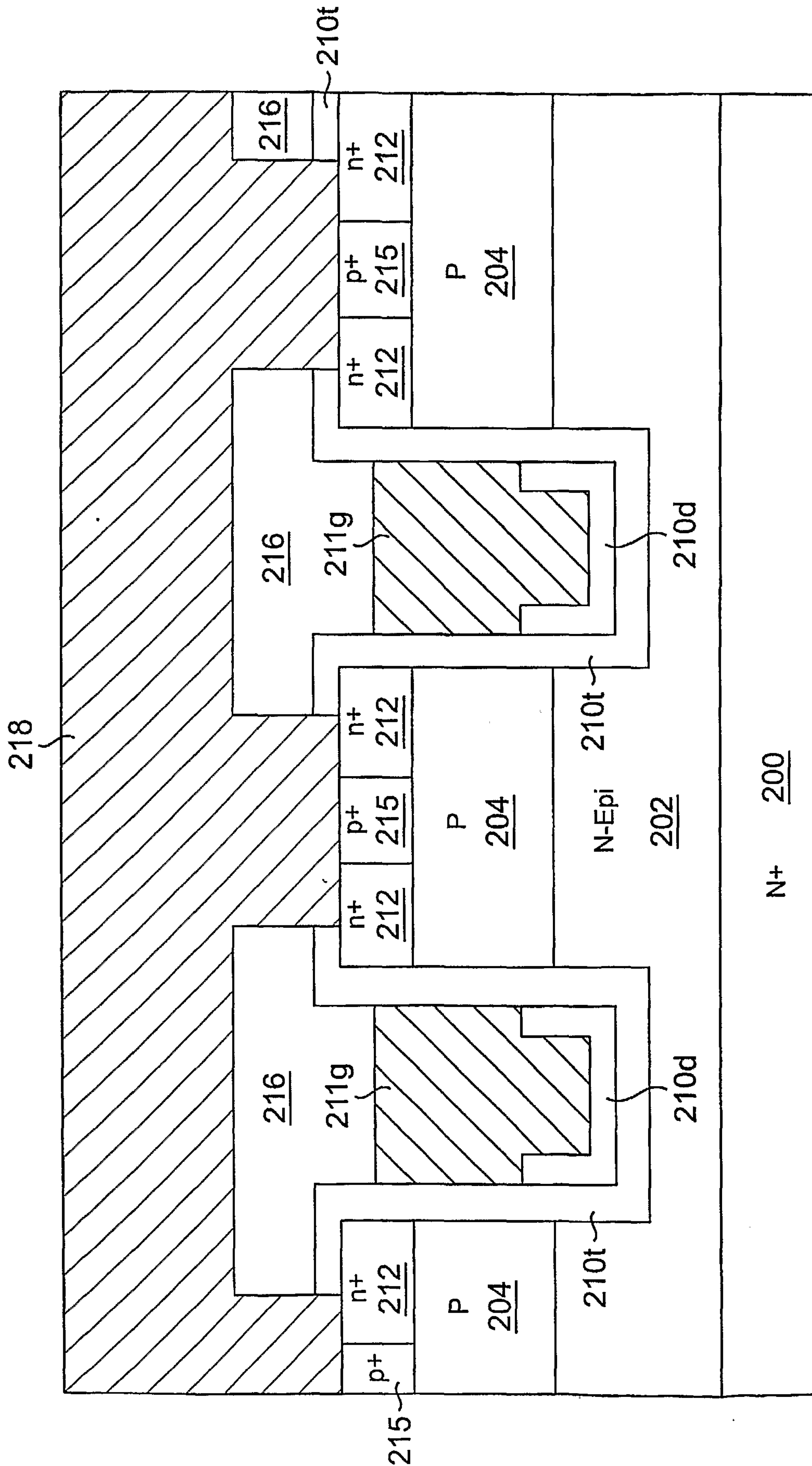


FIG. 9G

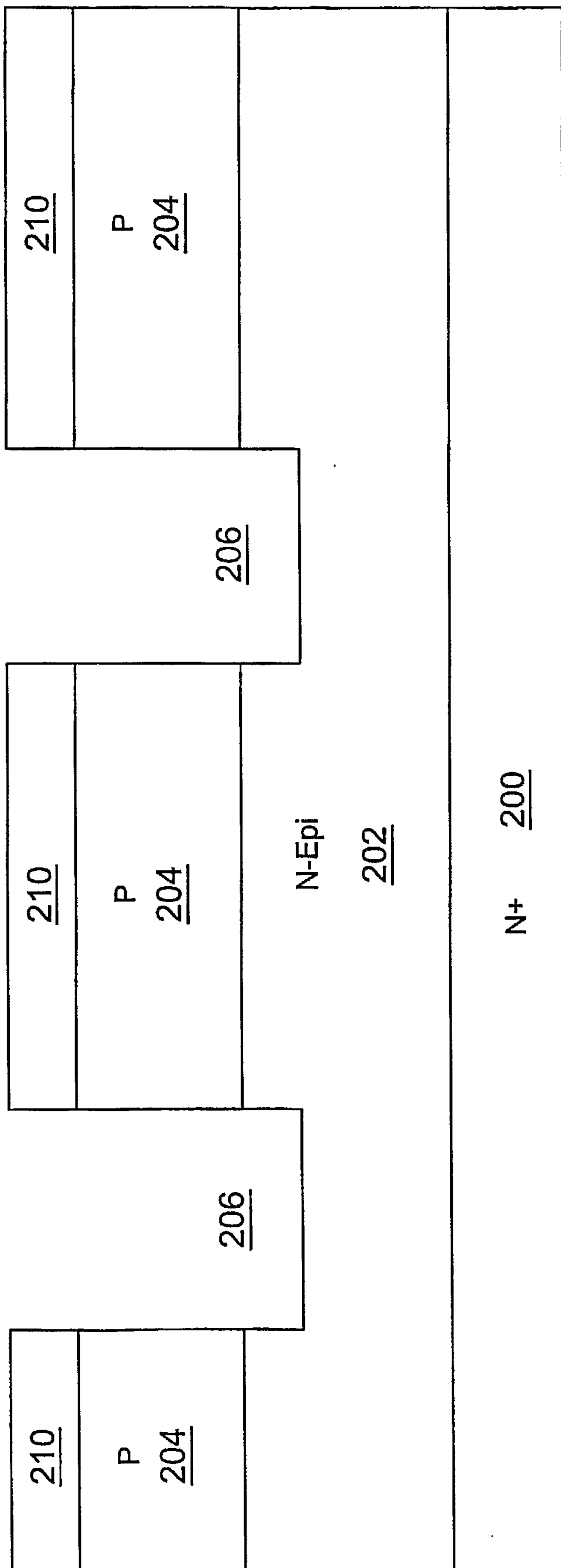


FIG. 10A

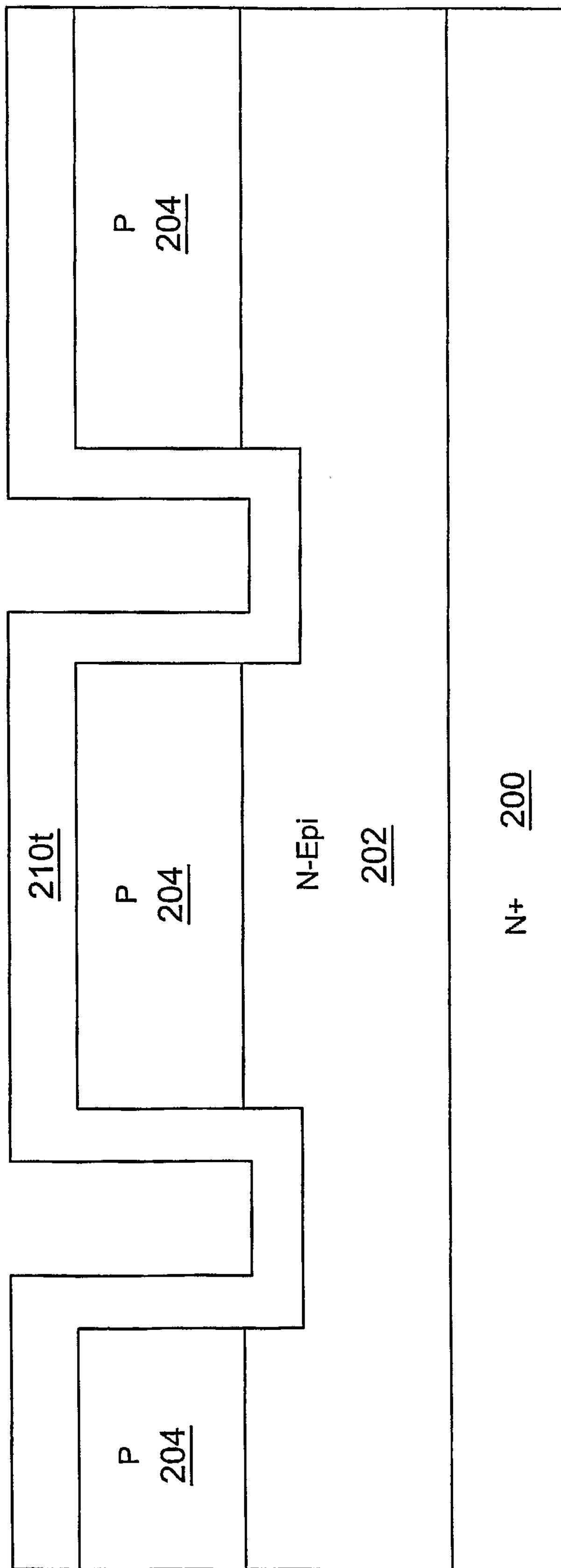


FIG. 10B

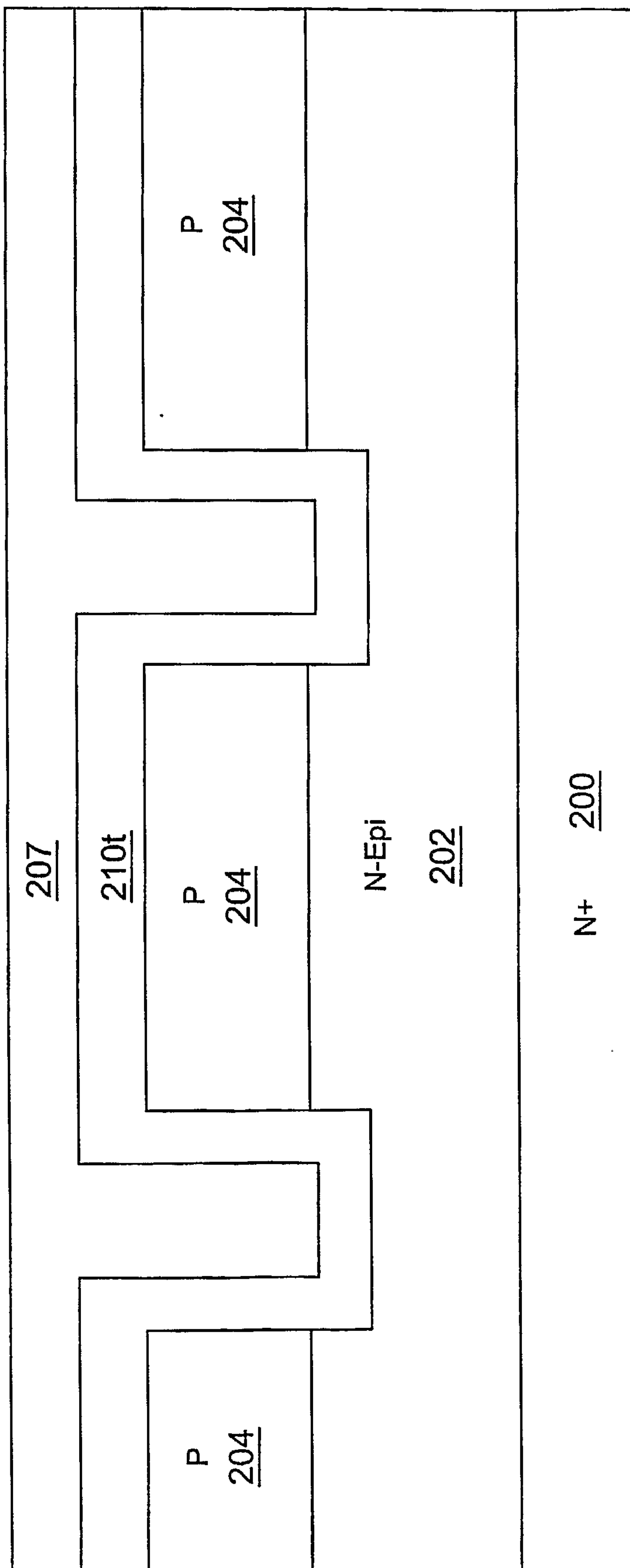


FIG. 10C

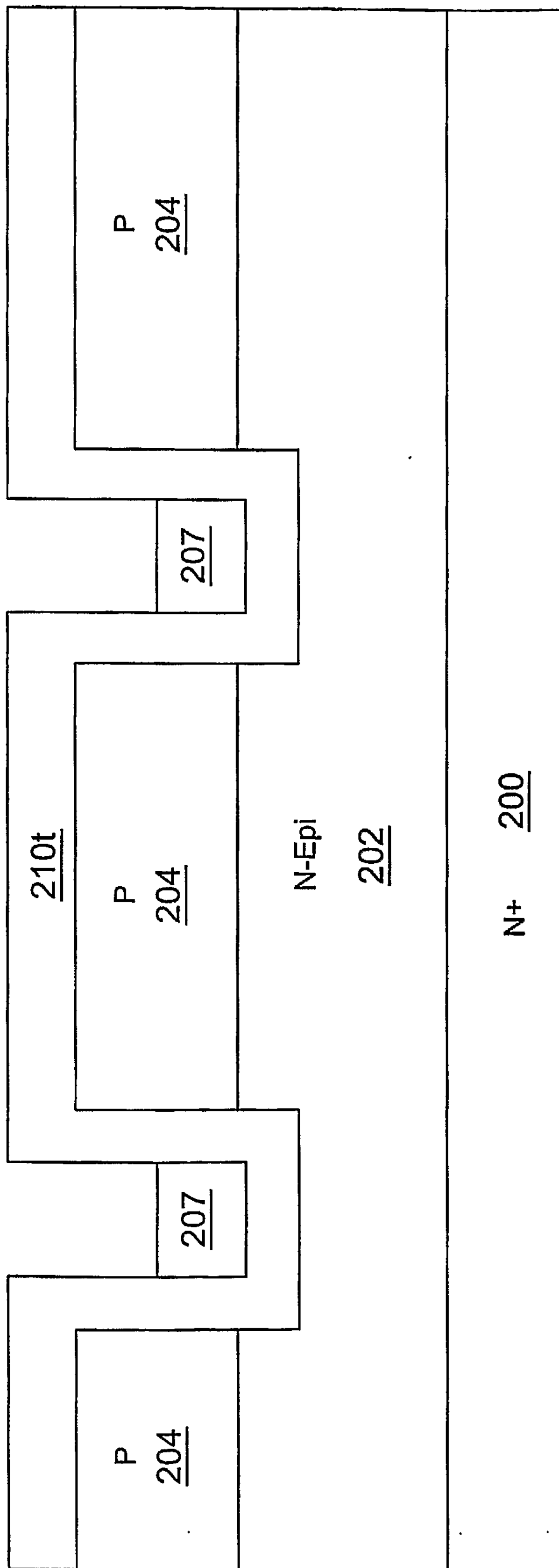


FIG. 10D

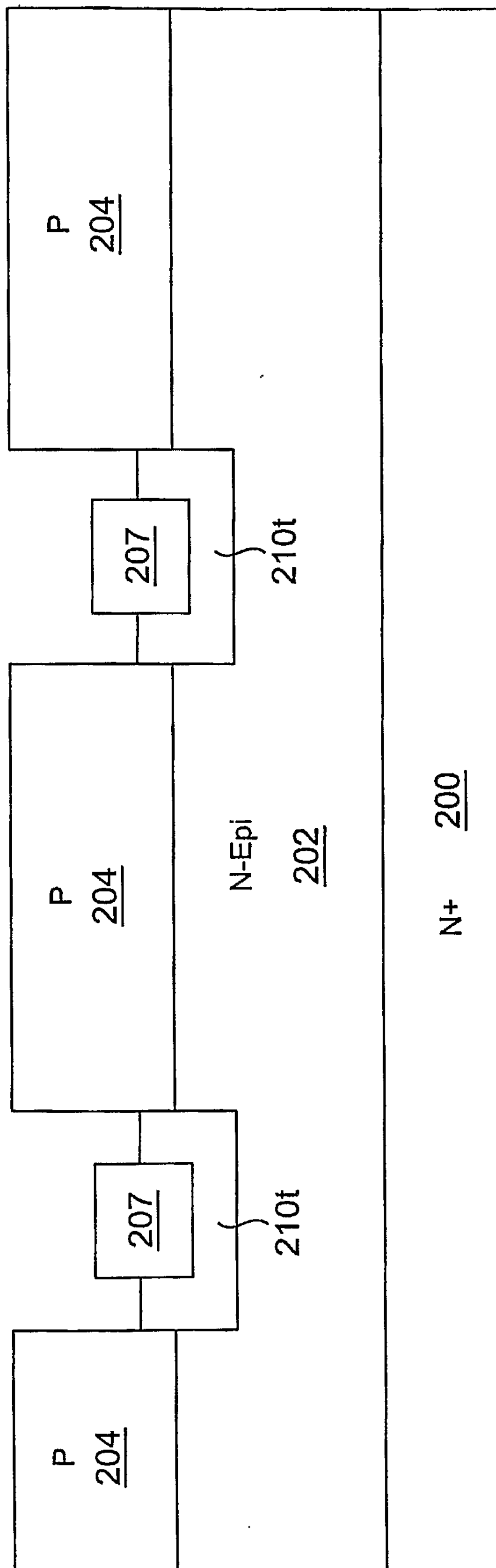


FIG. 10E

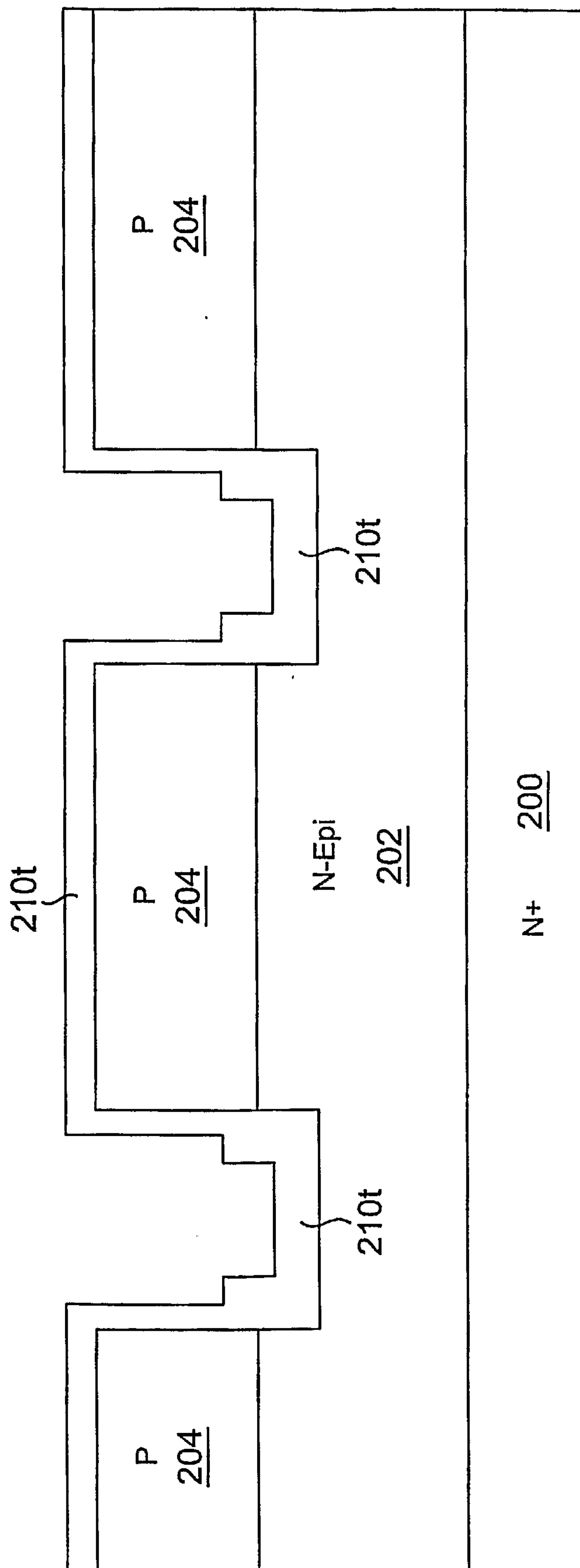


FIG. 10F

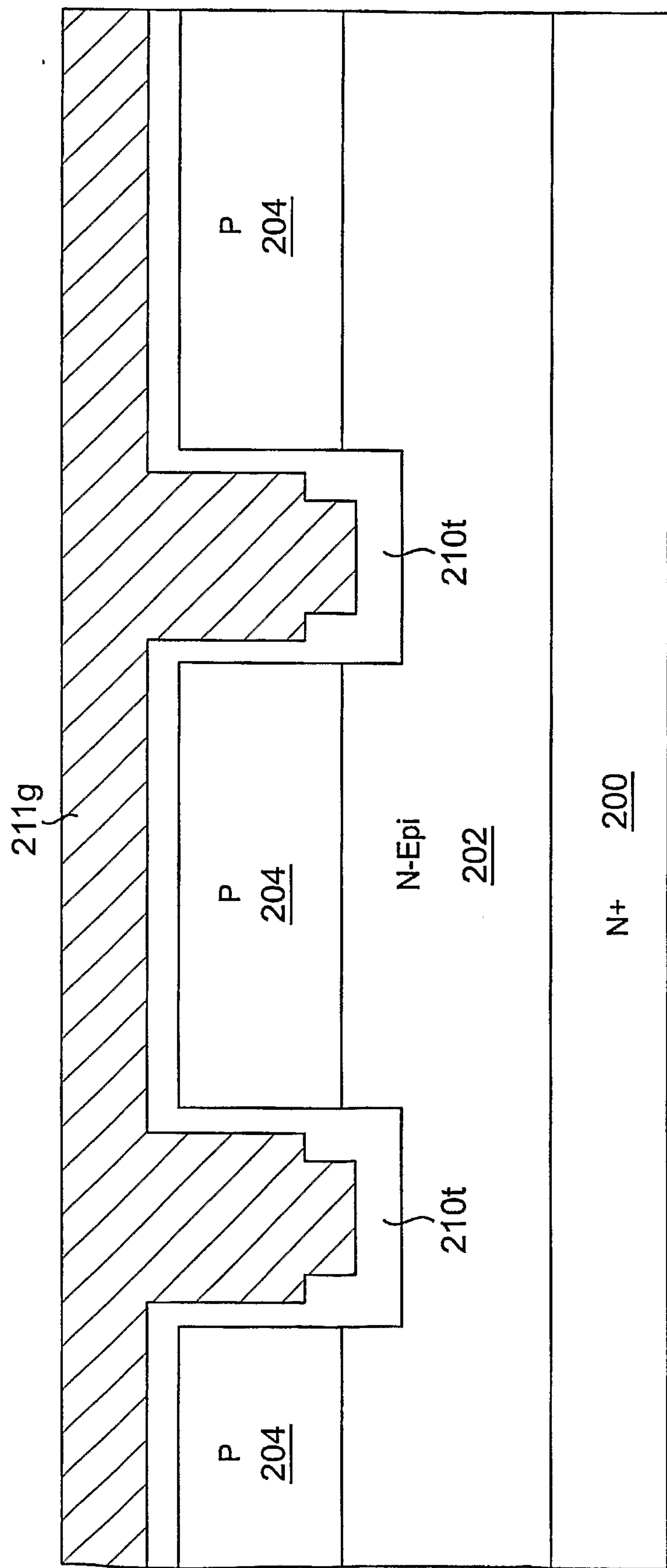


FIG. 10G

FIG. 10H

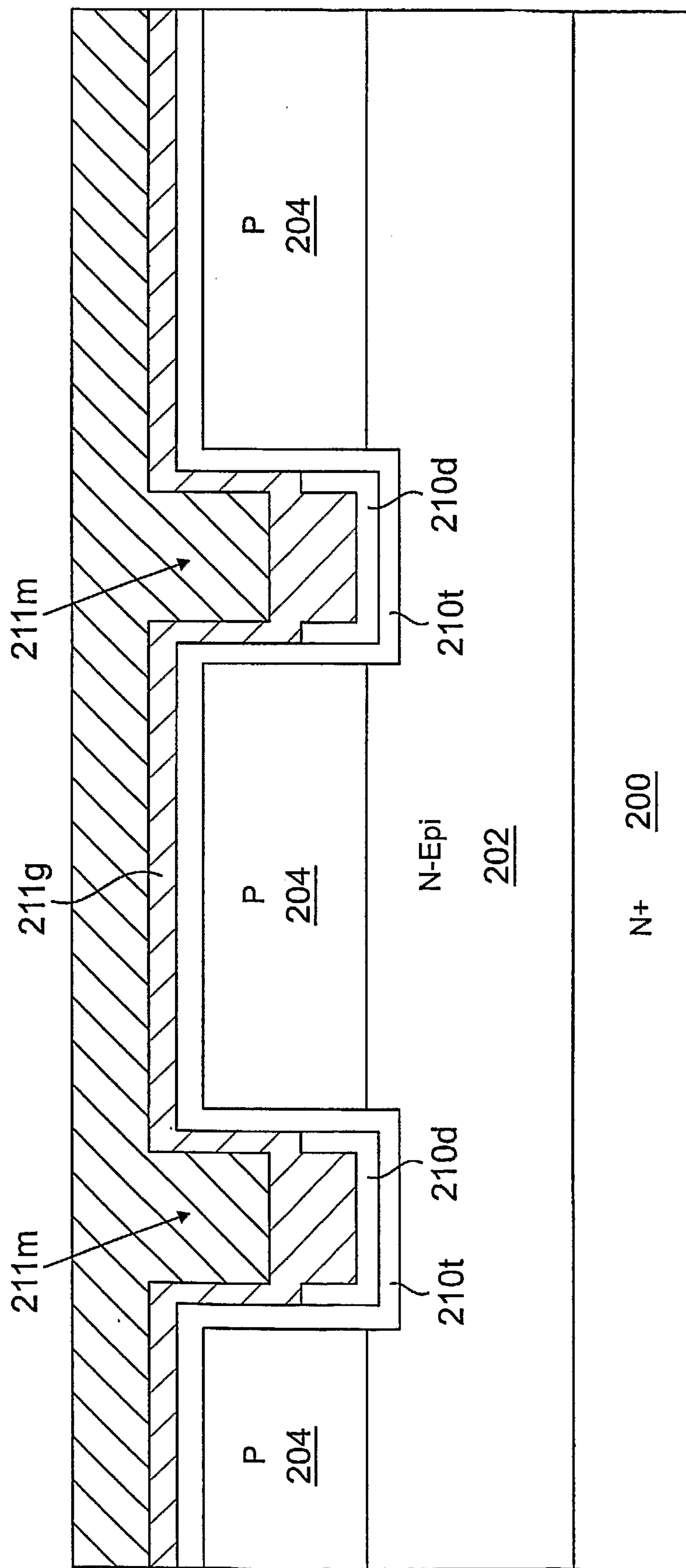


FIG. 11A

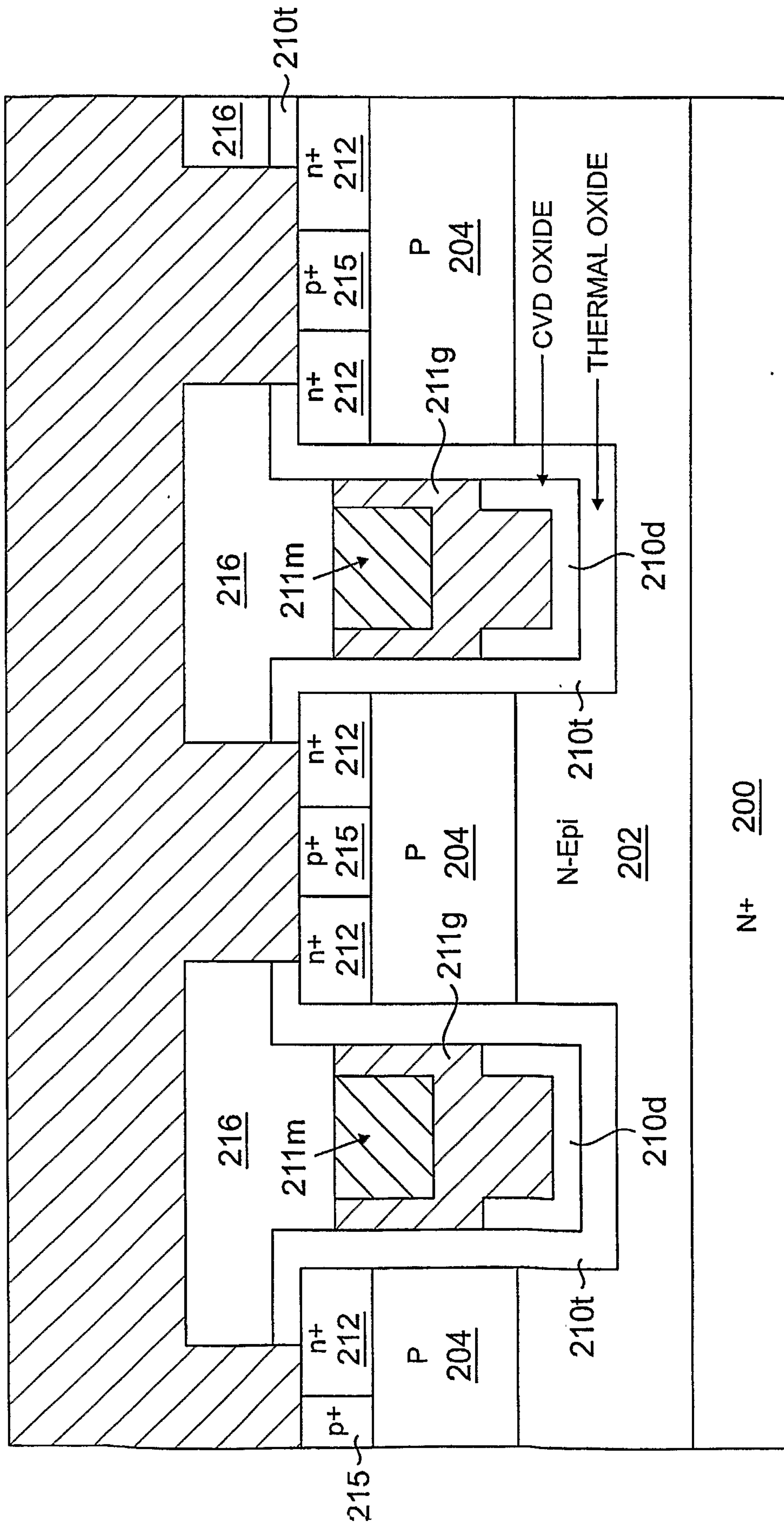


FIG. 11B

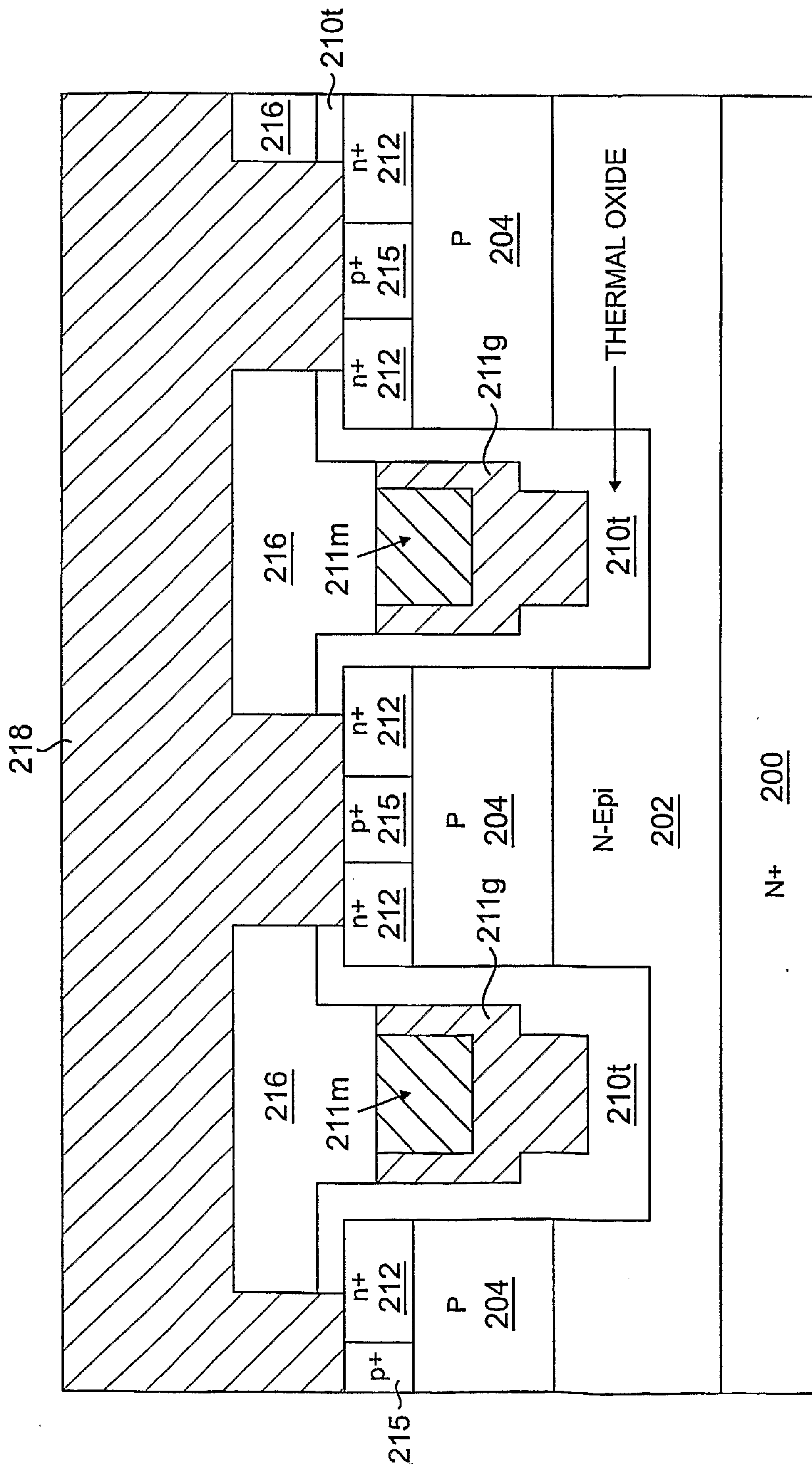


FIG. 11C

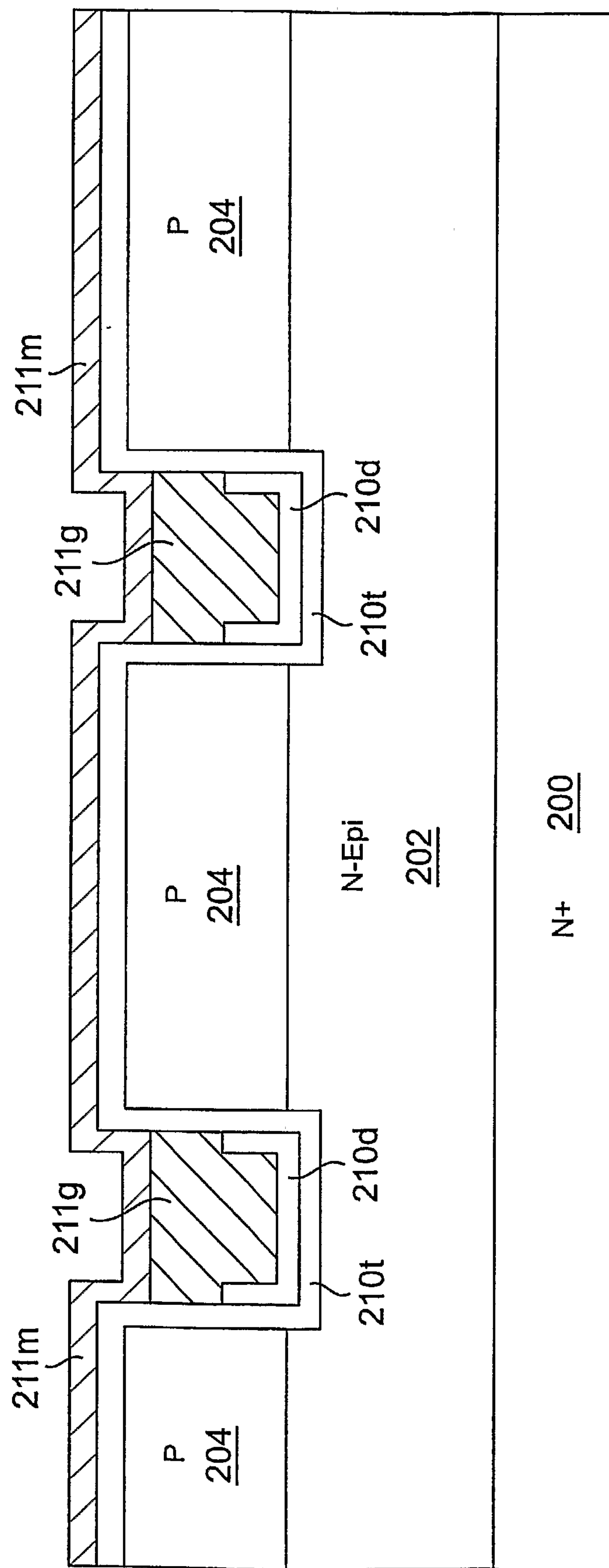


FIG. 12A

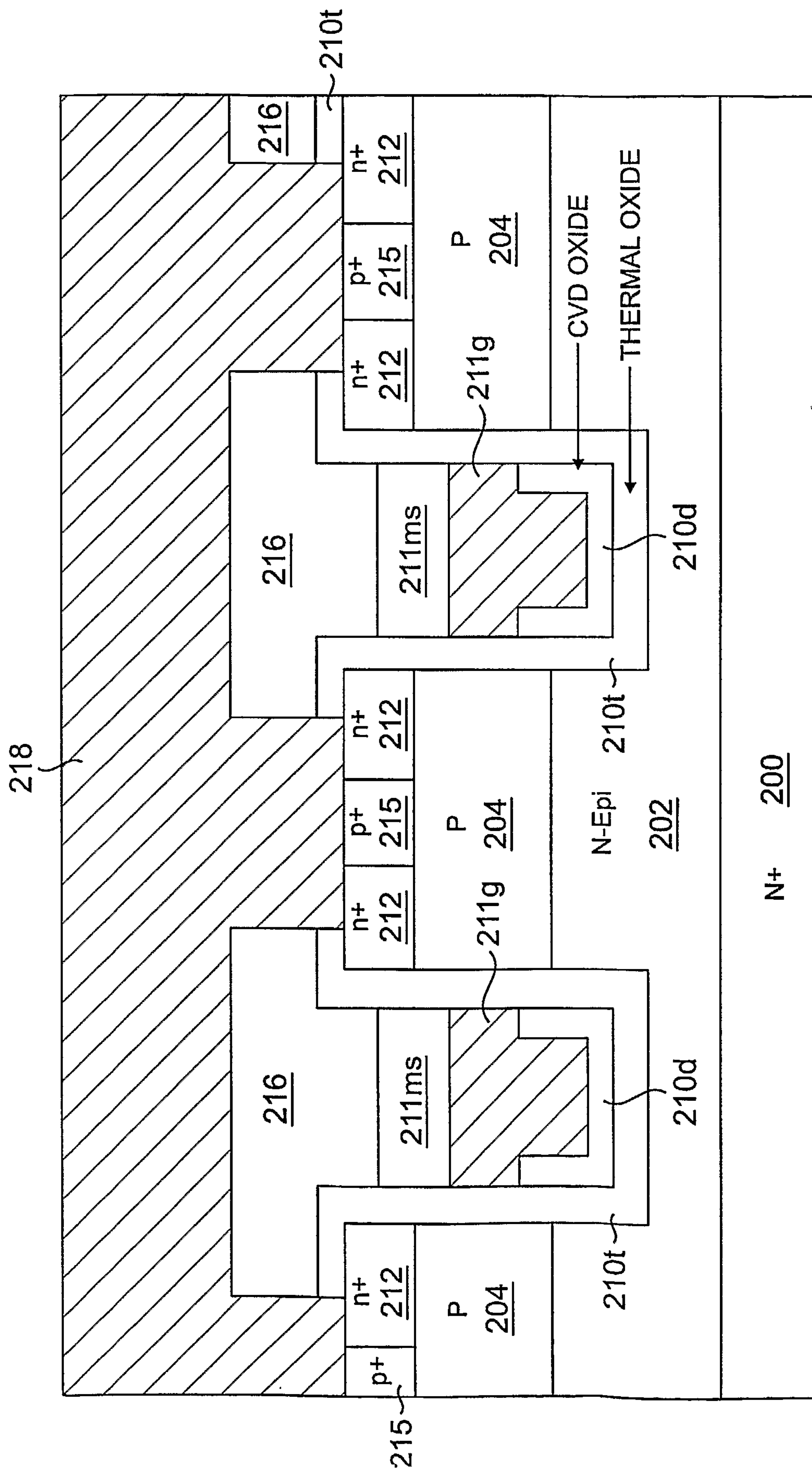


FIG. 12B

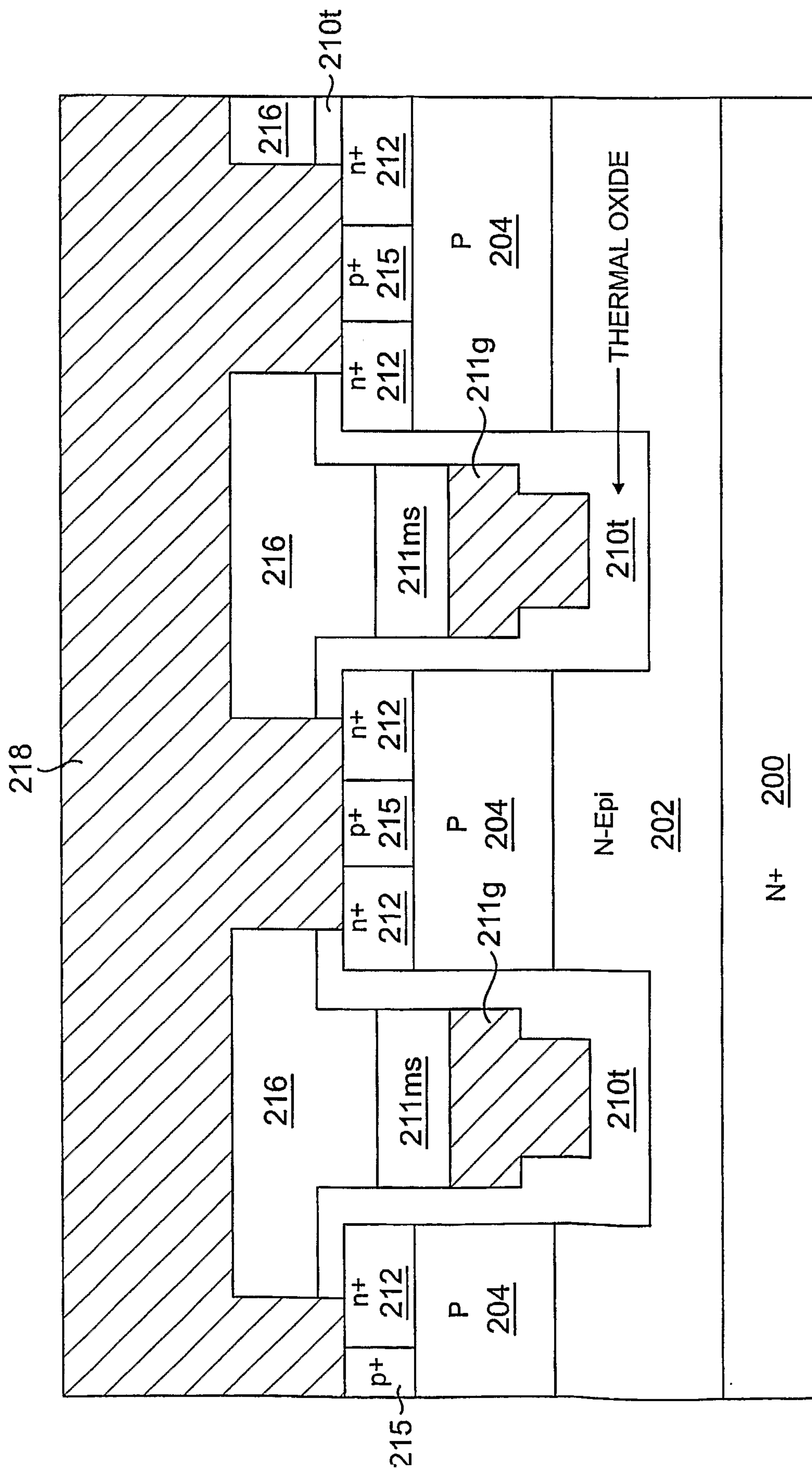


FIG. 12C

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US02/36517

**A. CLASSIFICATION OF SUBJECT MATTER**
IPC(7) : H01L 29/76; 29/94; H01L 21/336
US CL : 257/330; 438/270
According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/330; 438/270

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X<br>---<br>Y | US 5,637,898 A (BALIGA) 10 June 1997 (10.06.1997), column 5 line 33, 35-45, column 6 line 37, 40-41, column 7 lines 10, 24, 27 | 1-10, 16-27<br>-----------<br>11-15 |
| Y | US 6,274,905 B1 (MO) 14 August 2001 (14.08.2001), column 3 lines 47-50, 55-57 | 11-12, 14-15 |
| Y | US 2001/0028085 A1 (BLANCHARD) 11 October 2001 (11.10.2001), claim 3 | 13 |
| X | US 5,442,214 (YANG) 15 August 1995 (15.08.1995), fig. 2a-21, column 3 lines 1-68 | 1-10, 17-27 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 17 March 2003 (17.03.2003) | 07 APR 2003 |

| Name and mailing address of the ISA/US | Authorized officer |
|---|---|
| Commissioner of Patents and Trademarks<br>Box PCT<br>Washington, D.C. 20231 | Wael M Fahmy |
| Facsimile No. (703)305-3230 | Telephone No. 703-308-0956 |

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Technology Center 2800
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Form PCT/ISA/210 (second sheet) (July 1998)