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(54) Title: METHOD AND COMPOSITION

(57) Abstract: A composition comprising: a non-ordered substrate and a metal chalcogenide present on at least one surface of the substrate is disclosed. A method of forming a metal chalcogenide on ordered substrates is also disclosed.

METHOD AND COMPOSITION

Field of the Invention

5 This invention relates to a method of producing a composition comprising a metal chalcogenide, particularly on a substrate. This invention also relates to a composition comprising a metal chalcogenide on a substrate. It also relates to metal chalcogenide compositions produced by the method and devices including the metal chalcogenide on a substrate.

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Background to the Invention

Transition metal chalcogenides (TMDCs) such as MoS_2, $MoSe_2$, WS_2 and WSe_2 are noteworthy 2-D semiconductors with tunable band gap, offering advantages over graphene 15 in a number of optoelectronic applications: see Radisavljevic, B., et al., *Nat. Nanotechnol.* **6**, 147–150 (2011); H. Wang, et al., *Nat. Nanotechnol.* *7*, 699-712 (2012).

TMDCs have been demonstrated in a number of applications including transistors, photodetectors, electroluminescent and biosensing devices [Radisavljevic, et al., above; 20 Wang, et al. above; A. Splendiani, et al. *Nano Letters*, **10** (4), 1271-1275 (2010); Lee, H. S, et al., *Nano Letters*, **12** (7), 3695-3700 (2012); A. K. Geim and I. V.Grigorieva, *Nature*, **499**, 419-425 (2013); N. R. Pradhan, et al. *Appl. Phys. Lett.* 102 (12), 123105-08 (2013); Sarkar, D. et al., *ACS Nano*, 8(4), 3992-4003 (2014)].

25 MoS_2 is perhaps the most widely synthesized and studied TMDC, and monolayers up to tens of monolayers of the material have been characterized in a range of devices in order to optimize their optical and electronic properties.

Field effect transistors (FETs) require the incorporation of doped silicon layers in 30 complementary metal–oxide–semiconductor (CMOS) microfabrication. Replacement by 2-D MoS_2 atomically thin layers, for example, provides a route to a significantly reduced energy budget (and concomitantly less heating) by using 10^5 less energy in the stand-by state. Besides the energy saving aspect, the 2-D MoS_2 transistor is a higher-speed and efficient device due to the electrons move from the drain and source alone the only tunnel while 35 electrons scatter though thicker silicon device. FET transistors are ubiquitous in a huge range of electronic devices.

Additionally, both thermoelectric and photovoltaic devices require the incorporation of materials which provide effective p-n junctions, and in the case of photovoltaics, one of the materials must absorb the Sun's radiation effectively (a direct and tunable band-gap). Metal chalcogenide materials provide the ability to tune the band-gap to optimise absorption of radiation, and can exhibit either p-type or n-type conductivity.

The development of micro-processors incorporating FETs requires p-type and n-type materials which can be incorporated at temperatures below 350°C, a limitation set by the flexible substrate itself. Development of thermoelectric or photovoltaic devices on these substrates is also typically subject to similar requirements and limitations.

There are a wide range of synthetic methods which have been explored and exploited for producing metal chalcogenide materials, including exfoliation [Radisavljevic, et al., above; Coleman, J. N. et al, *Science* 331(6017), 568-571 (2011), Liu, K. K. et al. *Nano Letters*, 12(3), 1538-1544 (2012)], electrochemical [Liu et al. above], hydrothermal [Peng, Y. Y. et al. *Chemistry Letters*, **8**, 772-773, (2011), chemical synthesis [P. Roy and S. K. Srivastava, Thin Solid Films, 496(2), 293-298, 2006], thermolysis [Altavilla, C. Sarno, M. Ciambelli, P., *Chemistry of Materials*, **23**(17), 3879-3885 (2011)], spherization of molybdenum oxides [Balendhran, S. et al *Nanoscale*, **4** (2), 461- 466 (2012)], evaporative physical vapour deposition [Balendhran, S. et al, above], sputtering [S. Hussain et al, *Scientific Reports*, 6 (30791), 2016; Yu, Y. F. et al. , *Scientific Reports*, **3**, 2013], chemical vapour deposition (CVD) [Lee et al., above; Yu, et al. above; Nie, Z. G. et al., *ACS Nano*, **8** (10), 10931-10940 (2014); C. C. Huang, et al, *Nanoscale*, **6**, 12792-12797, 2014; van der Zande, A. M. *Nature Materials*, **12** (6), 554-561 (2013)]; atomic layer deposition (ALD) [Huang, Y. Z. et al, *Applied Physics Letters*, **111** (6), 2017] and molecular beam epitaxy (MBE) [D. Fu, et al, *J. Am. Chem. Soc.* **2017**, *139*, 9392-9400]. The majority of these methods produce flakes of only a few hundred square microns in area, and which would be difficult to incorporate within micro-fabricated device structures.

D. Fu, et al, *J. Am. Chem. Soc.* **2017**, *139*, 9392-9400, which is believed to represent the closest state of the art, describes the formation of monolayer MoS_2 on hexagonal boron nitride by molecular beam epitaxy. The method described in this document is carried out at 750 to 900°C; there is no disclosure or suggestion that the method may be carried out at lower temperatures, especially temperatures below 600°C. Moreover, the substrate on which the MoS_2 layer is formed, namely hexagonal boron nitride, exhibits long range atomic ordering; the document does not disclose or suggest that the method may be carried out on a non-ordered substrate.

US 2013/0045563 relates to a method for the production of a $Cu(In,Ga)Se_2$ semiconductor layer as an absorber layer for solar cells. The layer is formed through the deposition of Cu, In, Ga, Se and S on a substrate that carries a back contact. This method comprises evaporating Cu, In and/or Ga or their chalcogenide compounds in metal evaporator sources and focusing the resulting metal vapour beams onto the substrate. Selenium and/or sulfur exit in an ionised manner from a chalcogen low-energy broad-beam ion source and this beam strikes the surface of the substrate focused in such a manner that it overlaps with the metal vapour beams leading to deposition of the absorber layer on the substrate. However, the materials used to form the thin film are polycrystalline chalcogenide materials. These would therefore not be considered relevant to the problem of depositing a high quality (long range order) 2-D material at low temperatures on a non-ordered substrate.

WO 2016/013984 describes a process for making metal or metalloid chalcogenides from a metal/metalloid and elemental chalcogen using magnetron sputtering, comprising the steps of a) directing sputtering gas ions at a target comprising a metal or metalloid, b) reacting the ejected metal or metalloid atoms from the target surface with an elemental chalcogen vapour, and c) assembling the metal or metalloid chalcogenides on a substrate. However, the only example in this published application is carried out at 700°C, and the publication further teaches that carrying the process out at 700°C gives the best uniformity. It does not therefore enable any method in which a metal chalcogenide is formed on a non-ordered substrate at a lower temperature.

US 2018/0308692 also describes a method for making a transition metal dichalcogenide film. The method as described therein involves the initial step providing a precursor film comprising an amorphous transition metal dichalcogenide film deposited on a substrate by a physical vapour deposition process. Subsequent to this, in a further step the precursor film is annealed using illumination-based annealing, thereby changing the amorphous transition metal dichalcogenide film to a crystalline transition metal dichalcogenide film. This document discloses that the substrate employed may be a flexible and/or stretchable substrate material and, in particular, a polymeric material such as polydimethyl siloxane (PDMS), 2-methacryloyl-oxyethyl phosphorylcholine (MPC), or one or both thereof copolymerised with dodecyl methacrylate (DMA), or a polyimide or perylene sheet.

However, the process described therein is a two-step MoS_2 process which requires the laser crystallization annealing process as a mandatory second step. In contrast, the document teaches and exemplifies that a single-step is difficult to achieve. In addition, the diameter of

the laser spot (1.5 μm) and the scanning speed (25 μm/s) would mean that the process is very slow – the laser crystallization of a 1 mm x 1 mm MoS_2 area using this method would require 7.4 hours. Therefore, using this method to manufacture an amount of material in sufficient quantities for commercial applications (such as solar photovoltaics, which require square metres of substrate) would take so long, the method is completely unsuitable for this purpose.

Summary of the Invention

In a first aspect, the invention provides a method of forming a metal chalcogenide on a non-ordered substrate, said method comprising:
providing a vapour source of metal atoms and a vapour source of chalcogen atoms; and
co-depositing the metal and chalcogen atoms on the substrate, such that the metal chalcogenide forms on the substrate.

In a second aspect, the invention provides a method of forming a metal chalcogenide on a substrate, said method comprising:
providing a vapour source of metal atoms and a vapour source of chalcogen atoms; and
co-depositing the metal and chalcogen atoms on the substrate, such that the metal chalcogenide forms on the substrate;
wherein the method is carried out at a temperature below 600°C.

In a third aspect, the invention provides a method of forming a metal chalcogenide on a non-ordered substrate, said method comprising:
providing one or more vapour sources of metal atoms and one or more a vapour sources of chalcogen atoms; and
co-depositing the metal and chalcogen atoms on the substrate, such that the metal chalcogenide forms on the substrate;
wherein the method is carried out at a temperature below 600°C.

In a fourth aspect, the invention provides a metal chalcogenide obtained or obtainable by a method according to any of the above aspects.

In a fifth aspect, the invention provides a composition comprising: a substrate; and a metal chalcogenide present on at least one surface of the substrate.

In a sixth aspect, the invention provides a device including a metal chalcogenide according to the fourth aspect, or a metal chalcogenide produced by a method according to any of the first, second or third aspects, or a composition of the fifth aspect.

5 **Brief Description of the Figures**

Figure 1 illustrates an ultra-high vacuum (UHV) evaporation physical vapour deposition (ePVD) system according to an embodiment of the present invention;
Figure 2 illustrates (a) photoluminescence (532 nm laser) measurements of a MoS_2 film
10 produced according to the present invention, covering from 4 monolayers down to less than 1 monolayer; (b) excitation peak A blueshifts with the thickness of the MoS_2 film changing, and (c) a plot showing that a single layer of MoS_2 emerges the strongest photoluminescence;
Figure 3 shows Raman spectrum (532 nm laser) measurements carried out by Nanonics Cryoview Raman system on a MoS_2 film produced according to the present invention, Fig.
15 3a plotting intensity for 3, 2, 1 and less than 1 monolayer and Fig. 3b showing the correspondence between the modes as measured and those reported in the literature;
Figure 4 shows an X-Ray Diffractogram of 25 nm thick MoS_2 film produced according to the present invention;
Figure 5 illustrates (a) a schematic view of one MoS_2 based field effect transistors (FET)
20 device fabricated on 300 nm coated p type Si substrate according to the present invention; (b) an image of 196 MoS_2 based FET fabricated on the SiO_2 coated Si substrate; and (c) FET measurements on a 2 monolayer (ML) MoS_2 device with scanning the gate voltage from -25 Volts to 60 Volts by adding a bias voltage between source and drain of 0.1 Volts and 1 Volt;
25 Figure 6 shows: (a) photographic image of a fielded array of a 14 x14 regions of MoS_2 (1x1 mm fields) grown on a Si/SiO_2 (300nm) substrate at a substrate temperature of 350°C according to the present invention; and (b) a false colour map of the thicknesses of the MoS_2 in each of the fields across the substrate; and (c) a photographic image showing the result of using the wedge shutter and main shutter method of the invention as illustrated in Fig. 1;
30 Figure 7 shows: (a) an image of three different thickness strips of MoS_2 film produced according to the present invention on a 35 mm x 35 mm poly (4,4'-oxydiphenylene-pyromellitimide) (Kapton®) PI substrate, and (b) Raman signature peaks of MoS_2 measured on Kapton® flexible PI substrate.

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Detailed Description

Advantages and Surprising Findings

It has been surprisingly found by the present inventors that the method of the present invention allows metal chalcogenides to be deposited in thin layers on a range of non-ordered substrates. This runs contrary to the teaching of the prior art, all of which describe that such thin layers of metal chalcogenides, in particular MoS_2, can only be deposited successfully on highly ordered substrates (such as hexagonal boron nitride).

It has also been surprisingly found by the present inventors that the method of the present invention successfully allows thin layers of metal chalcogenides to be deposited onto substrates (both non-ordered and ordered) at lower temperatures, below 600°C. This runs contrary to the teaching of the prior art, which describes that all successful attempts to synthesise these materials has required substrate temperatures above 700°C. In particular, it had not been considered possible in the prior art that similar materials of sufficient quality for use in electronic devices could be synthesised at lower temperatures, particularly below 350°C.

In particular, and in contrast to the method described in WO 2016/013984, the method of the present invention makes it possible for the first time to successfully manufacture a metal chalcogenide from a metal/metalloid and elemental chalcogen on a non-ordered substrate at temperatures below 700°C, and in particular between 50°C and 400°C.

Composition

In one aspect, the present invention provides a composition comprising: a substrate; and a metal chalcogenide present on at least one surface of the substrate. In one embodiment, the substrate is a non-ordered substrate, as defined herein.

In one embodiment, the metal chalcogenide is formed as a film. In this specification the terms “film” and “layer” are synonymous. In one embodiment, the metal chalcogenide is present in the form of a film on the surface of the substrate.

The thickness of the film may be expressed either in terms of the number of layers of the metal chalcogenide on the substrate or as a measurement. The thickness may vary depending on the intended application of the substrate on which the metal chalcogenide is

formed. Different metal chalcogenides will form films of different thicknesses depending on their composition.

In one embodiment, the thickness of the film ranges from 0.5 nm to 500 nm. In one embodiment, the thickness of the film ranges from 1 nm to 200 nm. In one embodiment, the thickness of the film ranges from 2 nm to 100 nm. In one embodiment, the thickness of the film ranges from 5 nm to 50 nm.

In one embodiment, the present invention provides a composition comprising: a substrate; and one or more monolayers of the metal chalcogenide present on at least one surface of the substrate. In one embodiment, 1 to 1000 monolayers of the metal chalcogenide are present on the substrate. In one embodiment, 1 to 500 monolayers of the metal chalcogenide are present on the substrate. In one embodiment, 1 to 200 monolayers of the metal chalcogenide are present on the substrate. In one embodiment, 1 to 100 monolayers of the metal chalcogenide are present on the substrate. In one embodiment, 1 to 50 monolayers of the metal chalcogenide are present on the substrate. In one embodiment, 1 to 20 monolayers of the metal chalcogenide are present on the substrate. In one embodiment, 1 to 10 monolayers of the metal chalcogenide are present on the substrate. In one embodiment, 1 to 5 monolayers of the metal chalcogenide are present on the substrate. In one embodiment, 1 to 3 monolayers of the metal chalcogenide are present on the substrate. In one embodiment, 1 to 2 monolayers of the metal chalcogenide are present on the substrate. In one embodiment, 1 monolayer of the metal chalcogenide is present on the substrate.

Substrate

As described herein, a method of the present invention comprises a method of forming a metal chalcogenide on a substrate.

In one aspect of this invention, the substrate is a non-ordered substrate. In the context of this disclosure, the term “non-ordered” means “not crystalline”, i.e. that the substrate has no long range ordering in its lattice. This term covers substrates that are polycrystalline (i.e. the substrate is composed of many crystals having order at a microscopic level, but has no long-range order) and substrates which are amorphous where the lattice has no order even microscopically, but excludes crystalline substrates in which the lattice has long-range order. In one embodiment the substrate is polycrystalline. In one embodiment the substrate is amorphous.

Suitable substrates are well known to the person skilled in the art, and include metals (such as platinum, aluminium, titanium, rhodium, iridium, palladium, chromium, iron, zinc, gold, silver, copper, nickel, molybdenum and tungsten, including alloys thereof, which may include non-metals such as carbon), metal oxides (particularly conductive metal oxides such as aluminium zinc oxide and indium tin oxide), silicon, silica, silicon oxide (including doped silicon oxide), aluminosilicate materials, glasses, and ceramic materials.

In one embodiment, the substrate is an inert substrate. In one embodiment, the substrate is selected from the group consisting of: silicon, silica, silicon oxide, a glass, a metal, and a ceramic material.

In one embodiment the substrate is a metal.

In one embodiment, the metal is ordered (i.e. crystalline, in that it exhibits long range lattice ordering). Examples of ordered metals include chromium, titanium, rhodium, iridium, nickel, palladium, platinum, copper, silver and gold.

In one embodiment, the metal is non-ordered (as defined above, e.g. polycrystalline or amorphous). Examples of non-ordered metals include molybdenum and tungsten.

In one embodiment the substrate is a conductive metal oxide. In one embodiment the substrate is a non-ordered (as defined above e.g. polycrystalline or amorphous) conductive metal oxide. Examples of conductive metal oxides include indium tin oxide and aluminium zinc oxide.

In one embodiment the substrate is a semiconductor. In one embodiment the semiconductor is an ordered (i.e. crystalline) semiconductor. In one embodiment the semiconductor is a non-ordered (as defined above e.g. polycrystalline or amorphous) semiconductor. Examples of semiconductors include Group 14 elements such as silicon and germanium; Group 14 compound semiconductors such as silicon carbide; III-V semiconductors (compounds of Group 13 and Group 15 elements) such as gallium arsenide; II-VI semiconductors (compounds of Group 12 and Group 16 elements) such as cadmium sulphide). In one embodiment the substrate is silicon. In one embodiment the substrate is gallium arsenide.

In one embodiment the substrate is silica. In one embodiment the silica is in an ordered (i.e. crystalline) form; examples of such ordered, crystalline forms of silica include quartz. In one

embodiment the silica is in a non-ordered (as defined above e.g. polycrystalline or amorphous) form.

In one embodiment the substrate is a glass. As is known to the person skilled in the art, a glass has a non-ordered (preferably amorphous) structure at the atomic scale and exhibits a glass transition when heated towards the liquid state. In one embodiment the glass is silicate glass. In one embodiment the glass is fused silica glass. In one embodiment the glass is borosilicate glass. In one embodiment the glass is soda-lime-silica glass. In one embodiment the glass is lead oxide glass. In one embodiment the glass is aluminosilicate glass. In one embodiment the glass is germanium oxide glass.

In one embodiment the substrate is a ceramic. Typical ceramic materials which are capable of forming suitable substrates include silicon dioxide (SiO_2), aluminium oxide (Al_2O_3), zirconium oxide (ZrO_2), iron oxide (Fe_2O_3), titanium dioxide (TiO_2), calcium oxide (CaO), and magnesium oxide (MgO) or a combination of two or more of these materials.

In one embodiment the substrate is an organic polymer. In one embodiment the organic polymer is in an ordered (i.e. crystalline) form. In one embodiment the organic polymer is in a non-ordered (as defined above e.g. polycrystalline or amorphous) form. The organic polymer may be a homopolymer (i.e. containing only a single type of repeating unit) or a copolymer (i.e. containing two or more types of repeating units). Typical organic polymers which are capable of forming suitable substrates include polyimides such as poly (4,4'-oxydiphenylene-pyromellitimide) (Kapton®), polycarbonates, polyacrylates such as poly(methyl methacrylate), polyesters such as polyethylene terephthalate, polyamides, vinyl polymers (including polyolefins such as polyethylene and polypropylene, and halogenated polyolefins such as polyvinyl chloride, poly(vinylidene difluoride) and poly(tetrafluoroethylene) (PTFE, Teflon®), and mixtures thereof. In one embodiment the substrate is a polyimide. In one embodiment the substrate is poly (4,4'-oxydiphenylene-pyromellitimide) (Kapton®).

In one embodiment the substrate is selected from the group consisting of silica, silicon nitride, indium tin oxide, glass and polyimide. In one embodiment the substrate is selected from the group consisting of silica, silicon nitride, indium tin oxide, glass and polyimide.

Metal Chalcogenide

The present invention relates to a method of forming a metal chalcogenide on a substrate.

5 The metal element of the metal chalcogenide may be a single metal or a mixture of two or more metals. In one embodiment the metal element of the metal chalcogenide is a single metal. In one embodiment the metal element of the metal chalcogenide is a mixture of two or more metals (preferably two, three or four; more preferably two or three; even more preferably two) metals.

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The metal element may be any metal capable of forming a chalcogenide. Examples of metals include alkali metals such as Li, Na, K, Rb and Cs; alkaline earth metals such as Be, Mg, Ca, Sr and Ba; transition metals, for example first group transition metals such as Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn; second group transition metals such as Y, Zr, Nb, Mo, Tc, Ru, 15 Rh, Pd, Ag, Cd or third group transition metals such as Hf, Ta, W, Re, Os, Ir, Pt, Au, Hg; lanthanides such as La, Ce, Pr, Nd, Pm, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb and Lu; and p-block metals such as Al, Ga, In, Sn, Tl, Bi and Po, and mixtures of any thereof.

In one embodiment, the metal is selected from the group consisting of a transition metal and 20 a p-block metal, or a mixture of any thereof. In one embodiment, the metal is a first group transition metal. In one embodiment, the metal is a second group transition metal. In one embodiment, the metal is a third group transition metal. In one embodiment, the metal is a p-block metal.

25 In one embodiment, the metal is a tetravalent metal. In one embodiment, the metal is a trivalent metal. In one embodiment, the metal is a divalent metal.

In one embodiment, the metal is selected from the group consisting of Mo, W, Hf, Pt, and Sn, or a mixture of any thereof. In one embodiment, the metal is Mo. In one embodiment, 30 the metal is W. In one embodiment, the metal is Pt. In one embodiment, the metal is Sn.

The term “chalcogen” has its usual meaning in chemistry of an element of Group 16 of the periodic table, in other words an element selected from O, S, Se, Te and Po. In one embodiment, the chalcogen is selected from the group consisting of S, Se, and Te, or a 35 mixture of any thereof. In one embodiment, the chalcogen is S. In one embodiment, the chalcogen is Se. In one embodiment, the chalcogen is Te.

In one embodiment, the metal and the chalcogen are present in a stoichiometric ratio ranging from 2:1 to 1:4. In one embodiment, the metal and the chalcogen are present in a stoichiometric ratio ranging from 1:1 to 1:2. In one embodiment, the metal and the chalcogen are present in a stoichiometric ratio of 1:2. In one embodiment, the metal and the
5 chalcogen are present in a stoichiometric ratio of 1:1.

In one embodiment, the metal chalcogenide is selected from MoS_2, WSe_2, WS_2, $MoTe_2$ and SnS, or a mixture of any thereof. In one embodiment, the metal chalcogenide is MoS_2. In one embodiment, the metal chalcogenide is $MoSe_2$. In one embodiment, the metal
10 chalcogenide is $MoTe_2$. In one embodiment, the metal chalcogenide is WS_2. In one embodiment, the metal chalcogenide is WSe_2. In one embodiment, the metal chalcogenide is SnS.

In one embodiment, the metal chalcogenide has the formula $Mo_xSn_yS_2$, wherein: x is greater
15 than 0 and not more than 1; and y is greater than 0 and not more than 2; and $x + 2y = 2$.

Method

The present invention relates generally to methods of forming a metal chalcogenide on a
20 substrate, which may be an ordered (i.e. crystalline) or a non-ordered (e.g. polycrystalline or amorphous) substrate.

One general method used in accordance with one embodiment of the invention is a physical vapour deposition (PVD) method. According to this method, the composition is formed from
25 the component metal and chalcogen elements, by providing a vapour source of each component element of the compound and co-depositing the component elements from the vapour sources onto a substrate, typically a heated substrate, such that the metal chalcogenide forms on the substrate, typically as a film or layer on the substrate.

30 In one embodiment, the vapour source may provide only one element. In another embodiment, the vapour source may provide more than one element, such as two, three, four or five elements.

The physical vapour deposition (PVD) method according to the invention typically involves
35 co-depositing the component elements from the vapour sources onto a heated substrate. Typically, the substrate is heated, such that during the deposition process, a controlled flow

rate or flux of each component element is released from its respective vapour source onto the heated substrate, whereupon the various elements are co-deposited.

Any suitable method capable of forming a vapour of metal atoms and/or chalcogen atoms may function as the source. The nature of each vapour source will depend on the element it delivers, and also the amount of control required over the rate of delivery (i.e. flow rate or flux). Electron beam evaporators and Knudsen cells (K-Cells) are other examples of vapour sources; these are well-suited for materials with low partial pressures. In both cases the material is held in a crucible and heated to generate a flux of material. A Knudsen cell uses a series of heating filaments around the crucible, whereas in an electron beam evaporator the heating is achieved by using magnets to direct a beam of high energy electrons onto the material.

In one embodiment, the PVD method is an evaporative physical vapour deposition (ePVD) method. In the context of the present invention, an ePVD method comprises heating the metal and the chalcogen elements in separate sources in a chamber (for example, Knudsen cells or electron-beam evaporators) until each form a vapour. The vapour elements then condense on the substrate and react with each other to form the metal chalcogenide.

Accordingly, in this embodiment, there is provided a vapour deposition method comprising: providing a vapour source of metal atoms and a vapour source of chalcogen atoms, heating a substrate to between 100°C and 600°C; depositing the component elements from the sources onto the heated substrate, wherein the component elements react on the substrate to form the metal chalcogenide.

In an embodiment, there is provided a vapour deposition method comprising: providing a vapour source of metal atoms and a vapour source of chalcogen atoms, heating a substrate to between 300°C and 600°C; depositing the component elements from the sources onto the heated substrate, wherein the component elements react on the substrate to form the metal chalcogenide.

In one embodiment, the method is carried out at a temperature below 700°C. In one embodiment, the method is carried out at a temperature below 690°C. In one embodiment, the method is carried out at a temperature below 680°C. In one embodiment, the method is carried out at a temperature below 670°C. In one embodiment, the method is carried out at a temperature below 660°C. In one embodiment, the method is carried out at a temperature below 650°C. In one embodiment, the method is carried out at a temperature below 640°C.

In one embodiment, the method is carried out at a temperature below 630°C. In one embodiment, the method is carried out at a temperature below 620°C. In one embodiment, the method is carried out at a temperature below 610°C.

In one embodiment, the method is carried out at a temperature below 600°C. In one embodiment, the method is carried out at a temperature below 590°C. In one embodiment, the method is carried out at a temperature below 580°C. In one embodiment, the method is carried out at a temperature below 570°C. In one embodiment, the method is carried out at a temperature below 560°C. In one embodiment, the method is carried out at a temperature below 550°C. In one embodiment, the method is carried out at a temperature below 540°C. In one embodiment, the method is carried out at a temperature below 530°C. In one embodiment, the method is carried out at a temperature below 520°C. In one embodiment, the method is carried out at a temperature below 510°C. In one embodiment, the method is carried out at a temperature below 500°C. In one embodiment, the method is carried out at a temperature below 490°C. In one embodiment, the method is carried out at a temperature below 480°C. In one embodiment, the method is carried out at a temperature below 470°C. In one embodiment, the method is carried out at a temperature below 460°C. In one embodiment, the method is carried out at a temperature below 450°C. In one embodiment, the method is carried out at a temperature below 440°C. In one embodiment, the method is carried out at a temperature below 430°C. In one embodiment, the method is carried out at a temperature below 420°C. In one embodiment, the method is carried out at a temperature below 410°C. In one embodiment, the method is carried out at a temperature below 400°C. In one embodiment, the method is carried out at a temperature below 390°C. In one embodiment, the method is carried out at a temperature below 380°C. In one embodiment, the method is carried out at a temperature below 370°C. In one embodiment, the method is carried out at a temperature below 360°C. In one embodiment, the method is carried out at a temperature below 350°C. In one embodiment, the method is carried out at a temperature below 340°C. In one embodiment, the method is carried out at a temperature below 330°C. In one embodiment, the method is carried out at a temperature below 320°C. In one embodiment, the method is carried out at a temperature below 310°C. In one embodiment, the method is carried out at a temperature below 300°C. In one embodiment, the method is carried out at a temperature below 250°C. In one embodiment, the method is carried out at a temperature below 200°C. In one embodiment, the method is carried out at a temperature below 150°C.

In one embodiment, the method is carried out at a temperature above 100°C. In one embodiment, the method is carried out at a temperature above 150°C. In one embodiment,

the method is carried out at a temperature above 200°C. In one embodiment, the method is carried out at a temperature above 250°C. In one embodiment, the method is carried out at a temperature above 300°C. In one embodiment, the method is carried out at a temperature above 310°C. In one embodiment, the method is carried out at a temperature above 320°C. In one embodiment, the method is carried out at a temperature above 330°C. In one embodiment, the method is carried out at a temperature above 340°C. In one embodiment, the method is carried out at a temperature above 350°C. In one embodiment, the method is carried out at a temperature above 360°C. In one embodiment, the method is carried out at a temperature above 370°C. In one embodiment, the method is carried out at a temperature above 380°C. In one embodiment, the method is carried out at a temperature above 390°C.

In one embodiment, the method is carried out at a temperature in the range of 100°C to 600°C. In one embodiment, the method is carried out at a temperature in the range of 200°C to 500°C.

In one embodiment, the method is carried out at a temperature in the range of 300°C to 400°C. In one embodiment, the method is carried out at a temperature in the range of 305°C to 395°C. In one embodiment, the method is carried out at a temperature in the range of 310°C to 390°C. In one embodiment, the method is carried out at a temperature in the range of 315°C to 385°C. In one embodiment, the method is carried out at a temperature in the range of 320°C to 380°C. In one embodiment, the method is carried out at a temperature in the range of 325°C to 375°C. In one embodiment, the method is carried out at a temperature in the range of 330°C to 370°C. In one embodiment, the method is carried out at a temperature in the range of 335°C to 365°C. In one embodiment, the method is carried out at a temperature in the range of 340°C to 360°C. In one embodiment, the method is carried out at a temperature in the range of 345°C to 355°C.

In one embodiment, the method is carried out at a pressure in the range 1×10^{-13} to 1×10^{-7} Pa. In one embodiment, the method is carried out at a pressure in the range 2×10^{-13} to 1×10^{-9} Pa. In one embodiment, the method is carried out at a pressure in the range 5×10^{-13} to 1×10^{-11} Pa.

In one embodiment, a thermal cracker is used to provide the vapour source of chalcogen atoms. The function of the thermal cracker is to break the chalcogen molecules into chalcogen atoms, such that the vapour deposited comprises chalcogen atoms.

When the chalcogen is S, in one embodiment the thermal cracker operates at a cracking temperature of between 600 and 1000°C. In one embodiment, the thermal cracker operates at a cracking temperature of between 700 and 900°C. In one embodiment, the thermal cracker operates at a cracking temperature of between 750 and 850°C.

5

When the chalcogen is Se, in one embodiment the thermal cracker operates at a cracking temperature of between 300 and 1000°C. In one embodiment, the thermal cracker operates at a cracking temperature of between 600 and 900°C.

10 One PVD method for forming the metal chalcogenides of the invention is the “wedge” shutter method described in Guerin, S. and Hayden, B. E., *Journal of Combinatorial Chemistry* **2006,** *8* (1), 66-73.

In the methods of the present invention, the component elements of the metal chalcogenide 15 are preferably provided in highly pure form. In one embodiment the material providing a source of the metal is at least 99% pure metal. In one embodiment the material providing a source of the metal is at least 99.9% pure metal. In one embodiment the material providing a source of the metal is at least 99.99% pure metal. In one embodiment the material providing a source of the metal is at least 99.999% pure metal. In one embodiment the 20 material providing a source of the chalcogen is at least 99% pure chalcogen. In one embodiment the material providing a source of the chalcogen is at least 99.9% pure chalcogen. In one embodiment the material providing a source of the chalcogen is at least 99.99% pure chalcogen. In one embodiment the material providing a source of the chalcogen is at least 99.999% pure chalcogen. These percentages are all expressed as an 25 atomic percentage of the total elements in the source.

The vapour-deposition method of the present invention is typically a single-step method, in that no additional annealing step is required in order to produce the material in which the metal chalcogenide is formed on a non-ordered substrate. In one embodiment, the method 30 does not include a step of annealing the substrate with the metal chalcogenide formed thereon. In one embodiment, the method does not include a step of annealing by laser or other illumination the substrate with the metal chalcogenide formed thereon. In one embodiment, the method does not include a step of laser annealing the substrate with the metal chalcogenide formed thereon.

35

Applications

The substrate provided with a metal chalcogenide layer (or film) thereon has a wide variety of applications.

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Accordingly, the invention also provides a device including a composition including a metal chalcogenide according to the invention, and/or a metal chalcogenide when produced by a method according to the invention.

10 Examples of potential devices are numerous and include transistors (in particular field effect transistors), optoelectronic sensors, batteries (especially solid state batteries), photovoltaic cells, integrated circuits, LED's, and photodetectors. These devices can be incorporated into a wide range of electronic products such as mobile telephones and computers.

15 **Examples**

Example 1: Synthesis of MoS_2 thin films

The MoS_2 thin films were synthesised in a turbomolecular pumped ePVD chamber with a
20 base pressure of 1×10^{-12} Pa, incorporating multiple evaporation sources with shadow, or "wedge" shutters typically used in the synthesis of compositional gradient thin films [Guerin, S., et al. (2005) "Combinatorial synthesis and screening of chalcogenide materials for data storage" at PCOS 17th Symposium 17 - 18 Nov 2005].

25 An e-beam on axis source with a graphite crucible containing Mo rods (99.9999% purity; Goodfellow) was used together with the wedge shutter to continuously vary the Mo flux across the substrate.

Sulphur (99.999% purity; Sigma-Aldrich) was evaporated from a two-stage S cracking
30 source with an evaporation temperature of 110°C and cracking temperature of 800°C. The S cracker was mounted on the chamber side wall with the sulphur atoms impinging at a grazing angle of ca. 11 degrees. A shutter directly in front of the substrate can be moved in stages, allowing the thickness of the film to be varied in fixed steps during deposition. The step changes in thickness is aligned to be orthogonal to that produced by the "wedge"
35 shutter: The result is a fine control of the thickness across a 29x29mm^2 region of a 35x35 mm^2 substrate.

Figure 1 illustrates generally at 10 the evaporative physical vapour deposition (ePVD) ultra high vacuum (UHV) system used to implement this method incorporating a valved two-heating stage thermal sulphur cracker 12 and a high voltage evaporation (e-gun) source 14. Molybdenum rods having an Mo purity of 99.999% are loaded into a graphite crucible 16 on the e-gun system 14 which has an on-off shutter 26. This shutter starts and finishes the deposition, the shutter blocking (OFF) or opening (ON) the Mo source for deposition. Two shutters, main shutter 18 controlled by a micro head and a wedge shutter 20 also controlled by a micro head, are used to control a varying thickness of the MoS_2 across the heatable sample holder 22 which holds the substrate on the heatable manipulator 24.

A typical sample synthesised on silicon nitride (Si_3N_4) with these shutters shows 4 regions (strips) of thickness controlled using the main sample shutter (net deposition times 5, 10, 15 and 20 minutes), with the thickness varied in the orthogonal direction with the wedge shutter. The result is that thicknesses of between ca. 0.6 nm (1 monolayer) and 20 nm can be controllably synthesised over a single substrate.

Substrates were cleaned *ex situ* in an acetone ultrasonic bath for 10 minutes to remove a surface protecting layer of S1813 photoresist, followed by immersing in isopropanol for 10 minutes and then rinsed in deionized water for 30 minutes. Substrates were dried in flowing air and subsequently heated in the vacuum chamber to 600°C for 60 minutes.

The Mo evaporation rate was monitored using a quartz crystal monitor and was maintained at 0.020 nm s^{-1}. The rate of S deposition was chosen (evaporation and cracking zones set at 110°C and 800°C respectively) in order to produce just sufficient (slightly in excess) S to ensure stoichiometric MoS_2 at the rates of Mo deposition. Any excess S was not incorporated in the MoS_2 layers at substrate temperatures above 300 °C.

The chamber pressure was ca 1.2 × 10^{-10} Pa during deposition. A 300 nm SiO_2/Si substrate is chosen as it offers the contrast to the MoS_2 film that can be observed visually. For the fabrication of FET devices, the layer of 300 nm SiO_2 (NOVA Electronics) also provided effective bias fields for the accessible bias voltage range. A Si_3N_4/Si substrate (NOVA Electronics) was used for X-ray diffraction, Hall effect and 4 point probe measurements.

The surface morphology and layer thickness was determined using an Agilent LS500 atomic force microscope (AFM) in non-contact mode The AFM scans an area of 10 µm x 10 µm to

imagine the surface morphology to allow the roughness to be assessed. To determine the thickness of MoS_2 pads, the edge of the MoS_2 pads was scanned and the thickness calculated via the difference between MoS_2 and substrate.

The topography measurements were carried over the edges of 1x1mm^2 MoS_2 pads produced in ePVD chamber with a 14v14 shadow mask. Compositional measurements were carried out by using energy dispersive x-ray fluorescence (EDX, Oxford Instruments X-act) on a scanning electron microscope (SEM, JEOL model JSM-5910). The lattice vibration modes were measured by Raman spectroscopy using a conformal Raman microscope (Renishaw InVia Raman system) with 532 nm (green) laser excitation. The Raman microscope was also used to carry out the photoluminescence (PL) measurements.

Raman spectrum (532 nm laser) measurements were carried out by Nanonics Cryoview Raman system. Signatural MoS_2 E^1_{2g} and A_{1g} active modes were obtained on various thicknesses. The peak lists are shown in Table 1, and the difference between the two as measured and their comparison with differences as reported in the literature is plotted in Figure 3(c).

The difference between two modes went from 20.6 cm^{-1} down to 18.8 cm^{-1} counting from three layers to less than one monolayer, which perfectly match the literatures. The plots of the difference between E^1_{2g} and A_{1g} modes across different MoS_2 thin film thickness.

	E^1_{2g} Raman Peak 1 (cm^{-1})	A_{1g} Raman Peak 2 (cm^{-1})	Difference Δ (cm^{-1})
140 Å	382.5	406.3	23.8
125	382.7	406.2	23.5
110	383	406.1	23.1
100	383.2	405.9	22.7
90	383.4	405.9	22.5
80	383.7	405.8	22.1
70	383.9	405.6	21.7
60	384.1	405.6	21.5
40	384.6	405.4	21.0
25 (4ML)	384.6	405.2	20.6
3 ML	384.8	405.4	20.6
2 ML	384.9	405.3	20.4
1 ML	385.6	404.4	18.8
<1 ML	385.4	406	20.6

Table 1

Structural measurements were carried out on a Regaku Smartlab X-ray diffraction (XRD) system in a grazing incidence (2°) configuration. The characterisation measurements were carried out on 30 nm thick MoS_2 films grown on Si_3N_4 substrates at different temperatures in order to understand the influence growth temperature on the quality of the 2-D layers. Mobilities, carrier densities and resistivities were determined by Hall measurements directly

on the thin films using a Van Der Paw probe (ACCENT HL5500). The field effect transistor (FET) device was fabricated using two sets of shadow masks on fielded regions (80µm) of the MoS_2. The FET measurement was carried out employing 3-channels of an Agilent B1500 source meter in a Cascade station system.

5

The grazing incident XRD patterns of a series of 25 nm MoS_2 thin film grown on Si/Si_3N_4 under identical growth conditions, but at increasing substrate temperature, is shown in Figure 4. In all cases the diffractogram is dominated by the 2H-MoS_2 (0002) Bragg peak at $2\theta = 14.3^{\circ}$ (series code JCPDS (00-037-1492), International Center for Diffraction Data
10 (ICDD) (C.C. Huang, et al., *Nanoscale*, **2014**, *6*, 12792)) as one would expect for the preferred orientation of the 2-D layers. The full width at half maximum (FWHM) measurement decreases with increased substrate synthesis temperature, with a concomitant increase in the peak intensity.

15 Increasing the synthesis temperature above 350°C did not result in further reduction in the FWHM or increase in the peak intensity. As far as the long-range order determined by XRD, 350°C appears a sufficiently high temperature to synthesise well-ordered layers of MoS_2 in this particular example although this itself is a necessary but not sufficient criteria for ensuring layered materials with optimal electronic or optoelectronic properties in 2ML thin
20 films. Nevertheless, in this particular example 350°C was chosen as the synthesis temperature for the MoS_2 layers grown for further characterisations.

ePVD methods were used to synthesise MoS_2 of various thicknesses on a single substrate at a substrate temperature of 350°C. Figure 6(a) is a photographic image of an array of
25 14x14 fielded thin films (1mm x 1mm) deposited using a contact mask on a Si/SiO_2 (300nm) substrate. The overall area over which the fields are deposited is 29x29mm^2. The sample shutter has been moved 4 times during the deposition to yield strips of fields with an increasing total deposition time, and hence thickness.

30 For each strip, in the orthogonal direction, the "wedge" shutter has been set to give an additional thickness gradient. This achieves a sample with a fine control of thicknesses on a single substrate. The thickness of a matrix of 8 fields has been determined by AFM and the results interpolated to all fields in the array, with the result shown in Figure 6(b). The sample shown have MoS_2 thin films varying between an effective thickness of 0.5 – 13nm (ca. 1-
35 20ML), with a variation of thickness within each field of ca. 0.03nm. Figure 6(c) shows 4

stripes of MoS_2 with different thicknesses as controlled by the combination of 2 shutters as shown in Fig. 1.

To measure the electrical properties of MoS_2, a 25 nm thin film was prepared on Si_3N_4 substrate with the deposition temperature of 350ºC. A 14 by 14 Ti/Au (5 nm/100 nm) with the dimension of 1 mm by 1 mm array was then fabricated using an Edwards 500 E Beam Evaporator as the top ohmic contacts [H. J. Chuang, et al., *Nano Letters*, **16**, 1896-1902, 2016]. 5 and 10 µA Hall currents were used during the studies. The thin film electrical resistance was also examined by Four-Dimensions 280 series 4 point probe (4pp), which agrees the results from the Hall Effect measurement.

The results are shown in Table 2, wherein "Ω/□" indicates the resistance in ohms per square. It is notable that the negative carrier density also indicates that the MoS_2 thin film obtained from above PVD technique is presented as n-type.

Hall current (µA)	**Carrier Density (cm^{-2})**	**Mobility ($cm^2V^{-1}s^{-1}$)**	**Resistance Ω/□**	**Resistance Ω/□ (4pp)**
10	-1.21e16	1.23	125.3	130
5	-1.75e16	1.01	122.7	132.1

Table 2

To further understand the electrical properties of MoS_2 made by this method, a back gate structure FET device was fabricated with a thickness high throughput way. The 300 nm SiO_2 coated Si commercial substrates were firstly put into a Plasmalab 80+ reactive ion etching (RIE) system upside down to remove the back SiO_2 layer and expose the highly conductive Si as connected as gate channel in the electrical measurement.

To remove a 300 nm SiO_2 layer by RIE, 200 W power was applied to the RIE with a combination of CHF_3 (20 standard cubic centimetres per minute, sccm) and Ar (20 sccm) gases were used to generate the plasma. The process pressure was kept on 13.32 Pa (100 mTorr). The etching rate is 50 nm/min when using these processing parameters.

The processed SiO_2/Si substrate was then transferred to the ePVD chamber with a 14 x 14 of 500 µm x 1000 µm mask to produce isolated MoS_2 pads as the transistor material. A second shadow mask was then placed and aligned on the MoS_2 padded substrate for depositing an array of top contacts - see Fig. 5(b) - of 5 nm Ti and 50 nm Au by Edwards

500 E Beam Evaporator as and the distance between top 'T' shaped contacts are 70 μm. This non-chemical process can minimize the contamination and damages to the MoS_2 films. The 3 channels FET electrical measurement is carried out by an Agilent B1500 powered Cascade system by connecting the bottom Si as gate, two of the top contacts as source and
5 drain. The FET measurement scans the gate voltage from -25 V to 60 V with a bias between source and drain of 0.1 V and 1 V, respectively.

The FET mobility can be calculated via $\mu = L/W \times dI_{ds}/dV_{bg}/(C_{bg}V_{ds})$, where L is the space between source and drain contacts, 70μm. W is the length of the contacts, which are 400 μm.
10 $C_{bg} = 1.2 \times 10^{-8}$ Fcm^{-2} for the back-gate capacitance. From the FET curve of Fig 5(c), the FET mobility is calculated as 0.147 $cm^2V^{-1}s^{-1}$ for a 2 ML MoS_2 device.

Example 2: Synthesis of MoS_2 on flexible polyimide substrate

Due to the capability to synthesis MoS_2 by a low temperature deposition technique, a 50 μm
15 thick bendable commercial poly (4,4'-oxydiphenylene-pyromellitimide) (Kapton®) polyimide (PI) substrate (DuPont) was then introduced. Mo-S thin film fabricated by 300°C on a 35 mm x 35 mm PI substrate - Fig. 7 (a) - and then examined by the Raman spectra. Raman signature peaks were observed on 381.8 cm^{-1} and 406 cm^{-1} - Fig. 7 (b) indicating a MoS_2 thin film existing on the PI substrate.
20

The deposited MoS_2 thin film on the flexible Kapton® polyimide substrate retained its continuity without observing any cracks. This shows that the successful deposition of MoS_2 thin film on PI substrate allows the possibility to develop a MoS_2 based flexible nano-electronic device with the low temperature deposition technique as well as a potential for
25 large scale design. This can also applied to highly transparent Corning Willow glass for flexible optical or energy applications, such as flexible photovoltaics or flexible solid state batteries.

All publications mentioned in the above specification are herein incorporated by reference.
30 Various modifications and variations of the present invention will be apparent to those skilled in the art without departing from the scope and spirit of the invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. Indeed, various modifications of the described modes for carrying out the
35 invention which are obvious to those skilled in chemistry, materials science or related fields are intended to be within the scope of the following claims.

CLAIMS

1. A method of forming a metal chalcogenide on a non-ordered substrate, said method comprising:
providing one or more vapour sources of metal atoms and one or more a vapour sources of chalcogen atoms; and
co-depositing the metal and chalcogen atoms on the substrate, such that the metal chalcogenide forms on the substrate;
wherein the method is carried out at a temperature below 600°C.

2. A method according to claim 1 , wherein the method is carried out at a temperature below 400°C.

3. A method according to claim 1 or claim 2, wherein the method is carried out at a temperature in the range of 300°C to 400°C.

4. A method according to any preceding claim, wherein the metal is selected from the group consisting of a transition metal and a p-block metal.

5. A method according to any preceding claim, wherein the metal is selected from the group consisting of Mo, W, Hf, Pt, and Sn, or a mixture of any thereof.

6. A method according to any preceding claim, wherein the chalcogen is selected from the group consisting of S, Se, and Te, or a mixture of any thereof.

7. A method according to any preceding claim, wherein the metal chalcogenide is selected from MoS_2, WSe_2, WS_2, $MoTe_2$ and SnS, or a mixture of any thereof.

8. A method according to claim 7, wherein the metal chalcogenide is MoS_2.

9. A method according to any one of claims 1-7, wherein the metal chalcogenide has the formula $Mo_xSn_yS_2$, wherein: x is greater than 0 and not more than 1; and y is greater than 0 and not more than 2.

10. A method according to any one of claims 1-9, wherein the substrate is selected from a metal, a metal oxide, silicon, silica, an aluminosilicate material, a glass, and a ceramic.

11. A method according to any one of claims 1-10, wherein the substrate is selected from the group consisting of silica, silicon nitride, indium tin oxide, glass and polyimide.

12. A method according to any preceding claim, wherein the source of chalcogen atoms is a thermal cracker.

13. A metal chalcogenide obtained or obtainable by a method according to any preceding claim.

14. A composition comprising:
a non-ordered substrate; and
a metal chalcogenide present on at least one surface of the substrate.

15. A composition according to claim 14, wherein the metal chalcogenide is present as a film of 0.5 to 500 nm thickness on the substrate.

16. A composition according to claim 14 or 15, wherein the metal chalcogenide is present as a film of 1 to 20 monolayers on the substrate.

17. A composition according to claim 14, 15 or 16, wherein the metal chalcogenide is MoS_2.

18. A device including a composition of any one of claims 14 to 17, or a metal chalcogenide according to claim 13, or a metal chalcogenide produced by a method according to any one of claims 1-12.

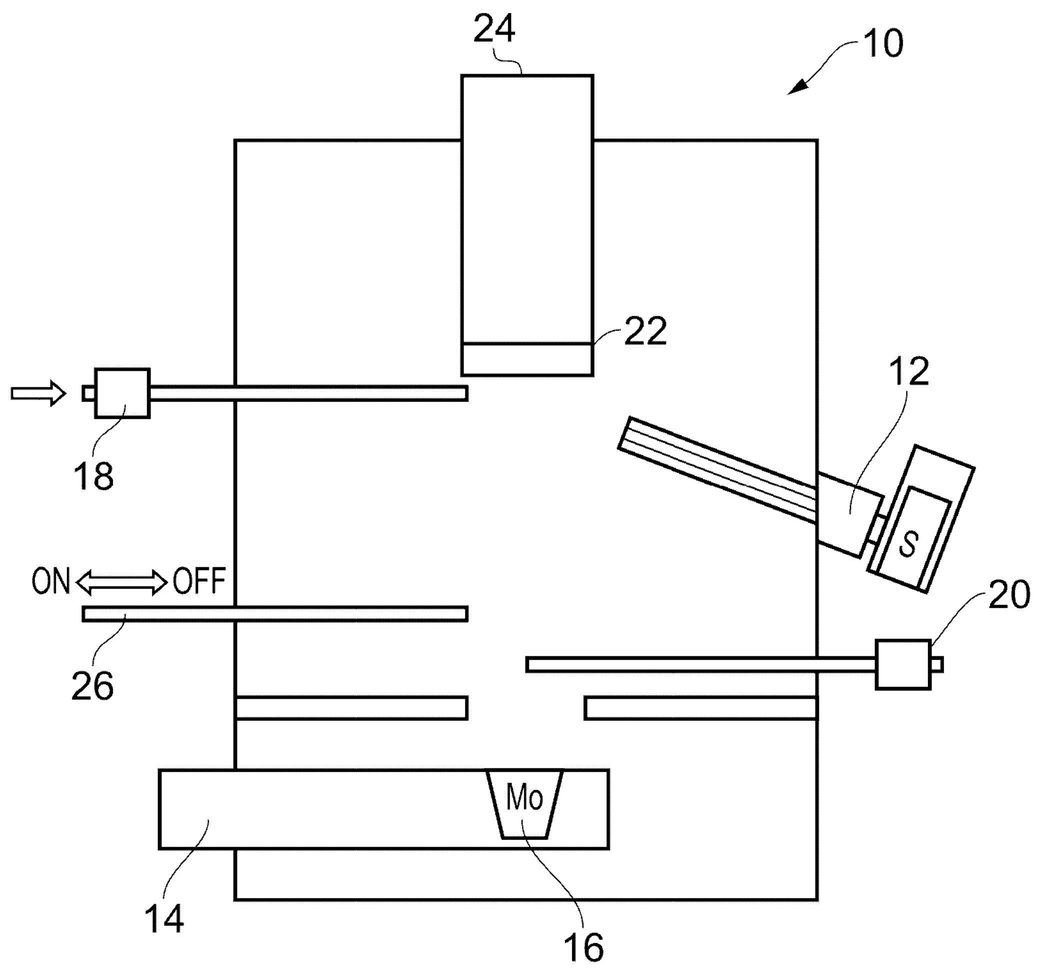

FIG. 1

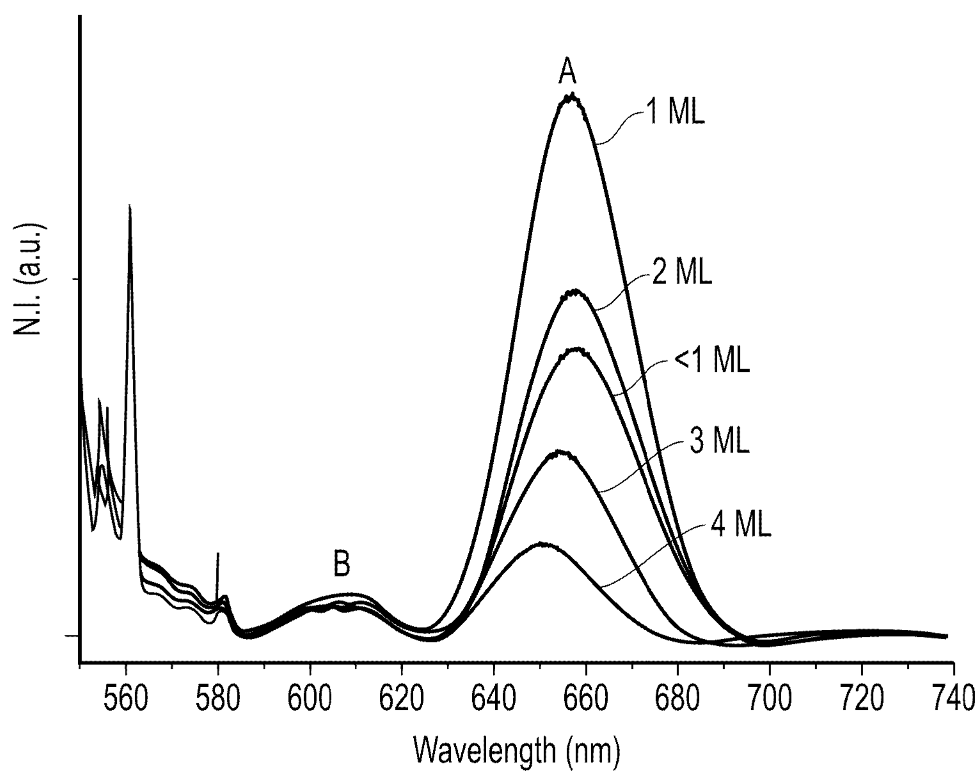

FIG. 2(a)

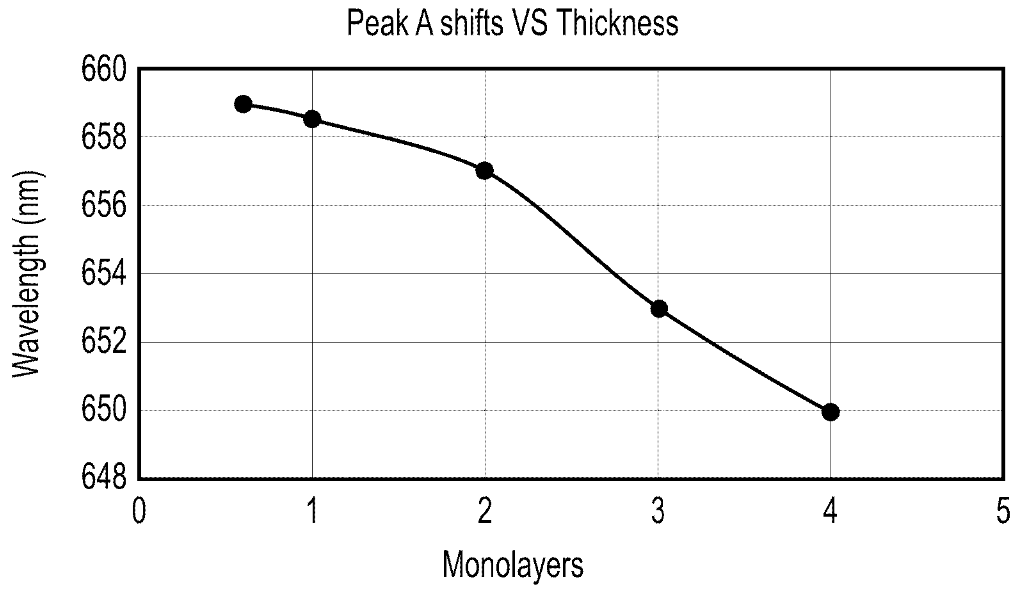

FIG. 2(b)

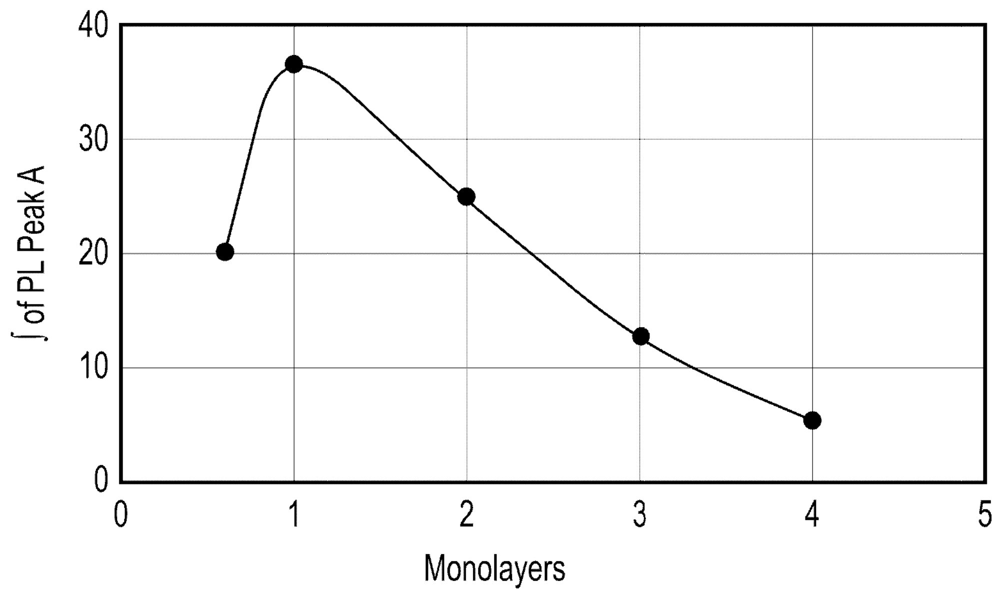

FIG. 2(c)

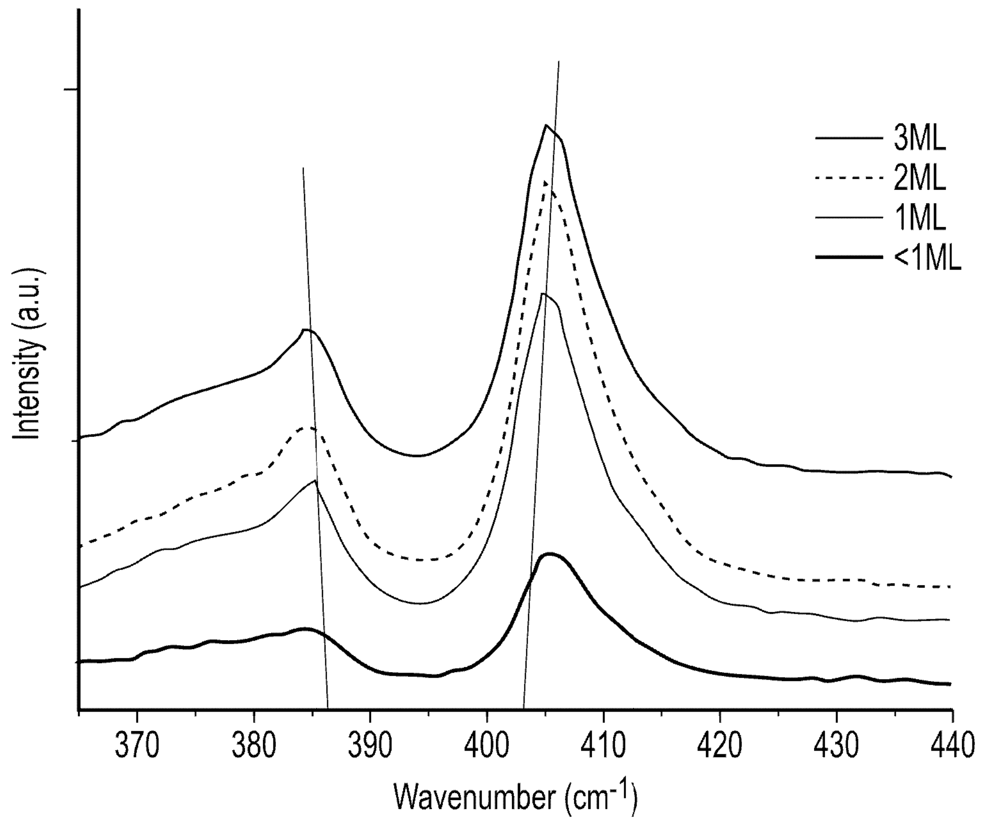

FIG. 3(a)

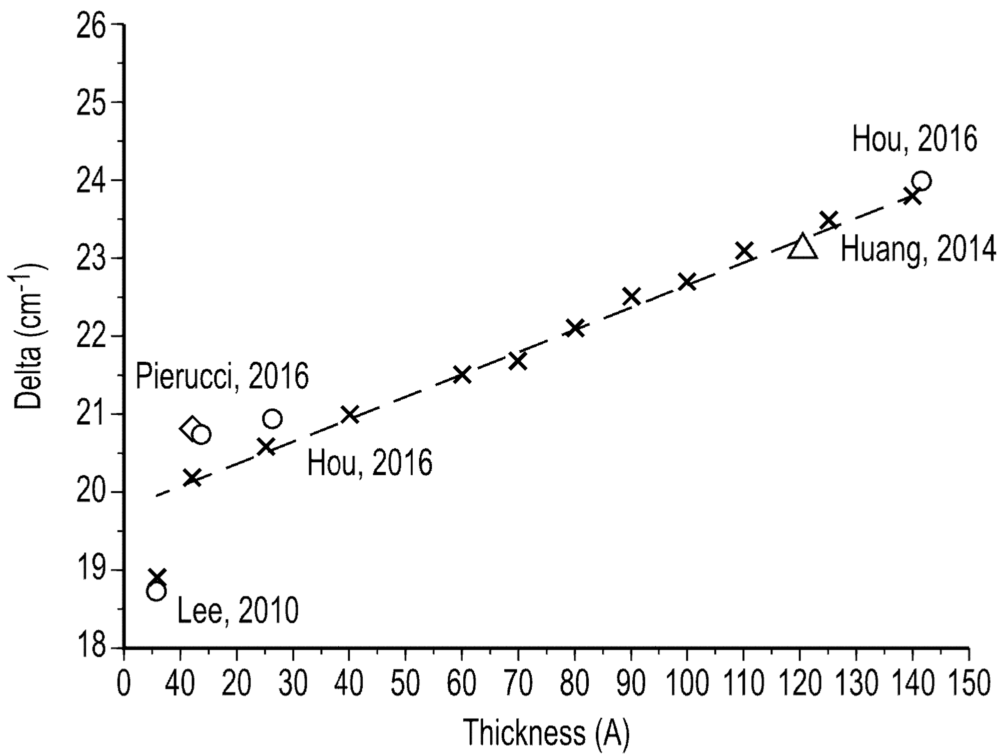

FIG. 3(b)

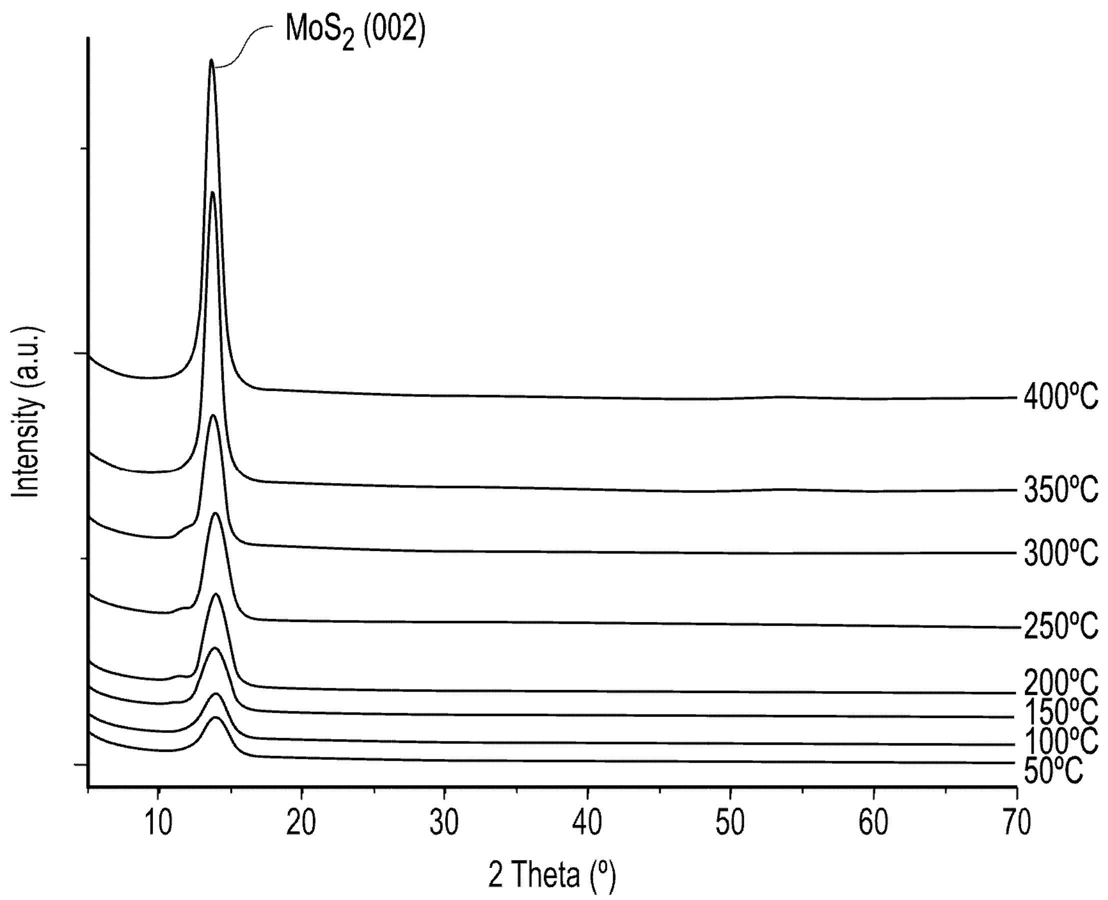

FIG. 4

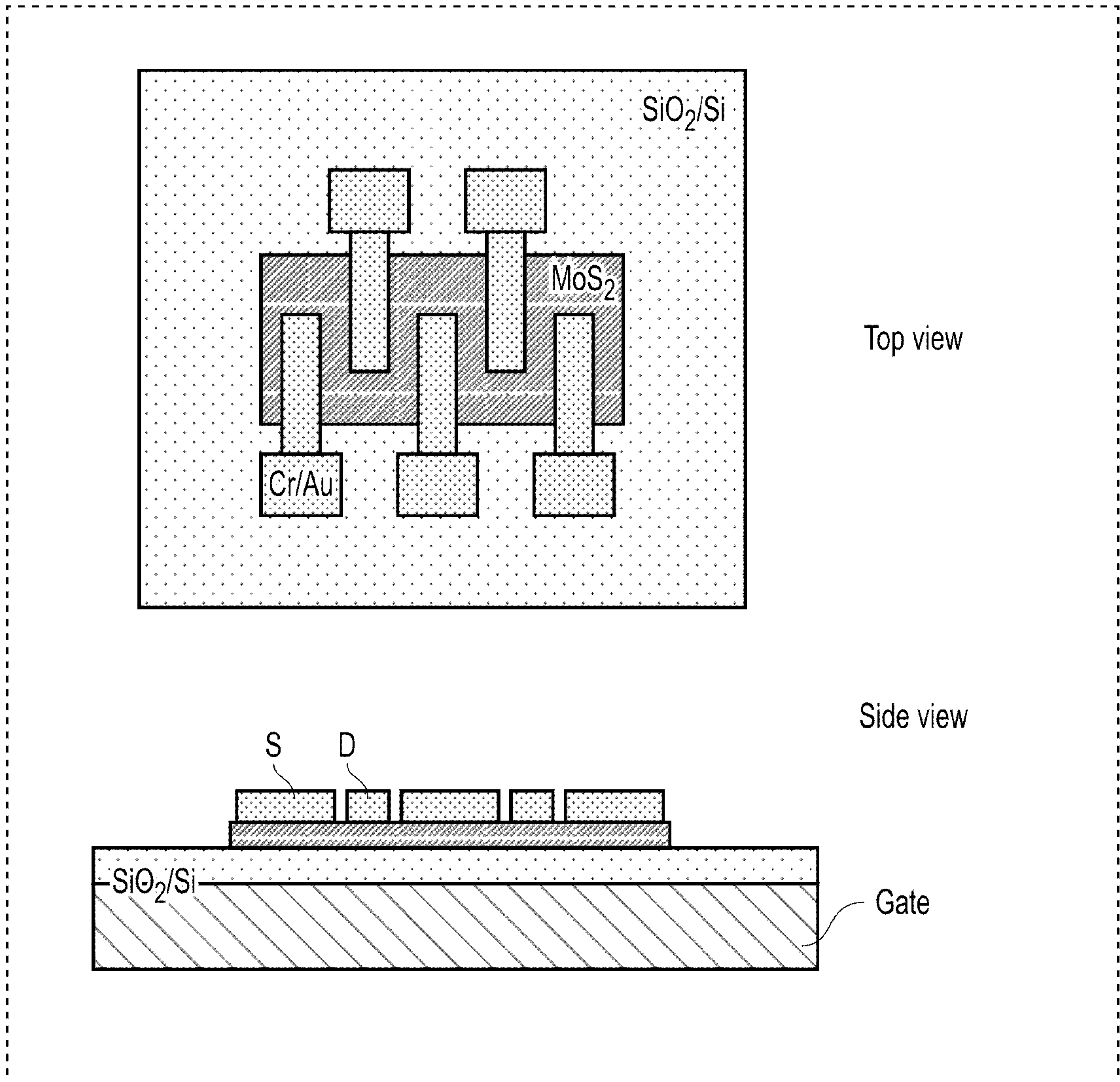

FIG. 5(a)

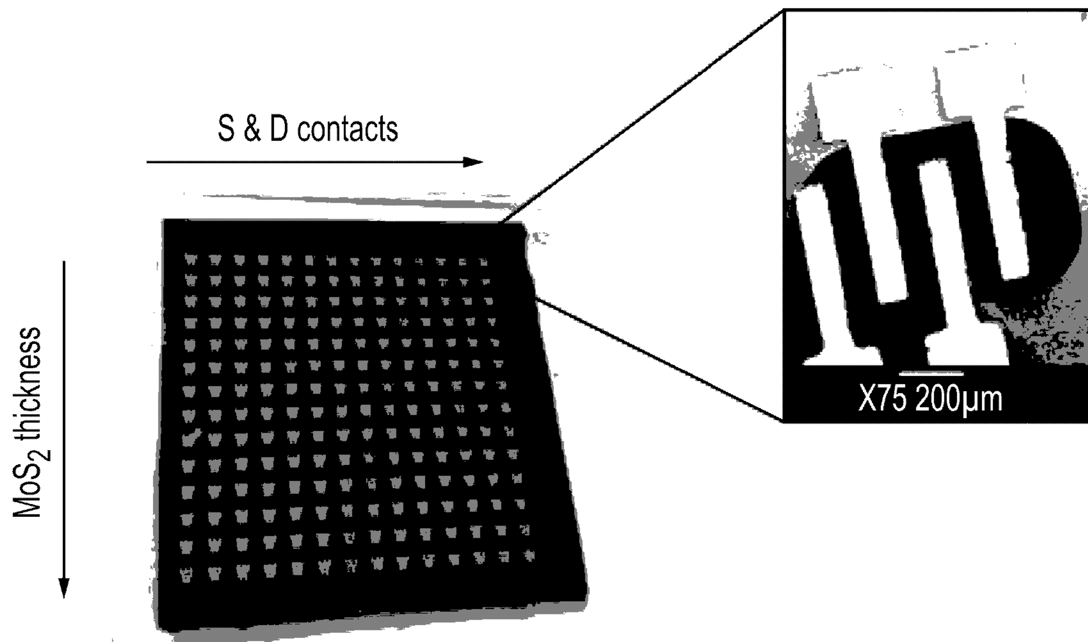

FIG. 5(b)

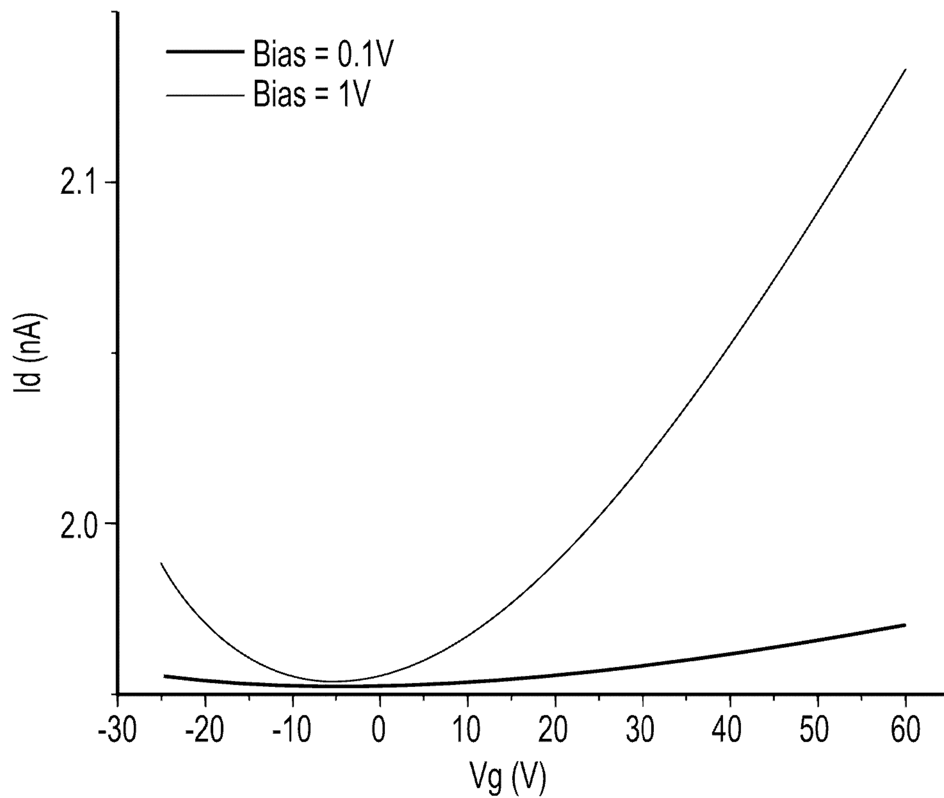

FIG. 5(c)

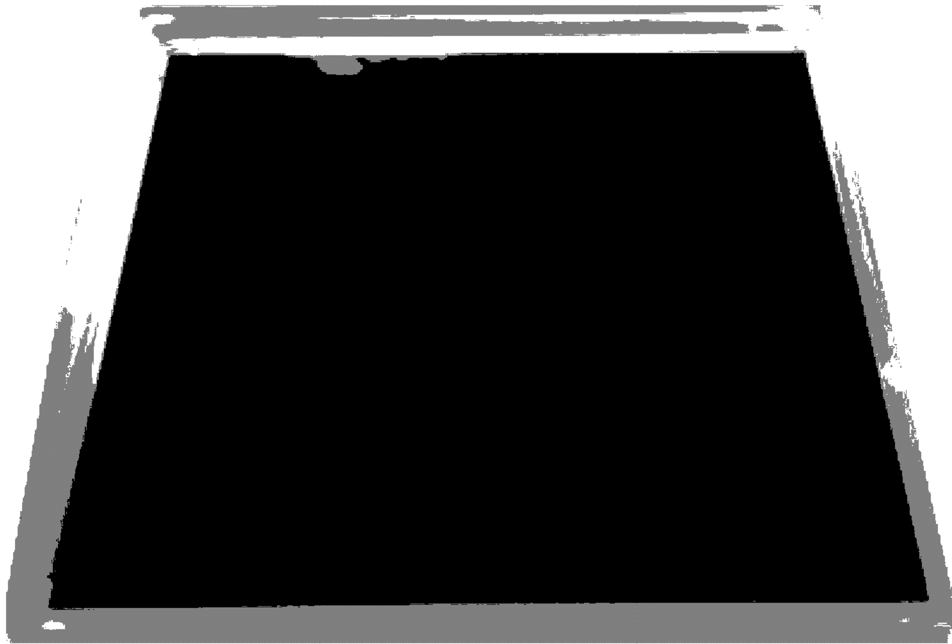

FIG. 6(a)

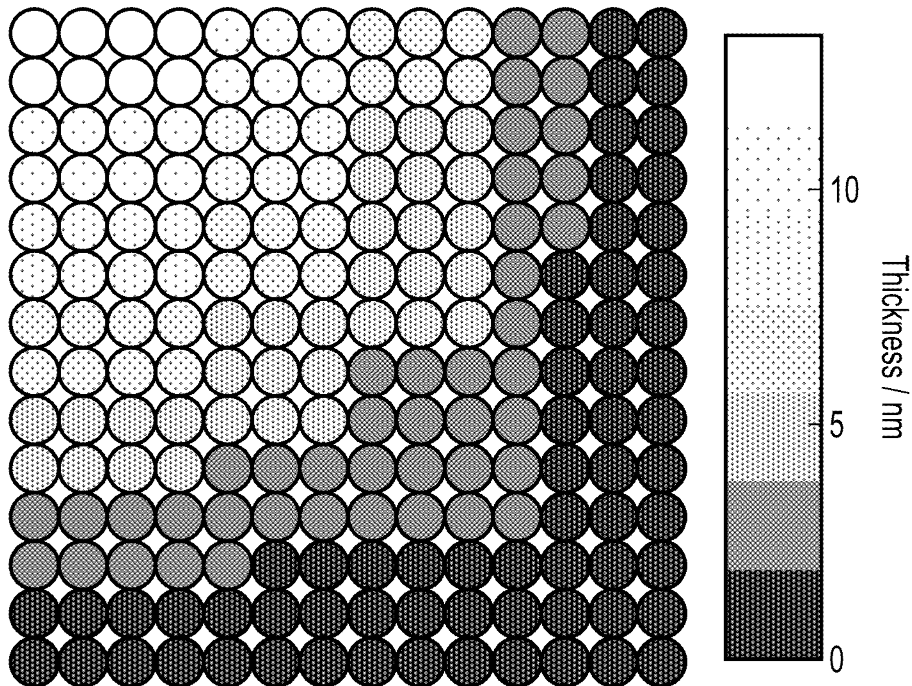

FIG. 6(b)

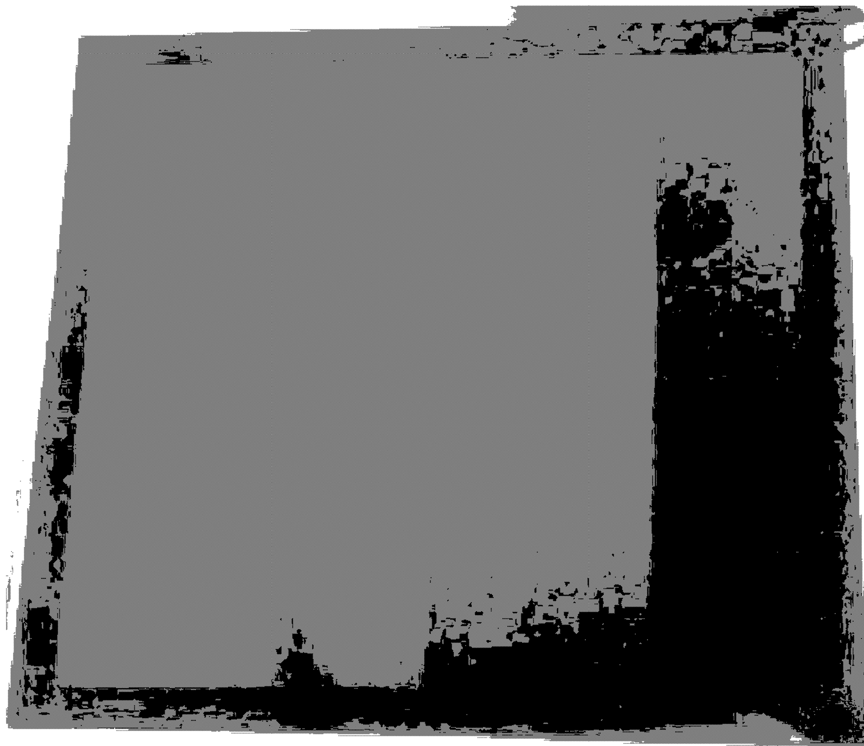

FIG. 6(c)

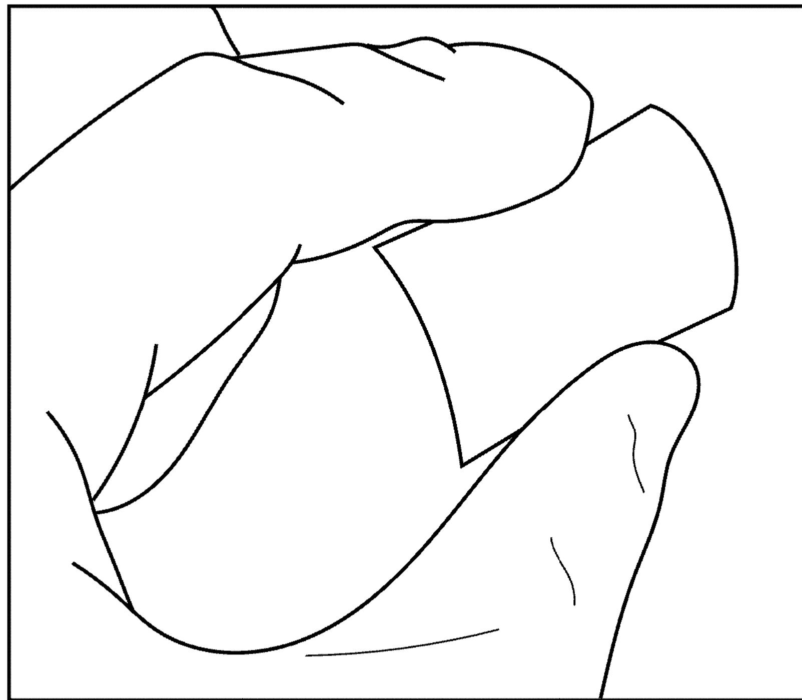

FIG. 7(a)

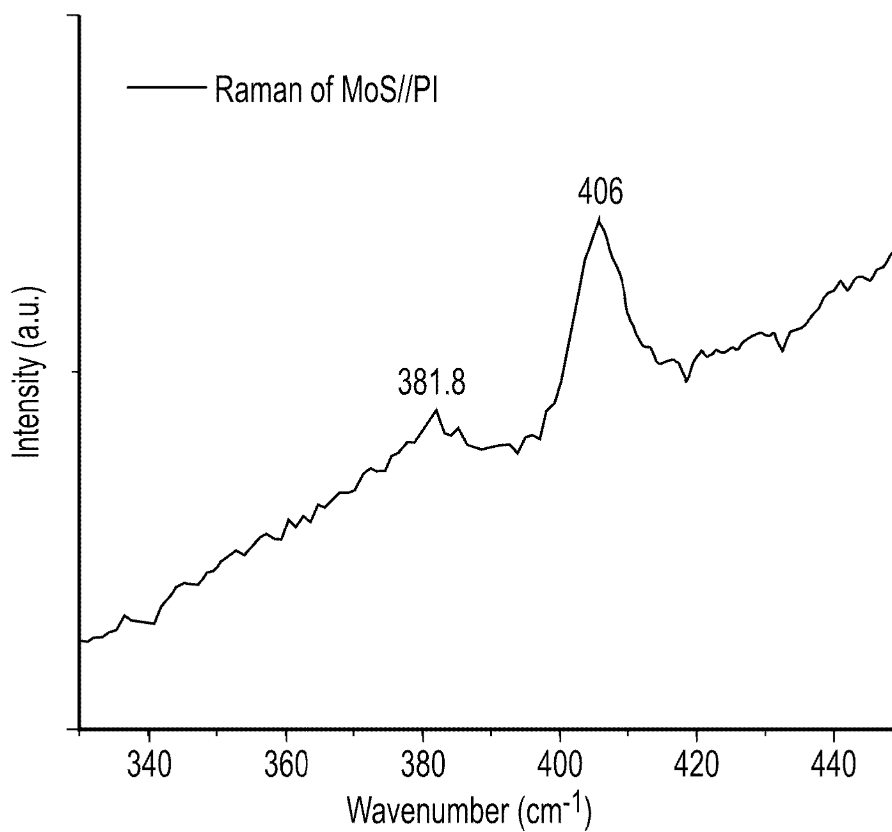

FIG. 7(b)

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2020/051893

A. CLASSIFICATION OF SUBJECT MATTER
INV. C01B17/20 C01B17/22 C01B17/42 C01B19/00 H01L21/02
H01L45/00 C23C14/06
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
C01B H02N H01L C23C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	YUXI ZHAO ET AL: "Low-temperature synthesis of 2D MoS 2 on a plastic substrate for a flexible gas sensor", NANOSCALE, vol. 10, no. 19, 8 May 2018 (2018-05-08), pages 9338-9345, XP055612351, United Kingdom ISSN: 2040-3364, DOI: 10.1039/C8NR00108A abstract figures 1,2 paragraph [Resultsanddiscussion] -----	1-11, 13-18 12

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 October 2020	10/11/2020

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Mertins, Frédéric

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	YONGJI GONG ET AL: "Tellurium-Assisted Low-Temperature Synthesis of MoS 2 and WS 2 Monolayers", ACS NANO, vol. 9, no. 12, 22 December 2015 (2015-12-22), pages 11658-11666, XP055745495, ISSN: 1936-0851, DOI: 10.1021/acsnano.5b05594 abstract paragraph [Resultsanddiscussion]	1,4-11, 13-18 12
X Y	US 2017/218498 A1 (CHAI JIANWEI [SG] ET AL) 3 August 2017 (2017-08-03) abstract paragraphs [0011], [0044], [0022], [0063], [0084] figure 1 claims 24,39,40	1-11, 13-18 12
Y	Dae-Hyung Cho ET AL: "This is an Accepted Manuscript Non-Toxically Enhanced Sulfur Reaction for Chalcogenide Thin Film Using a Thermal Cracker", J. Name, 1 January 2012 (2012-01-01), pages 1-3, XP055745543, Retrieved from the Internet: URL:https://pubs.rsc.org/en/content/getauthorversionpdf/C4TA02507E [retrieved on 2020-10-30] the whole document	12
A	WO 2015/091781 A2 (IMEC VZW [BE]; UNIV LEUVEN KATH [BE]) 25 June 2015 (2015-06-25) the whole document	1-18

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/GB2020/051893

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 2017218498 A1	03-08-2017
		WO 2016013984 A1	28-01-2016
WO 2015091781 A2	25-06-2015	EP 3084033 A2	26-10-2016
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