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Declarations under Rule 4.17:

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(54) Title: METHODS, CIRCUITS, SYSTEMS AND ARRANGEMENTS FOR UNDRIVEN OR DRIVEN PINS

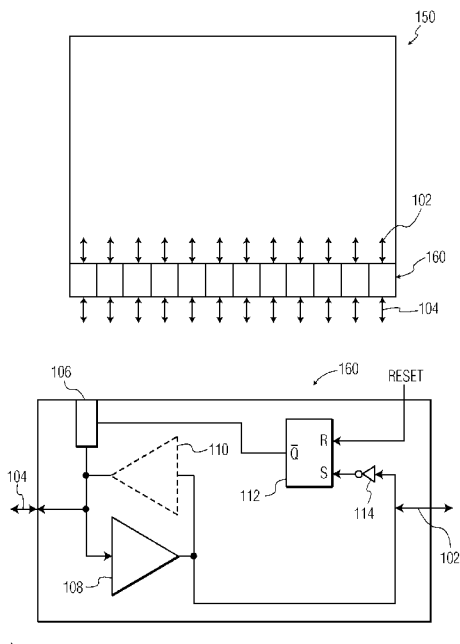


FIG. 1

(57) Abstract: Input/Output (I/O) pin circuits, devices, methods and systems are implemented in various fashions. According to one such method, a valid signal level is provided for a pin of an integrated circuit (IC) die. Responsive to a reset signal, a first mode (304) is entered where one of a pull-up circuit or pull-down circuit is enabled (308, 310) to set the pin to the valid signal level. A change in signal level of the pin that is a deviation from the valid signal level is detected (312). Responsive to detecting the change, a second mode (314) is entered where the one of a pull-up circuit or pull-down circuit is disabled (316).

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  - *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*
- Published:**
- *with international search report (Art. 21(3))*

## METHODS, CIRCUITS, SYSTEMS AND ARRANGEMENTS FOR UNDRIVEN OR DRIVEN PINS

5           The present invention relates generally to input/output pins, and more specifically, to dynamic pull-up or pull-downs for input/output pins.

          Integrated circuits (ICs) are continually increasing in their complexity. In addition to added functionality, ICs sometimes consolidate functionality from several ICs into a single IC. In addition to increasing processing power within an IC, an  
10           important factor is often the communication bandwidth between an IC and other components in the system. For example, increased processing power (and increased functionality) often results in a need for more data throughput to and from the IC (*e.g.*, to provide sufficient data for the increased processing power). In one instance, the communication bandwidth can be increased using faster serial data rates and/or  
15           more parallel data lines. Thus, increasing the complexity of an IC often results in an increase in the number of input/output pins. This can lead to increased power draw from the input/output pins. Moreover, integrated circuits are sometimes used in environments with limited power constraints. These and other factors are often at odds with desires to increase the complexity of ICs and offer a backdrop for many of  
20           the problems seen in IC development efforts.

          Often the input/output pins use a pull-up and/or pull-down to ensure that a particular pin is set to a valid signal level even when not driven externally. This would include an input pin that was not driven or a bi-directional pin that was not active (*e.g.*, a three-state output in high-impedance mode). These pull-ups/downs can  
25           be implemented in a number of different manners including, but not limited to, an input cell contained within the IC or an external element (*e.g.*, a resistor tied to a valid signal level). When active, pull-up/down circuits dissipate power. The power dissipation can be particularly large for situations where the pin is driven to a substantially different voltage level relative to the pull-up/down voltage level. For  
30           example, if the pull-up/down is implemented using a resistor, the dissipated power for each pin is commensurate with the difference between the pull-up/down voltage level and the driven voltage level. For a large number of input/output (I/O) pins, such dissipated power can be substantial. Moreover, the presence of a pull-up/down may slow some signal transitions. This may require an increase in the strength of the

driver and might not only result in increased power draw, but worsened voltage supply drops. For example, local voltage supply levels can be lowered due to current draw from a near simultaneous transition of a number of pins. Such transitions can be relatively common for pins of a common data bus.

5           Various aspects of the present invention are directed to methods, systems, circuits and arrangements for implementing dynamically controlled pull-ups or pull-downs on input/output (I/O) pins of IC die. One of a pull-up or a pull-down is enabled on the I/O pins. Upon sensing that the pin is being driven, the pull-up or pull-down is disabled. This can be particularly useful for reducing the power consumption  
10 of the IC die and/or the system in general. For example, embodiments of the present invention can be useful for disabling unnecessary pull-up and/or pulls-downs without the use of external components.

Consistent with another example embodiment, a method provides a valid signal level for a pin of an integrated circuit (IC) die. Responsive to a reset signal, a  
15 first mode is entered where one of a pull-up circuit or pull-down circuit is enabled to set the pin to the valid signal level. A change in signal level of the pin, such as a deviation from the valid signal level, is detected. Responsive to detecting the change, a second mode is entered where the pull-up/down is disabled.

Consistent with another example embodiment, a circuit provides a valid signal  
20 level for a pin of an integrated circuit (IC) die. When enabled, one of a pull-up circuit or a pull-down circuit is able to set the pin to the valid signal level. An enabling circuit is provided. The enabling circuit enables either the pull-up circuit or the pull-down circuit in response to a reset signal. The enabling circuit also disables the enabled pull-up/down circuit in response to a change from the valid signal level at the  
25 pin.

Consistent with another example embodiment, a system is implemented with an integrated circuit (IC) die. Within the IC die are a variety of components. A pin connects signals external to the IC die with signals internal to the IC die. Either a pull-up circuit or pull-down circuit sets the pin to the valid signal level when enabled.  
30 An enabling circuit enables the pull-up/down circuit in response to a reset signal. The enabling circuit also disables the pull-up/down circuit in response to the pin changing from the valid signal level.

The above summary is not intended to describe each embodiment or every implementation of the present disclosure. The figures and detailed description that follow more particularly exemplify various embodiments.

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 shows a circuit diagram for an IC die having dynamic pull-ups/downs for I/O pins, according to an example embodiment of the present invention;

FIG. 2 shows a circuit for providing dynamic pull-up and pull-down control, according to an example embodiment of the present invention;

FIG. 3 shows a flow diagram that is consistent with a method for providing dynamic pull-up or pull-down functionality on an I/O pin, according to an example embodiment of the present invention; and

FIG. 4 shows a circuit diagram for an IC die having dynamic pull-ups/downs for I/O pins, according to an example embodiment of the present invention.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the scope of the invention including aspects defined by the appended claims.

The present invention is believed to be applicable to a variety of different types of processes, devices and arrangements for use with communication pins of an integrate circuit (IC) die, and in particular, to approaches for dynamic pull-ups/downs. While the present invention is not necessarily so limited, various aspects of the invention may be appreciated through a discussion of examples using this context.

Embodiments of the present invention relate to a method for implementing dynamically controlled pull-ups or pull-downs on input/output (I/O) pins of an IC die. As used herein, unless otherwise stated, I/O pin is used to denote any of an input pin or a bidirectional (input and output) pin. By default either a pull-up or a pull-down is enabled on the I/O pins. Upon sensing that the pin is being driven, the pull-up or pull-down is disabled. This can be particularly useful for reducing the power consumption of the IC die and/or the system in general.

In a specific embodiment, the pull-up or pull-down remains disabled until reset by a signal. For example, the system can generate a reset signal upon startup. This enables the pull-ups and/or pull-downs on the I/O pins. After initialization, the system can assume normal operation. As signals are driven on the I/O pins, the pull-ups on those I/O pins are disabled. This results in the pull-ups and pull-downs for actively driven I/O pins being disabled over time (*e.g.*, as they are driven/used), while the pull-ups and pull-downs for those I/O pins that are not actively driven remain enabled.

The various signals discussed herein can be implemented in a variety of manners including either active high or active low. For simplicity, such aspects of the signals are not mentioned for each instance. The invention, however, should not be so limited.

FIG. 1 shows a circuit diagram for an IC die having dynamic pull-ups/downs for I/O pins, according to an example embodiment of the present invention. IC die 150 includes a plurality of I/O pins, including I/O pin 160. I/O pin 160 communicatively couples internal data line 102 to external data line 104. External data line 104 is desired to be maintained at a valid signal level, even where it is otherwise unused. Pull-up/down element 106, when enabled and not overdriven, sets data line 104 to a valid signal level. Buffer/driver 108 formats the signal to generate signal 102. Signal 102 can then, if so desired, be used within the IC die. Optionally, I/O pin 160 can be a bi-directional pin that is driven by buffer/driver 110.

When I/O pin 160 is initialized by the reset signal, SR latch 112 is set. Once set the SR latch 112 output enables pull-up/down 106. The SR latch maintains the enablement of pull-up/down 106 until the signal is driven. If pull-up/down element 106 is a pull-up, inverter 114 can be implemented. If pull-up/down element 106 is a pull-down, inverter 114 can be removed. Alternatively, a different SR latch configuration can be used, such as the configuration shown in connection with the pull-down of FIG. 2. In this manner, SR latch 112 detects a change in the signal level. In particular, SR latch 112 is reset when signal 104 is driven to a level that is opposite of the signal level of pull-up/down element 106. Once pull-up/down element 106 is disabled, it remains disabled until a reset pulse is provided.

A reset pulse can be provided at any point. In a first instance, a reset pulse is provided only once (*e.g.*, upon power-up of the IC die). In another instance, a reset pulse is provided at anytime during which the I/O interface has the potential to

change. For example, the reset pulse can be provided after power-up/initialization in response to an external device being disabled. External devices can be disabled for any number of reasons including, but not limited to, changes in operating (*e.g.*, power-saving) modes or physical removal (or addition) of a device. Another instance  
5 involves the application of a reset pulse in response to detecting corrupted data or spurious data on one or more pins. In yet another instance, the reset can be periodically provided. While such periodic reset pulses could result in increased power draw relative to a single reset pulse, the periodic reset could correct for incorrectly disabled pull-up/down elements that could otherwise accumulate overtime.

10 FIG. 2 shows a circuit for providing dynamic pull-up and pull-down control, according to an example embodiment of the present invention. I/O pin 200 connects to an external pin of the IC. Pull-up 202 and pull-down 204 are connected to a high and low voltage, respectively. Switches 201 and 203 connect (and disconnect) pull-up 202 and pull-down 204, respectively, to I/O pin 200. Input buffer 206 buffers the  
15 signal from I/O pin 200. Logic blocks 208 and 210 control switches 201 and 203, respectively. Logic blocks 208 and 210 each have inputs for pull-up/down selection, reset and the current state of I/O pin 200. The pull-up/down selection signal allows for flexible selection of either a pull-up or a pull-down implementation for I/O pin 200. The logic also ensures that only one of the pull-up 202 or pull-down 204 is  
20 enabled at any one time.

The resetn signal places both logic blocks 208 and 210 in a state to enable respective pull-up 202 or pull-down 204, as further conditioned upon the pull-up/down selection signal. Once the resetn signal has been removed, the enabled pull-up/down remains enabled until a change in signal value of I/O pin 200 is detected. In  
25 particular, logic block 208 detects a transition (on I/O pin 200) from a pull-up signal value to a low signal value. Upon such detection, the enable signal sent to switch 201 is removed so as to disable pull-up 202. Alternatively, logic block 210 detects a transition (on I/O pin 200) from a pull-down signal value to a high signal value. Upon such detection, the enable signal sent to switch 203 is removed so as to disable  
30 pull-down 204. Once either pull-up/down is disabled, the appropriate logic block maintains the disabled state until a reset pulse is received.

Table 1 shows an example logic function for such a circuit.

TABLE 1

PU/PD	Resetn	I/O Pin	PU-Enable	PD-Enable
0	0	X	0	1
1	0	X	1	0
0	1	0	0	Maintain State
0	1	0->1	0	0
1	1	1	Maintain State	0
1	1	1->0	0	0

As shown in Table 1, a resetn (active low) pulse enables the appropriate pull-up or pull-down. Once enabled, the I/O pin state should settle to the corresponding pull-up/down value unless otherwise driven. Thereafter, Table 1 shows the selected PU/PD as maintaining state. Thus, after the resetn is removed the selected pull-up/down will maintain the current (enabled) state so long as the I/O pin is not driven to a different value. If the signal level changes (0 -> 1, for pull-down; 1 -> 0, for pull-up), then the selected pull-up/down is disabled. After such a state, Table 1 shows that the selected pull-up/down will remain disabled (*i.e.*, either disabled or maintain current (disabled) state) unless a reset is received.

The pull-up/down selection signal can be implemented in various manners. In one instance, a register (or registers) contains a pull-up or down setting that determines the status of the PU/PD signal provided to one or more pins. This register setting can be, among other things, loaded from a non-volatile memory (*e.g.*, at startup), part of an initialization process or program, or set using external logic or configuration pin(s). In another instance, the particular pull-up or pull-down setting can be hard-coded into the logic of the IC. This can be useful, for example, where certain pins have predetermined functionality. In yet another instance, the IC can be initialized according to a first default setting for the pull-up and pull-downs. Thereafter the IC can be reinitialized (*e.g.*, using an internal or external configuration protocol). An example re-initialization protocol can be implemented by setting pull-up/down register(s) and triggering the resetn signal to the appropriate pins.

The skilled artisan would recognize the specific logic implementation shown in the various figures is merely representative of one example that provides similar functionality. As such, various changes to the circuit are envisioned without

departing from the spirit of the invention. For example, the logic can be modified to account for inverted input signals and/or inverted active switch enables. Other examples include, but are not limited to, latches other than SR latches (*e.g.*, clocked (D) flip-flops or gated SR latches) and combinations of discrete components providing similar functionality.

FIG. 3 shows a flow diagram that is consistent with a method for providing dynamic pull-up or pull-down functionality on an I/O pin, according to an example embodiment of the present invention. Should a reset 302 be received, at any point, the system enters mode 304. In mode 304, decision block 306 represents a selection of a pull-up or a pull-down for the I/O pin. The selected pull-up or pull-down is enabled at steps 310 and 308, respectively. The enable steps 308 or 310 each implies that the alternative/non-selected pull-up or pull-down is disabled. Mode 304 is maintained, along with the enabled/disabled pull-up and pull-down settings until a signal level change is detected at decision block 312. The signal level change is indicative of the pin being driven.

Mode 314 is entered in response to the detection of decision block 312. In mode 314, the enabled pull-up or pull-down (from enable step 308 or 310) is disabled. This results in both the pull-up and the pull-down being disabled. Mode 314 is maintained (along with the disabled pull-up/down) until a reset is received.

It should be noted that the flow diagram shown in FIG. 3 is merely representative of one embodiment of the present invention. The present invention is not so limited and can include various modifications or additions to the flow diagram. As a non-limiting example, the selection of a pull-up or pull-down at step 306 can be removed for a pin that only requires one of a pull-up or pull-down. While such an implementation might reduce the flexibility of the pin to provide both a pull-up and a pull-down, such a change can be useful to simplify the logic and possibly to reduce the area and/or power requirements of the system.

FIG. 4 shows a circuit diagram for an IC die having dynamic pull-ups/downs for I/O pins, according to an example embodiment of the present invention. In particular, FIG. 4 is a variation of the circuit of FIG. 1 in which additional logic 402 has been added. SR latches have what is sometimes referred to as restricted conditions on their input signals. If the inputs correspond to the restricted conditions for an SR latch, the output of the latch can be subject to what is sometimes referred to as a race condition. For example, race conditions exist in certain SR latches when

both the set and reset inputs are active. This results in an output state that is dependent upon signal propagation delays of the components of the SR latch. These propagation delays can be difficult to ascertain with certainty because they are often dependent upon a number of different circuit properties, some of which may be unknown at the design phase. To compensate for this potential issue, logic 402 prevents both the inputs of the SR latches from being active. Instead, one input is set to an inactive state, while the other remains active. For example, for a situation where S = active and R = active, the input seen due to logic 402 is one of the inputs is inactive and the other is active.

10           The skilled artisan would recognize that other logic could be implemented to achieve the same or similar functionality. For example, the dual active set/reset could be converted (by logic similar to that of 402) into either S = inactive and R = inactive, S = inactive and R = active, or S = active and R = inactive.

15           While the present invention has been described above and in the claims that follow, those skilled in the art will recognize that many changes may be made thereto without departing from the spirit and scope of the present invention.

What is claimed is:

1. A method for providing a valid signal level for a pin of an integrated circuit (IC) die (150), the method comprising:
  - 5 responsive to a reset signal, entering a first mode (304) where one of a pull-up circuit and a pull-down circuit (106) is enabled to set the pin to the valid signal level; detecting a change in signal level of the pin (312), the change being a deviation from the valid signal level; and
  - responsive to detecting the change, entering a second mode (314) where the  
10 one of a pull-up circuit and a pull-down circuit (106) is disabled.
2. The method of claim 1, further including the step of selecting said one of a pull-up circuit and a pull-down circuit for enablement in response to a pull-up/pull-down signal.
3. The method of claim 1, wherein the modes are implemented using a set-reset  
15 (SR) latch having a set input and a reset input, the reset signal connected to one of the set input and the reset input and a signal indicative detecting a change in the signal level as inputs connected to the other of the set input and the reset input.
4. The method of claim 1, wherein in the first mode the other of the one of a pull-up circuit and a pull-down circuit is disabled.
- 20 5. The method of claim 1, wherein in the second mode the other of the one of a pull-up circuit and a pull-down circuit is disabled.
6. The method of claim 1, further including the step of selecting said one of a pull-up circuit and a pull-down circuit for enablement in response to a pull-up/pull-down signal that is responsive to a memory element within the IC die.
- 25 7. The method of claim 1, wherein the one of a pull-up circuit and a pull-down circuit includes a resistor between the valid signal level and the pin.
8. A circuit for providing a valid signal level for a pin of an integrated circuit (IC) die, the circuit comprising:
  - one of a pull-up circuit and a pull-down circuit (106) that when enabled sets  
30 the pin to the valid signal level; and
  - an enabling circuit (112) that
  - enables the one of a pull-up circuit and a pull-down circuit (106) in response to a reset signal, and

disables the one of a pull-up circuit and a pull-down circuit (106) in response to a change from the valid signal level at the pin.

9. The circuit of claim 8, wherein the one of a pull-up circuit and a pull-down circuit includes a resistor tied to the valid signal level, the valid signal level being  
5 either a high level or a low level, respectively.
10. The circuit of claim 8, wherein the enabling circuit includes a set-reset (SR) latch having a set input connected to a signal indicative of a current signal level of the pin and a reset input connected to the reset signal.
11. The circuit of claim 10, wherein the enabling circuit further includes a second  
10 SR latch having a set input connected to a signal indicative of a current signal level of the pin and a reset input connected to the reset signal, wherein one of the SR latches enables a pull-up resistor and the other of the SR latches enables a pull-down resistor.
12. The circuit of claim 8, wherein the one of a pull-up circuit and a pull-down circuit includes a resistor and switch that are in series and between the valid signal  
15 level and the pin.
13. The circuit of claim 8, further including the other of the pull-up circuit and a pull-down circuit.
14. The circuit of claim 8, further including  
the other of the pull-up circuit and a pull-down circuit, and  
20 a register for storing a setting that is used to select the one of a pull-up circuit and a pull-down circuit by indicating one of a pull-up and a pull-down setting.
15. A system comprising:  
an integrated circuit (IC) die (150) having  
a pin (160) for connecting signals external to the IC die (150) with  
25 signals internal to the IC die (150);  
one of a pull-up circuit and a pull-down circuit (106) that when enabled sets the pin (160) to the valid signal level; and  
an enabling circuit (112) that  
enables the one of a pull-up circuit and a pull-down circuit  
30 (106) in response to a reset signal, and  
disables the one of a pull-up circuit and a pull-down circuit (106) in response to the pin (160) changing from the valid signal level.

16. The system of claim 15, wherein the one of a pull-up circuit and a pull-down circuit includes a resistor tied to the valid signal level, the valid signal level being either a high level or a low level, respectively.

17. The system of claim 15, wherein the enabling circuit includes a set-reset (SR) latch having a set input connected to a signal indicative of a current signal level of the pin and a reset input connected to the reset signal.

18. The system of claim 15, wherein the enabling circuit further includes a second SR latch having a set input connected to a signal indicative of a current signal level of the pin and a reset input connected to the reset signal, wherein one of the SR latches enables a pull-up resistor and the other of the SR latches enables a pull-down resistor.

19. The system of claim 15, wherein the one of a pull-up circuit and a pull-down circuit includes a series resistor and switch circuit connected between the valid signal level and the pin.

20. The system of claim 15, further including a register for storing a setting that is used to select the one of a pull-up circuit and a pull-down circuit by indicating one of a pull-up and a pull-down setting.

21. The system of claim 18, further including logic to prevent first SR latch and the second SR latch from entering a restricted condition.

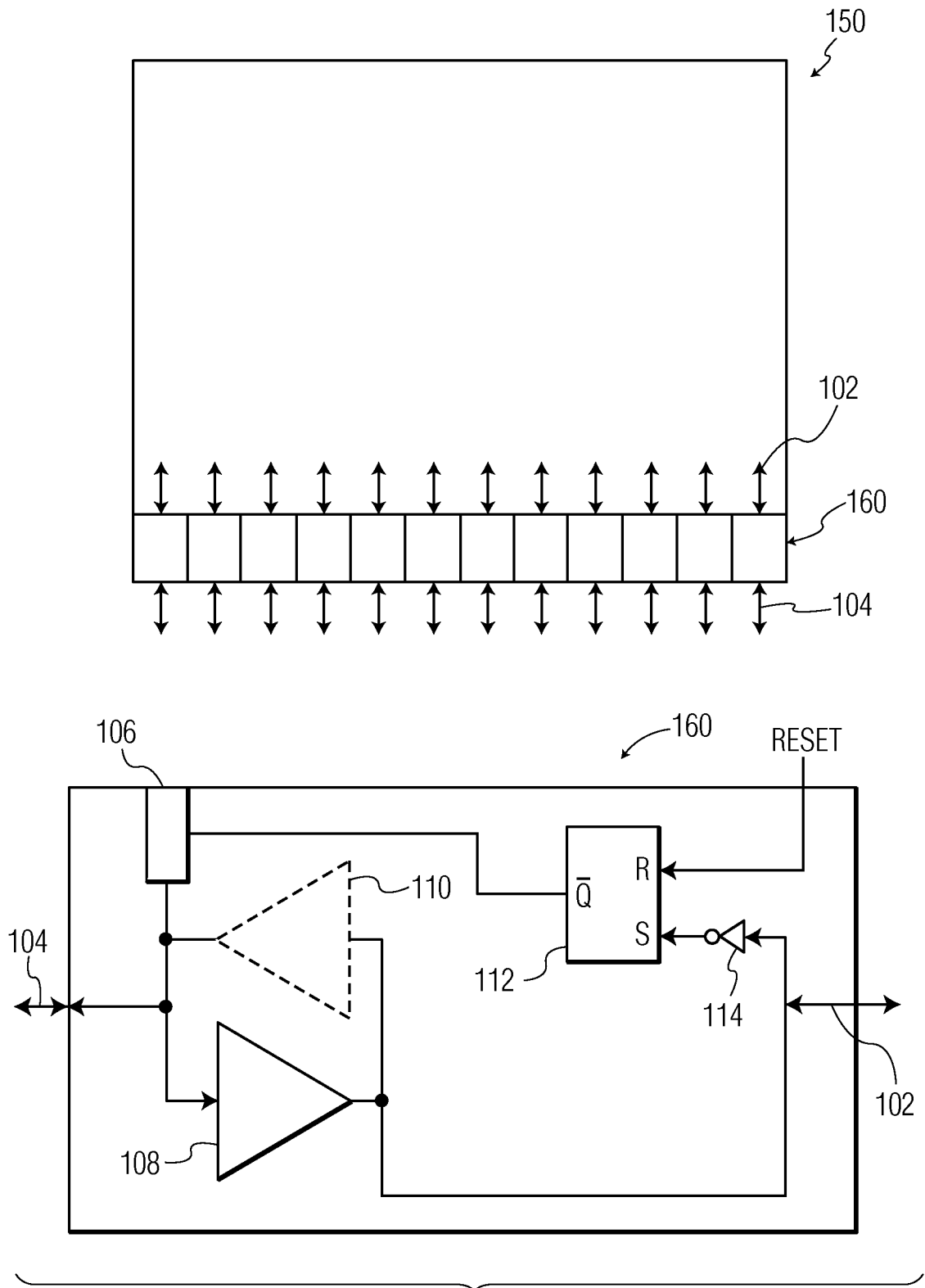


FIG. 1

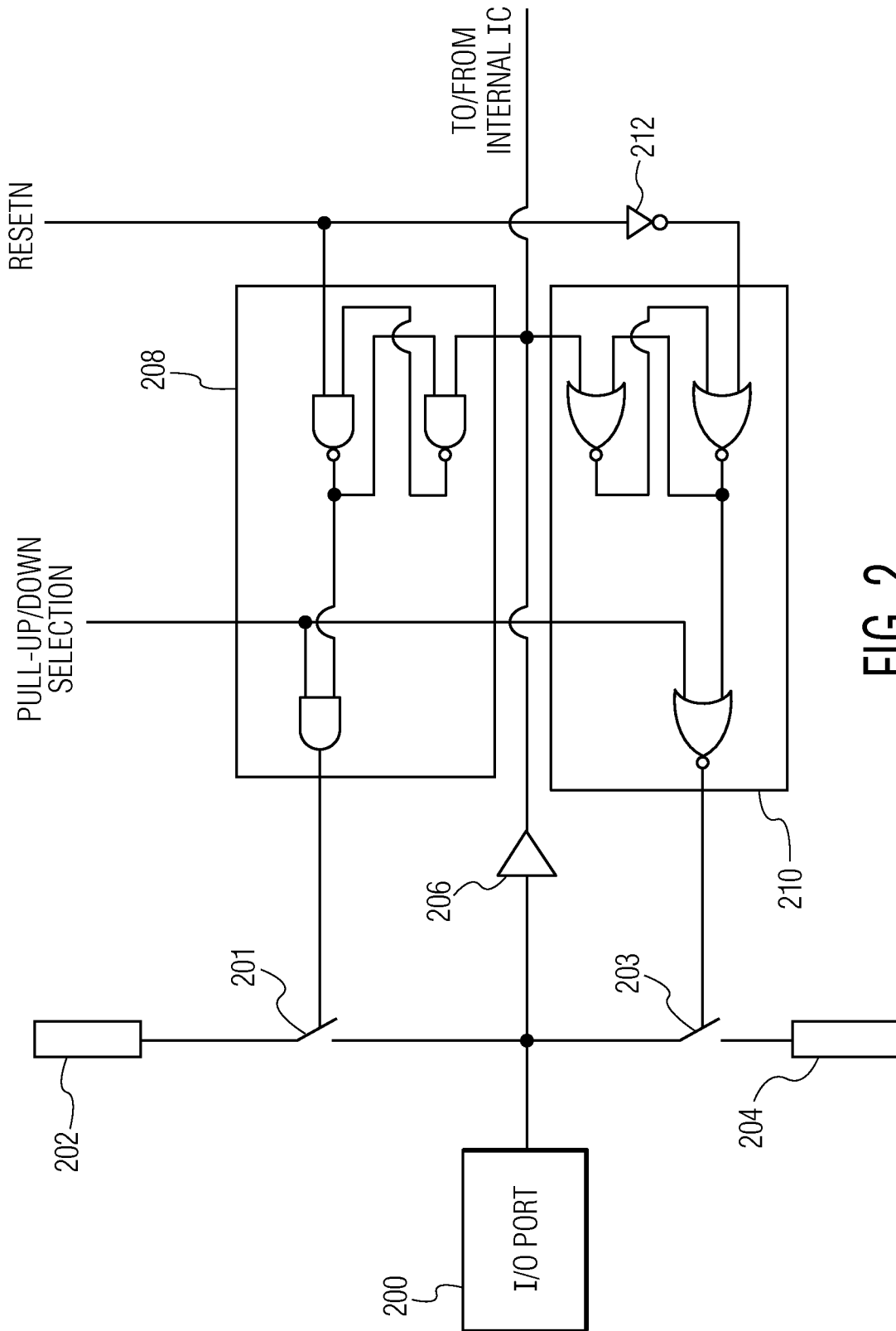


FIG. 2

3/4

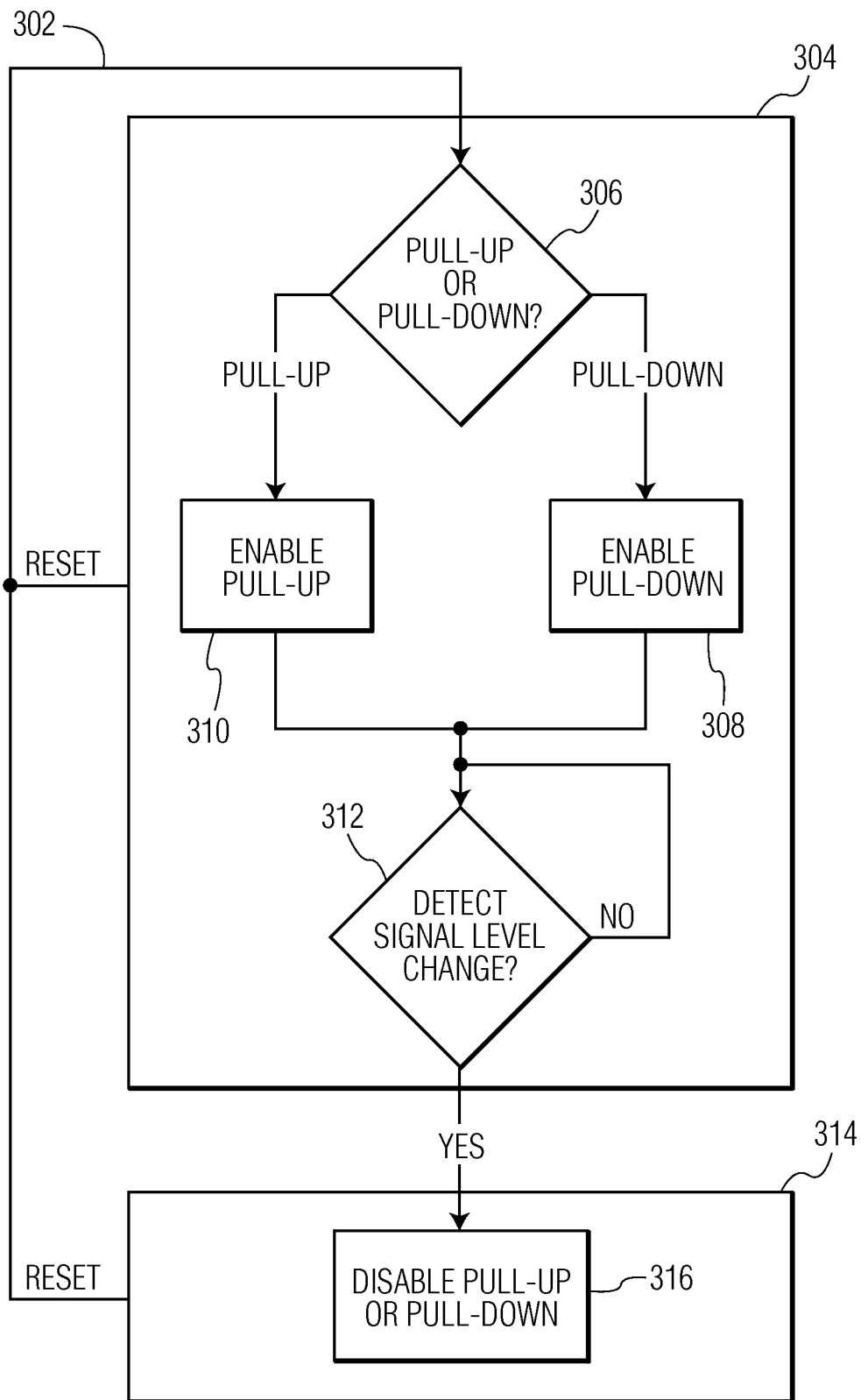


FIG. 3

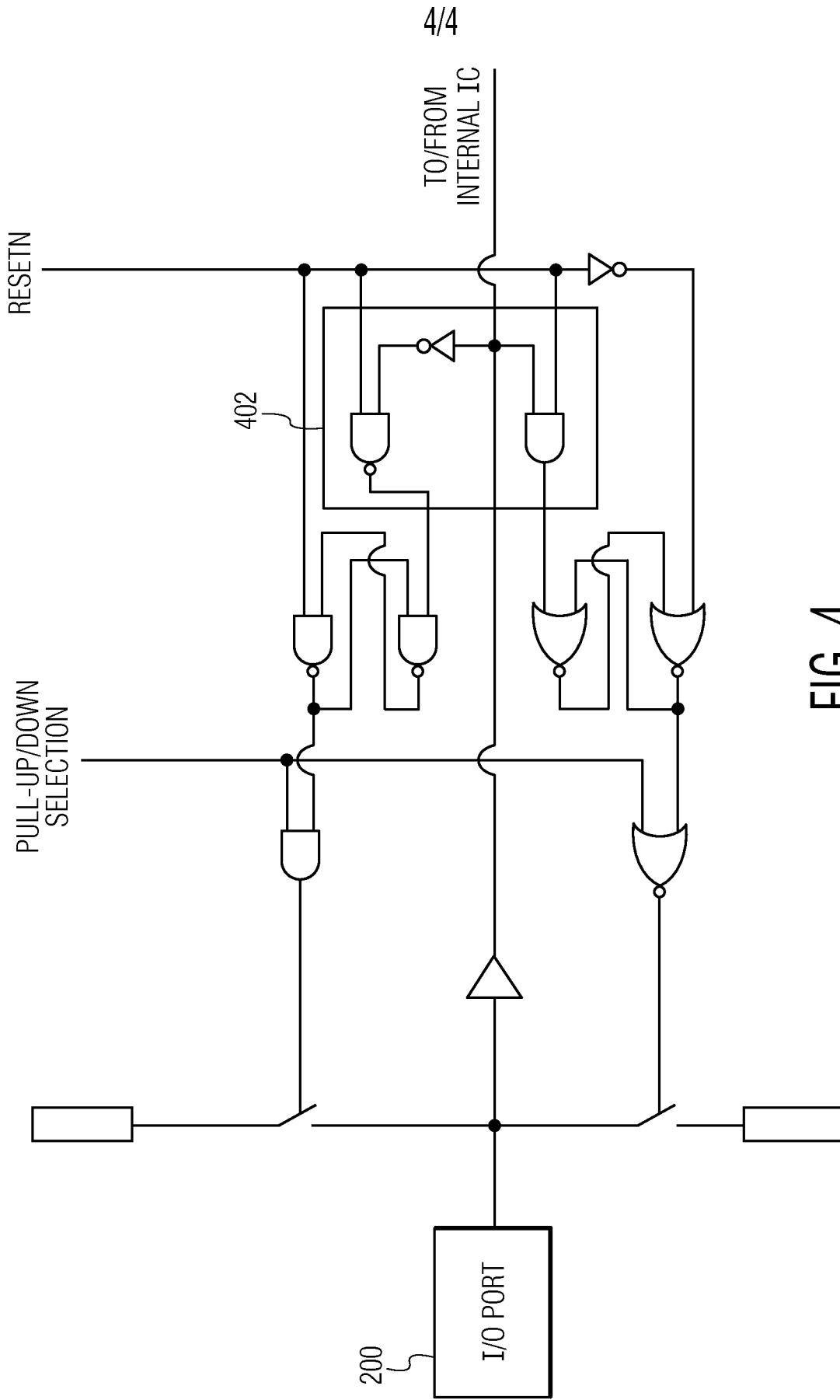


FIG. 4

**INTERNATIONAL SEARCH REPORT**

International application No  
PCT/IB2009/051079

**A. CLASSIFICATION OF SUBJECT MATTER**  
INV. H03K19/173 H03K5/003 H03K5/007

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**  
Minimum documentation searched (classification system followed by classification symbols)  
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)  
EPO-Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/205804 A1 (BROWN RAY [GB]) 6 September 2007 (2007-09-06)  paragraphs [0014] - [0028], [0032]; figures 1,2	1-6,8, 13-15, 17,20
X A	US 5 594 362 A (OWEN JEFFREY R [US]) 14 January 1997 (1997-01-14) column 3, line 8 - column 5, line 10; figures 1-4	1-6,8, 10,15,17 7,9, 11-14, 16,18-20
X	EP 0 726 653 A (TEXAS INSTRUMENTS INC [US]; TEXAS INSTRUMENTS LTD [GB]) 14 August 1996 (1996-08-14) column 3, line 55 - column 6, line 43; figures 1-7	1,2,7-9, 15,16
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Further documents are listed in the continuation of Box C.       See patent family annex.

\* Special categories of cited documents:

*A* document defining the general state of the art which is not considered to be of particular relevance	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
*E* earlier document but published on or after the international filing date	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
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Date of the actual completion of the international search  2 July 2009	Date of mailing of the international search report  08/07/2009
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer  Villafuerte Abrego
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# INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2009/051079

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 335 648 B1 (MATSUSHITA HIROSHI [JP]) 1 January 2002 (2002-01-01) column 3, lines 49-55; figure 2 column 4, lines 15-19; figure 2 column 5, lines 1-6; figure 2 -----	1-20

# INTERNATIONAL SEARCH REPORT

Information on patent family members

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