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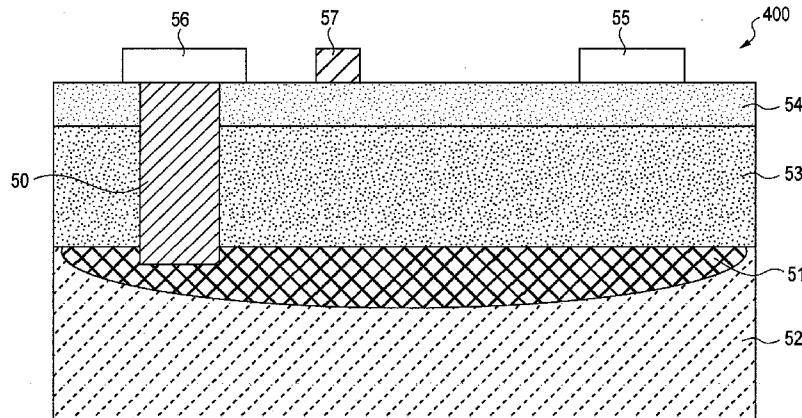


FIG. 4A

(57) Abstract: Circuits, structures and techniques for independently connecting a surrounding material in a part of a semiconductor device to a contact of its respective device. To achieve this, a combination of one or more conductive wells that are electrically isolated in at least one bias polarity are provided.

## **SEMICONDUCTOR DEVICES WITH BACK SURFACE ISOLATION**

### **BACKGROUND OF THE INVENTION**

**[0001]** Semiconductor devices use the conductive properties of semiconductor materials. Such semiconductor materials may include, for example, silicon (Si) or Si-containing materials, germanium (Ge), or materials including gallium nitride (GaN).

**[0002]** In particular, GaN semiconductor devices are increasingly desirable for power semiconductor devices because of their ability to carry large current and support high voltages. Development of these devices has generally been aimed at high power/high frequency applications. Devices fabricated for these types of applications are based on general device structures that exhibit high electron mobility and are referred to variously as heterojunction field effect transistors (HFET), high electron mobility transistors (HEMT), or modulation doped field effect transistors (MODFET). These types of devices can typically withstand high voltages while operating at high frequencies.

**[0003]** One example of a GaN HEMT device includes a semiconductor substrate (e.g., a Si substrate) with at least two interior layers. The different interior layers have different band gaps, which causes polarization that contributes to a conductive two-dimensional electron gas (2DEG) region near the junction of the two layers, specifically in the layer with the narrower band gap. In a GaN semiconductor device, the layers that cause polarization typically include a barrier layer of AlGaN formed adjacent to a current conducting layer of GaN. The polarization creates the 2DEG region in the current conducting layer, allowing charge to flow through the device. This barrier layer may be doped or undoped.

**[0004]** Because a 2DEG region typically exists under the gate of a GaN transistor device when the gate is at zero gate bias, most GaN devices are normally on, or depletion mode devices. If the 2DEG region can be depleted, i.e. removed, when the gate is at zero applied gate bias, the GaN device can operate as an enhancement mode device. Enhancement mode devices are normally off and are desirable because of the added safety they provide. An enhancement mode device requires a positive bias applied at the gate in order to conduct current.

**[0005]** FIG. 1 illustrates a conventional GaN transistor device 100. Device 100 includes: a substrate 11, which may be composed of, for example, silicon (Si), silicon carbide (SiC), sapphire, or other material; one or more transition layers 12 formed over the substrate 11, which may be composed of layers of aluminum nitride (AlN) and aluminum gallium nitride (AlGaN) each about 0.1 to about 1.0  $\mu\text{m}$  in thickness; a buffer layer 13 formed over the one or more transition layers 12, which is typically composed of GaN and typically about 0.5 to about 3  $\mu\text{m}$  in thickness; a current conducting region 14 formed over the buffer layer 13 for providing a current conducting channel, which may be composed of GaN or indium gallium nitride (InGaN) typically about 0.01 to about 0.1  $\mu\text{m}$  in thickness; contact regions 15 formed over or beside the current conducting region 14, which are typically composed of AlGaN, Al, titanium (Ti), and Si, and which may typically be about 0.01 to about 0.03  $\mu\text{m}$  in thickness; a barrier layer 16 formed over the current conducting region 14 and between the contact regions 15, which is typically composed of AlGaN where the Al to Ga ratio is about 0.1 to about 1 with a thickness of about 0.01 to about 0.03  $\mu\text{m}$ ; a gate structure 17 formed over the barrier layer 16 and composed of p-type GaN with a nickel (Ni) and gold (Au) metal contact; and ohmic contact metals 18, 19 formed over the contact regions 15 at a source and drain contact areas, respectively, which may be composed of Ti and Al with a capping metal such as Ni and Au. Current conducting region 14, contact regions 15, and barrier layer 16 collectively form a device layer that provides for electrical connection to and control of device 100.

**[0006]** FIG. 2 illustrates another conventional GaN transistor device 200. Device 200 includes substrate 21, transition layers 22, buffer layers 24, channel layer 25, contact region 26, barrier layer 27, gate structure 28, and source and drain contact 29 and 30. These layers may have similar parameters as those described for FIG. 1. In addition, device 200 has a through-wafer via 20 that extends from a top side contact (i.e., from source contact 30, as shown in FIG. 2, or from drain contact 29) and through all material layers including the substrate to a metal layer 31 on the bottom side of the substrate 21. Metal layer 31 may be, for example, a heat sink.

**[0007]** FIG. 3 illustrates another GaN transistor device 300. Device 300 includes substrate 41, transition layers 42, buffer layers 43, current conducting region 44 including a channel

layer, contact region 45, barrier layer 47, gate structure 48, and source and drain contacts 46 and 49. These layers may have similar parameters as those described for FIGS. 1 and 2. Device 300 includes a substrate connection via 40 that connects substrate 41 to the source contact 49. Unlike the via 20 of semiconductor device 200 (FIG. 2), via 40 of semiconductor device 300 terminates in substrate 41 without extending all the way to the backside of substrate 41.

**[0008]** Via connections such as those described in connection with FIGS. 2 and 3 provide a very low inductance and low resistance path from the back side of the semiconductor device (e.g., the backside of the substrate) to a front side connection of the device (e.g., a source or drain contact, gate structure, or other element). This is important for the high frequency operation for which these devices are intended. Conventional GaN transistor devices 100, 200, and 300 have disadvantages. Device 100 (FIG. 1) has a floating substrate potential when conducting substrates 11, such as Si, are used. This can lead to inadvertent device turn-on if the substrate voltage becomes too positive. In addition, negative substrate voltage can lead to resistance increase of the device 100. Devices 200 and 300 (FIGS. 2, 3) address this problem by electrically tying the respective substrates 21, 41 to the respective contacts 30, 49. For integrated devices, however, the desired substrate potential can be different for each device. Electrically connecting the substrate to the contact may result in some integrated devices having non-optimal substrate potentials.

**[0009]** In addition, it is often desirable to have a heat sink connected on the back side of a device, as shown, for example, with heat sink 31 of device 200 (FIG. 2). Electrically connecting the substrate 21 to the contact 30 may result in an undesirable voltage being present at the heat sink 31, unless intervening insulating material is included between the heat sink 31 and the substrate 21. Including insulating material between the heat sink 31 and the substrate 21, however, can be detrimental to the effectiveness of the heat sink 31. Insulating material adds thermal resistance, and the insulating material between 31 and 21 keeps heat inside the device. It often becomes necessary to include this material nonetheless, such as when multiple devices are used to form a circuit and utilize the same heat sink.

**[0010]** One example where it is undesirable, but often necessary, to include insulating material between the heat sink 31 and the substrate 21 is when two GaN field effect transistors (“FETs”) are connected in series to form a buck converter. A first FET in a buck converter has a source connected to ground, and a drain connected to a switch node. The second device has a source connected to the switch node and a drain connected to a high voltage. Thus, the two FET devices are connected to the same potential at the switch node, and are turned on in alternating fashion, such that the switch node voltage alternates between ground and high potential. If the entire substrate is connected to ground (i.e., the first FET device’s source potential), then the second device’s source will become high in potential relative to the substrate, leading to very large resistance increase in this second FET device. If the substrate potential is set to a switch node voltage, the first device will have high negative potential relative to the substrate beneath the source, and its resistance will become high.

**[0011]** It would therefore be desirable to be able to control the potential under each contact of an integrated semiconductor device independently, while also having the flexibility to set the back side of the semiconductor device at an independent potential.

**[0012]** The GaN family of materials, including AlGaN, InGaN, and InAlGaN, are all direct band gap materials. This leads to unique device behavior, such as light generation when electrons recombine with holes, very short minority carrier lifetimes, and rapid carrier generation during avalanche events. The latter characteristic makes GaN device very difficult to control when an avalanche event occurs, and generally leads to destruction of the part. Si, on the other hand, has an indirect band gap, allowing for smooth and controlled avalanche, and safe device operation under avalanche conditions.

**[0013]** It would therefore be desirable to combine the advantageous avalanche capabilities of the Si based devices with the improved speed and resistance characteristics of GaN in a single device.

## SUMMARY OF THE INVENTION

**[0014]** Embodiments described below address the problems discussed above and other problems, by providing for independently connecting a substrate region in a part of a semiconductor device to a contact of its respective device. To achieve this, a combination of one or more implanted wells or diffused conductive regions and via connections are described which provide for isolating the substrate and other elements from each other, while allowing other elements to be tied electrically.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0015]** FIG. 1 illustrates a cross-sectional view of a conventional GaN transistor device.

**[0016]** FIG. 2 illustrates a cross-sectional view of a conventional GaN transistor device utilizing a through wafer via.

**[0017]** FIG. 3 illustrates a cross section view of a conventional GaN transistor device utilizing a substrate connection via.

**[0018]** FIG. 4A illustrates a cross-sectional view of a transistor device formed according to a first embodiment of the present invention.

**[0019]** FIGS. 4B-4G illustrate a process for forming the transistor device of FIG. 4A.

**[0020]** FIG. 5 illustrates a cross-sectional view of a transistor device formed according to a second embodiment.

**[0021]** FIG. 6 illustrates a cross-sectional view of a transistor device formed according to a third embodiment.

**[0022]** FIG. 7A illustrates a cross-sectional view of a transistor device formed according to a fourth embodiment of the present invention.

**[0023]** FIGS. 7B-7G illustrate a process for forming the transistor device of FIG. 7A.

**[0024]** FIG. 8 illustrates a cross-sectional view of a transistor device formed according to a fifth embodiment.

**[0025]** FIGS. 9A-C illustrates a cross-sectional view of a transistor device formed according to a sixth embodiment.

**[0026]** FIG. 10 illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0027]** FIG. 11 illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0028]** FIG. 12 illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0029]** FIG. 13 illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0030]** FIG. 14 illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0031]** FIG. 15 illustrates a top-down view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0032]** FIG. 16 illustrates a top-down view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0033]** FIG. 17 illustrates schematic diagrams of integrated semiconductor devices, in accordance with embodiments described herein.

**[0034]** FIG. 18 illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0035]** FIG. 19 illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0036]** FIG. 20 illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0037]** FIG. 21 illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0038]** FIG. 22A illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0039]** FIG. 22B illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0040]** FIG. 23 illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0041]** FIG. 24 illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0042]** FIG. 25A illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0043]** FIG. 25B illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

**[0044]** FIG. 26 illustrates a cross-sectional view of a transistor device, in accordance with embodiments described herein.

**[0045]** FIG. 27 illustrates a cross-sectional view of an integrated semiconductor device, in accordance with embodiments described herein.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0046]** In the following detailed description, reference is made to certain embodiments. These embodiments are described with sufficient detail to enable those skilled in the art to practice them. It is to be understood that other embodiments may be employed and that various structural, logical, and electrical changes may be made. Also, various methods and processes are described, each including several steps. It should be understood that the steps may be performed in the order described, or in any different order, unless specified otherwise.

**[0047]** While embodiments described herein include GaN semiconductor devices, it should be understood that the invention is not limited to GaN semiconductor devices. For example, the described embodiments may be applicable to semiconductor devices and other devices that use different conductive materials, such as, for example, Si or SiC semiconductor devices and Ge-material semiconductor devices, to name but a few.

**[0048]** In addition, while implanted or diffused conductive regions or wells are described, it should be understood that these are only two processes for providing regions of different polarity within a substrate. Thus, while the described embodiments may refer to implanted or diffused regions or wells, it should be understood that other types of opposite-polarity regions and methods of fabrication thereof may be used.

**[0049]** Described embodiments include a transistor or other semiconductor device, such as a GaN transistor or an integrated circuit including transistors, which has a conductive well that is electrically isolated in at least one bias polarity from surrounding layers or substrate. In some embodiments, a device has a conductive substrate, where regions of the substrate are doped with an oppositely-polarized conductivity to that of the substrate. The regions of opposite polarity may be, for example, an n-type material in a p-type substrate. The device has an electrical connection, such as through a via, from a contact at its front side to the regions of opposite polarity. In other embodiments, the regions may have the same doping type as the substrate, and may be surrounded by one or more insulating layers. In other embodiments, the substrate may be substantially non-conductive, while the regions have either a p-type or n-type doping. In other embodiments, silicon-

on-insulator (SOI) embodiments, and embodiments including parallel conducting channels, are also described. The electrical isolation permits independent control of the substrate or other materials under each device and/or under individual contacts within a single device, among other benefits.

**[0050]** FIG. 4A illustrates a cross-sectional view of a GaN transistor device 400.

Device 400 includes: a substrate 52, which may be composed of one or more Si, SiC, GaN, GaAs, aluminum-nitride (AlN), and/or sapphire-based materials; buffer layers 53 formed over substrate 52, which may be composed of one or more layers of compound semiconductor materials (e.g., AlN material) having a thickness in a range of 0.1-0.5  $\mu\text{m}$ , one or more layers of AlGaN having a thickness of 0.1 to 2  $\mu\text{m}$ , and one or more layers of GaN having a thickness of 0.01 to 5  $\mu\text{m}$ ; and a device layer 54 formed over buffer layers 53, which may include a layer of AlGaN having a thickness of 0.005 to 0.03  $\mu\text{m}$  with 15-100% Al that serves as a barrier layer 16 (FIG. 1). Although not shown for purposes of clarity in explaining other aspects of the embodiments herein, it should be understood that elements for providing electrical connection to and control of device 400 would typically be formed in device layer 54, including a current conducting region 14 (FIG. 1) providing a primary current conducting channel, and contact regions 15 (FIG. 1) under one or both of contacts 55 and 56. The current conducting region may be composed of GaN or indium gallium nitride (InGaN) preferably in a range of about 0.01 to about 0.5  $\mu\text{m}$  in thickness, or other suitable materials known in the art. The contact regions may be composed of AlGaN, Al and titanium (Ti) that may have Si, preferably in a range of about 0.01 to about 0.03  $\mu\text{m}$  in thickness, or other suitable materials known in the art. Device layer 54 may also include a barrier/channel/barrier layer configuration, with a channel layer between two barrier layers.

**[0051]** Device 400 includes contacts 55 and 56 (e.g., source and drain contacts) and a gate structure 57 formed over device layer 54. Contacts 55, 56 may be composed of a mixture of Ti and Al, and gate structure 57 may be composed of p-type GaN and TiN or Ni and Au.

**[0052]** Device 400 also includes a conductive well 51 implanted in substrate 52, and a connection via 50 terminating within the conductive well 51. In one embodiment, substrate 52 can be an n-type substrate with doping between 1e14 and 1e16 electrons/cm<sup>3</sup>, and conductive well 51

can be a p-type well composed of a boron implanted region with concentration of boron between 1e17 and 1e20 atoms/cm<sup>3</sup>. Such a device operates at a negative potential in relation to the substrate. In another embodiment, substrate 52 can be a p-type substrate, and well 51 can be an n-type well, providing a device that operates at a positive potential in relation to the substrate. In another embodiment, conductive well 51 can be p-type or n-type, and substrate 52 can be a substantially non-conductive (i.e., intrinsic) substrate. The different polarities electrically isolate conductive well 51 and substrate 52. Connection via 50 can be composed of Al material in a range of 1 to 5  $\mu$ m thick and a thin layer of TiN in a range of 0.01 to 0.1  $\mu$ m thick. SiO<sub>2</sub> may also be used within or above via 50. Alternatively, tungsten (W) or copper (Cu) plug technologies can be applied to the filling of smaller, higher aspect ratio vias, while utilizing thin layers of TiN in a range of 0.01 to 0.1  $\mu$ m thick for contacting the Si well. The ability to use tungsten or copper technologies for via 50 enables integrating existing charge-coupled device (“CCD”) manufacturing process steps to form via 50.

**[0053]** Via 50 provides a very low inductance and low resistance path from the back side of the semiconductor device 400 to a front side of the device (e.g., as shown, to a contact 56 at the front side), which is beneficial for high frequency operation of device 400. The presence of well 51 below the device and buffer layers 54, 53 at the back side of the device 400 isolates the back surface potential from the substrate potential. One benefit of isolating the substrate potential is that it allows for a heat sink 31 (FIG. 2) connected at a backside of the substrate 52 to be at a different potential than the device 400.

**[0054]** A process for fabrication of device 400 will now be described in connection with FIGS. 4B-4G. In FIG. 4B, a substrate 52 is provided, such as on a wafer substrate, and an implanted well region 51 is formed in a surface of substrate 52. Implanted well region 51 can be formed by performing a Si oxidation on substrate 52, developing a photo-resist pattern definition over substrate 52 using photo lithography, exposing substrate 52 to a dopant, such as high energy boron atoms, using an implanter, stripping away the remaining photo-resist, annealing the wafer at high temperatures (e.g., 1100° C) for an appropriate duration (e.g., 3 hours), and then stripping any surface oxide by immersion in hydrogen-fluoride containing acid.

**[0055]** Buffer layer 53, device layer 54 and gate structure 57 can be grown on substrate 52, and material processing to form gate structure 57 and source and drain contacts 55, 56. For example, as shown in FIG. 4C, buffer layers 53 composed of one or more layers of AlN and/or AlGaN materials preferably about 0.1 to about 1.0  $\mu\text{m}$  in thickness, and one or more layers of GaN material preferably with a thickness of about 0.5 to about 3.0  $\mu\text{m}$ , can be formed on substrate 52 using nucleation and growth processes.

**[0056]** As shown in FIG. 4D, device layer 54 can then be formed on the buffer layers 53. Device layer 54 can include a barrier layer 66 formed above a current conducting region 64 that serves as a primary current channel. Formation of device layer 54 can include depositing a layer of GaN or InGaN material typically about 0.01 to about 0.5  $\mu\text{m}$  in thickness to form current conducting region 64, and depositing a layer of material composed of AlGaN where the Al fraction (which is the content of Al such that Al fraction plus Ga fraction equals 1) is in a range of about 0.1 to about 1.0 and the thickness is in a range between about 0.01 and about 0.03  $\mu\text{m}$  to form barrier layer 66. Device layer 54 may also include depositing a layer of Mg-doped GaN material above layer 66 to form an electron absorption region 66b. Contact regions 65 can be formed by implanting Si into side areas of the deposited barrier layer 66.

**[0057]** As shown in FIG. 4E, gate structure 57 and ohmic contacts 55 and 56 are then formed over the device layer 54 (shown as a single layer in FIG. 4E for purposes of clarity). Gate structure 57 can be formed, for example, by depositing p-type GaN material on a surface of device layer 54 (e.g., over electron absorption region 66b of FIG. 4D), etching the gate structure 57 from the p-type GaN material, and forming a refractory metal contact such as tantalum (Ta), titanium (Ti), titanium nitride (TiN), tungsten (W), or tungsten silicide (WSi<sub>2</sub>) over the GaN material. It should be understood that other known methods and materials for providing a gate structure 57 can also be used. Ohmic contacts 55, 56 can be formed from any known ohmic contact metals, such as Ti and/or Al, along with a capping metal such as Ni, Au, Ti or TiN. The metal and gate layer are each preferably about 0.01 to about 1.0  $\mu\text{m}$  in thickness, and then annealed at high temperature, such as 800C for 60 seconds.

**[0058]** As shown in FIG. 4F, an opening 67 for the connection via 50 (FIG. 4G) may be fabricated by covering device layer 54 (shown as a single layer in FIG. 4F for purposes of clarity) with SiO<sub>2</sub> and a photo-resist everywhere except at the site of the via 50, and then exposing the covered device to a high energy plasma in an etch chamber. The high energy plasma typically contains chlorine based gases, such as BCl<sub>3</sub> or Cl<sub>2</sub>, and is generated through high frequency oscillating fields produced within the etch chamber. After etching through the device and buffer layers, the photo-resist is stripped off of device layer 54 using chemical strippers, oxygen plasma, or combinations of these techniques.

**[0059]** As shown in FIG. 4G, the conductive via 50 is then formed in opening 67 (FIG. 4F). TiN and Al can be deposited into the opening 67 to form the via 50, with the TiN material forming an outer layer along the walls of opening 67 with a thickness in a range of about 100-200Å, and the Al material forming the interior of via 50 having a thickness in a range of about 1-5 um. The TiN outer layer promotes adhesion of an Al material. Routing metal may then be deposited and etched to form connections between the via 50 and other connections, for example the source contact of a GaN FET.

**[0060]** Referring to FIG. 5, another semiconductor device 500 is shown, including substrate 52, buffer layers 53, device layer 54, gate structure 57, and source and drain contacts 55 and 56. Device 500 also includes connection via 50 and well 51. These elements can have similar parameters and can be formed through similar fabrication processes as those described for device 400 in FIG. 4.

**[0061]** Device 500 also includes a plurality of isolation layers 58, 59, 60 between well 51 and substrate 52. Isolation layers 58, 59, 60 form a diode structure along with substrate 52 and well 51. In particular, well 51 and substrate 52 may be materials of the same polarity (e.g., n or p), with isolation layers 58, 59, 60 forming a layer of opposite polarity. The diode structure formed by well 51, substrate 52, and isolation layers 58, 59, 60 provides isolation of the voltage in well 51 from substrate 52 for either polarity of voltage, and thus allows device 500 to be configured with either a positive or negative potential relative to the substrate 52. While three isolation layers are

shown in FIG. 5, there may be greater or fewer isolation layers between well 51 and substrate 52, including a single isolation layer. In a preferred embodiment, at least one isolation layer 58, 59, 60 between well 51 and substrate 52 includes a minority carrier recombination dopant, e.g., platinum (Pt), to prevent latch-up of the diode structure.

**[0062]** Referring to FIG. 6, another semiconductor device 600 is shown, including substrate 52, buffer layers 53, device layer 54, gate structure 57, and source and drain contacts 55 and 56. Device 600 also includes connection via 50 and well 51. These elements can have similar parameters and be formed through similar fabrication processes as those described for device 400 in FIG. 4.

**[0063]** Device 600 includes oppositely-doped isolation layers 68 and 69, which form a thyristor along with well 51 and substrate 52. For example, well 51 may be an n-doped material, substrate 52 may be a p-doped material, isolation layer 68 may be an n-doped material, and isolation layer 69 may be a p-doped material, forming an n-p-n-p junction. The thyristor is characterized in that it has a blocking p-n junction in either direction. In a preferred embodiment, one of isolation layers 68 and 69 is a lightly doped region and will form the blocking region (i.e., either 68 or 69 are low doped regions, typically in a range of 1e14 to 1e 16 atoms/cm<sup>3</sup>).

**[0064]** Device 600 provides for control of the back surface potential of substrate 52. The formed n-p-n-p or p-n-p-n junction also allows either polarity of voltage to be isolated, thus allowing the contacts 55, 56 and gate structure 57 to be held at either positive or negative potential relative to the substrate 52. In another embodiment, for example if it is desirable to have the well 51 and substrate 52 of the same type of doping (i.e., either both p or both n), then a third isolation region (not shown) can be added between substrate 51 and well 52.

**[0065]** Referring to FIG. 7A, another semiconductor device 700 is shown, including buffer layers 53, device layer 54, gate structure 57, source and drain contacts 55 and 56, and connection via 50. These elements can have similar parameters and can be formed through similar fabrication processes as those described for device 400 in FIG. 4. Device 700 also includes a substrate 72, isolation layers 78 and 79, and well 71, which may consist of similar materials as

substrate 52, isolation layers 68 and 69, and well 51, respectively, in device 600 (FIG. 6), but which are formed as flat layers. Device 700 also includes isolation regions 70 formed on respective sides of device 700, which provide isolation between neighboring semiconductor devices. As discussed further below, the configuration of device 700 is operationally similar to device 600, but provides for ease of fabrication. In one example, device 700 may be formed using silicon on insulator (“SOI”) materials. For example, layer 78 may be formed of an insulating material, such as SiO<sub>2</sub>, and layer 79 may be Si of the SOI substrate.

**[0066]** A method of fabricating device 700 is now described in connection with FIGS. 7B-7G. It should be recognized that the method of fabrication described herein may be easily applicable to individual semiconductor devices, or to multiple integrated semiconductor devices on a single wafer substrate.

**[0067]** In FIG. 7B, substrate 72 is provided and isolation layers 78 and 79 are formed as substantially flat layers of material over substrate 72, for example, through epitaxial deposition of Si or other appropriate materials, as described above, or a SOI substrate composed of a Si layer 79 over an SiO<sub>2</sub> layer 78 over a conductive substrate 72.

**[0068]** In FIG. 7C, well 71 is then formed over isolation layers 78, 79, for example, through epitaxial deposition of a boron doped Si material. Alternatively, if SOI substrates are used in device 700, formation of well 71 may not be required to isolate substrate 72.

**[0069]** In FIG. 7D, buffer layers 53 and device layer 54 may then be formed epitaxially using GaN materials or other appropriate materials, in similar form as discussed above in connection with buffer layers 53 and device layer 54 of FIGS. 4C and 4D discussed above, respectively.

**[0070]** As shown in FIG. 7E, gate structure 57 and ohmic contacts 55 and 56 are then formed over the device layer 54 and connection via 50, in the manner described above in connection with FIG. 4E.

**[0071]** As shown in FIG. 7F, a connection via 50 is then formed through device layer 54 and buffer layers 53, and extending into well 71, in the manner described above in connection with FIGS. 4F and 4G. Alternatively, if SOI materials are used and a separate well 71 is not formed in device 700, via 50 may extend into Si layer 79 or SiO<sub>2</sub> layer 78.

**[0072]** As shown in FIG. 7G, isolation regions 70 may then be formed in order to isolate well 71 of device 700 from neighboring devices. Isolation regions 70 can be formed by covering the portion of device layer 54 between the area where contacts 55 and 56 (FIG. 7E) will be formed with a photo-resist, and then etching down the exposed layers at least below well 71, and preferably to isolation layer 78. The etched regions can then be filled with oxide or other suitable isolating materials.

**[0073]** Referring to FIG. 8, a semiconductor device 800 with a silicon on insulator (“SOI”) configuration is shown. Device 800 includes buffer layers 53, device layer 54, source and drain contacts 55 and 56, and gate structure 57. These elements may have similar parameters and be formed through similar fabrication processes as those described for device 600 in FIG. 6. Device 700 also includes a substrate 72, which may be formed as a substantially flat layer, or in an otherwise suitable form.

**[0074]** Device 800 also includes an SOI layer 89 and a buried oxide layer 82 between SOI layer 89 and substrate 72. SOI layer 89 may be, for example, composed of a doped Si material with a concentration in a range of approximately 1e14 to 1e19 atoms/cm<sup>3</sup>. The SOI layer 89 may have either a p or n-type doping, depending upon the desired configuration of device 800. Device 800 includes a connection via 80 electrically tying one or more of the device contacts (e.g., as shown, contact 55) to the SOI layer 89. Buried oxide layer 82 electrically isolates substrate 72 from SOI layer 89.

**[0075]** As shown in FIG. 8, isolation implants 88 may be used to isolate respective SOI regions 89 of neighboring devices. Isolation implants 88 are formed with oppositely-doped material to that used to form SOI layer 89, thus preventing conduction across respective SOI regions 89 of neighboring integrated devices. While isolation implants 88, if thick enough, may be capable of

providing electrical isolation to SOI layer 89 in both directions, there is a possibility that isolation implants 88, which would have an opposite polarity to SOI layer 89, could form an n-p-n diode with the SOI layer 89. This could result in the n-p-n diode, having an open base, conducting between neighboring SOI regions. Accordingly, in another embodiment, a minority carrier lifetime reducing dopant, such as Pt, or any other suitable dopant known in the art, may be added to isolation implants 88.

**[0076]** Referring to FIG. 9A, another semiconductor device 900, including epitaxially-based substrate isolation, is shown. Device 900 includes a substrate 72 and buffer layers 94, which may be formed of similar materials as substrate 72 and buffer layers 53 in device 700 (FIG. 7A). For example, buffer layers 94 may be composed of AlN material having a thickness in the range of 0.1-0.5  $\mu\text{m}$ , one or more layers of AlGaN having a thickness 0.1 to 2  $\mu\text{m}$ , and GaN having a thickness of 0.01 to 5  $\mu\text{m}$ . Substrate 72 may be composed of one or more Si, SiC, or GaAs-based materials.

**[0077]** Device 900 includes one or more substrate isolation layers 92 formed on substrate 72. Substrate isolation layer 92 may be formed of a material such as AlN, or a high Al-content AlGaN material, or other suitable material. The preferred thickness of substrate isolation layers 92 depends on the voltage rating desired for device 900, and may preferably be in a range of .5 to 1  $\mu\text{m}$  per every 100 V desired to be blocked.

**[0078]** Device 900 also includes a current conducting region 95 providing a primary current conducting channel, and a barrier layer 96 above the current conducting region 95. Current conducting region 95 may be composed of GaN, InGaN, or other suitable materials known in the art, and preferably has a thickness in a range of about 0.01 to about 0.1  $\mu\text{m}$ . Barrier layer 96 may be composed of AlGaN where the Al to Ga ratio is preferably in a range of about 0.1 to about 1, with a thickness preferably in the range of about 0.01 to 0.03  $\mu\text{m}$ , or other suitable materials known in the art. Although not shown for clarity in explaining other aspects of the embodiment, it should be understood that device 900 may also include contact regions 15 (FIG. 1) under one or both of contacts 55 and 56, which may be composed of AlGaN, Al and titanium (Ti) that may have Si,

preferably having a thickness in the range of about 0.01 to about 0.03  $\mu\text{m}$ , or other suitable materials known in the art.

**[0079]** Device 900 also includes a conductive well 93 that serves as a parallel current conducting region, forming a parallel channel between substrate isolation layers 92 and buffer layers 94. Parallel current conducting region 93 may be formed of an n-type GaN material with Si doping in a range of  $1\text{e}17$  to  $1\text{e}19 \text{ Si/cm}^3$ . In another embodiment, parallel current conducting region 93 may be formed with an AlGaN material on top of a GaN material, similar to the manner in which current conducting region 95 is formed. Due to the Piezo effect in nitride materials, a 2DEG is formed at the bottom of each AlGaN layer. In such an embodiment, the AlGaN material preferably has a thickness in a range of about .02 to .03  $\mu\text{m}$ , and a concentration of Al in a range of about 20% to 30%. The GaN material preferably has a thickness of approximately 0.1  $\mu\text{m}$ .

**[0080]** Device 900 also includes a channel connection 90 in buffer layers 94 between current conducting region 95 and parallel current conducting region 93. Channel connection 90 may be formed by implanting Si atoms into buffer layers 94, preferably with a density in a range of about  $1\text{e}17$  to  $1\text{e}19 \text{ atoms/cm}^3$ . In other embodiments, channel connection 90 may be composed of tungsten or aluminum with titanium nitride. Device 900 may optionally also include isolation regions 97, which may be composed of similar materials to and formed in a similar manner as isolation regions 70 of device 700 (FIG. 7), or through other suitable materials and processes. For example, isolation regions 97 may be formed by etching the external portions of device 900 to a depth at least below parallel current conducting region 93, and preferably into substrate isolation layers 92, and filling the etched areas with oxide.

**[0081]** FIG. 9B shows a comparison of simulated conduction paths between a conventional semiconductor device (e.g., device 100 of FIG. 1) shown in simulation 920, and a semiconductor device 900 shown in simulation 930. Simulation 920 illustrates a conduction path of a semiconductor device with only a single current conducting region 14 providing a single channel, formed above buffer layers 13. Simulation 930 illustrates a conduction path of a semiconductor device, such as semiconductor device 900, having a primary current conducting region 95, buffer

layers 94, a parallel current conducting region 93 forming a parallel channel, and a substrate isolation layer 92.

**[0082]** FIG. 9C depicts, in graphic form, a comparison of the current conduction paths 940, 950 in simulations 920, 930, respectively. The current conduction path 940 in FIG. 9C shows current flowing through a single primary channel in current conducting region 14, while the current conduction path 950 shows current flowing from a primary channel in a first primary current conducting region 95 across a buffer layer 94 and to a parallel channel in a parallel current conducting region 93.

**[0083]** Referring to FIG. 10, an integrated semiconductor device 1000 is shown. Integrated device 1000 includes two neighboring semiconductor devices integrated on a single substrate 102: a first device controlled by contacts 105, 107 and gate 106; and a second device controlled by contacts 108, 110, and gate 109. The first and second semiconductor devices may be, for example, GaN semiconductor devices similar to semiconductor device 400 described above in connection with FIG. 4A. For example, in device 1000, substrate 102 may be composed of one or more Si, SiC, GaAs, and/or sapphire-based materials. Buffer layers 103 may be composed of AlN material having a thickness in the range of 0.1 to 0.5  $\mu\text{m}$ , one or more layers of AlGaN having a thickness in a range of 0.1 to 2  $\mu\text{m}$ , and GaN having a thickness in the range of 0.01 to 5  $\mu\text{m}$ . Device layer 104 may be composed of AlGaN having a thickness in the range of 0.01 to 0.03  $\mu\text{m}$ , and having an Al concentration within a range of approximately 15-30%. Contacts 105, 107, 108, 110 may be composed of a mixture of Ti and Al. Gate structures 106, 109 may be composed of p-type GaN and TiN or Ni and Au. It should be understood that the respective components for each semiconductor device within integrated device 1000 need not have identical, or even similar, characteristics, although semiconductor devices having similar characteristics may provide for ease in fabrication and other benefits.

**[0084]** Integrated device 1000 includes respective well regions 101 beneath each semiconductor device, and respective connection vias 100 leading from contacts 110, 107 of each semiconductor device to the respective well regions 101. As discussed above, substrate 102 can be

an n-type substrate, and implanted well 101 can be a p-type well, providing a device that operates at a negative potential in relation to the substrate 102. In another embodiment, substrate 102 can be a p-type substrate, and well region 101 can be an n-type well, providing a device that operates at a positive potential in relation to the substrate 102. Via 100 can be composed of Al material having a thickness in the range of 1 to 5  $\mu\text{m}$  and a thin layer of TiN having a thickness in the range of 0.01 to 0.1  $\mu\text{m}$ , as well as SiO<sub>2</sub> to completely fill the via 100.

**[0085]** In integrated device 1000, via 100 provides a very low inductance and low resistance path from the back side of the semiconductor device to a front side connection of the device (e.g., as shown, contacts 107, 110). These properties can be beneficial for high frequency operation. The presence of wells 101 below the device and buffer layers 104, 103 at the back side of the device 1000 provides these properties, while also isolating the back surface potential from the substrate potential. Each respective semiconductor device in integrated device 1000 thus has an independently controlled back surface potential which is isolated from the substrate potential, as well as from the potential at respective gate, source, and drain contacts 105-110, providing completely independent semiconductor devices.

**[0086]** While integrated device 1000 provides significant benefits, one potential problem with conductive wells 101 is that neighboring wells may create an n-p-n or p-n-p junction that could cause an undesirable short circuit condition, known as latch up, between the wells 101. Referring to FIG. 11, another integrated device 1100 includes elements similar to those discussed above with regard to device 1000 (FIG. 10), and also includes a suppression region 111 between respective wells 101 of the neighboring semiconductor devices in integrated device 1100. Suppression region 111 may be configured as a minority carrier recombination region, and may be formed using Pt or other appropriate recombination center materials. Suppression region 111 suppresses latch-up condition between neighboring respective wells 101.

**[0087]** Referring to FIG. 12, integrated semiconductor device 1200 having a silicon on insulator (“SOI”) configuration is shown. Device 1200 includes buffer layers 123 and device layer 124. These elements may have similar parameters and be formed through similar fabrication

processes as those described for device 800 (FIG. 8), described above. Device 1200 also includes a substrate 122, an SOI layer 121, and a buried oxide layer 130 between buffer layers 123 and substrate 122, which may have similar parameters and be formed through similar fabrication processes as those described for device 800 (FIG. 8), described above. Device 1200 includes connection vias 120 which connect electrical contacts (e.g., as shown, source contacts 129, 127) to the SOI layer 121. Buried oxide layer 130 electrically isolates substrate 122 from the SOI layer, making the substrate voltage independent of the SOI layer voltage.

**[0088]** Device 1200 includes source and drain contacts 125, 127, 129, and gate structures 126, 128. In this embodiment, the two neighboring semiconductor devices in integrated devices 1200 share a common contact 127, which serves as a drain to source contact 129 and a source to drain contact 125, forming a half-bridge circuit device.

**[0089]** Isolation implants 131 are used to isolate regions of SOI layer 121 corresponding to respective transistor devices in integrated device 1200. Isolation implants 131 are formed with oppositely-doped material to that used to form SOI layer 121, thus preventing conduction across SOI regions of neighboring integrated devices. As discussed above with regard to device 800, in other embodiments, a minority carrier lifetime reducing dopant, such as Pt, or any other suitable dopant known in the art, may be added to isolation implants 131.

**[0090]** Referring to FIG. 13, an integrated semiconductor device 1300 in a parallel channel configuration is shown. Device 1300 includes multiple semiconductor devices, such as semiconductor device 900 (FIG. 9). Integrated device 1300 includes a first current conducting region 135 providing respective primary channels for each respective semiconductor device in integrated device 1300, and a barrier layer 136 above each primary channel 135 and below contacts 137, 138, 141, 142. These elements may include similar characteristics and can be formed through similar processes as the elements in device 900 (FIG. 9) described above.

**[0091]** Integrated device 1300 also includes a conductive well 133 forming respective parallel conducting channels for each device between substrate isolation layers 132 and buffer layers 134. Parallel current conducting regions 133 may be formed of an n-type GaN material with

Si doping or with an AlGaN material on top of a GaN material, or through any other appropriate semiconductor material, as discussed above with regard to device 900 (FIG. 9). Respective channel connections 140 in buffer layers 134 are formed between current conducting regions 135 and parallel current conducting regions 133. Channel connections 140 may be formed by selectively implanting Si atoms into buffer layers 134, preferably with a density in a range of about 1e17 to 1e19 atoms/cm<sup>3</sup>, and more preferably at a density of approximately 1e18 atoms/cm<sup>3</sup>, and annealed at 1150° C for two hours. Preferably, current conducting regions 135, parallel current conducting regions 133, and channel connections 140 are all n-type material. Respective current conducting regions 135 and parallel current conducting regions 133 are electrically connected through channel connections 140.

**[0092]** Integrated device 1300 also includes one or more substrate isolation regions 132 formed on substrate 131. Substrate isolation layers 132 may be formed of a material such as AlN, or a high Al-content AlGaN material, or other suitable material. As discussed above with regard to device 900 (FIG. 9), the preferred thickness of substrate isolation layers 132 may be varied depending upon the voltage rating desired for integrated device 1300.

**[0093]** Device 1300 may optionally also include isolation regions 143, which may be composed of similar materials to and formed in a similar manner as isolation regions 70 of device 700 (FIG. 7), or through other suitable materials and processes. For example, isolation regions 143 may be formed by etching the indicated portions of device 1300 to a depth at least below parallel current conducting region 133, and preferably into substrate isolation layers 132, and filling the etched areas with oxide. Channel connections 140 provide a very low inductance and low resistance path from the back side of the semiconductor device to a front side connection of the device (e.g., as shown, contacts 142, 138), while the presence of isolation regions 143 between neighboring devices and substrate isolation layers 132 at the back side of the device allows each respective semiconductor device to have an independently controlled back surface potential which is isolated from the substrate potential and from the potential of channels of neighboring devices.

**[0094]** Referring to FIG. 14, another integrated semiconductor device 1400 having a parallel channel configuration is shown, including multiple semiconductor devices similar to semiconductor device 1300 described above in connection with FIG. 13. Integrated device 1400 also includes a back barrier layer 144 between the parallel current conducting layer 133 and buffer layers 134. Back barrier layer may be composed of a high Al-content AlGaN or AlN material. Providing back barrier layer 144 between the parallel current conducting layer 133 and buffer layers 134 increases the breakdown voltage of integrated device 1400 by preventing electrons from migrating from parallel current conducting region 133 to contacts 137, 138, 141, 142.

**[0095]** Integrated semiconductor device 1400 also includes metal channel connections 145, which are composed of a metal material and extend from parallel current conducting region 133 to contacts 138, 142. Metal channel connections 145 may present advantages over other types of channel connections (such as Si channel connections) for devices using high Al-content materials for the parallel current conducting layer 133, because implanting Si into high Al-content AlGaN material may result in non-conductive material, and thus in a faulty connection. Metal channel connections 145 may be formed by etching the selected areas of metal channel connections 145 from the surface of integrated device 1400 to parallel current conducting region 133, and filling the etched area with metal. The metal used to fill metal channel connections 145 may be the same metal used for contacts 137, 138, 141, 142, such as Ti, Al, TiN, W or any other suitable metal, or combinations thereof.

**[0096]** Referring to FIG. 15, a top-down view of an integrated semiconductor device 1500 is shown. Integrated semiconductor device 1500 includes four individual semiconductor devices 1551, 1552, 1553, 1554 integrated on a single substrate 1500. Each semiconductor device in integrated semiconductor device 1500 includes a respective implant region 1502, 1505, 1508, 1511, in each of which a respective implanted well 51 (FIG. 4) is formed beneath a surface, and active device regions 1503, 1506, 1509, 1512 where device layer 54 (FIG. 4) and electrical connections (e.g., contacts 55, 57, and gate 56 of FIG. 4) are formed for each device. Within each implant region 1502, 1505, 1508, 1511, but outside of the respective active device regions 1503, 1506, 1509, 1512, are vias 1501, 1504, 1507, 1510, which can be used to provide a very low

inductance and low resistance path from a respective implanted well to a front side connection of the respective semiconductor device (e.g., a source and/or drain contact). Semiconductor devices 1551, 1552, 1553, 1554 may include semiconductor devices as described above in reference to any of FIGS. 1 to 14, and preferably include at least one semiconductor device as described in reference to any of FIGS. 4 to 14. Features described above with regard to FIGS. 4 to 14 may be used to provide each respective semiconductor device with an independently controlled back surface potential which is isolated from the substrate potential and/or conducting regions which are isolated from those of neighboring devices.

**[0097]** Referring to FIG. 16, a top-down view of another integrated semiconductor device 1600 is shown. Integrated semiconductor device 1600 includes two individual semiconductor devices 1651, 1652 integrated on a single substrate. Each semiconductor device includes an active region 1610, 1620 with multiple (in this case, four) vias 1601-1608 at connections for the semiconductor devices 1651, 1652. Semiconductor devices 1651, 1652 may include semiconductor devices as described above in reference to any of FIGS. 1 to 14, and preferably include at least one semiconductor device as described in reference to any of FIGS. 4 to 14. Features described above with regard to FIGS. 4 to 14 may be used to provide each respective semiconductor device with an independently controlled back surface potential which is isolated from the substrate potential, and/or conducting regions which are isolated from those of neighboring devices, or from other conducting regions within the same device.

**[0098]** The semiconductor devices described above can be used for numerous purposes. For example, the structures and processes described above can be used to form active devices in a substrate that operate as part of an integrated circuit. General categories of such devices may include diodes, bipolar junction transistors (“BJT”), and field effect transistors (“FET”).

**[0099]** Referring to FIG. 17, schematic diagrams of examples of integrated semiconductor devices are shown. The schematic diagrams include (a) a single transistor; (b) a pair of transistors connected in series to form a half bridge, (c) a group of four transistors connected to form a full bridge circuit, and (d) a group of six transistors connected to form a 3 phase bridge.

Groups of transistors formed in parallel (i.e., as shown in configuration (c)), can be used to form high-speed switching circuits.

**[00100]** Referring to FIG. 18, an integrated GaN semiconductor device 1800 is shown. Device 1800 includes a substrate 202, buffer layers 203, and device layer 204, which may be formed using materials and processes described above. Device 1800 also includes a drain contact 205, source contact 206, and gate structure 207 formed on device layer 204, which may be formed using materials and processes described above. Device 1800 also includes a via 200 connecting source contact 206 to a well 201 formed in the substrate 202 at a backside of device 1800.

**[00101]** Device 1800 also includes a gate protection diode formed between a second conductive well 211 in substrate 202, which can also be referred to as a gate well. The gate protection diode is connected to gate structure 207 through via 212, gate pad 208, and metal routing 209 (or other structures). The gate protection diode protects gate structure 207 from high voltages which may exceed the gate oxide breakdown voltage. Gate pad 208 is formed on a region of device 1800 which is isolated from the device layer 204 by an isolation region 210. Isolation region 210 may be formed by etching away device layer 204 in the desired region, and/or by implanting the region in device layer 204 with materials having high energy atoms, such as Ni, Fe, V, or any other suitable material, which will damage the device layer 204 to prevent conduction. Metal routing 209 connecting the gate structure 207 and the gate pad 208 may be composed of, for example, Al doped with Si and/or Cu. Alternatively, metal routing 209 may be composed of the same metal material used for making drain and source contacts 205, 206, described above, or a poly-Si material, which can be particularly beneficial for use when high temperatures are to be applied subsequently in the fabrication process.

**[00102]** Via 212 extends from gate pad 208 to gate well 211. Gate well 211 is a conductive well region, and is preferably an oppositely-doped material to substrate 202. For example gate well 211 may be composed of n-type material, and substrate 202 may be a p-type substrate, thereby forming a p-n Zener diode between gate well 211 and substrate 202 as the gate-protection diode. In one preferred embodiment, gate well 211 is composed of a heavily-doped n-

type material formed over a heavily doped p-type material that is located over the p-type substrate 202. Such a diode can be used to block current flowing between gate pad 208 and substrate 202 until a critical voltage is reached, after which current will flow between gate pad 208 and substrate 202. Negative voltage on gate structure 207 will cause current at a small bias from the forward-biased p-n diode. Unlike conventional gate protection diodes, which may connect the gate structure 207 to a source contact 206, the configuration shown in device 1800 allows excess current to flow to substrate 202 through vias 200, 212, rather than to the source contact 206.

**[00103]** While device 1800, described with reference to FIG. 18, provides protection to gate structure 207 and other elements of device 1800, problems may arise because the voltage at which the current flows across the gate protection diode is based on the voltage between the gate structure 207 and substrate 202. Thus, the biasing of substrate 202 loses some amount of independence.

**[00104]** Referring to FIG. 19, another integrated GaN semiconductor device 1900 is shown, where a gate protection diode is formed by a gate well 211 contained within well 221. The gate protect voltage of the gate protection diode is set by the gate-to-source bias of device 1900, rather than the gate-to-substrate bias (as in device 1800 of FIG. 18), thus allowing an independent substrate bias. Although not shown in FIG. 19, it should be understood that the isolation techniques and structures described above with regard to FIGS. 1 to 17 may be used to further isolate well 221 from substrate 202 and buffer layers 203.

**[00105]** Referring to FIG. 20, another integrated GaN semiconductor active device 2000 is shown. Device 2000 includes multiple forward-biased diodes in series within an SOI layer 224 to form a gate protection circuit. Device 2000 is formed on an SOI substrate, including a substrate 202, a buried oxide layer 223, and an SOI layer 224.

**[00106]** SOI layer 224 may be an n-type material. Diodes are formed within SOI layer 224 from (e.g., p-type) implanted conductive regions 225 and heavily-doped (e.g., n-type) tunnel regions 226, such that the junction between conductive regions 225 and tunnel regions 226 forms a tunnel-type configuration. A tunnel-type contact is one where the doping is so high in the p-n

junction (for example, approximately  $1e20$  atoms/cm $^3$ ) that no voltage can be blocked. Such a contact may occur when electrons in the n-region can transfer (i.e., tunnel) directly into the valence band of the p-region. Thus, although a p-n junction exists, it appears as an ohmic, or conductive, connection. In one preferred embodiment, each diode may form a voltage drop of approximately one volt, such that five diodes in series would create a voltage drop of approximately five volts. Although an SOI substrate may increase the cost of manufacturing device 2000, the above-described configuration requires fewer implant steps than alternative configurations and provides a natural isolation for the active elements of device 2000 from substrate 202.

**[00107]** Referring to FIG. 21, another integrated GaN semiconductor active device 2100 is shown. Device 2100 includes a substrate 202, which may be a p-type substrate, and a conductive well 201 and gate well 211, which may be n-type implanted conductive wells.

**[00108]** Device 2100 includes multiple GaN layers used as gate dielectrics to form a recessed FET device with a back channel region 228 formed between gate well 211 and well 201. Device 2100 can be configured to operate similar to a conventional MOSFET device. In device 2100, well region 201 and gate well region 211 act as a drain and a source, respectively, for the recessed FET, while gate pad 208 acts as a gate for the recessed FET. Via 222 shorts gate pad 208 to gate well 211, and via 227 shorts well 201 to substrate 202. In this configuration, well 201 acts as a source for the buried FET. A potential applied at gate pad 208 causes accumulation of electrons in back channel region 228, turning the recessed FET to an “on” state, allowing current to flow between connection 205 or substrate 202 and gate pad 208, and limiting a voltage present at gate pad 208.

**[00109]** Referring to FIG. 22A, another integrated GaN semiconductor active device 2200 is shown. Device 2200 is a GaN FET device with two vias 230, 231 extending into conductive well 221. A first via 230 connected to a source contact 206 extends into an ohmic region 232 that is formed within conductive well 221. Ohmic region 232 can be formed using a high dose implant of a material having the same carrier type (i.e., n-type or p-type material) used to form conductive well 221. For example, conductive well 221 may be formed of a p-type material

having a concentration of approximately  $1e16$  atoms/cm $^3$ ; and ohmic region 232 may be formed with a concentration of  $5e18$  atoms/cm $^3$ . A second via 231 connected to a drain contact 205 extends into and creates a Schottky contact with conductive well 221.

**[00110]** During a reverse bias position of device 2200 (e.g., when drain contact 205 is positive compared to source contact 206, and gate structure 207 has a zero bias), the Schottky diode formed by conductive well 221 and region 231 blocks current flow from via 231 into well region 221. When the bias of drain contact 205 becomes negative compared to that of source contact 206, current flows through ohmic region 232 into and across conductive well 221 and up to drain contact 205, while the gate bias remains at zero (and the FET remains in an “off” state).

**[00111]** Device 2200 provides for current flow between source contact 206 and drain contact 205 when gate 207 is “off,” with a lower power loss. For example, a conventional threshold voltage for a GaN FET may be approximately 2.1 volts. The voltage drop across the diode formed by region 231 and well 221, on the other hand, is only approximately 0.7 volts, while source contact 206 is electrically connected to conductive well 221 by via 230. Thus, for a constant current, current flow across device 2200 with the gate in an “off” state results in a voltage drop that is approximately 33% of that which is experienced across a conventional GaN FET device.

**[00112]** Referring to FIG. 22B, another integrated GaN semiconductor active device 2200B is shown. Device 2200B includes similar features as those discussed in connection with device 2200, but also includes a second ohmic region 232B formed within well 221 under via 231. Second ohmic region 232B can be formed using a high dose implant of a material having the opposite carrier type (i.e., n-type or p-type material) used to form conductive well 221 and ohmic region 232, thereby forming a PIN junction.

**[00113]** Referring to FIG. 23, another integrated GaN/Si semiconductor device 2300 is shown. Device 2300 includes a recessed Si FET using the buffer layers 203 as a gate insulator. Device 2300 includes a substrate 202, buffer layers 203, device layer 204, contacts 205, 206, gate structure 207, and conductive well 201, which may be formed of similar materials and processes as the elements described above with regard to device 2100 (FIG. 21). Device 2300 also includes

isolation region 210, a first via 222, a second via 227, a Si FET well 241, and a back channel region 228 between conductive well 201 and Si FET well 241, which also may be formed of similar materials and processes as the elements described above with regard to device 2100 (FIG. 21). Device 2300 also includes an independent drain and gate structure for the Si FET. Si gate structure 243 and Si FET drain 242 may be formed with similar material and processes as the gate pad 208 described above with regard to device 1800 (FIG. 18), or through any other known suitable materials and processes.

**[00114]** Device 2300 further includes isolation structure 240, which represents one or more of the isolation configurations described above with regard to FIGS. 4 to 22, such as suppression region 111 (FIG. 11), isolation implant 131 (FIG. 12), or isolation region 143 (FIG. 13). It should be understood, however, that any other isolation configurations described above, as well as conventional isolation techniques known in the art, may be represented by isolation structure 240.

**[00115]** Referring to FIG. 24, another integrated GaN/Si semiconductor device 2400 is shown. Device 2400 includes a substrate 202, buffer layers 203, device layer 204, contacts 205, 206, GaN gate structure 207, and conductive well 201, which may be formed of materials and processes described above. Device 2400 also includes isolation region 210, via 222, via 227, FET well 241, and back channel region 228 between conductive well 251 and FET well 241, which also may be formed of materials and processes described above.

**[00116]** Device 2400 includes an independent FET source 244 and drain 242 contacts, as well as an independent MOS gate 243 which is recessed into device layer 204 and buffer layers 203. Gate 243 may be achieved by etching through device layer 204 and partially through buffer layers 203, until an AlN nucleation layer within buffer layers 203 is reached. Selective etching of GaN can be achieved by addition of O<sub>2</sub> during the etching step, or through any other suitable process known in the art.

**[00117]** Device 2400 also includes a low-doped depletion region 250 between FET well 241 and a back channel region 228. Preferably, depletion region 250 has a lower dopant level (e.g., in a range of about 1e14 to 1e17/cm<sup>2</sup>) than FET well 241 and FET source well 251 (e.g., well 241

and 251 may be doped at  $1e17$  to  $1e19/cm^2$ ). This increases the breakdown voltage of the integrated Si FET. Device 2400 provides the capability to integrate p-channel transistors in Si with n-channel transistors in GaN to allow CMOS (complementary metal oxide semiconductor)-type circuits. For example, well 202 may be formed by implantation of antimony at a dose of  $4-8e16/cm^3$  to form a n-type well. Region 250 may be implanted with  $1e17/cm^3$  boron to form an p-type drift well, resulting in a drift well having a net p-type doping of  $2e16/cm^3$ . Regions 241 and 251 may be implanted with  $1e18$  boron to form heavily doped ohmic contact regions. The p-n junction formed between drift well 250 and well 202 will block voltage when the Si FET drain voltage applied to contact 242 is negative and back channel region 228 is in the “off” state. A negative bias at gate 243 will result in accumulation of holes in region 228, turning the device “on”. Current can then flow from connection 244 through p-type well 251, through back channel region 228, into drift well 250, and out through contact region 241 and connection 242.

**[00118]** Device 2400 includes isolation structures 240 separating conductive well 201 and wells 241, 251. Isolation structures 240 in FIG. 24 each represent one or more of the isolation configurations described above with regard to FIGS. 4 to 22, such as suppression region 111 (FIG. 11), isolation implant 131 (FIG. 12), or isolation region 143 (FIG. 13). It should be understood, however, that any other isolation configurations described above, as well as conventional isolation techniques known in the art, may be represented by isolation structure 240.

**[00119]** Referring to FIG. 25A, another integrated GaN/Si semiconductor device 2500 is shown. Device 2500 includes similar elements as described above with regard to device 2400 (FIG. 24), and description of those elements will not be repeated here. Device 2500 also includes a high-dielectric constant (“high-k”) dielectric material 260 around Si gate 243. High-k dielectric material 260 refers to the material having a higher dielectric constant than the silicon dioxide or similar materials that are typically used in forming gate structures. Adding high-k dielectric material 260 increases gate capacitance while reducing the potential for current leakage. High-k dielectric material 260 may be formed from known suitable materials, and is preferably formed from materials in the family of  $AlHfSiO_x$  materials, such as Aluminum Hafnium Silicate, Aluminum Hafnium Dioxide. The most suitable compositions of Al, Hafnium (Hf), and Si in the high-k dielectric

material 260 may vary. High-k dielectric material 260 may be deposited at a low-temperature method, for example, using methods such as atomic layer deposition (“ALD”), Plasma-enhanced chemical vapor deposition (“PECVD”), or other suitable deposit methods, prior to formation of gate structure 243. In another embodiment of device 2500, an Si oxidation technique, or a low-temperature oxidation technique combined with deposition of a dielectric, may be used to provide similar benefits at Si gate structure 243.

**[00120]** In another embodiment shown in FIG. 25B, device 2500B includes a gate structure 243B with high k insulator 260B etched completely through the buffer layers 203. This results in a gate structure that is formed without buffer layer material between the high-k gate oxide and gate structure 243. The advantages include lower gate voltage required to turn the device on, and the recess step may be combined with the via 222 etch step, reducing cost and complexity of manufacture.

**[00121]** Referring to FIG. 26, another GaN transistor device 2600 is shown. Device 2600 includes a substrate 302, which may be, for example, Si, SiC, or other semiconductor material, and a conductive well 301 formed in the substrate 302, which is connected to a source contact 308 by a first via 300. Conductive well 301 covers the area beneath the active portion of device layer 304. Device 2600 also includes a second via 307 making an ohmic contact to the region surrounding conductive well 301, forming a neighboring ohmic well 305. Conductive well 301 may be formed of a highly-doped p-type Si material, and ohmic well 305 may be formed of a highly doped n-type Si material, such that the non-implanted portion of substrate 302 between conductive well 301 and ohmic well 305 is a lower-doped material.

**[00122]** Device 2600 advantageously uses the semiconductor characteristics of substrate 302 to protect the device 2600 from high voltage spikes to the drain contact 306. Conductive well 301, ohmic well 305, and the portion of substrate 302 between conductive well 301 and ohmic well 305 form a pin diode. During high voltage spikes at drain contact 306, the pin diode formed between conductive well 301 and ohmic well 305 would experience avalanche conditions, resulting in charge being transferred across substrate 302 to conductive well 301. Conductive well 301,

ohmic well 305, and substrate 302 can be doped such that the avalanche conditions across the pin diode would be triggered before the energy of the high voltage spike reaches a critical voltage that could result in damage or destruction of the device 2600. It should be understood that isolation structures described above with regard to FIGS. 1 to 25 may also be incorporated into device 2600, in order to isolate device 2600 and conductive and ohmic wells 301, 305 from neighboring structures and devices.

**[00123]** Referring to FIG. 27, another integrated GaN semiconductor active device 2700 is shown. Device 2700 includes a bipolar transistor device integrated within a GaN device, using via connections 400, 473, 474. The GaN portion of integrated device 2700 is formed by GaN drain 466, GaN source 468, and GaN gate 469, which may be formed and operated in accordance with embodiments described above. In device 2700, well 401 is located in the SOI layer 224 in the area under the active region of device layer 204 of the GaN device, and isolates the backside potential of the GaN device.

**[00124]** As shown in FIG. 27, device 2700 includes a SOI insulating structure, as described above with regard to device 2000 (FIG. 20). In one embodiment, well 401 is a p-type well, and SOI layer 224 is formed of an n-type material. It should be understood, however, that any isolation structure described above with regard to any of FIGS. 1-26 may be used instead or in addition. Also, in an alternative embodiment, device 2700 may not include well 401, or may include other types of backside isolation.

**[00125]** The bipolar portion of integrated device 2700 is formed by bipolar drain contact 472 and bipolar base contact 471. Although not shown in FIG. 27, bipolar base contact 471 and bipolar drain contact 472 can be isolated from the active GaN areas of device layer 204 by one or more isolation configurations described above with regard to FIGS. 4-26, such as suppression region 111 (FIG. 11), isolation implant 131 (FIG. 12), or isolation region 143 (FIG. 13).

**[00126]** The bipolar portion of integrated device 2700 is “buried” using vias 473 and 474. The bipolar drain 472 of device 2700 is created using an implanted well 470, with doping in the range of  $1e16$  to  $1e19/cm^2$ , into which via 474 extends from bipolar drain contact 472. Well 470

may be a p-type material in n-type SOI layer 224. In an alternative embodiment, another well (not shown) may be implanted under bipolar base connection 471 to further improve contact, or well 401 may be composed of high and low doped regions to increase breakdown voltage. An example is well regions 401 and 470 implanted with boron of density  $1e18/cm^3$  with SOI layer As doped at  $1e17/cm^3$ . Connection via 474 makes contact to the SOI layer, while vias 400 and 474 connect to the collector and emitter regions 401, and 470 respectively. When negative bias is applied at connection 471, the SOI layer becomes negative biased relative to emitter and collector regions 470 and 401. Holes can then conduct through the SOI layer in the region between well 401 and 470.

**[00127]** The above description and drawings are only to be considered illustrative of specific embodiments, which achieve the features and advantages described herein. Modifications and substitutions to specific process conditions can be made. Accordingly, the embodiments of the invention are not considered as being limited by the foregoing description and drawings, but only by the elements of the claims.

**CLAIMS**

1. A transistor device comprising:

a substrate;

at least one interior layer comprising a compound semiconductor material;

a device layer including a current conducting region;

at least one contact formed on the device layer; and

a conductive well electrically connected to the contact through the interior layer, wherein the conductive well is electrically isolated in at least one bias polarity from surrounding material.

2. The transistor device of claim 1, wherein the conductive well has a doping of opposite polarity to the surrounding material.

3. The transistor device of claim 1, wherein the conductive well has a doping and the surrounding material is substantially undoped.

4. The transistor device of claim 1, wherein the compound semiconductor material of the at least one interior layer comprises:

aluminum nitride;

aluminum gallium nitride; and

gallium nitride.

5. The transistor device of claim 1, wherein said substrate comprises at least one of:

silicon;

silicon carbide;

sapphire;

aluminum nitride;

gallium-nitride; and

gallium-arsenide.

6. The transistor device of claim 1, further comprising an insulating layer formed on the substrate and a doped conductive material formed on the insulating layer.

7. The transistor device of claim 1, wherein the surrounding material comprises a p-type substrate, and the conductive well comprises an n-type material.

8. The transistor device of claim 1, wherein the surrounding material comprises an n-type substrate, and the conductive well comprises a p-type material.

9. The transistor device of claim 1, wherein said surrounding material is substantially non-conductive, and the conductive well comprises a conductive material.

10. The transistor device of claim 1, wherein the conductive well comprises conductive material implanted within the substrate.

11. The transistor device of claim 1, wherein the conductive well comprises a layer of conductive material formed above the substrate.

12. The transistor device of claim 1, further comprising a conductive via extending from a top surface of the device layer to the conductive well electrically connecting the contact to the conductive well.

13. The transistor device of claim 12, wherein the conductive via comprises tungsten or copper.

14. The transistor device of claim 12, wherein the conductive via comprises aluminum, silicon, or gold.

15. The transistor device of claim 12, further comprising a plurality of conductive wells.

16. The transistor device of claim 15, further comprising:

a source contact and a drain contact formed on the device layer; and

a gate structure formed between the source contact and the drain contact on the device layer,

wherein the plurality of conductive wells form a pin diode, and wherein respective conductive wells are electrically connected to the source and drain contacts.

17. The transistor device of claim 15, further comprising:

a source contact and a drain contact formed on the device layer; and

a gate structure formed between the source contact and the drain contact on the device layer,

wherein the plurality of conductive wells form a series of P-N diodes, and wherein respective conductive wells are electrically connected to one of the source and drain contacts and the gate structure.

18. The transistor device of claim 17, wherein alternating P-N diodes in the series of P-N diodes include a tunnel junction.

19. The transistor device of claim 15, wherein at least one of the plurality of conductive wells has a Schottky connection to a conductive via.

20. The transistor device of claim 15, wherein at least one of the plurality of conductive wells comprises an ohmic region at a connection to a conductive via.

21. The transistor device of claim 1, further comprising a plurality of conductive layers formed between the substrate and the conductive well, wherein the plurality of conductive layers have alternating doped polarities.

22. The transistor device of claim 1, further comprising:

a first current conducting region in the device layer; and

a second current conducting region in the conductive well.

23. The transistor device of claim 22, further comprising a channel connection extending through the interior layers and connecting the first and second current conducting regions.

24. The transistor device of claim 23, wherein the channel connection comprises at least one of tungsten, aluminum with titanium nitride, or silicon.

25. The transistor device of claim 1, wherein the transistor device is part of an integrated circuit comprising a plurality of transistor devices.

26. The transistor device of claim 25, wherein respective substrates below the transistor devices are electrically isolated in at least one polarity.

27. The transistor device of claim 25, wherein the integrated circuit comprises a plurality of respective current conducting regions for each transistor device, wherein the plurality of respective current conducting regions are isolated from one another by isolation structures.

28. The transistor device of claim 25, wherein the plurality of transistor devices includes a second transistor device comprising:

a contact formed on the device layer electrically connected to another respective current conducting region; and

a second conductive well electrically connected to the contact of the second transistor device through the interior layer.

29. The transistor device of claim 27, wherein the isolation structures comprise diodes formed within a current conducting layer to separate the respective current conducting regions.

30. The transistor device of claim 29, wherein the diodes comprise implanted conductive regions having a first doping polarity and tunnel regions having a second doping polarity.

31. The transistor device of claim 25, wherein at least two of the plurality of transistor devices share a common contact.

32. The transistor device of claim 1, further comprising a source contact, a drain contact, and a metal oxide semiconductor gate structure, and wherein the metal oxide semiconductor gate structure is positioned over a back channel region for accumulating electrons.

33. The transistor device of claim 1, further comprising:

a source contact, wherein the source contact is electrically connected to the conductive well through the interior layer;

a drain contact electrically connected to a second conductive well through the interior layer;

an etched opening in the device layer between the source and drain contacts;  
a gate structure formed at least partially within the etched opening; and  
a back channel depletion region for accumulating electrons formed between  
the conductive well and the second conductive well.

34. The transistor device of claim 33, further comprising a depletion  
region formed between one of the conductive well and the second conductive well  
and the back channel region, wherein the depletion region has a lower dopant level  
than the conductive well.

35. The transistor device of claim 34, further comprising a dielectric  
material lining the etched opening, wherein the dielectric material has a higher  
dielectric constant than the gate structure.

36. A method of forming a transistor device, said method comprising:  
providing a substrate;  
forming a conductive well, wherein the conductive well is electrically  
isolated in at least one bias polarity from surrounding material;  
forming at least one interior layer over the substrate and the conductive well;  
forming a device layer over the interior layer;  
forming a contact on a surface of the device layer;  
forming a conductive via extending through the device layer and the interior  
layer to the conductive well and electrically connecting the contact to the conductive  
well.

37. The method of claim 36, wherein forming the conductive well comprising implanting a dopant into the substrate.

38. The method of claim 37, wherein the dopant comprises boron.

39. The method of claim 36, wherein forming the conductive well further comprises:

performing a silicon oxidation on the substrate;

forming a photo-resist pattern definition over the substrate;

removing silicon oxide from within the patterned area;

implanting the dopant into the substrate;

stripping away the photo-resist pattern and remaining oxide; and

annealing the wafer at high temperatures.

40. The method of claim 36, wherein forming the conductive well and the substrate are part of a silicon-on-insulator wafer.

41. The method of claim 40, further comprising forming an isolation structure in the conductive well.

42. The method of claim 41, wherein forming the isolation structure comprises:

depositing an oxidation barrier material over the conductive well;

forming a photo-resist pattern definition over the barrier material;

removing the oxidation barrier material in exposed areas of the photo-resist pattern;

stripping away the photo-resist pattern; and  
oxidizing exposed portions of the conductive well down to a buried oxide layer of the silicon-on-insulator wafer by exposing the exposed portions to high temperature steam.

43. The method of claim 41, wherein forming the isolation structure comprises:

depositing an implant barrier material;  
forming a photo-resist pattern definition over the barrier material;  
removing the implant barrier material in exposed areas of the photo-resist pattern;  
stripping away the photo-resist pattern and implant barrier material; and  
annealing the conductive well at high temperatures.

44. The method of claim 36, further comprising:

forming an integrated device comprising a plurality of transistor devices on the substrate; and

forming a plurality of conductive wells corresponding to respective transistor devices, wherein each conductive well is electrically isolated in at least one bias polarity from surrounding material.

45. The method of claim 44, further comprising electrically isolating the respective transistor devices.

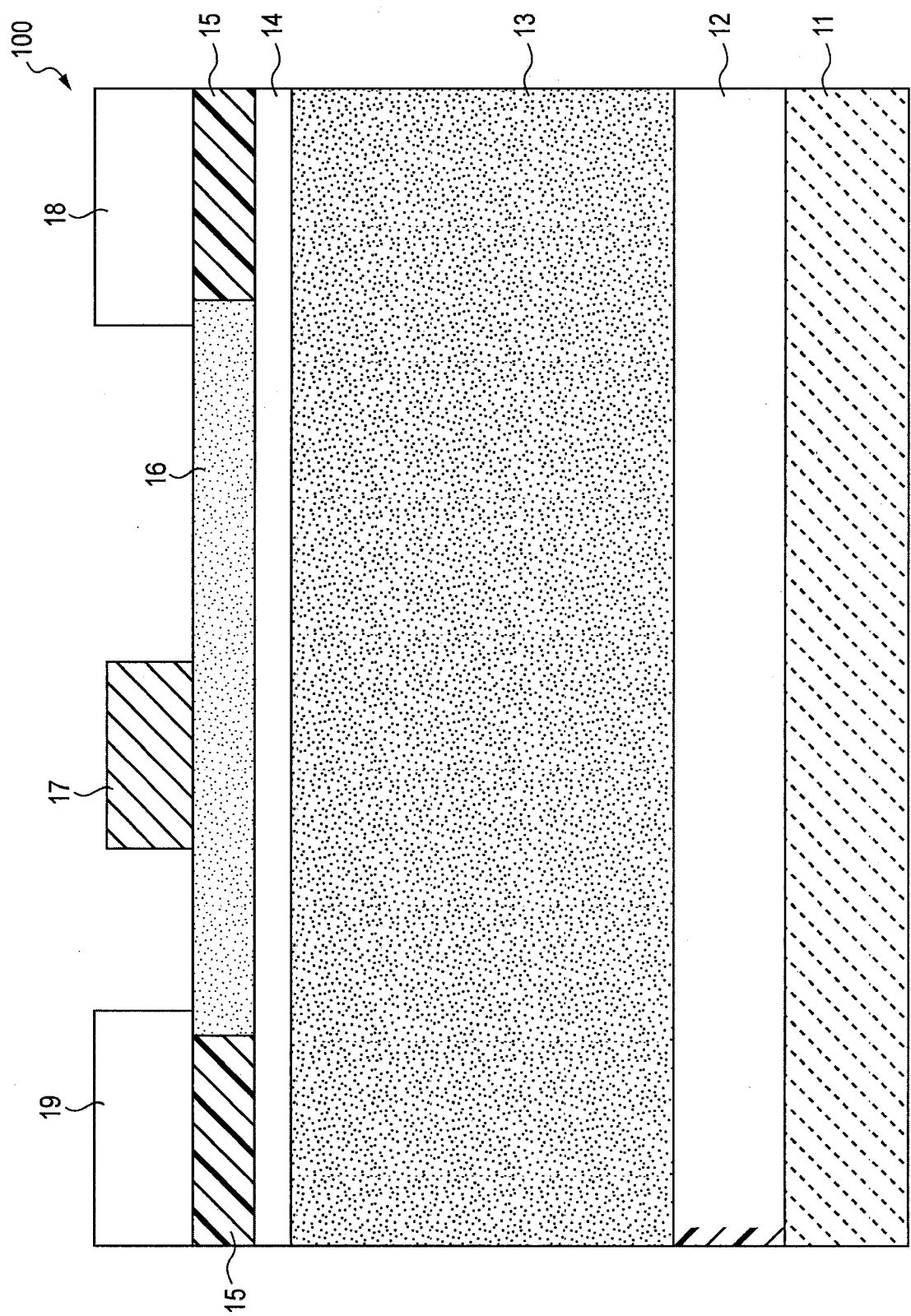
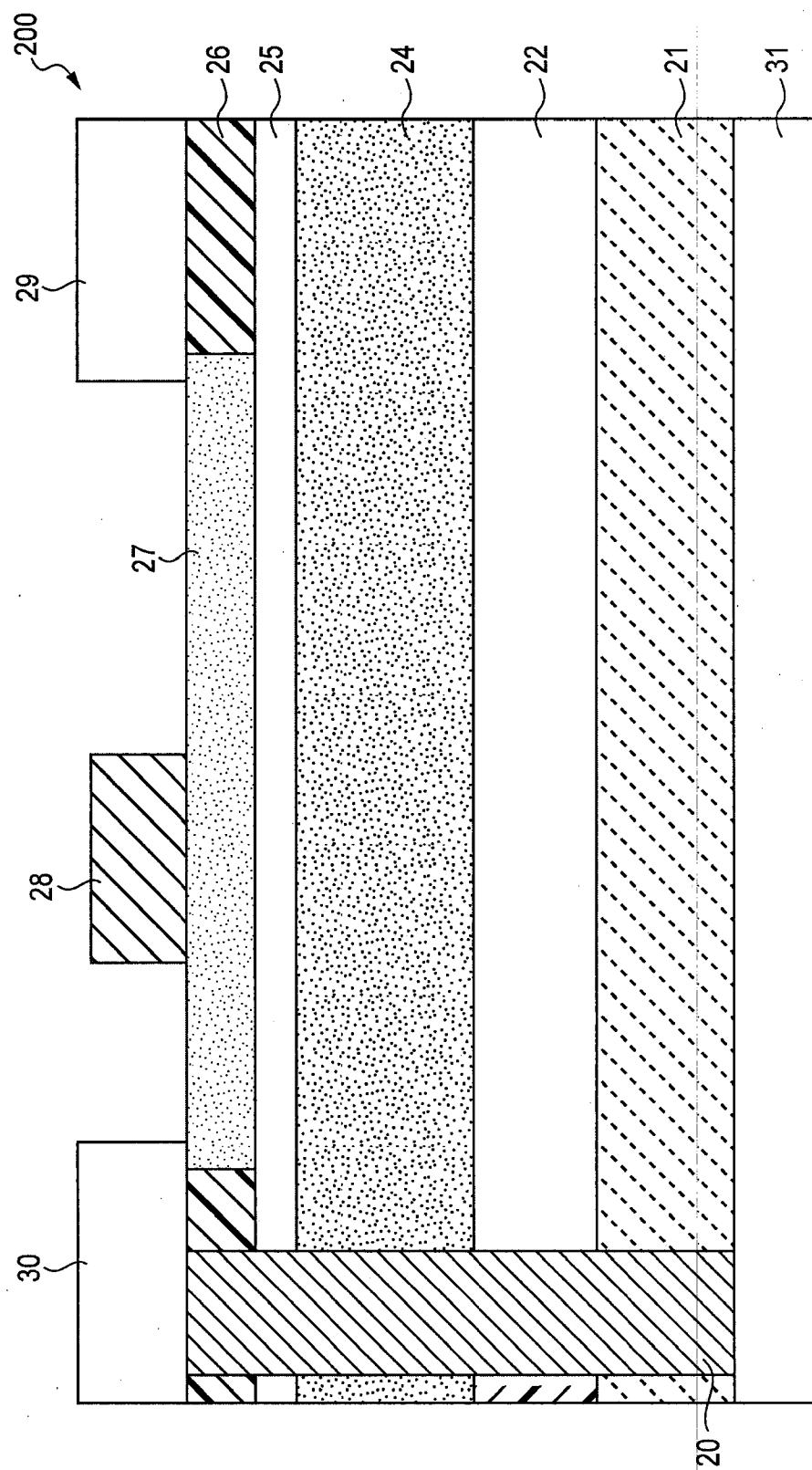
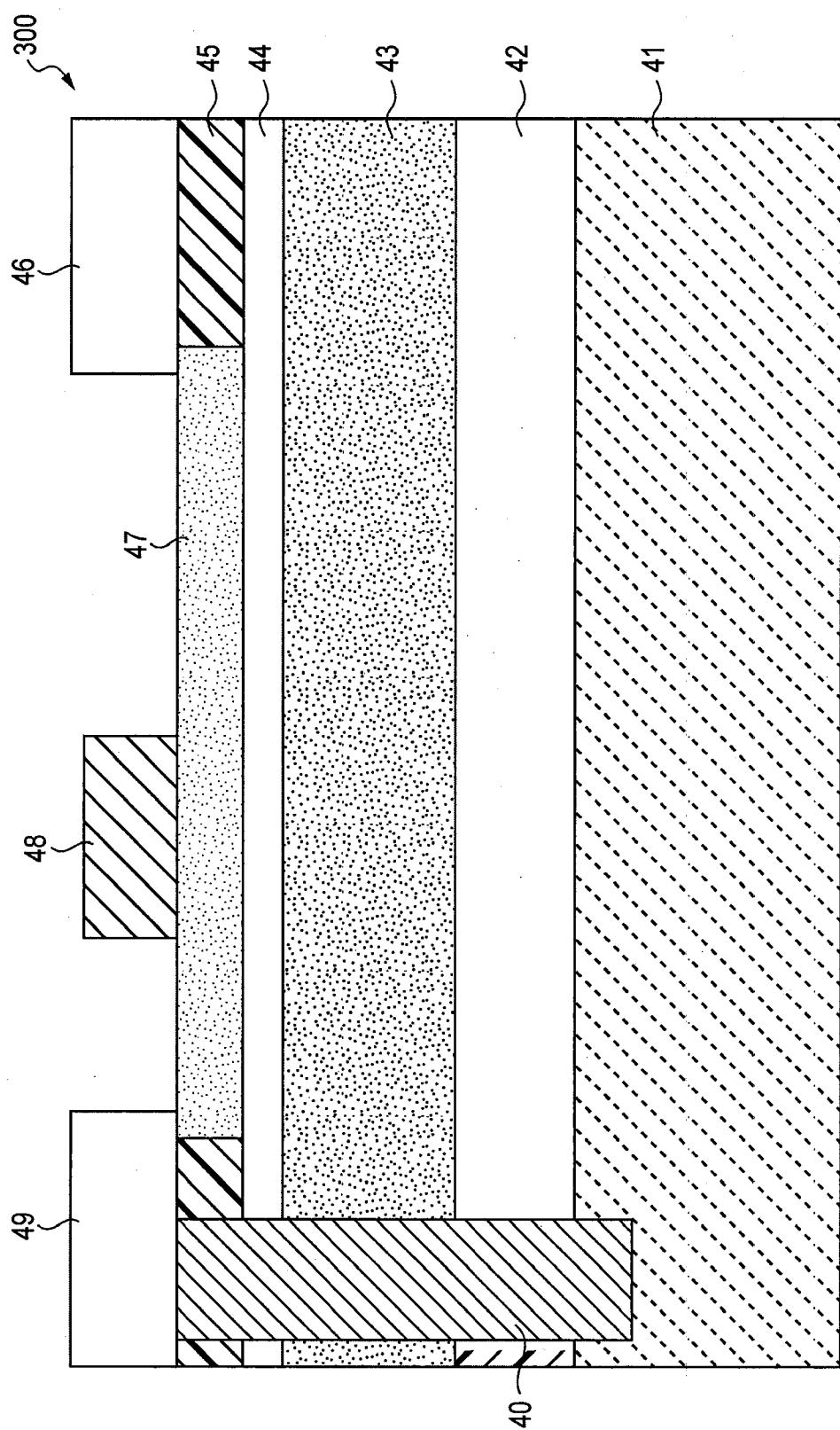


FIG. 1  
PRIOR ART



**FIG. 2**  
PRIOR ART



**FIG. 3**  
PRIOR ART

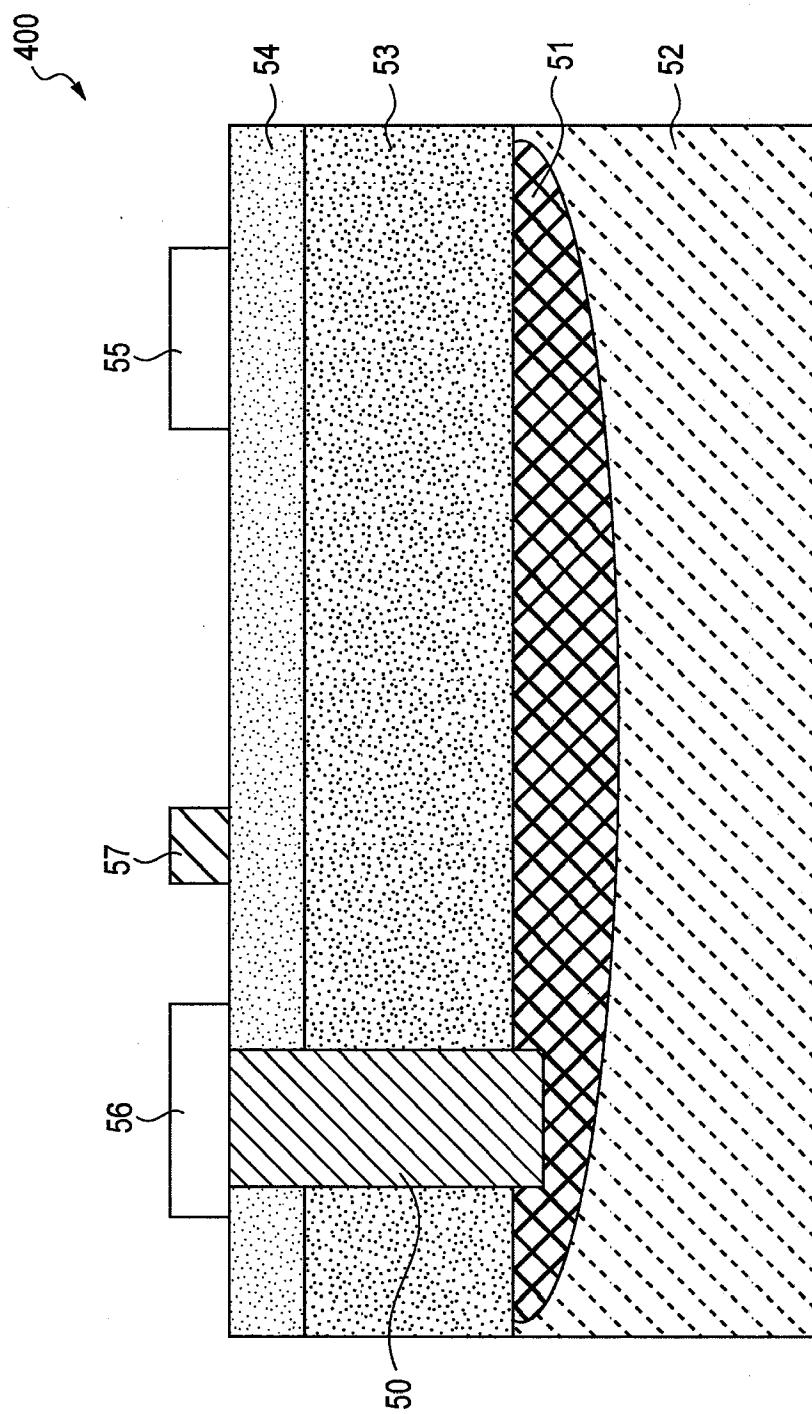


FIG. 4A

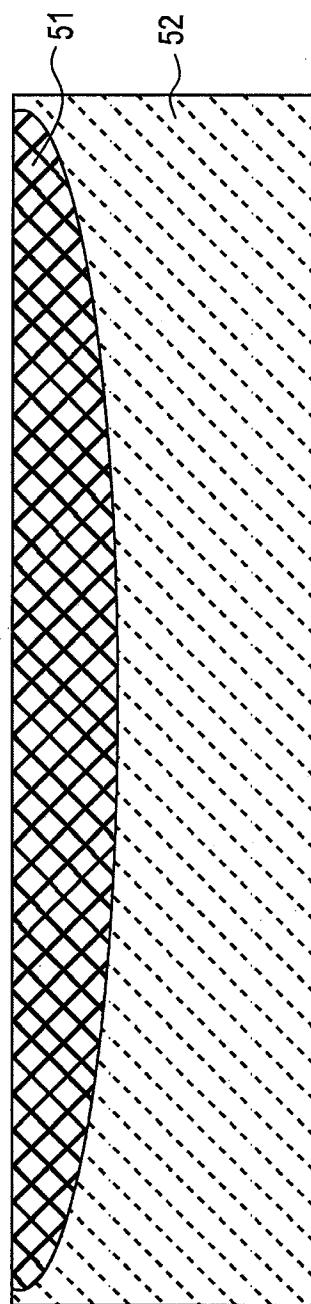


FIG. 4B

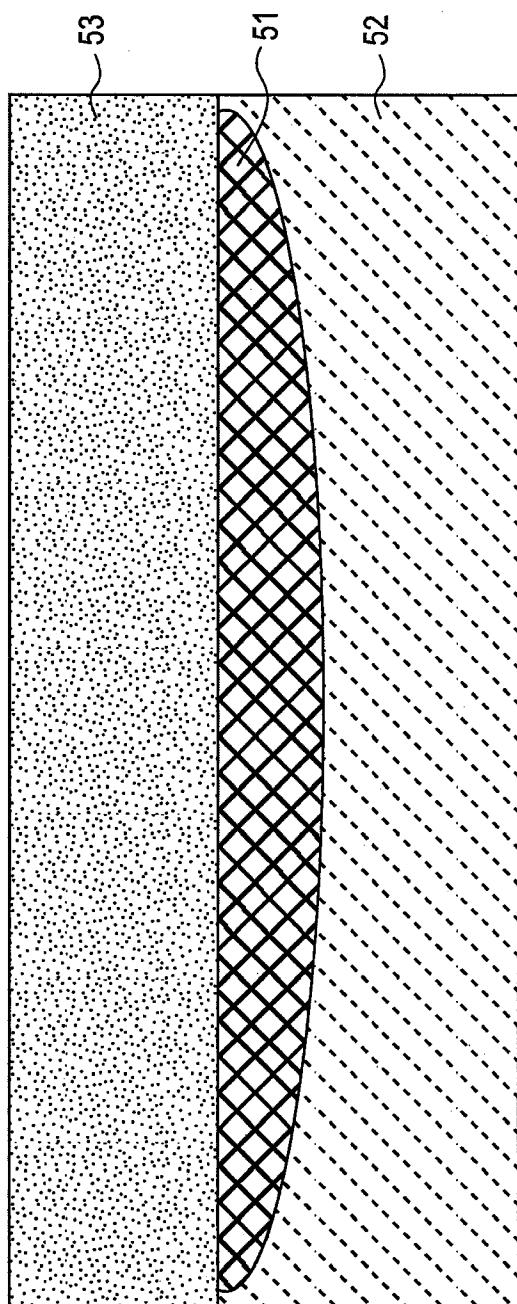


FIG. 4C

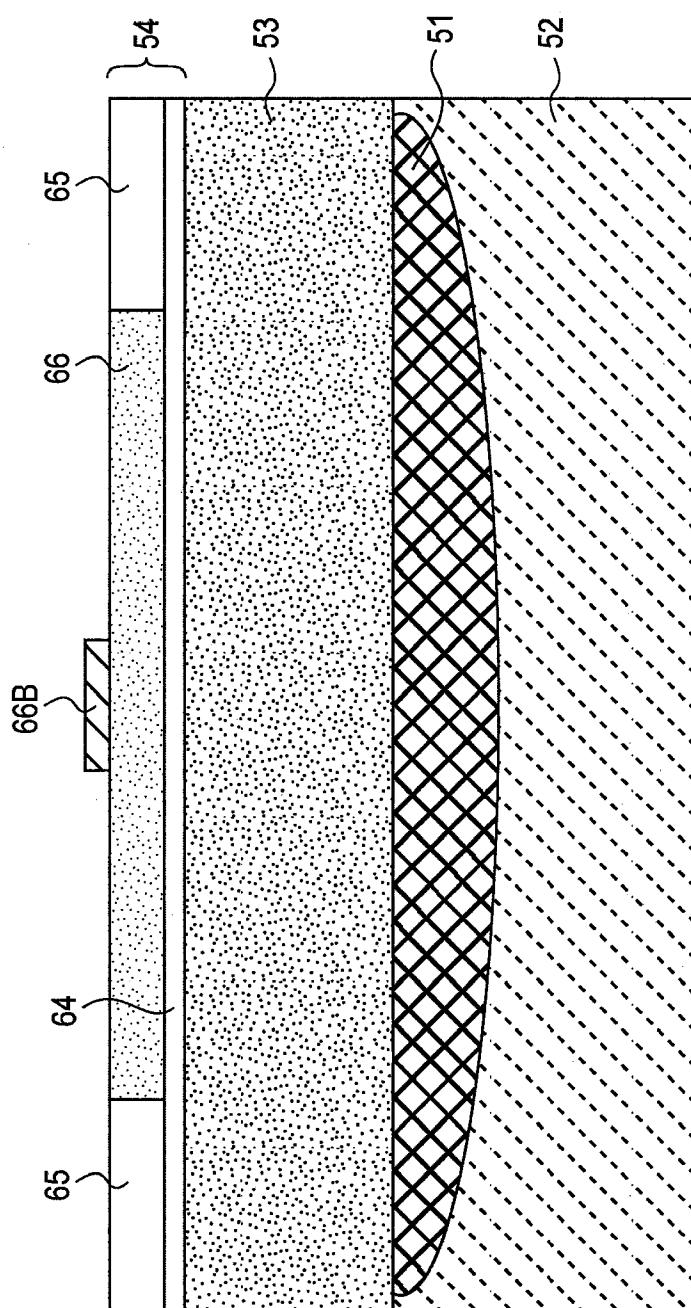


FIG. 4D

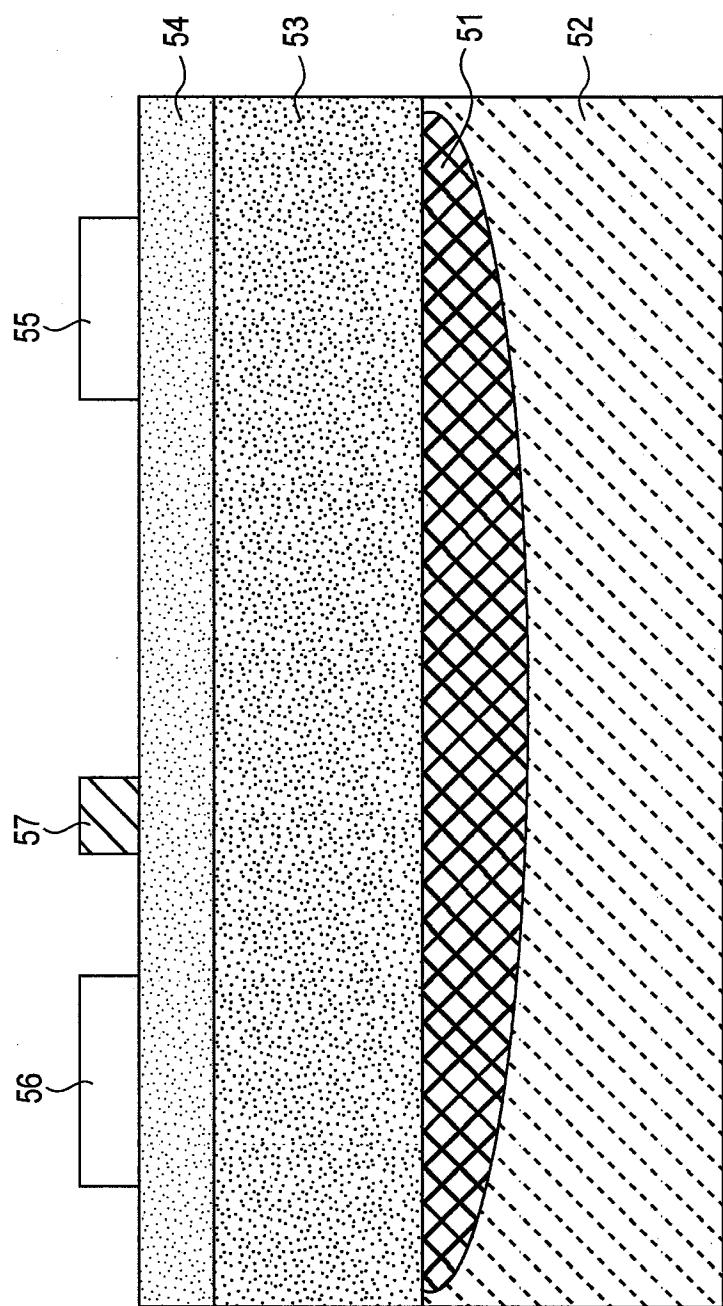


FIG. 4E

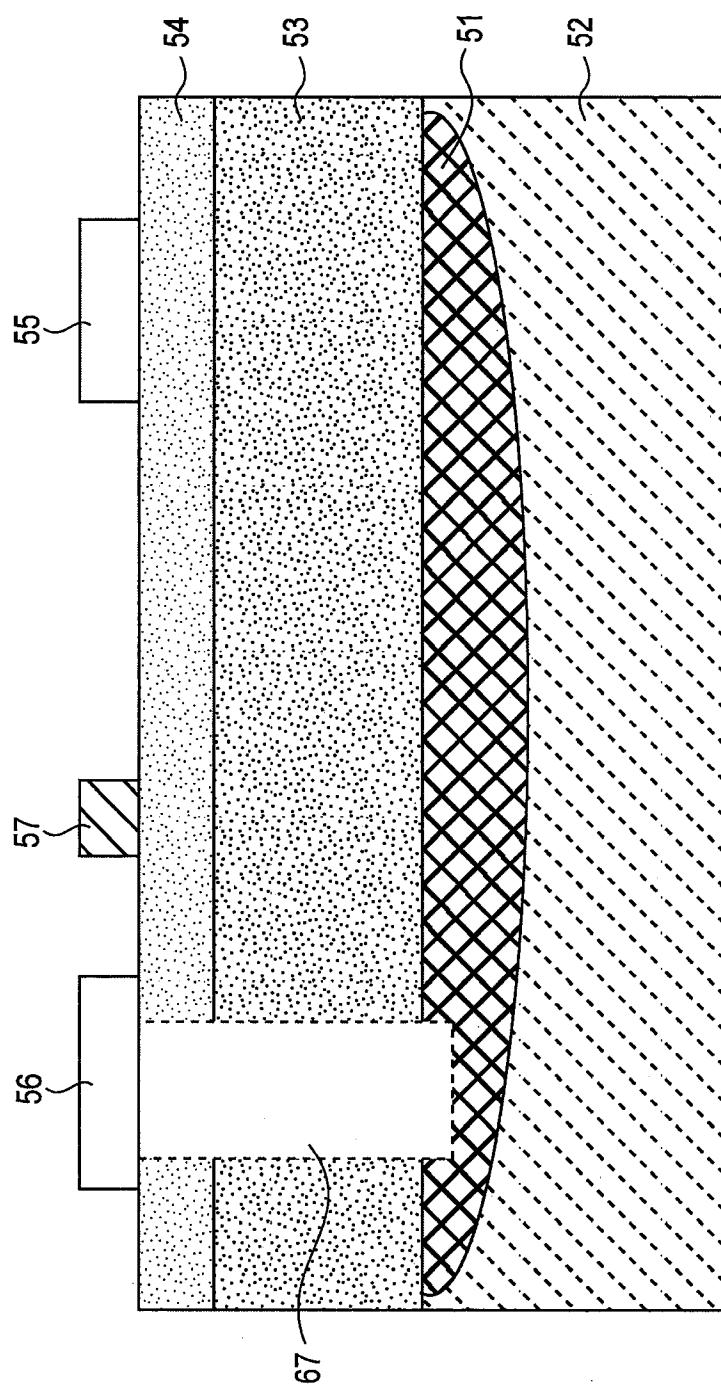


FIG. 4F

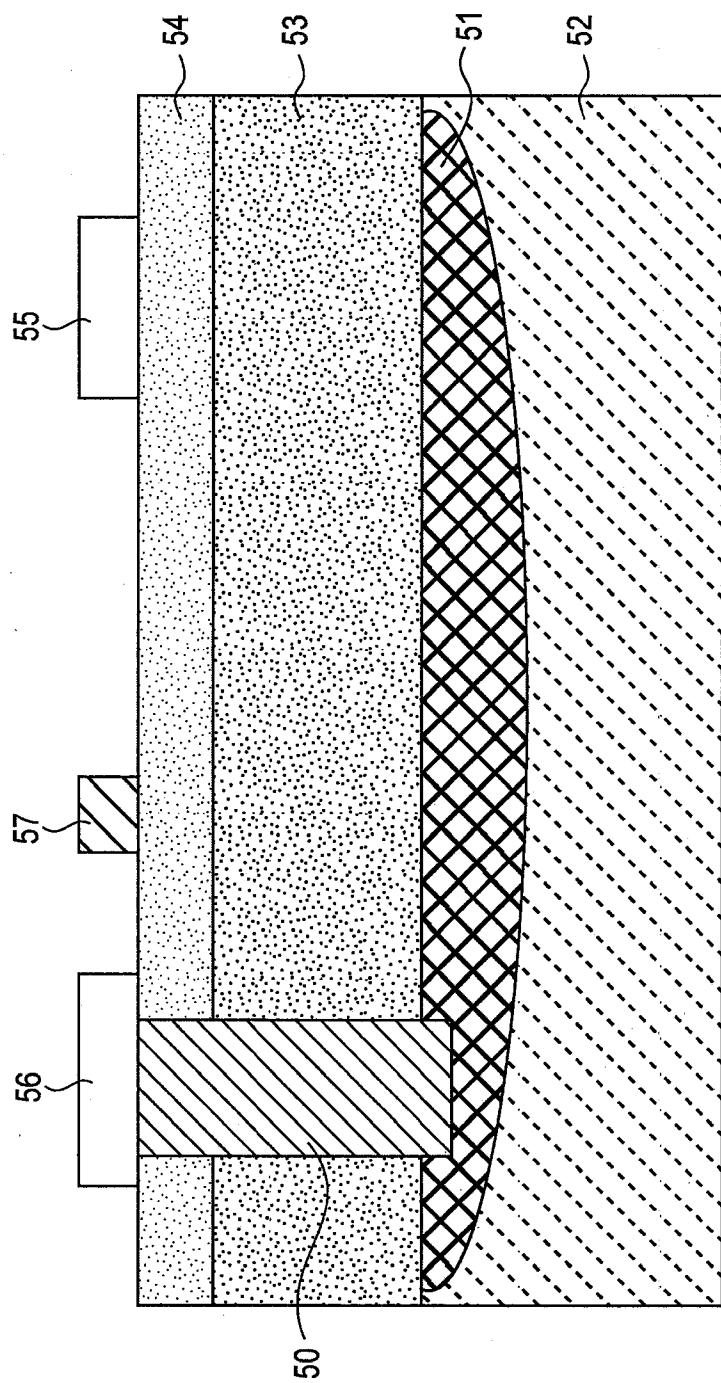


FIG. 4G

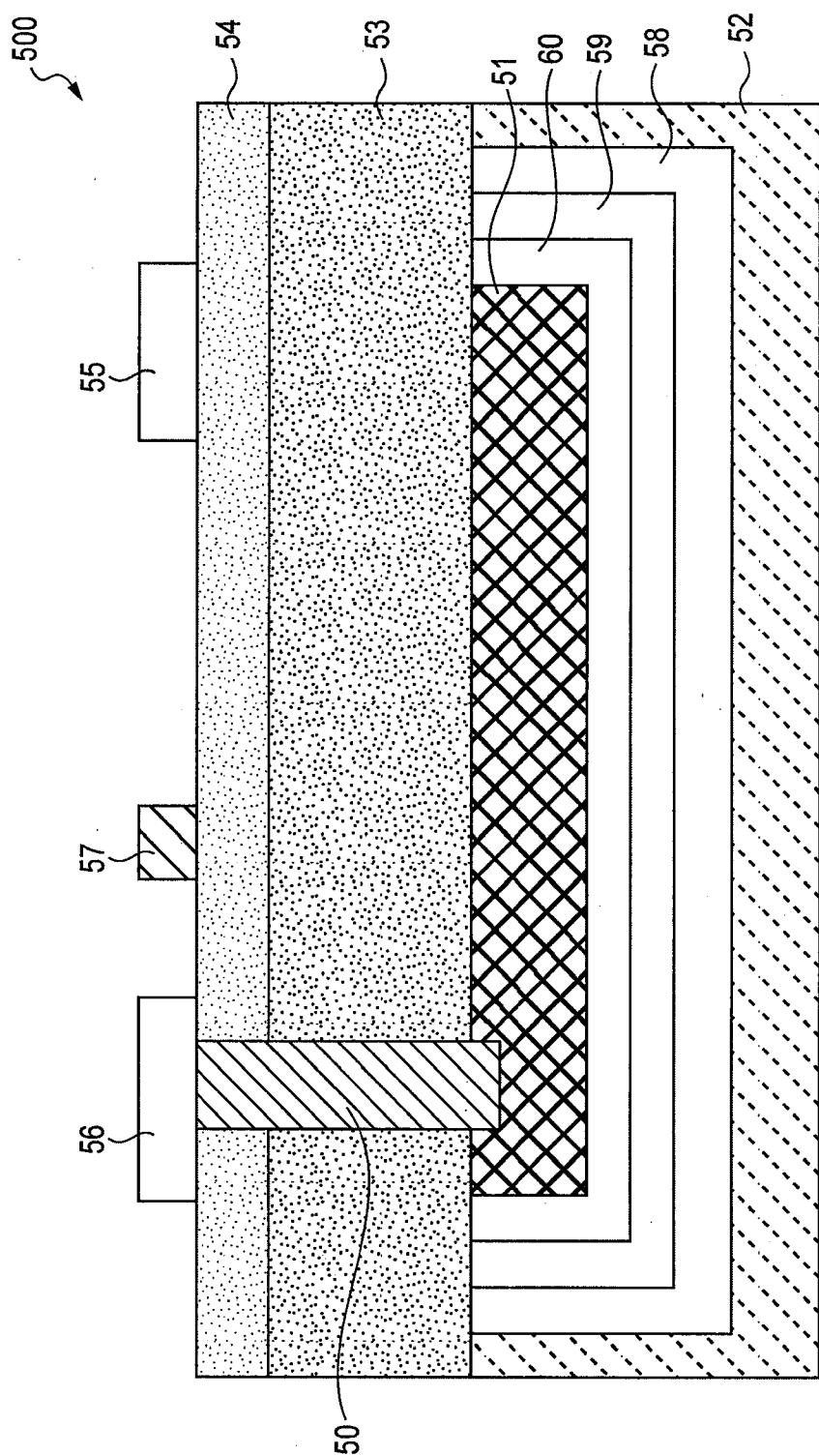


FIG. 5

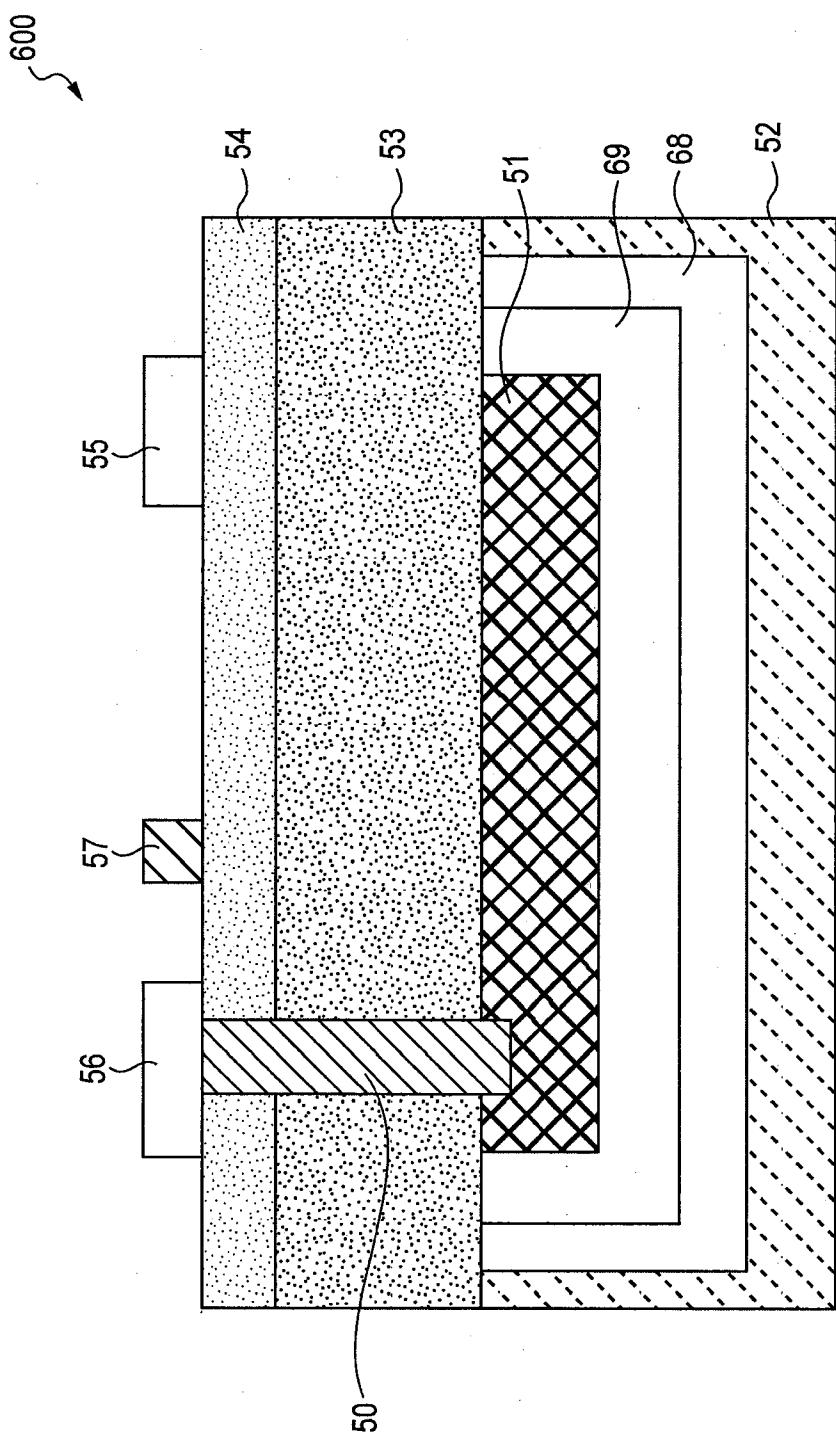


FIG. 6

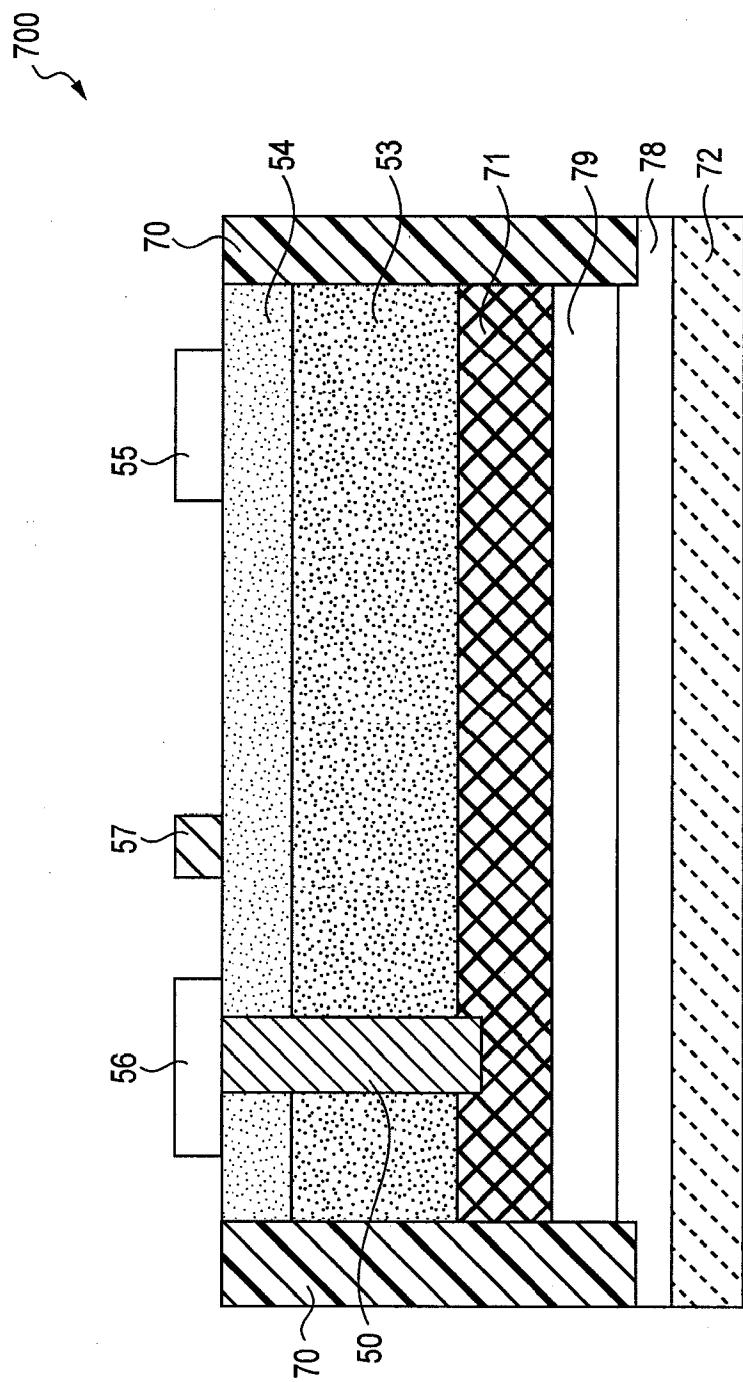


FIG. 7A

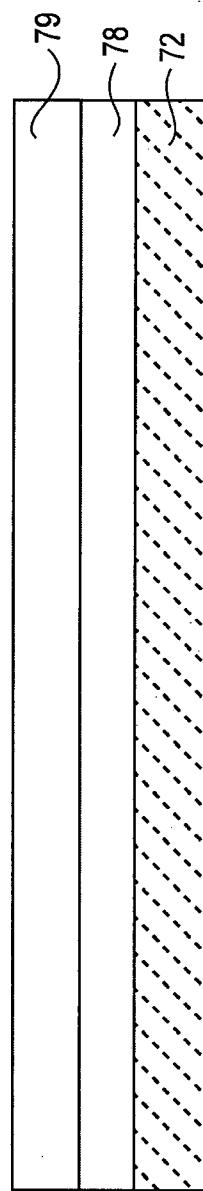


FIG. 7B

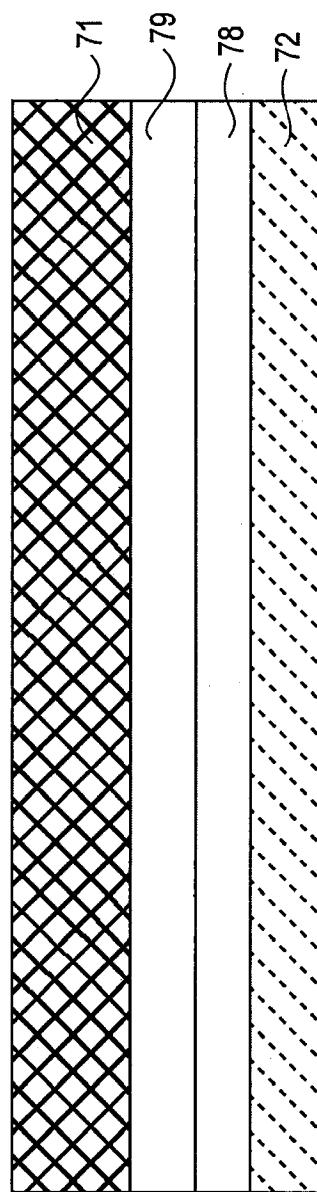


FIG. 7C

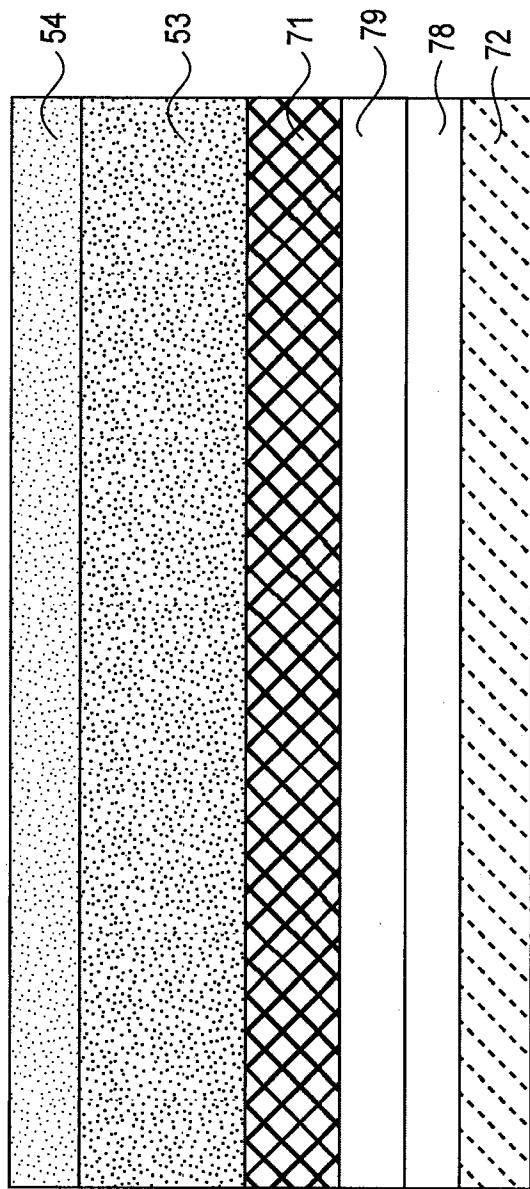


FIG. 7D

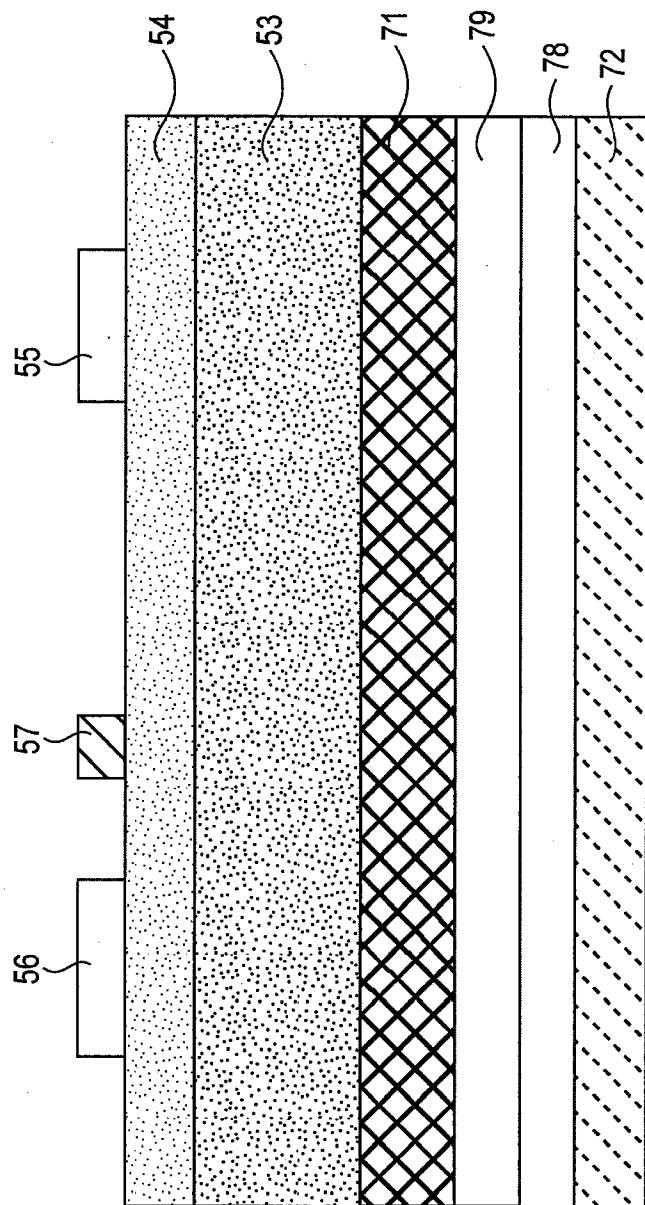


FIG. 7E

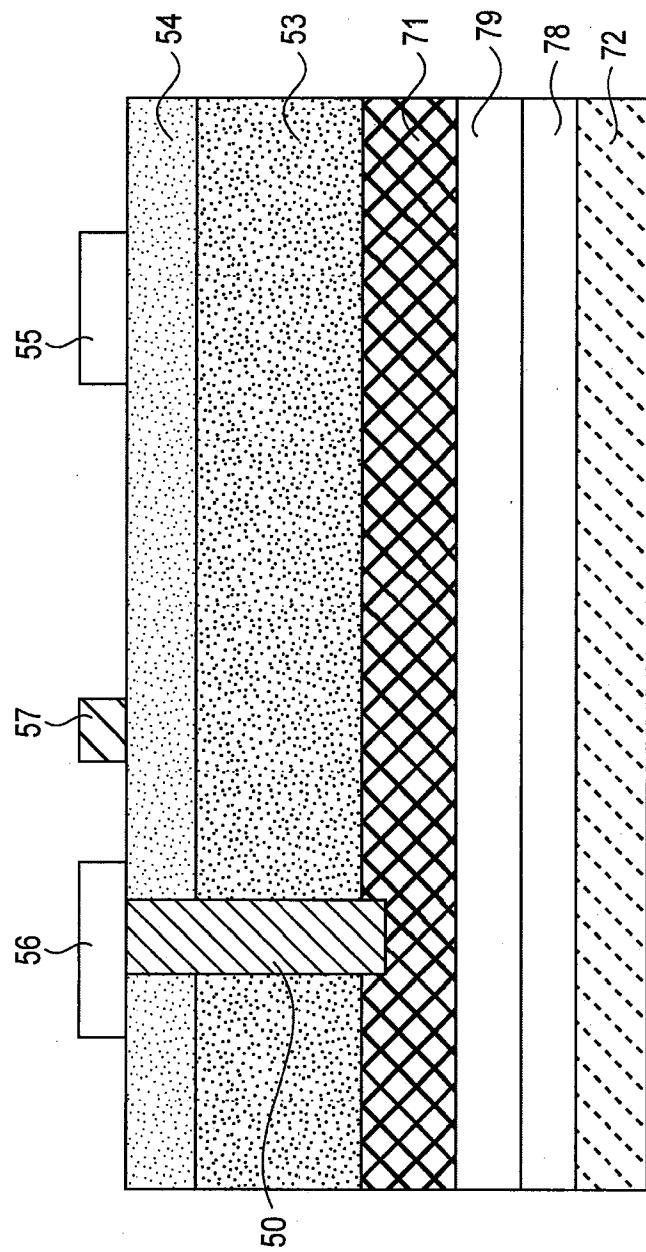


FIG. 7F

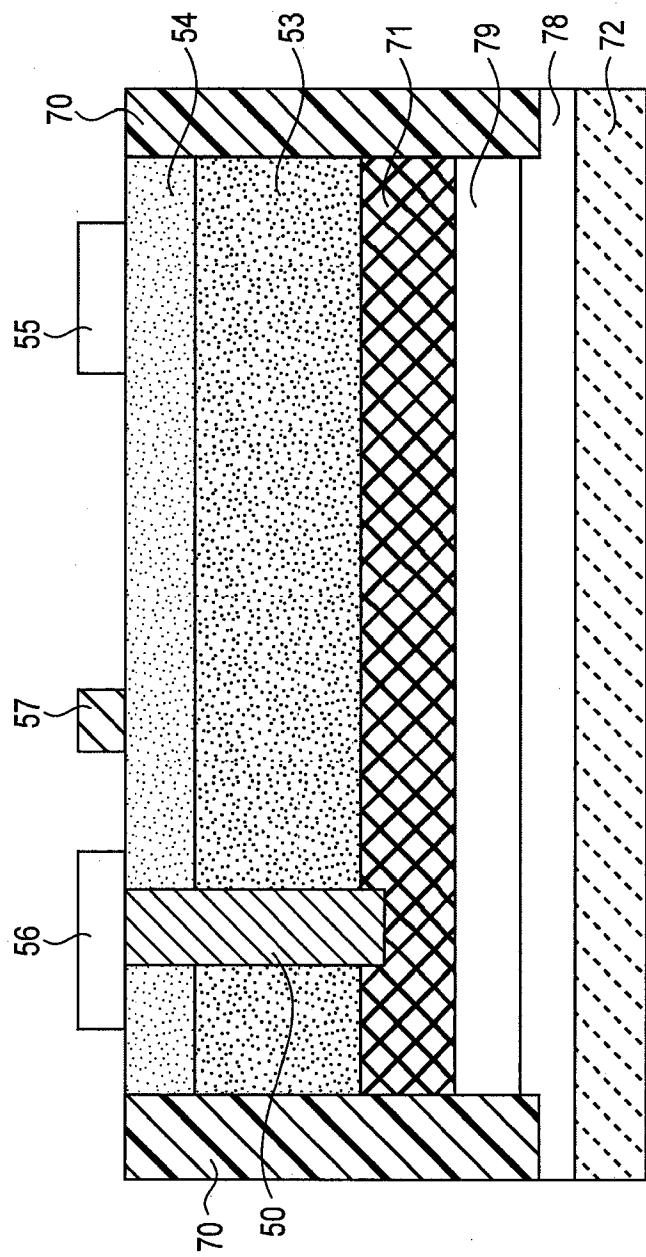


FIG. 7G

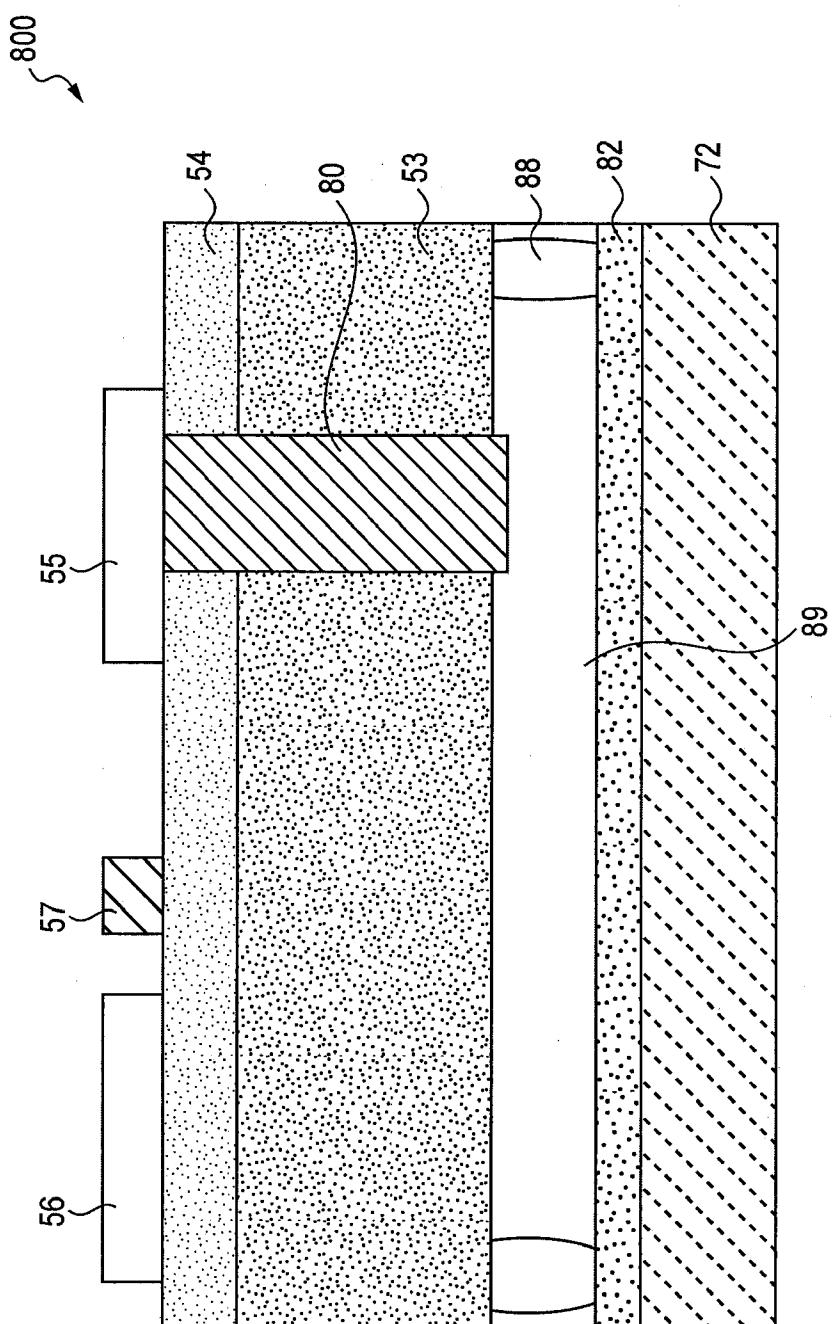


FIG. 8

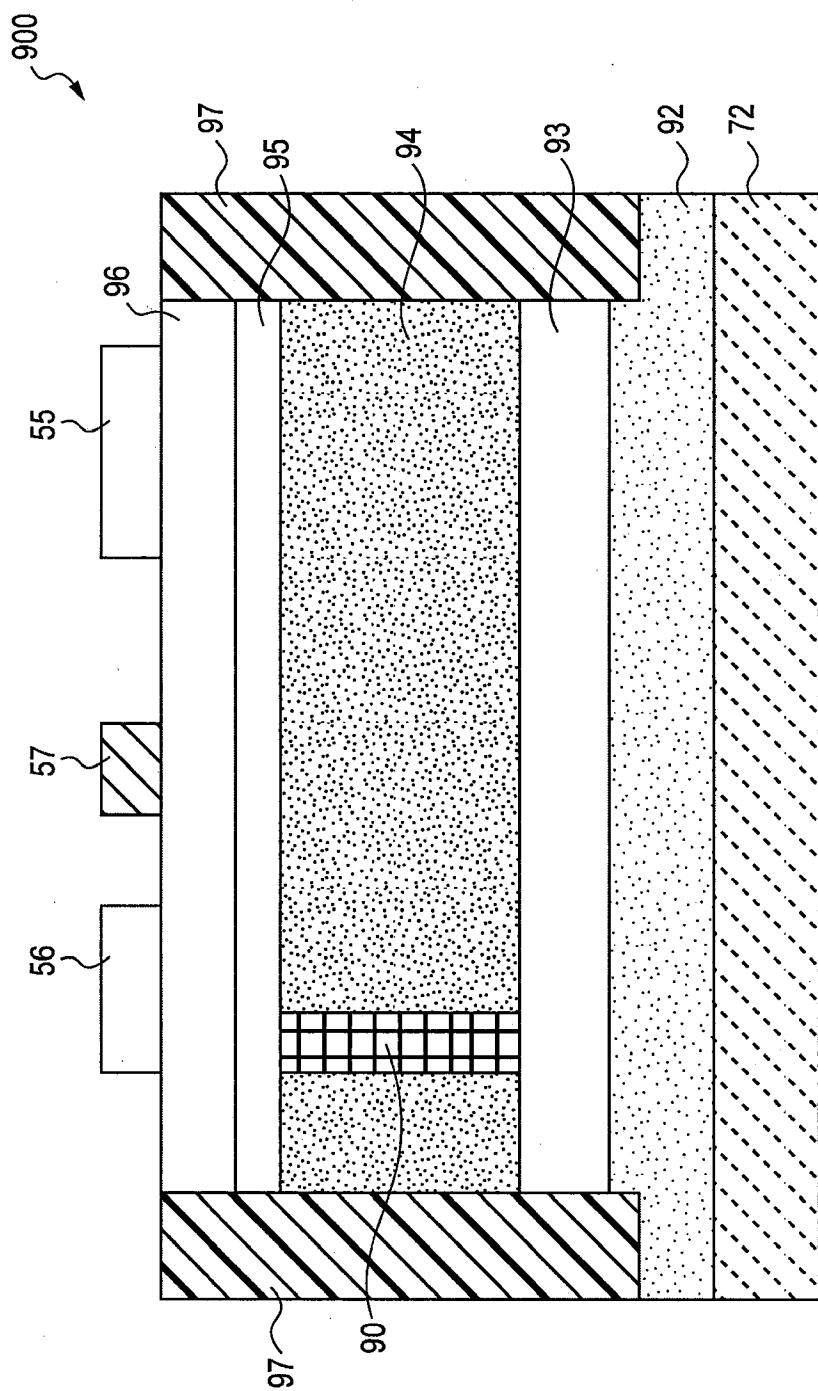


FIG. 9A

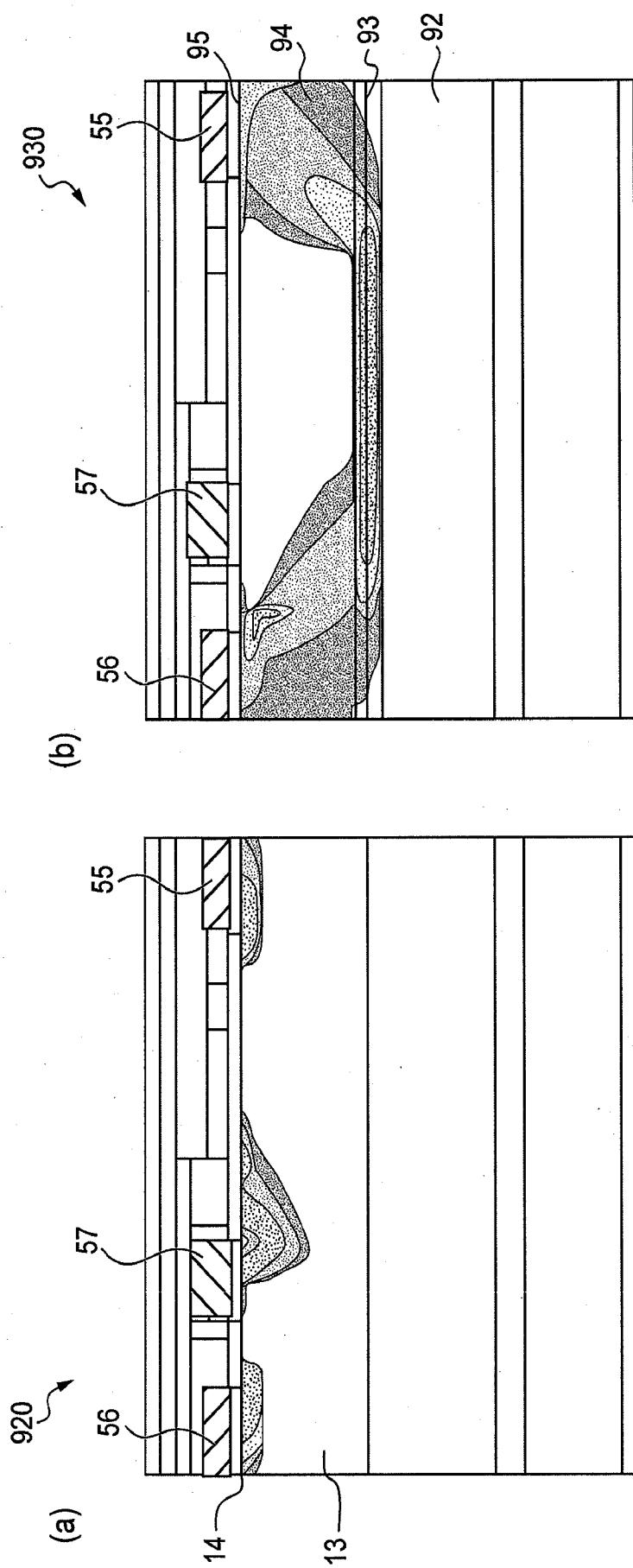


FIG. 9B

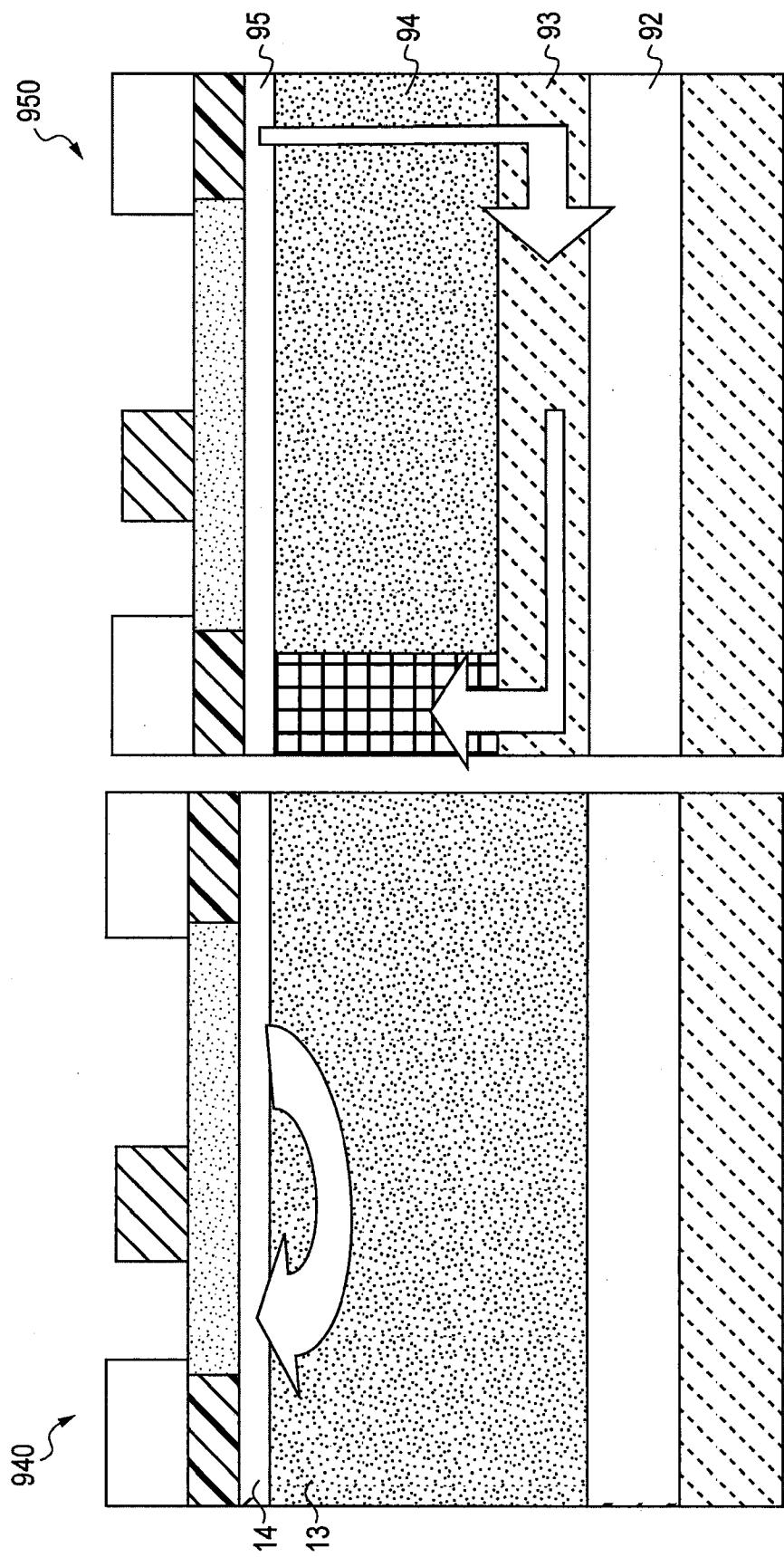


FIG. 9C

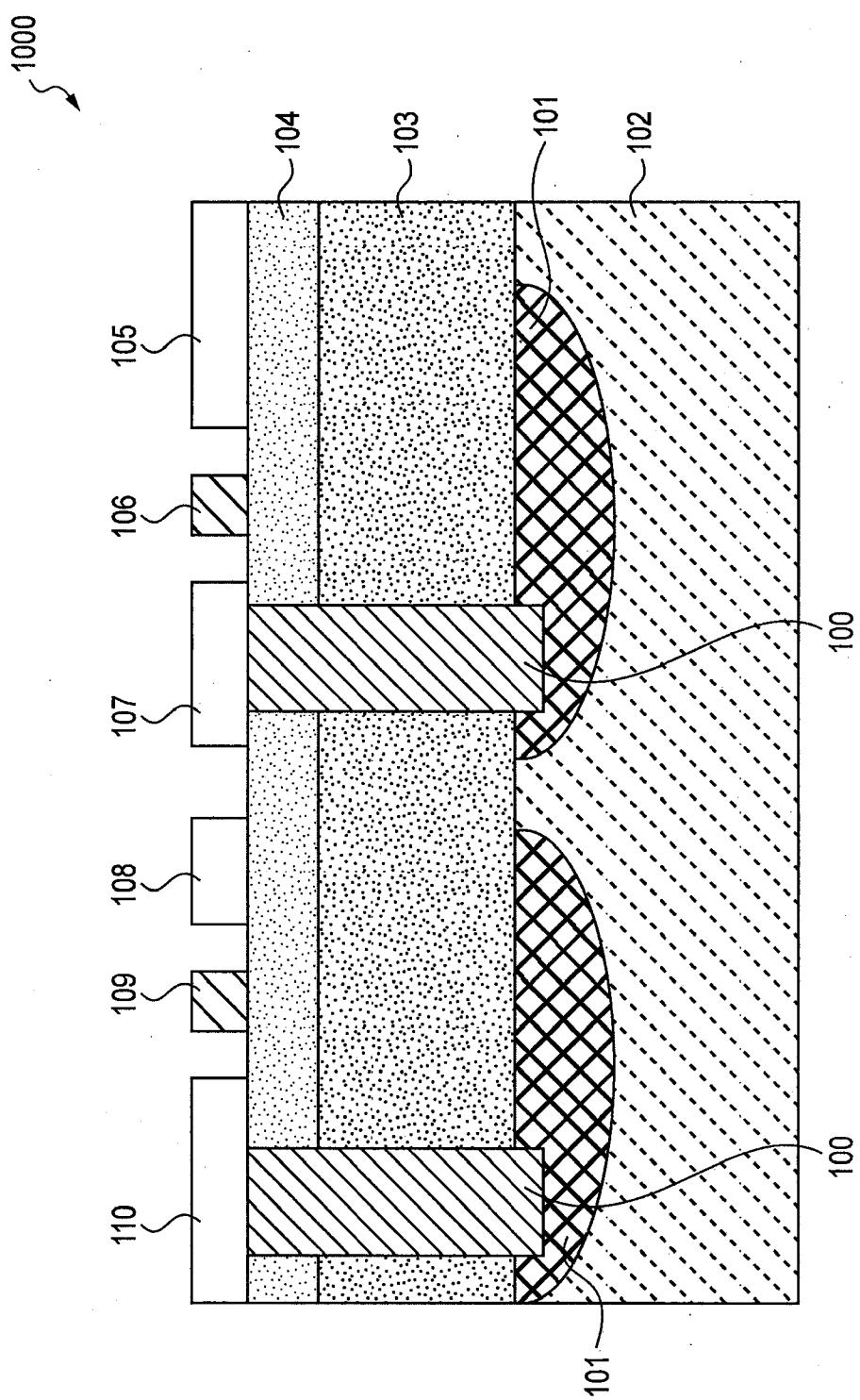


FIG. 10

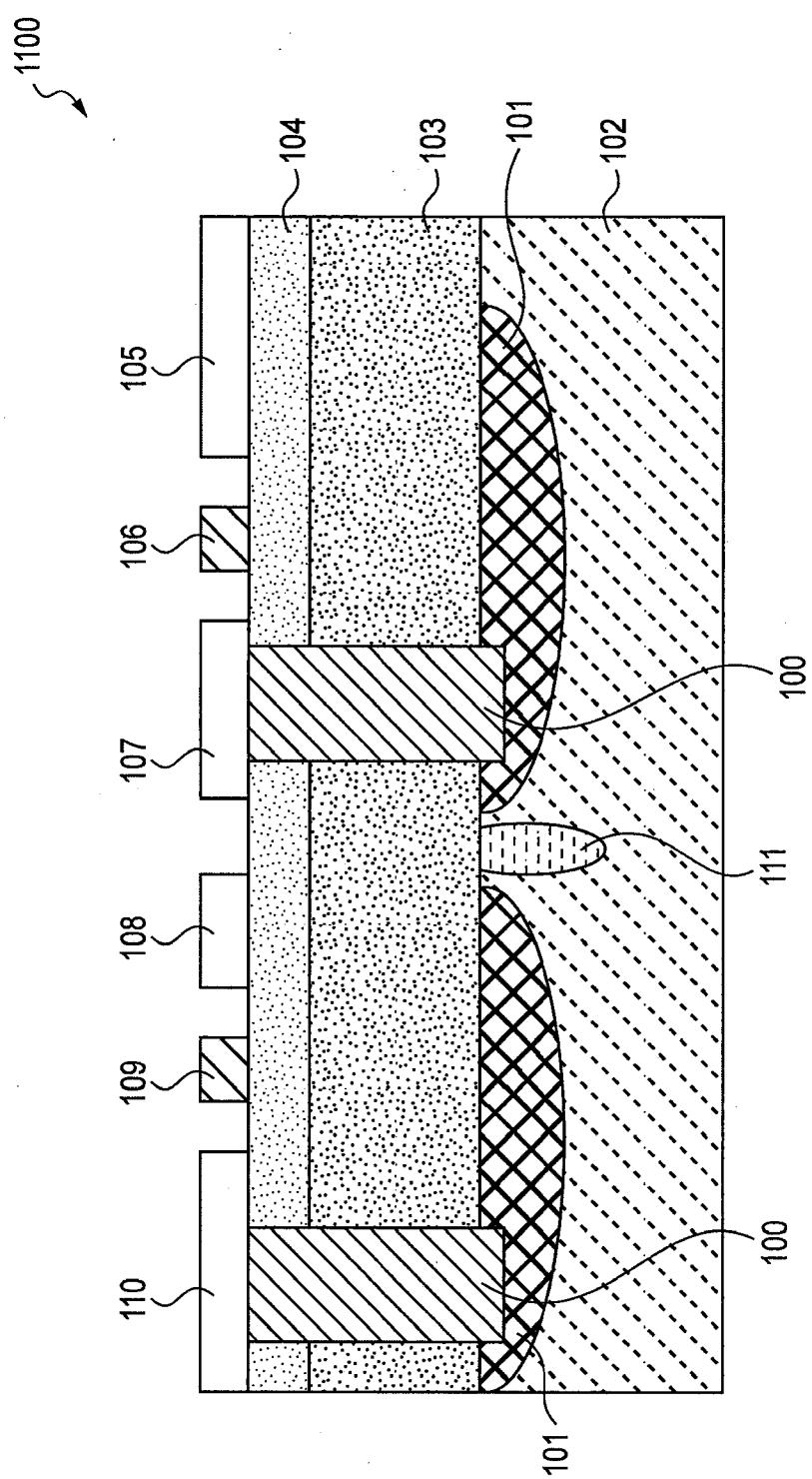


FIG. 11

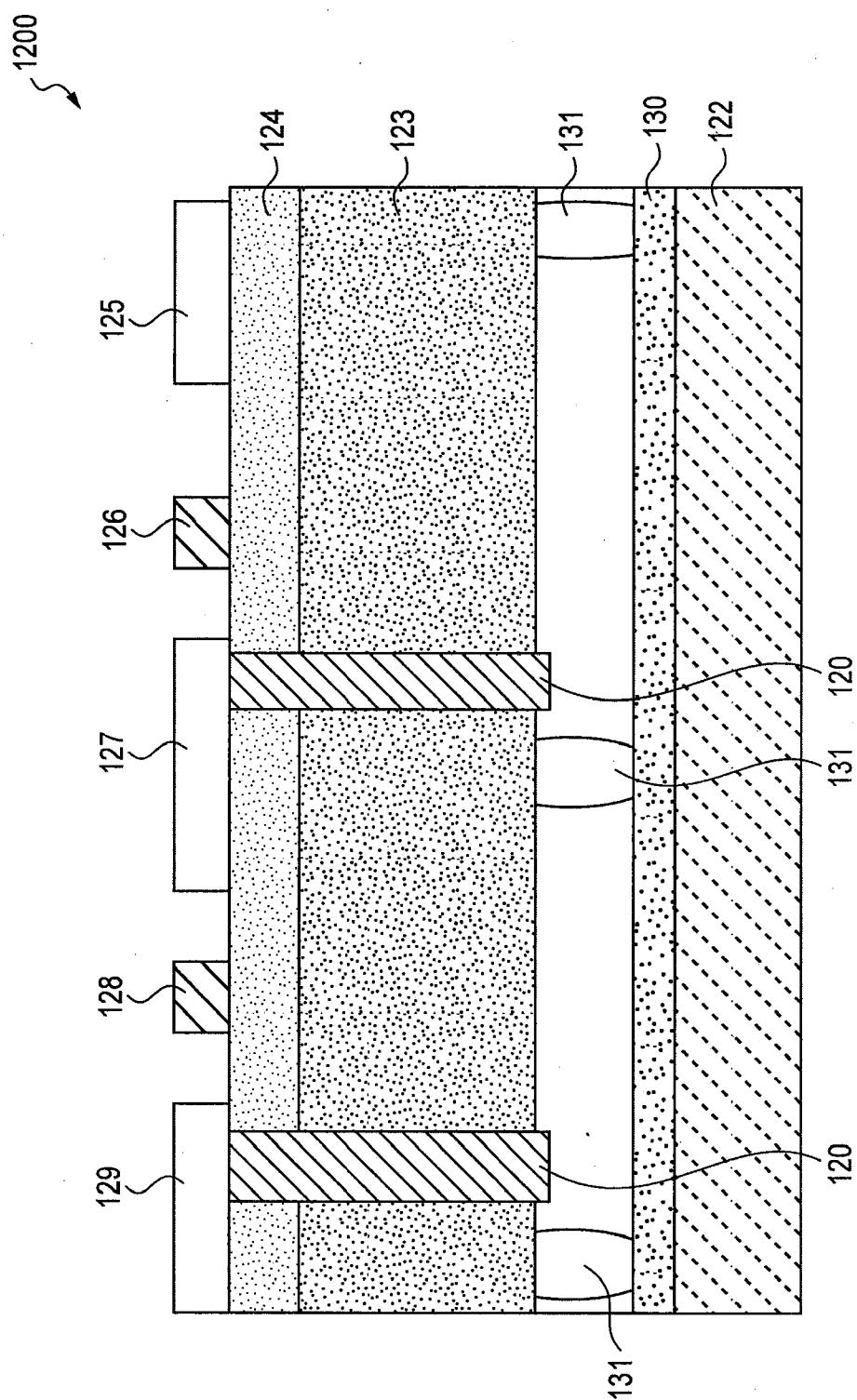


FIG. 12

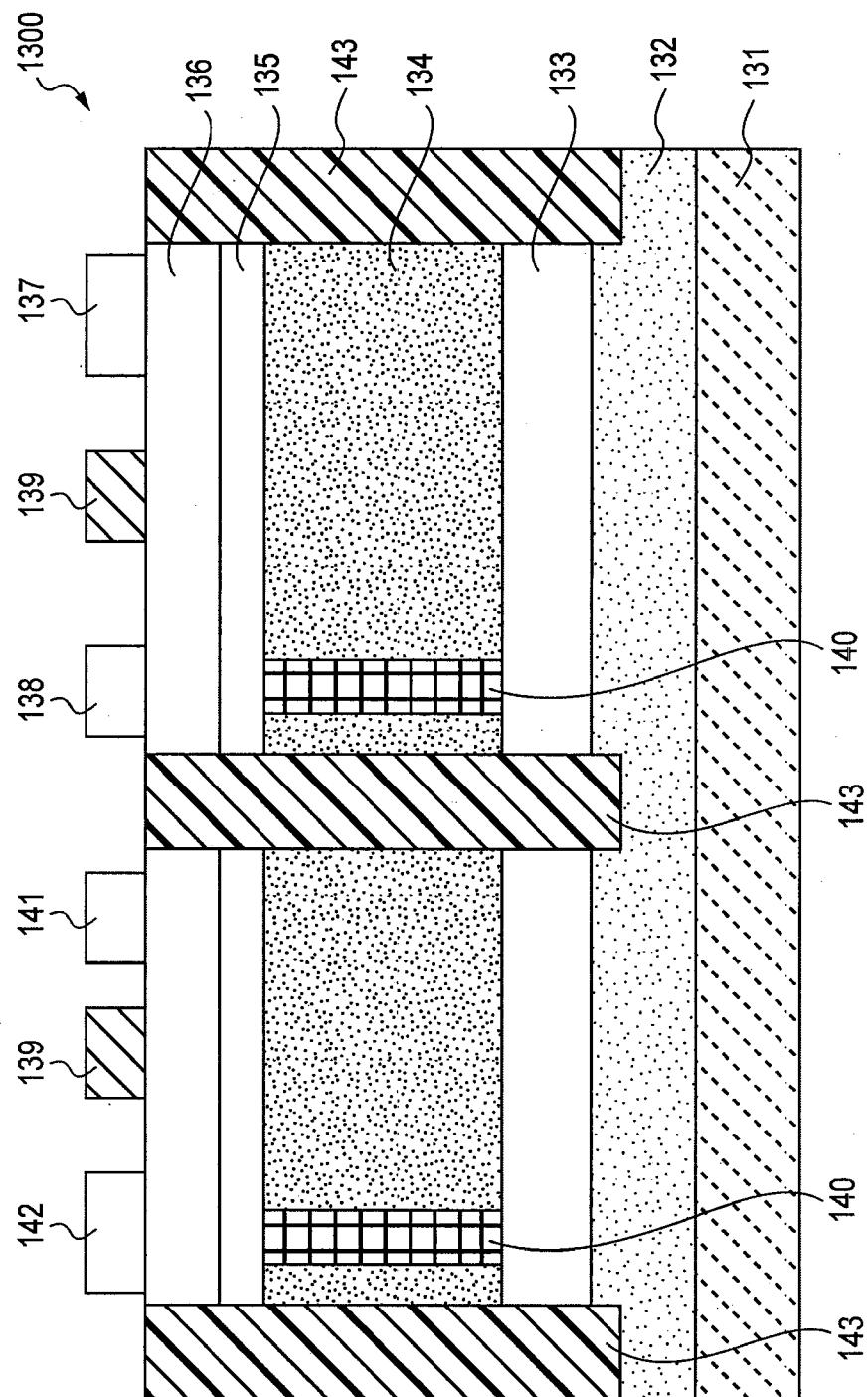


FIG. 13

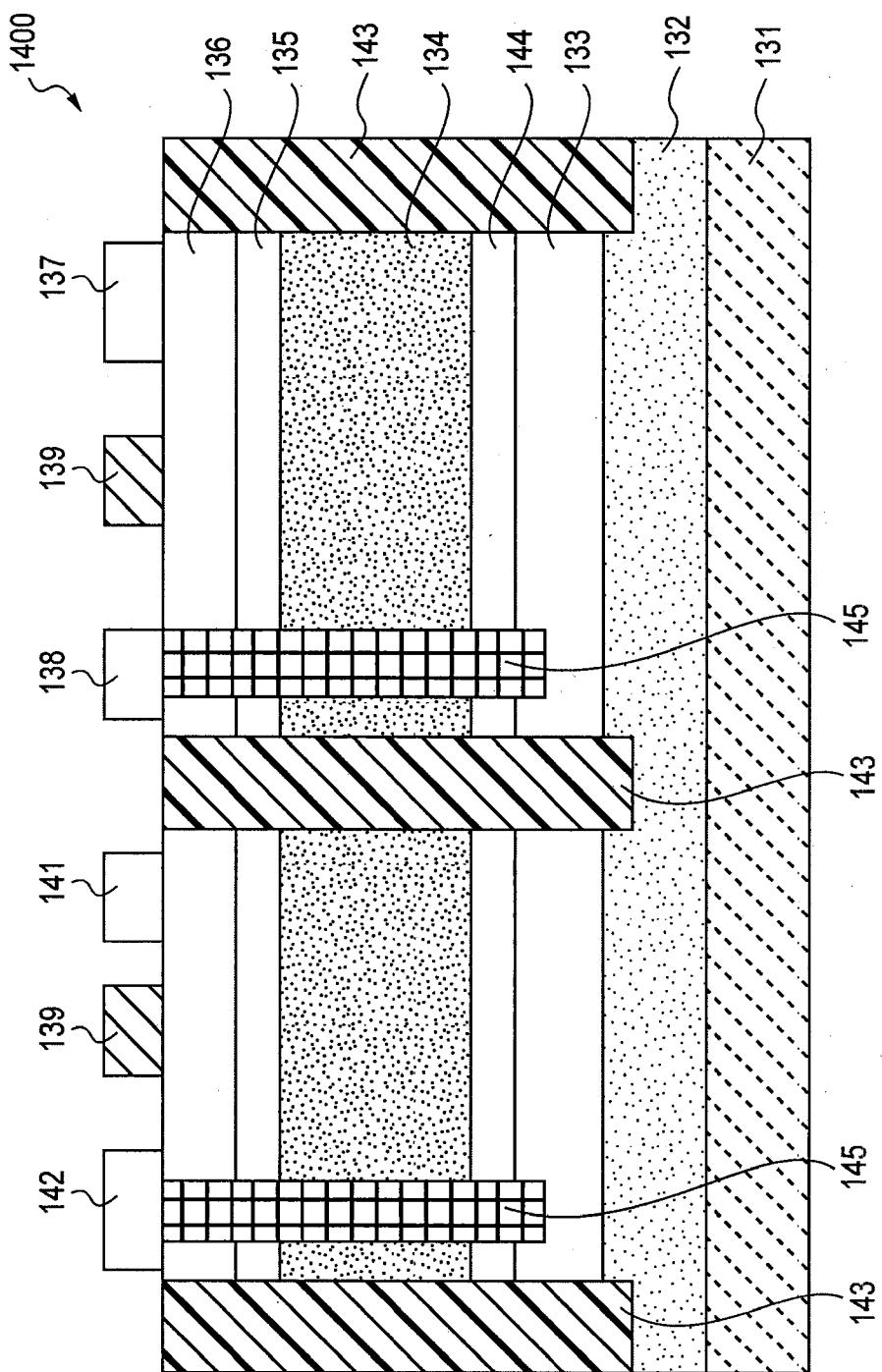
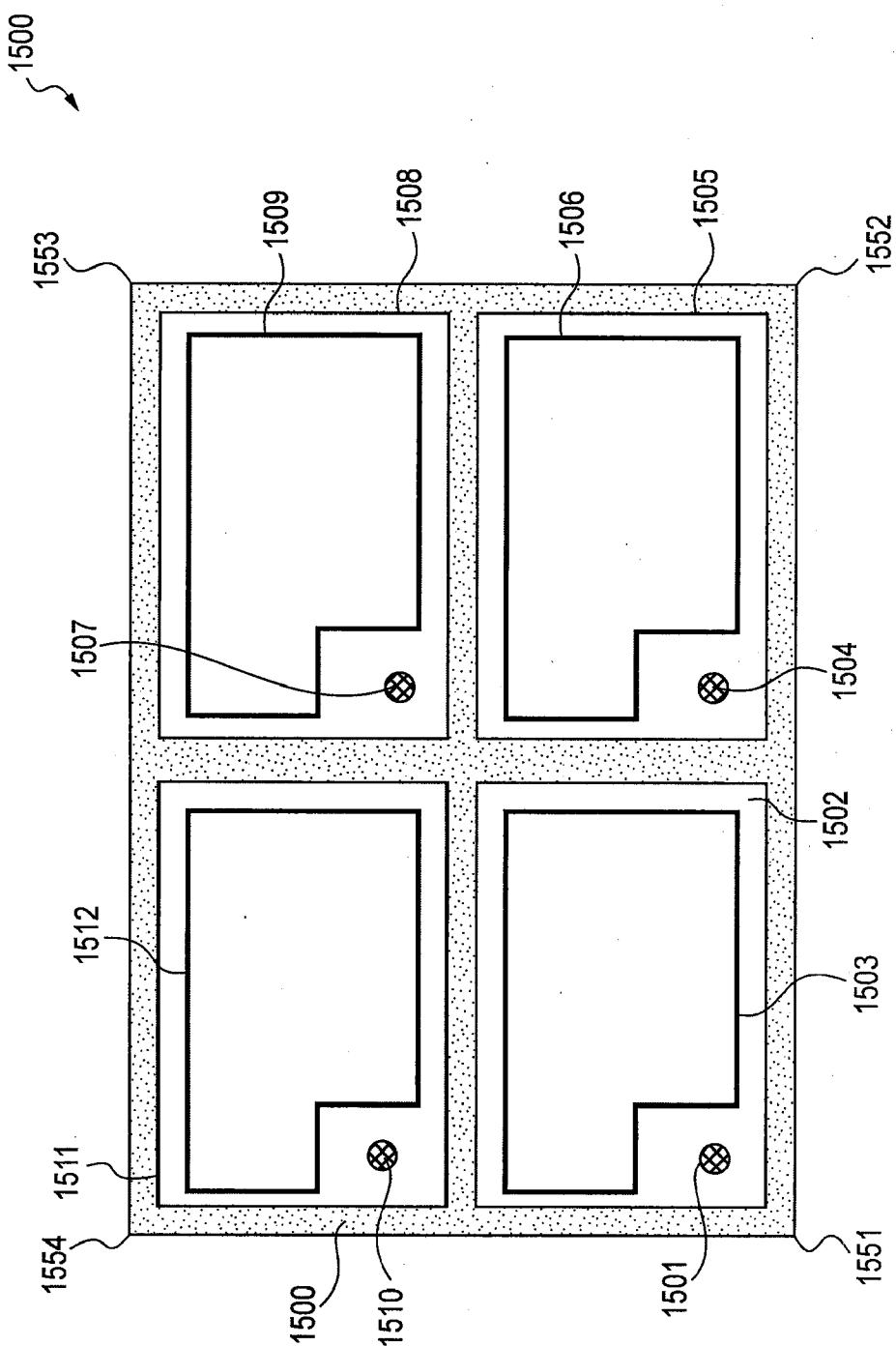


FIG. 14

**FIG. 15**

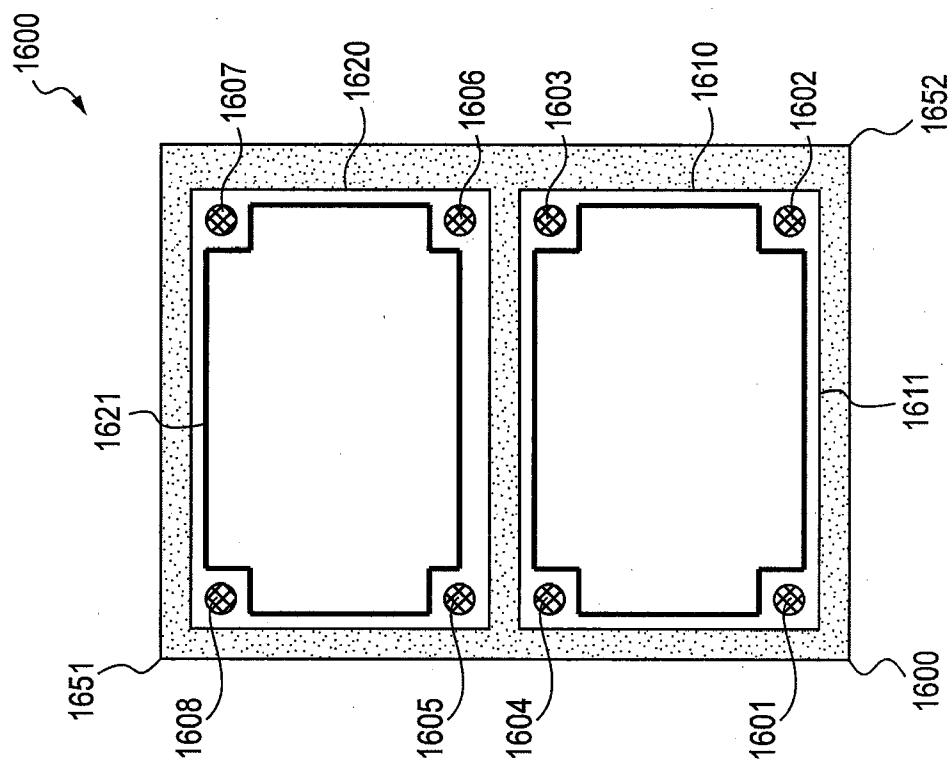


FIG. 16

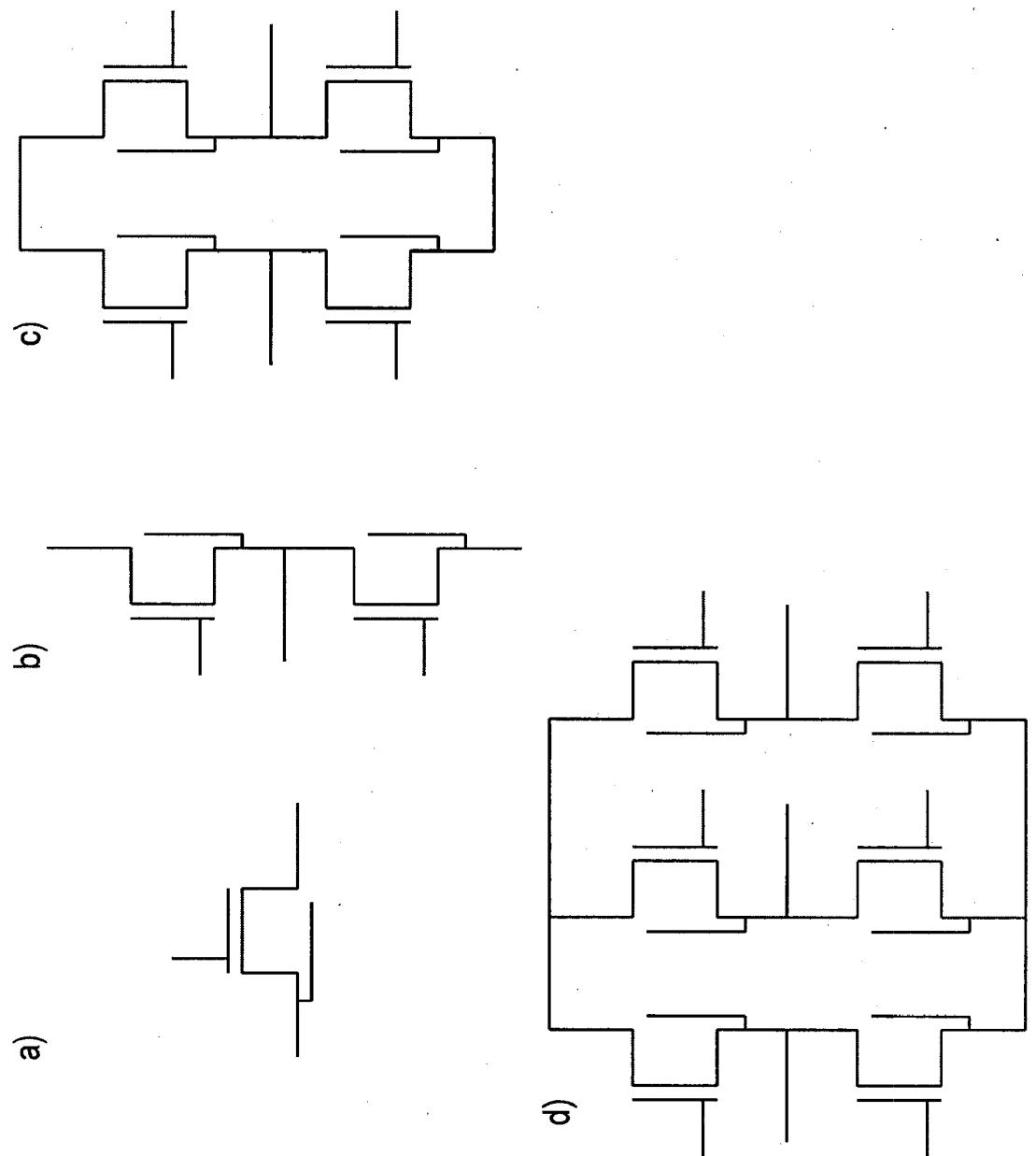


FIG. 17

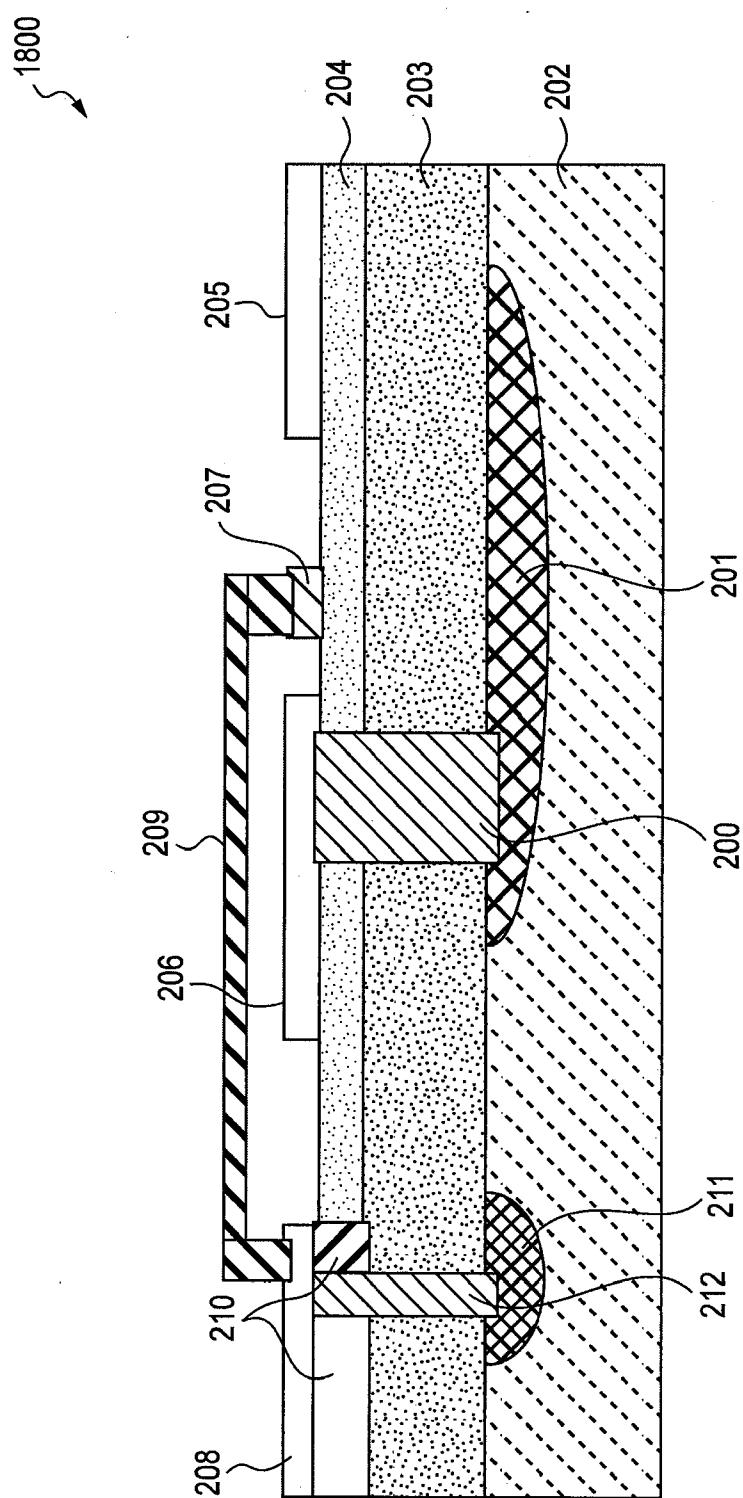


FIG. 18

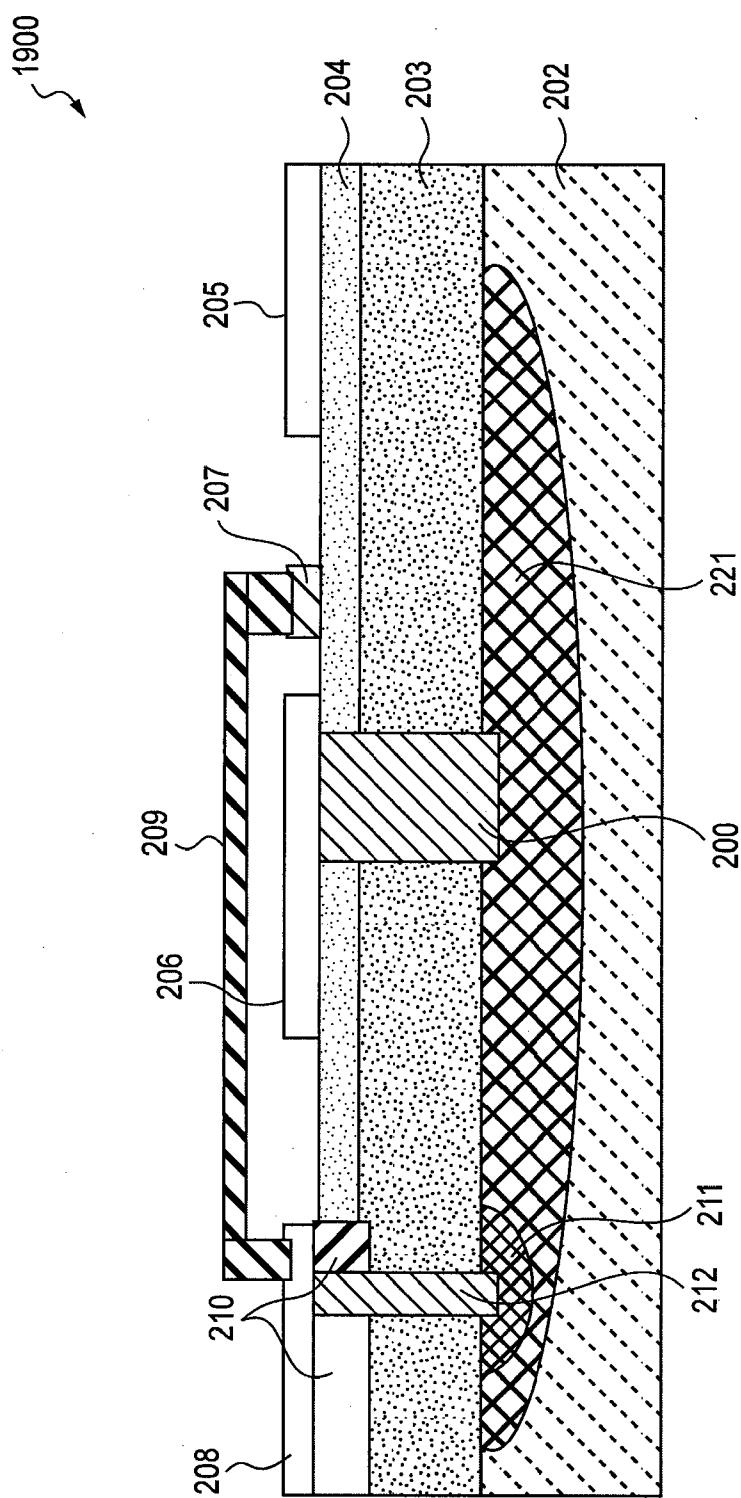


FIG. 19

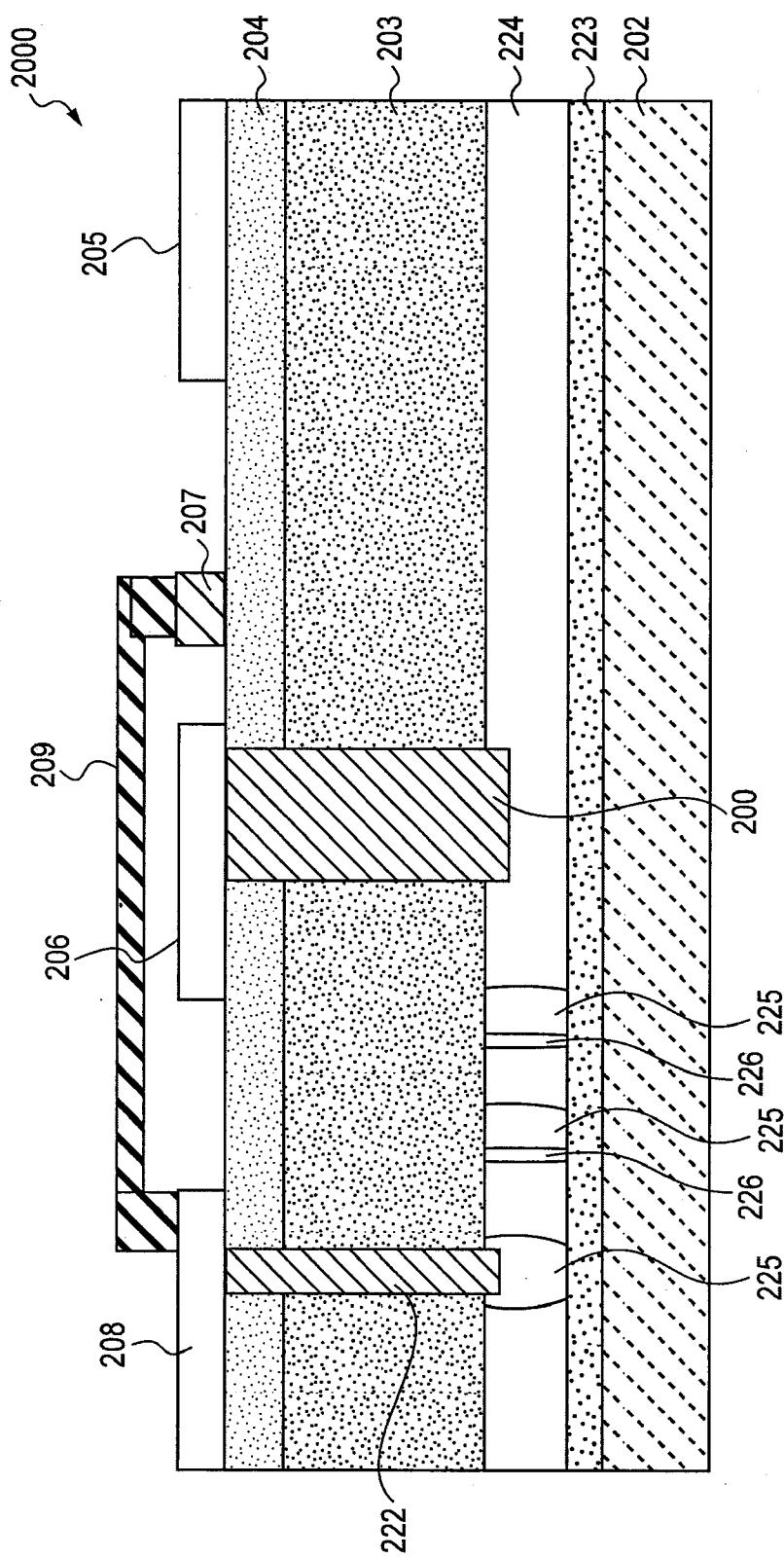


FIG. 20

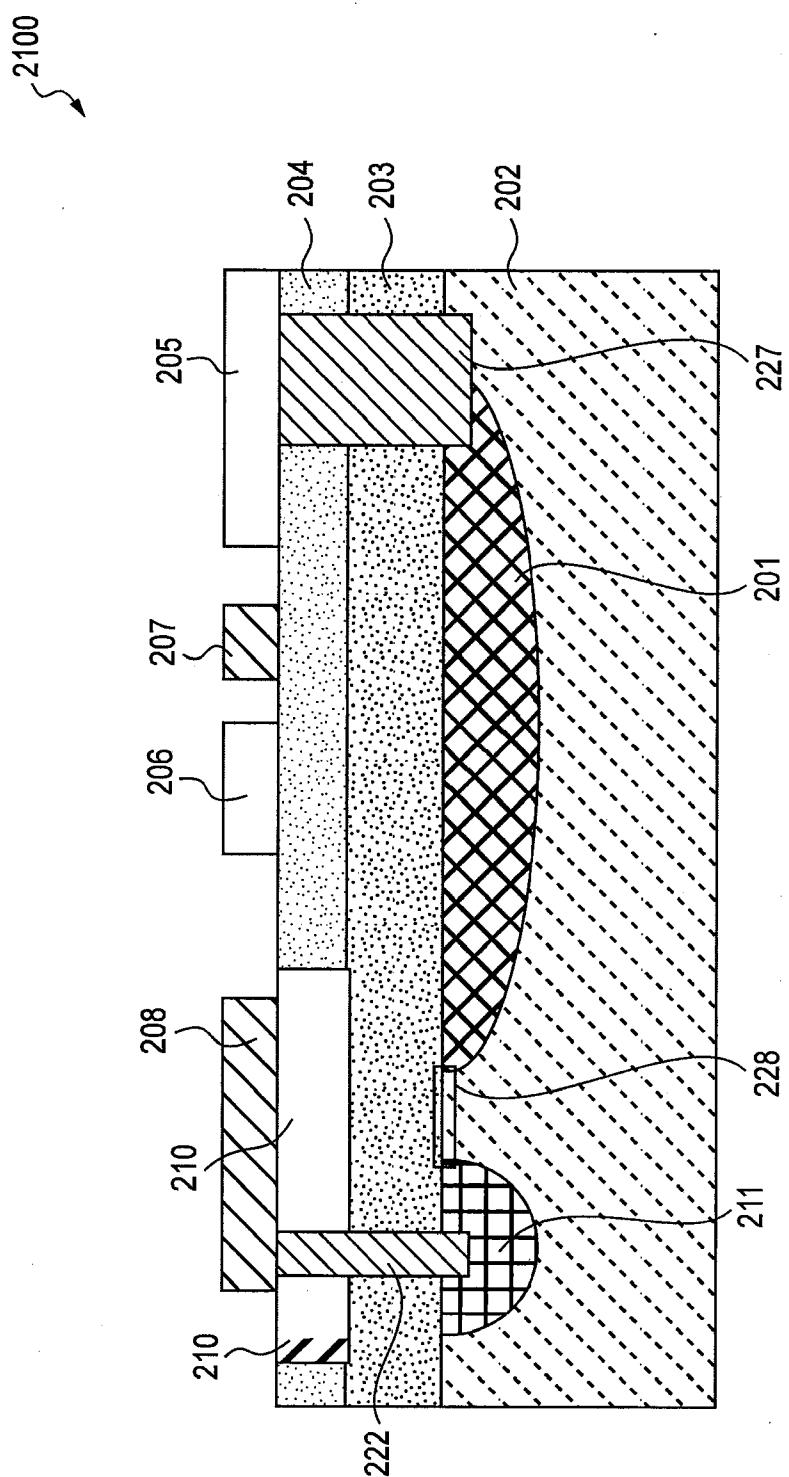


FIG. 21

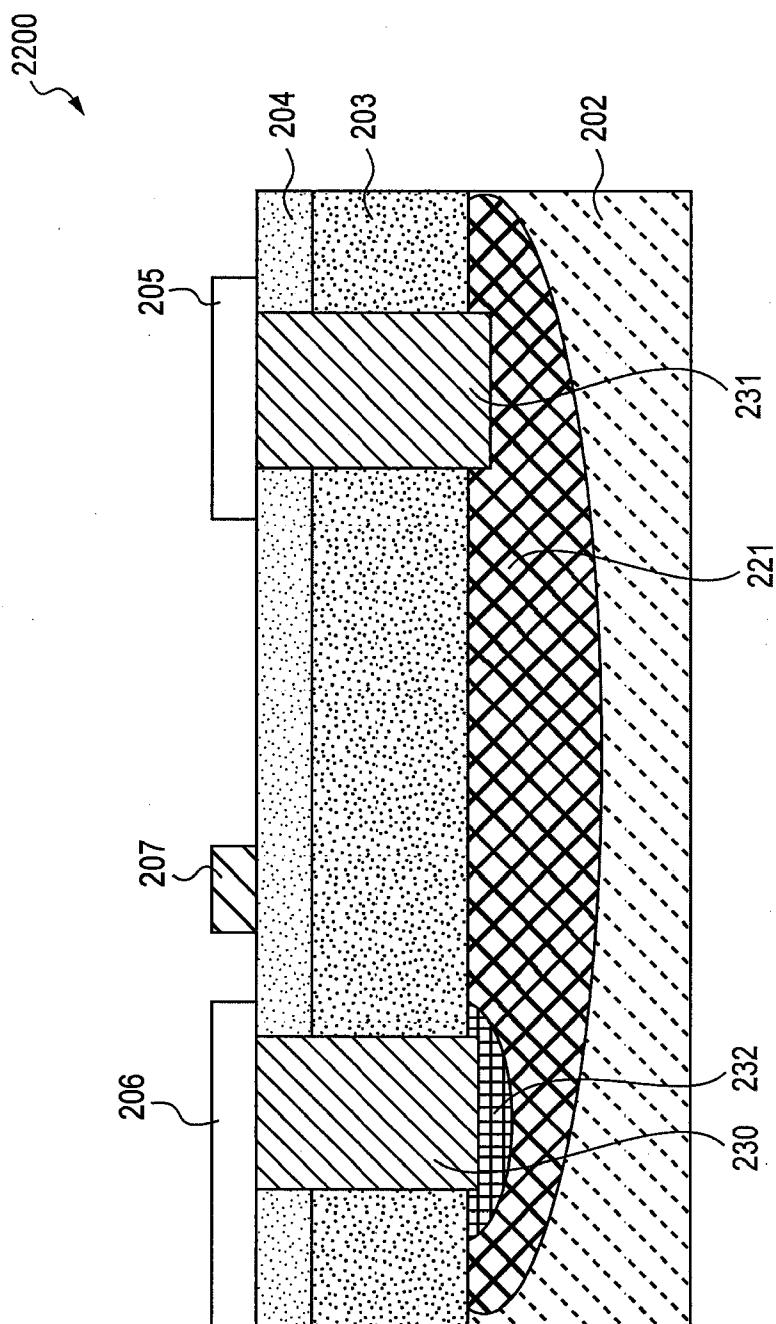


FIG. 22A

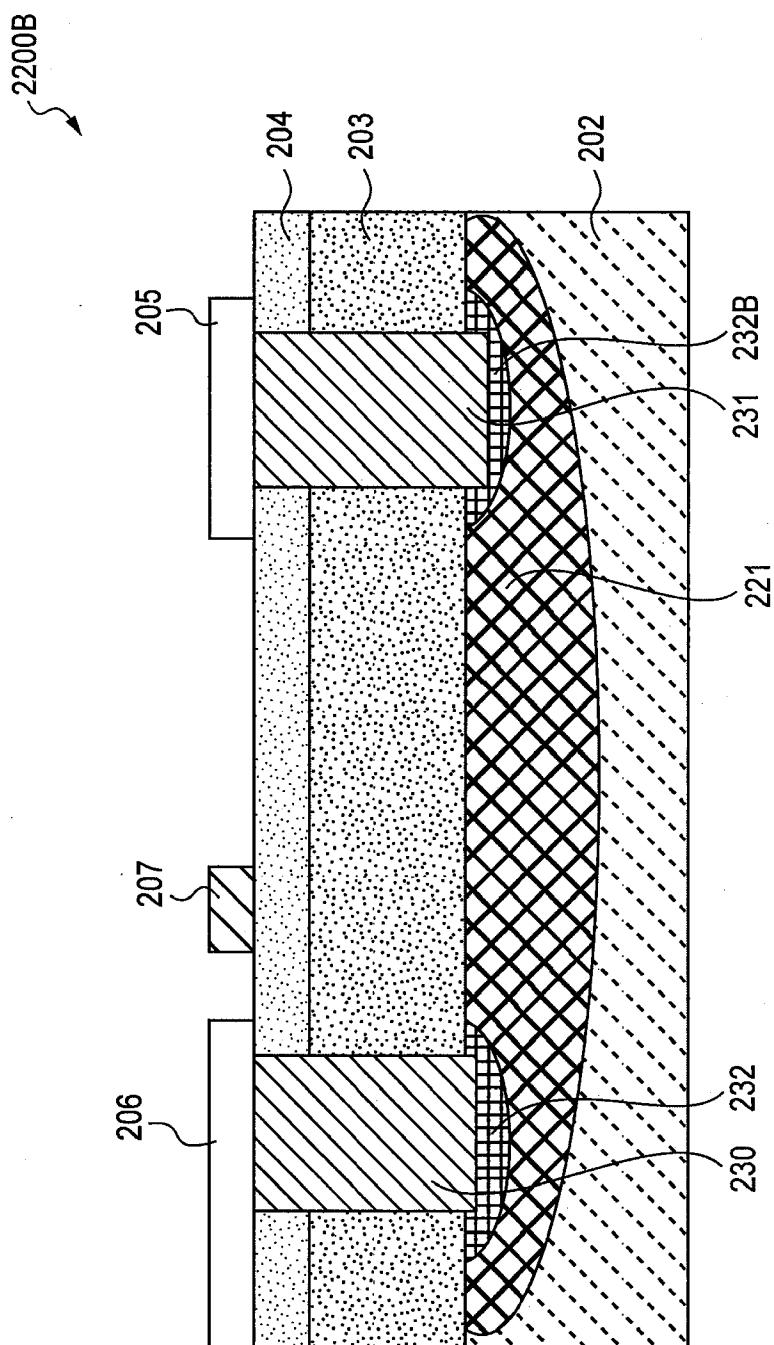


FIG. 22B

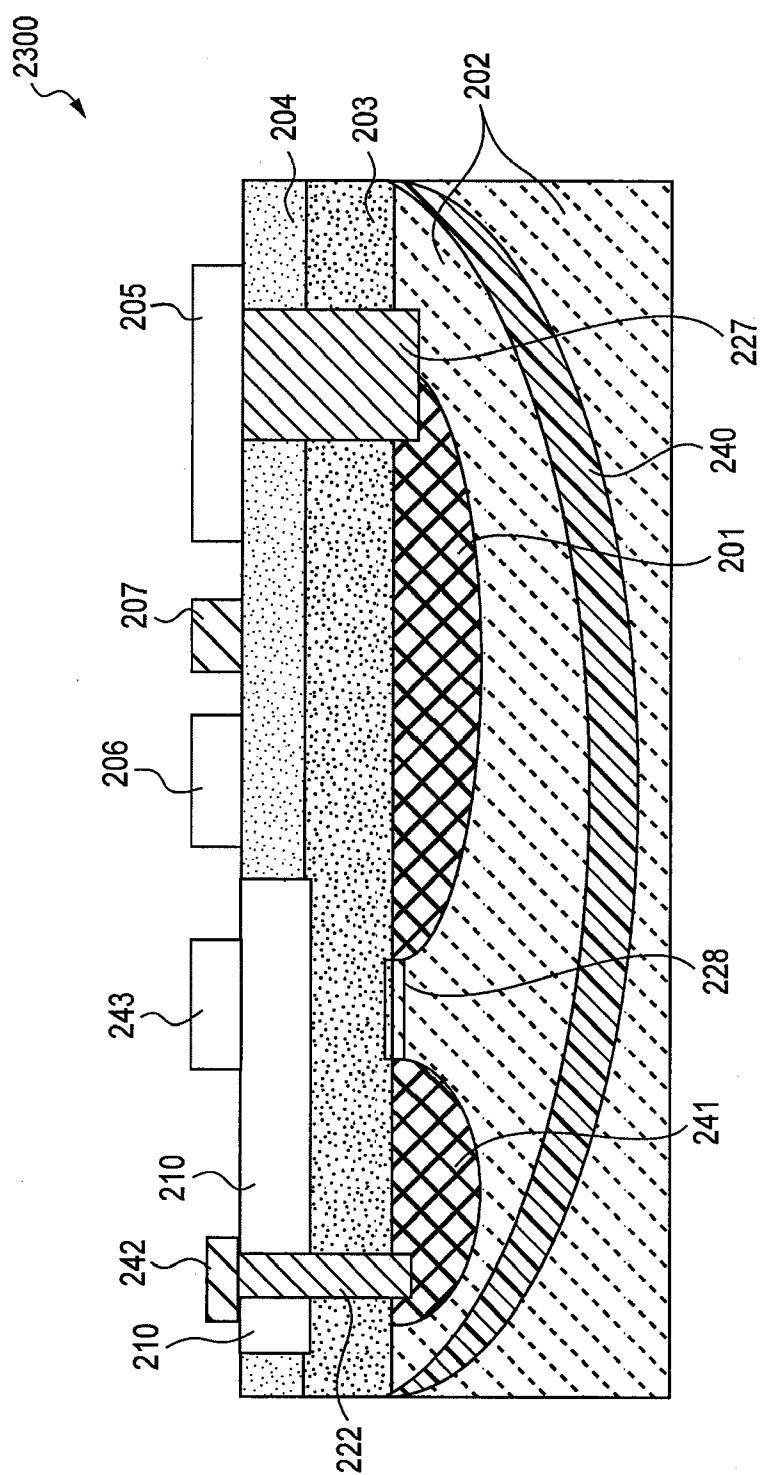


FIG. 23

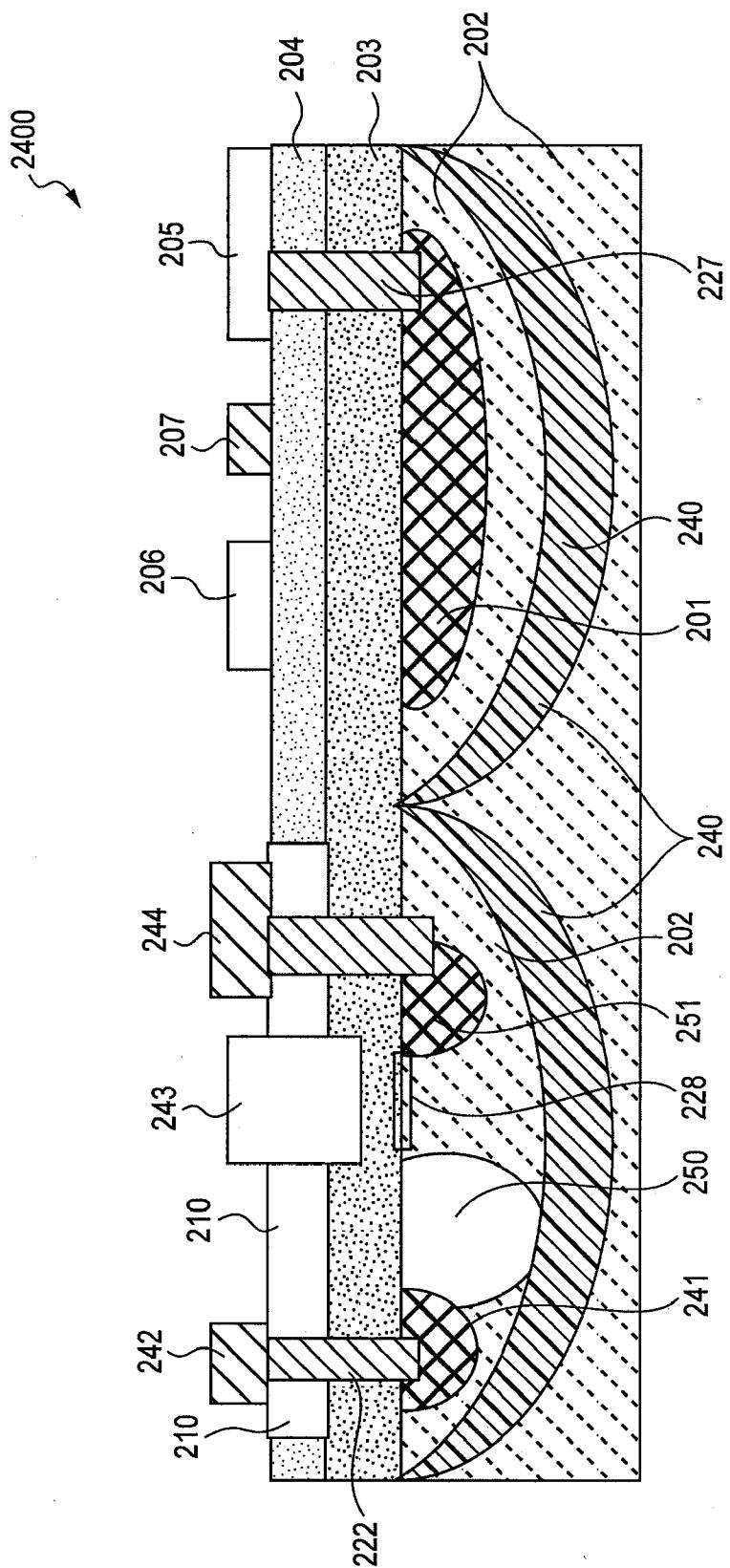


FIG. 24.

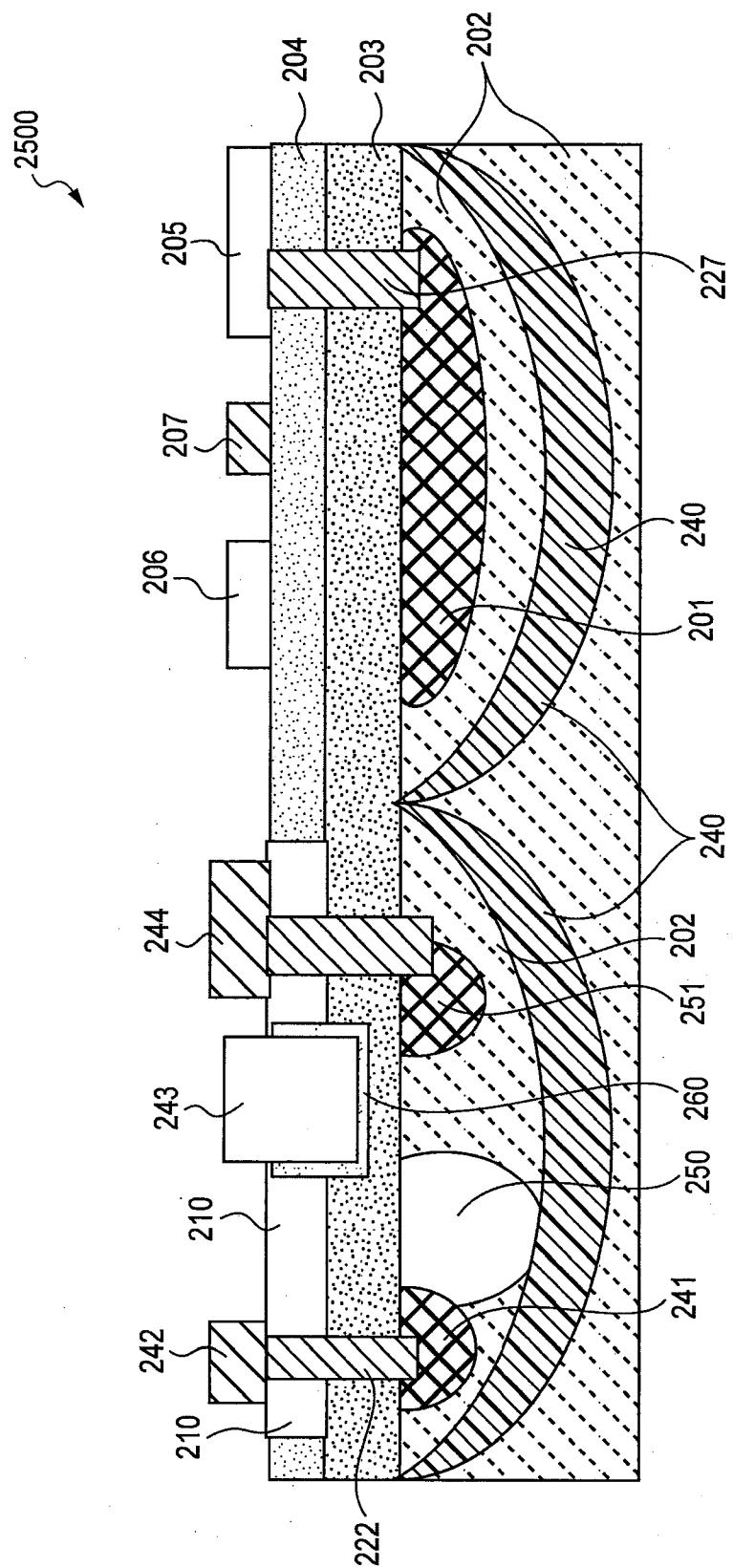


FIG. 25A

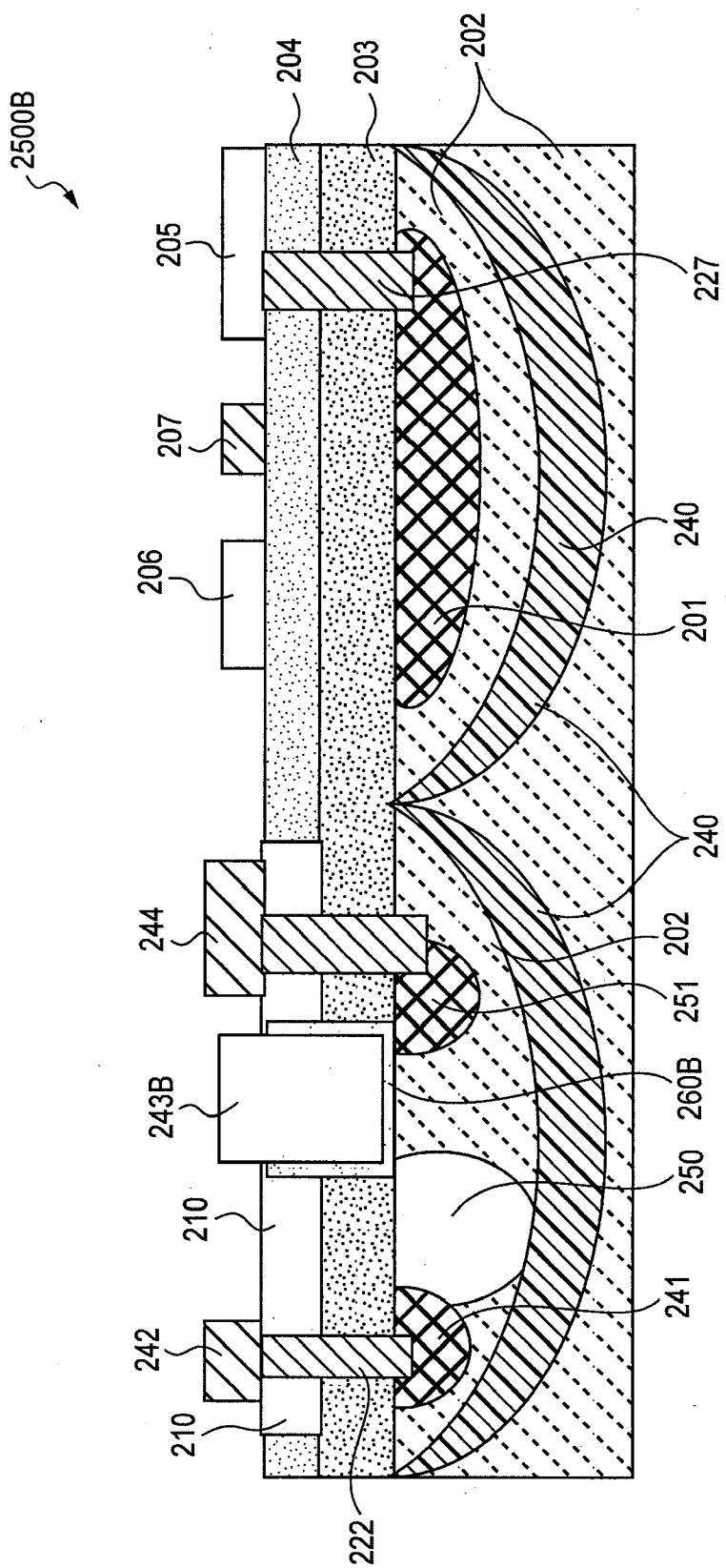


FIG. 25B

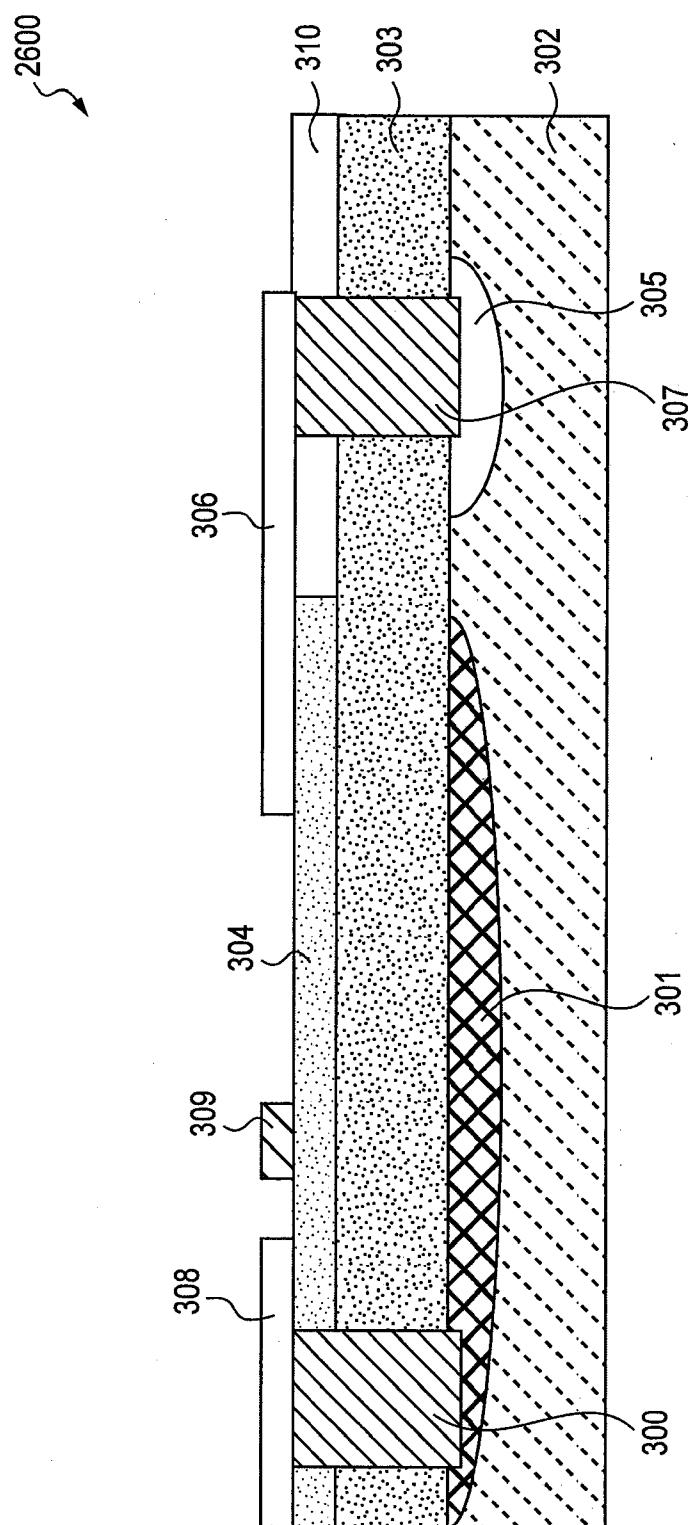


FIG. 26

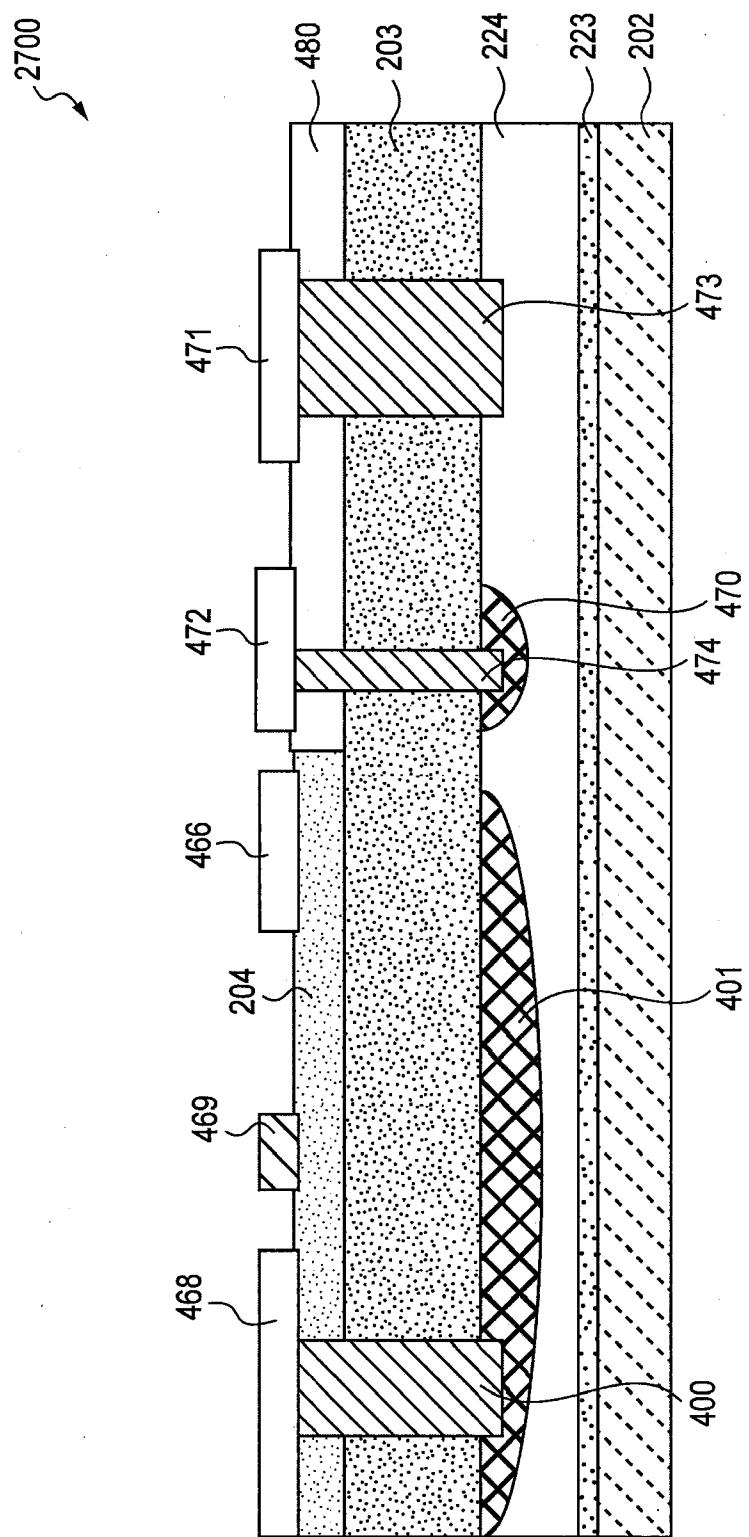


FIG. 27

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2011/064803

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 21/337 (2012.01)

USPC - 438/196

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - H01L 21/336, H01L 21/337; H01L 29/66 (2012.01)

USPC - 257/272; 438/191, 438/196, 438/282

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

MicroPatent, Google Patents, Google Scholar

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/0305470 A1 (ANDERSON et al) 10 December 2009 (10.12.2009) entire document	36-38,40-42,44-45
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Y	US 2008/0272408 A1 (VORA) 06 November 2008 (06.11.2008) entire document	1-35,39,43
Y	US 5,552,622 A (KIMURA) 03 September 1996 (03.09.1996) entire document	1-35,39,43
A	US 6,537,861 B1 (KROELL et al) 25 March 2003 (25.03.2003) entire document	18-19,30
		1-45

Further documents are listed in the continuation of Box C.

\* Special categories of cited documents:

- “A” document defining the general state of the art which is not considered to be of particular relevance
- “E” earlier application or patent but published on or after the international filing date
- “L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- “O” document referring to an oral disclosure, use, exhibition or other means
- “P” document published prior to the international filing date but later than the priority date claimed
- “T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- “X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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05 April 2012

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