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(54) **Method of fabricating MOSFETs**

(57) A method for fabricating an integrated circuit semi-conductor device comprised of an array of MOSFET elements having self-aligned or self-registered connections with conductive interconnect lines involves the formation on a substrate 22 of a thick oxide insulation layer 30 surrounding openings therein for the MOSFET elements. A gate electrode 38 within each opening is utilised to provide self-registered source and drain regions 42, 44 and is then covered on all sides and on its top surface with a dielectric layer. After source-drain diffusions, a relatively thin dielectric protective layer is initially applied to the entire device prior to the application of an upper insulative layer. When oversized windows are etched in the upper insulative layer the protective layer prevents overetching of the gate dielectric layer, thus preventing shorts or leaks between conductive and active areas and providing self-aligned contacts with minimum spacing from adjacent conductive area.

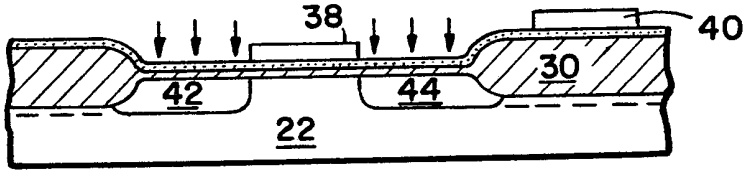

FIG_9a

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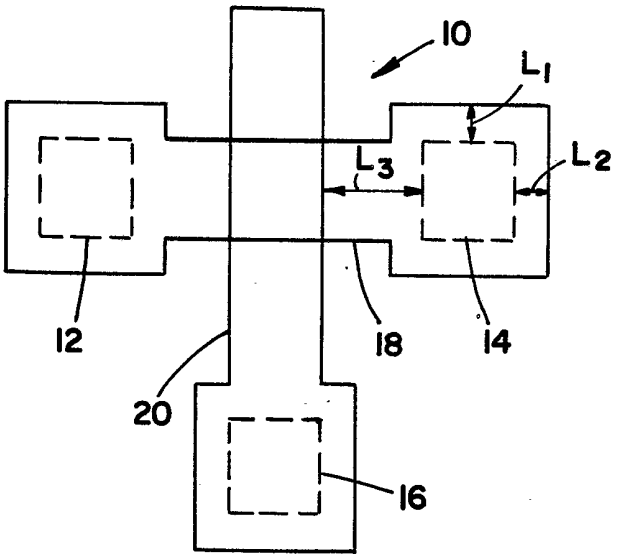

FIG_1

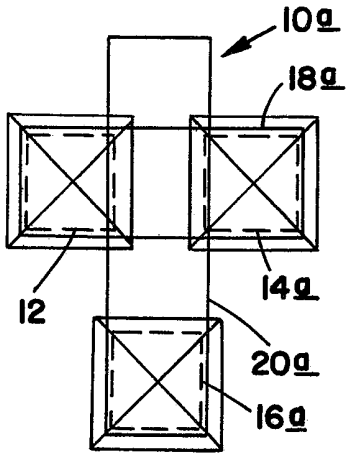

FIG_2

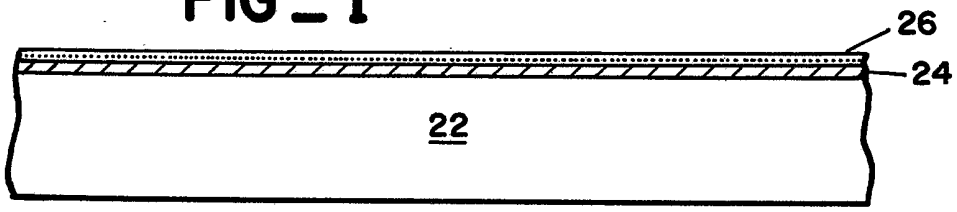

FIG_3a,b

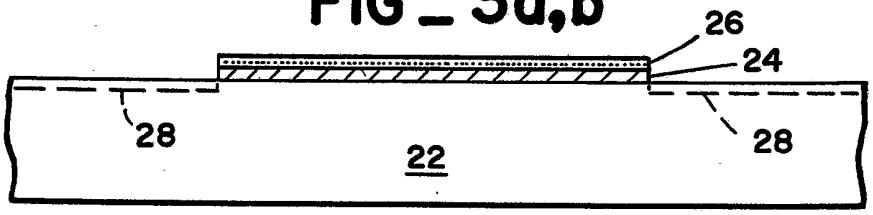

FIG_4a,b

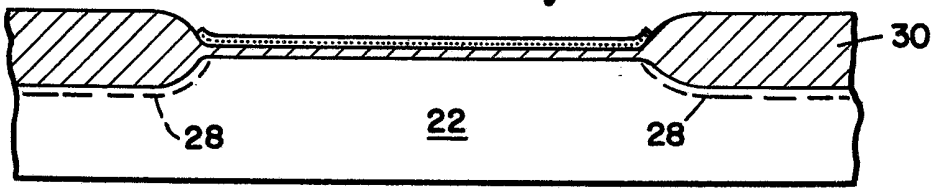

FIG_5a,b

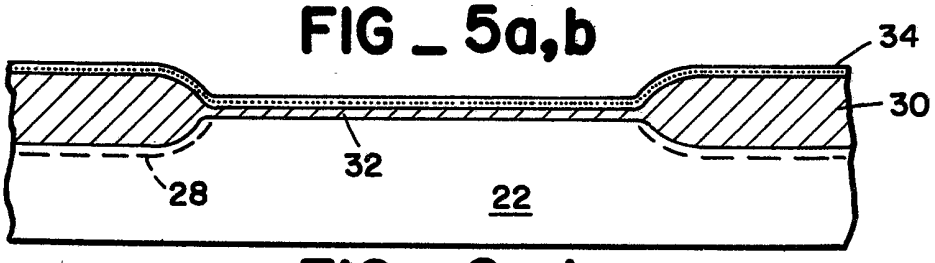

FIG_6a,b

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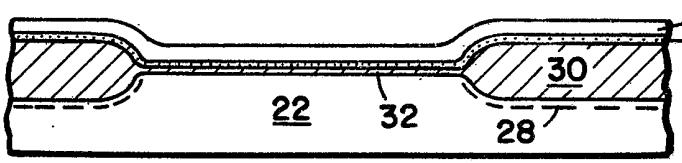

FIG_7a

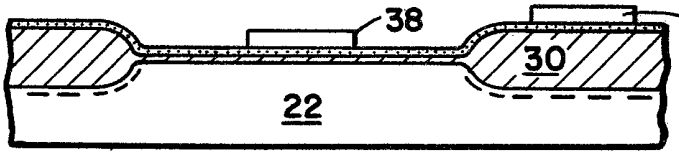

FIG_8a

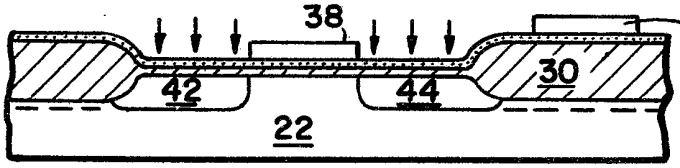

FIG_9a

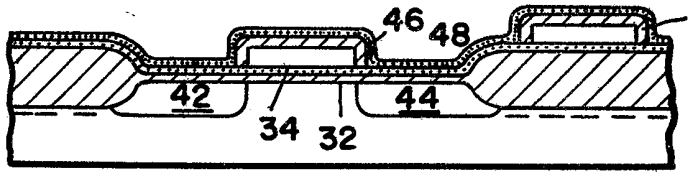

FIG_10a

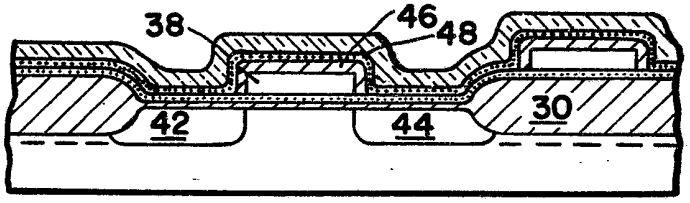

FIG_11a

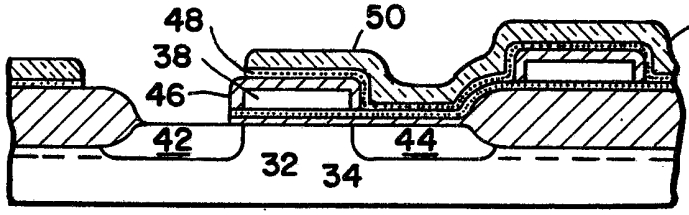

FIG_12a

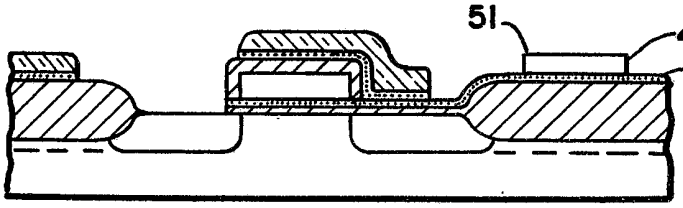

FIG_13a

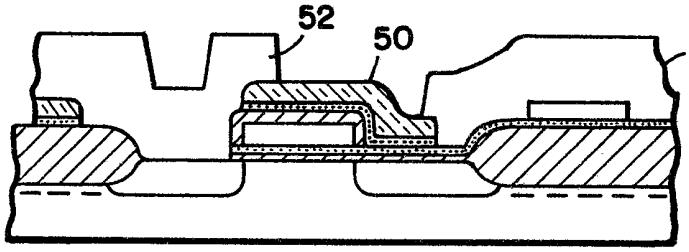

FIG_14a

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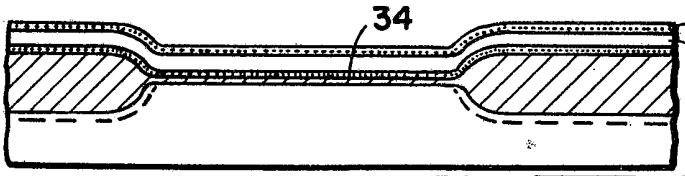

FIG_7b

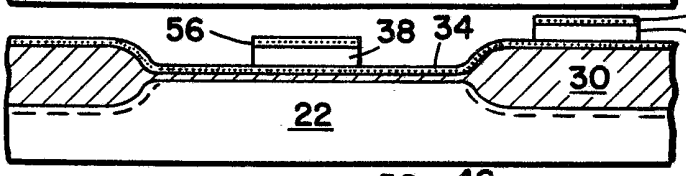

FIG_8b

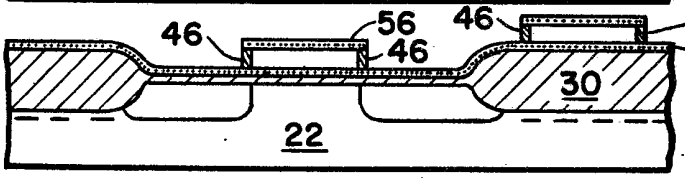

FIG_9b

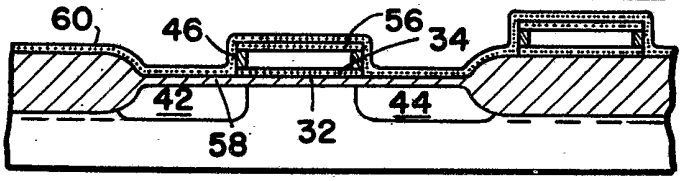

FIG_10b

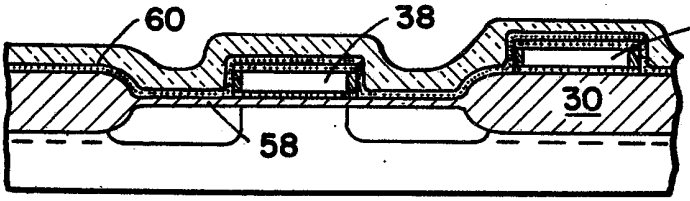

FIG_11b

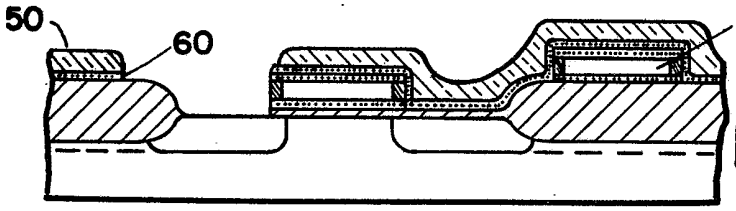

FIG_12b

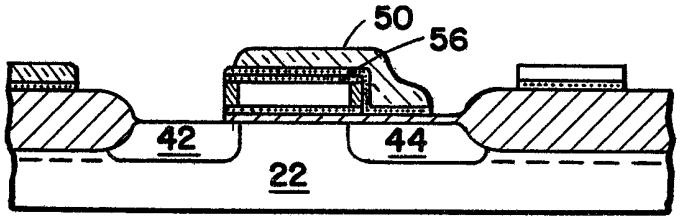

FIG_13b

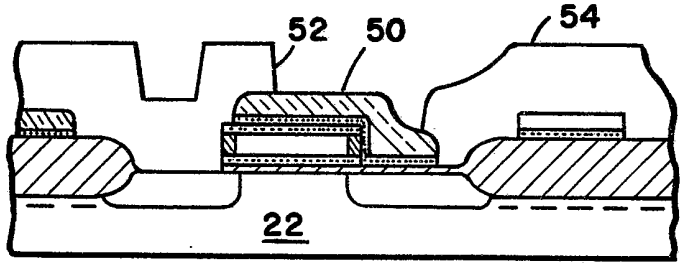

FIG_14b

SPECIFICATION

Improvements in or relating to a method for fabricating an integrated circuit semiconductor.

The present invention relates to integrated circuit semi-conductor devices and more particularly to a method for fabricating such devices with aligned contacts.

Large-scale integrated circuit often having thousands of MOSFET's on a single semiconductor chip must have a multiplicity of contacts to provide the necessary inter-connections between circuit lines, source-drain regions and gate electrodes of individual transistor elements. Using long-established conventional procedures, it was necessary to make the conductive areas oversized and larger contact openings in order to accommodate mask alignment tolerances. This generally resulted in devices requiring a relatively large chip area. With the rapid increase in large-scale integrated circuit devices having even greater numbers of MOSFET elements, efforts have been made to reduce not only the element size but also the size of the required contacts. With the trend toward reduced design tolerances and narrower interconnect lines this became an increasingly severe problem. One suggested solution described in J. Electrochem, Soc. Solid State Science and Technology, Vol. 125, No. 3, March 1978, pp. 471—472, was to provide a gate material of poly crystalline silicon which was coated on its sides and top with a thin silicon dioxide (SiO_2) layer. However, this proved to be unsatisfactory because it failed to eliminate the problem of shorts due to coccasional breakdowns or fractures of the SiO_2 layer during subsequent process steps.

According to one aspect of this invention there is provided a method for fabricating an integrated circuit semiconductor device having a plurality of field effect transistor (FET) elements with self-registering electrical contacts on their source and rain regions and their gate electrodes connected to the device interconnection lines, said method comprising the steps of: providing a doped semiconductive substrate of a first conductive type; providing field oxide regions above or recessed into said substrate surrounding open areas on the substrate surface for each of said FET elements; forming a relatively thin gate dielectric layer within said open areas; forming a gate electrode comprising a layer of conductive material of a predetermined shape and thickness into gate areas over said gate dielectric layer within said open areas; forming a layer of dielectric material on the sides and top of each said gate area of conductive material; forming, within each said open area surrounded by said field oxide doped silicon, source and drain regions of a second conductivity type material opposite to said first conductivity type, the boundaries of said source and drain regions being determined by the edges of said gate areas so that said source and drain regions are self-aligned with respect to the edges of said gate electrode; forming a relatively thin layer of protective dielectric material over substantially the entire surface of the device including all areas of conductive material in said open areas and said field oxide areas; covering said thin layer of protective material on said device with a relatively thick layer of insulating material; etching predetermined oversized access openings through said insulating material over said gate electrode and over said source and drain regions and removing oxide and dielectric material from the surfaces of said source and drain regions and from predetermined portions of said gate electrode; depositing a predetermined metallic-type, high-electrical conductivity interconnection lines pattern extending into said access openings to make electrical connections with said source and drain regions and with said gate electrode.

Preferably said protective layer is silicon nitride formed by vapour deposition to a thickness in the range of 150Å to 300Å, and the upper surface of said silicon nitride protective layer is oxidized before application of said insulating material.

Alternatively said protective layer is silicon carbide or aluminium oxide.

Preferably said gate dielectric layer is a sandwich of silicon nitride over silicon dioxide.

In one embodiment said conductive gate electrodes are poly crystalline silicon covered on all sides and on top with an outer layer of silicon dioxide and said source and drain regions are formed by ion implantation and said silicon dioxide layer on said gate electrodes has a thickness of around 3000Å to 5000Å.

In an alternative embodiment the conductive gate electrodes are poly crystalline silicon whose sides are covered with a layer of silicon dioxide and whose top is covered with a layer of silicon nitride and the thickness of the silicon dioxide layer on the sides of said gate electrode is substantially 3000Å to 5000Å and the thickness of said silicon nitride layer on top thereof is substantially 1000Å to 2000Å. Preferably said source and drain regions for each said FET are formed by a diffusion process.

According to another aspect of this invention there is provided an integrated circuit semiconductor device having an array of field effect transistor (FET) elements each with self-aligned electrical contacts on their source and drain regions and their gate electrodes for connection with the device interconnection lines, said device comprising: a doped semiconductive substrate of a first conductive type; field oxide regions above or recessed into said substrate surrounding open areas on the substrate surface for each of said FET elements; a layer of conductive material of a predetermined shape and thickness forming said gate electrodes within said open areas; a layer of dielectric material on the sides and top of each said gate electrode; doped silicon source and drain regions of second conductivity type material opposite to said first conductivity type on opposite sides of said gate electrode, the boundaries of said source and drain regions being determined by the edges of said

gate electrode; a relatively thin layer of protective dielectric material covering substantially the entire top portion of each said gate electrode; a relatively thick layer of insulating material covering said thin layer of protective material on said device and having oversized access openings located over said gate electrode and over said source and drain regions; and a predetermined metallic-type, high-electrical conductivity interconnection line pattern on said device extending into said access openings to make electrical connections with said self-aligned source and drain regions and with said gate electrode.

It will be appreciated that in performing a method in accordance with the present invention MOSFET elements with self-aligned contacts forming an integrated circuit device may be fabricated in a semiconductor substrate having a first conductivity type by a method wherein a permanent internal protective layer is formed. The preliminary steps of the method utilise conventional fabrication techniques. After the field oxide areas are formed with openings for transistor elements, polysilicon gate areas are provided within the openings. Polysilicon conductive lines are also simultaneously formed on the field close or adjacent to such openings where necessary. Thereafter, contact areas with the minimum dimensions required are formed on opposite sides of each gate area and also where required on the conductive lines. In one version of the present method, all of these poly gates and conductive lines are first provided with a top layer of silicon nitride and thereafter a thin oxide layer on their sides. Source-drain regions then are formed by diffusion technieques and thereafter the thin protective layer of silicon nitride is provided over the entire chip, covering the field oxide areas, the poly silicon areas and the areas surrounding the poly gate areas. Now, a standard layer of phosphorous impregnated glass (PVX) is also applied to the entire chip covering the thin nitride layer, and thereafter a contact mask on the PVX layer is used to form the necessary contact openings by first etching away the PVX in the contact opening regions but stopping at the protective nitride layer. The thick field oxide and the thin oxide layer on the sides of the poly gate areas are prevented from being attacked during this PVX etch by the thin nitride protective layer. Following this, the thin protective nitride layer in the contact areas is etched away by an etchant that will not attack the field oxide and the protective poly oxide. Thereafter, a poly contact mask is used to form contact openings in the PVX layer and the top nitride layer on the poly lines for the contacts on the poly interconnect lines. Both of these latter masks can utilise the relatively large openings to assure registration or self-alignment with the desired contact areas, because the previously applied thin nitride layer provides protection for the field oxide and the poly oxide on the gate areas and assures against circuit shorts between gates, poly lines and N^+ interconnect lines. With this added internal protection the alignment tolerances heretofore required between poly gates, poly lines and contact openings are substantially reduced, yet without requiring unusually close tolerances on the contact masks for forming the contact openings. The presently described method thus greatly reduces the problems of producing integrated circuit devices with more closely packed elements per unit area and yet a higher yield.

In an alternative form of the present method, the poly gates and conductive lines, after being formed, are provided with a thin silicon dioxide layer on their sides and also on their top surface instead of the initial nitride layer. The source-drain regions are then formed by ion implantation techniques with the poly silicon gate serving as a mask in the well-known manner. Thereafter, the thin internal protective nitride layer is applied over the entire chip surface before fabrication is completed. The protective layer again performs its function of preventing internal shorts and any over-etching of the thin oxide layer on the conductive poly gates or poly lines and during the formation of oversized holes in the insulating PVX layer.

In order that the invention may be more readily understood and so that further features thereof may be appreciated the invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a plan view of a typical MOS transistor structure with contacts formed as in the prior art;

Figure 2 is a plan view of an MOS transistor structure formed with self-aligned contacts;

Figures 3*a*—14*b* illustrate the steps for forming self-aligned contacts for a semiconductor device according to the method of the present invention; and

Figures 3*a*—14*b* illustrate the steps for forming self-aligned contacts for a semiconductor device using a somewhat modified method according to the present invention.

With reference to the drawing, Figure 1 illustrates in plan view a conventional MOS transistor 10 of the prior art having non-self-aligned source and drain contacts 12 and 14 and a gate contact 16. Generally accepted design rules for such transistors in a large scale integrated circuit required each contact on a source and drain region 18 and on a gate electrode 20 extending over it to have a minimum area. Because of alignment tolerances in forming such contacts using conventional fabrication procedures, it was necessary for the underlying source-drain region 18 to be considerably larger than the minimum contact area in order to assure proper registration of the contacts. For example, in order to have a minimum required contact area, a uniform tolerance around all sides of the contacts (shown at L_1 and L_2) and predetermined minimum spacing between contact edge and poly silicon edge (L_3) was required using conventional fabrication technology. The design requirements resulted in an MOS semiconductor device as shown in Figure

1 in order to prevent shorts and leakage problems in an integrated circuit comprised of many such MOS devices.

The reduction in chip area that can be accomplished for a single MOS transistor 10*a* with self-aligned contacts is illustrated in Figure 2. Here, the source, drain and gate contacts 12*a*, 14*a* and 16*a*, all having the minimum area, are automatically registered with the borders of their source-drain region 18*a* or the gate electrode 20*a* and the surrounding field oxide. The tolerances L_1, L_2 and L_3 are reduced to zero, and each diffused region 18*a* can have minimum dimensions in width and in length using conventional design rules. Also, because each contact is self-aligned or completely contained on its respective contact area, the spacing from an adjacent conductive line can be minimized, thereby further decreasing the overall chip area required for a semiconductor device.

The more important method steps for making such a semiconductor device with self-aligned contacts according to the present invention will now be described relative to Figures 3*a*—14*a*.

As shown in Figure 3*a*, the method commences with the provision of a semiconductor substate 22 (e.g. <100> plane silicon material) that is doped in a suitable range to provide the desirable characteristics. This substate is covered with an initial oxidation layer 24 of 500—1000Å on which is deposited a second layer 26 of silicon nitride of approximately equal thickness.

Using a field oxide mask, the layers 24 and 26 are removed by etching in the field areas as indicated in Figure 4*a*, and these areas are then field implanted as indicated by the dotted lines 28 to adjust field threshold levels in the conventional manner.

As shown in Figure 5*a*, a relatively thick field oxide 30 is now grown in the field areas, also in the conventional manner. This drives the field implanted areas 28 further into the substate 22 under the oxide areas. In a typical semiconductor structure, the field oxide is configured to form holes or openings within which each MOS transistor is to be formed.

After the field oxide is formed, the original nitride layer 26 and the gate oxide layer 24 are removed by etching. Thereafter, a new gate oxide layer 32 is formed within the hole in the field oxide.

Now, over the entire device surface, including the new oxide layer 32 and the field oxide 30 (as shown in Figure 6*a*), a thin (e.g. 150—300Å) nitride layer 34 is deposited using conventional vapour deposition techniques. In order to ensure stability of the product, the upper surface of this nitride layer is oxidized in a stream of dry oxygen (not shown). The step illustrated in Figure 6*a* provides a new nitride/oxide sandwich, that hasn't undergone the heat treatment which was applied during formation of the field oxide, adjusted to appropriate thicknesses. However, the original oxide/nitride sandwich 24, 26, shown in Figure 3*a*, adjusted to appropriate thicknesses, could be used as the gate dielectric.

In the next step of the method (see Figure 7*a*,) a layer 36 of poly-crystalline silicon (poly) is deposited, by a standard vapour deposition process, onto the entire surface of the chip being fabricated to a typical thickness of around 3000—5000Å.

A mask is then used and portions of the poly are etched away, leaving portions of the poly to define gate electrodes 38 within the active areas formed in the field oxide and interconnect lines 40 situated on top of the field oxide 30 and adjacent to one or more gate elements. At this point, all portions of conductive poly within a field oxide opening and on the field oxide are situated on a nitride/oxide sandwich. Using known silicon gate procedures wherein the gate serves as a mask, ion implantation techniques are employed, as represented by the vertical arrows in Figure 9*a*, to form source and drain regions 42 and 44 just below the substate surface within the field oxide opening and on opposite sides of the polysilicon gate 38.

In the next step, as shown in Figure 10*a*, a layer 46 of silicon-dioxide is grown on all sides and also on the top of all conductive poly areas including the gate poly areas 38 and the adjacent poly interconnect lines 40. The thickness of this covering layer on the poly is generally much greater than that of the gate oxide 32 (e.g. around 3000Å), and its purpose is to provide a protective layer on the poly for making the self-aligned contact structure.

In the next step, as also shown in Figure 10*a*, a thin protective nitride layer 48 is deposited over the entire structure including the field areas 30, the source and drain areas 42 and 44 and the areas 38 and 40 of oxide covered poly. This nitride layer will later serve to provide protection for field oxide and poly oxide during subsequent process steps. Following this application of the thin nitride layer the entire chip, as shown in Figure 11*a*, is covered with a relatively thick layer 50 of phospho-silicate glass (PVX) in the conventional manner.

Now, as shown in Figure 12*a*, a first mask (not shown) for the N^+ contacts is applied to the PVX and a suitable etchant (e.g. buffered hydrofluoric acid) is used to etch away the PVX layer 50 and the nitride/oxide sandwich 32, 34 in the contact area. Thereafter, a second contact mask is applied to the chip in the same manner as the first mask and etchant is used to etch away the PVX, nitride and the oxide on the polysilicon lines. These latter two masks for the N^+ and polysilicon contacts may be applied in reverse order, if desired. This leaves the chip, as shown in Figure 13*a*, with the PVX layer 50 coincident with the thin nitride layer 48 having windows to expose the drain contact area 42 and also an exposed contact area 51 on the adjacent poly interconnect line 40 having no oxide covering.

At this point, standard fabrication method steps can be used to deposit metal in the contact areas to define metal contacts 52 and 54 as part of a

desired metal interconnect pattern on the semiconductor device. Generally, these metallization steps include the evaporation of metal and definition thereof with an appropriate metal mask and thereafter the application of a top protection dielectric layer over the entire chip (not shown) for passivation.

In this modified version of method according to the present invention, illustrated by Figures 3*b*—14*b*, the initial steps of figures 3*b*—6*b*, inclusive are identical to those of Figures 3*a*—6*a*. However, this modified version avoids the necessity for using ion implantation equipment and procedures for forming the source and drain regions.

Thus, as shown in Figure 7*b*, a poly layer 36 having a typical thickness in the range of 3000—5000Å is formed on the chip over the gate nitride layer 34 by conventional chemical vapour deposition techniques. This poly layer is then doped by diffusing phosphorous into it to make it more conductive. Thereafter, a nitride layer 56 having a thickness that is considerably greater than that of the gate nitride layer 34 (e.g. 1000—2000Å) is deposited on the polysilicon layer 36.

As shown in figure 8*b*, the polysilicon layer 36 is defined into gate areas and interconnect lines by using a poly mask (not shown) and standard etching techniques which removes the unwanted material in the poly and nitride layers. This leaves the structure with a doped polysilicon gate or electrode 38 within an area surrounded by field oxide 30 and an adjacent poly interconnect line 40 situated on the oxide, both of these poly elements having the nitride layer 56 on their top surfaces.

In the next step, shown in Figure 9*b*, the poly gate elements and the poly interconnect lines 40 are provided with an oxide layer 46 on their sides having a thickness of around 3000Å. This is accomplished by simple thermal oxidation in a chamber in accordance with well-known procedures.

Now, as shown in Figure 10*b*, the source and drain regions 42 and 44 are formed by diffusion techniques. First, the gate nitride layer 34 is etched away from every surface except the tops of the poly layers. Then, the gate oxide layer 32 is etched in all the area surrounding the gate poly layer. Standard diffusion procedures are now applied to form the source and drain regions 42 and 44. Following this, a new thin oxide layer 58 is formed in the diffused regions, to a thickness of around 500Å.

As shown in Figure 10*b*, a think protective nitride layer 60 (e.g. 150—300Å) is applied to the structure. This layer 60 is thus much thinner than the nitride layer 56, and as with the previous embodiment, layer 60 extends over the entire chip including the field areas 30, the source and drain areas and the nitride covered gate 38 and line poly areas 40.

Now, the PVX layer 50 is applied and etched, using contact masks in the same manner as previously described with respect to the first embodiment of the method. Also with oversized contact holes formed in the PVX layer as previously described, the metallization of the MOS elements on the chip is performed to form its metal contacts 52 and 54 with accompanying interconnect lines in the standard manner.

By utilisation of either of the above described methods is it possible to produce large-scale semi-conductor devices with a multiplicity of MOSFET elements having self-aligned contacts and therefore requiring a minimum of chip area in a closely-packed array. For example, in a typical random access memory (RAM) the area required for a single memory cell was 1344 square microns, whereas, with the self-aligned contacts made possible using one of the above described methods, the same memory cell has an area of only 950 square microns, reduction in area of approximately 30%. Yet, the above described methods, the yield of such closely-packed devices with self-aligned contacts can be even higher than with prior conventional devices because the internal protective nitride layers 48 and 60 maintain circuit integrity during critical process steps by preventing shorts or failures heretofore caused during the various process steps. Whilst silicon nitride is a preferred material for the protective layers, other materials could be used such as silicon carbide of aluminium oxide.

CLAIMS

1. A method for fabricating an integrated circuit semiconductor device having a plurality of field effect transistor (FET) elements with self-registering electrical contacts on their source and drain regions and their gate electrodes connected to the device interconnection lines, said method comprising the steps of: providing a doped semiconductive substrate of a first conductive type; providing field oxide regions above or recessed into said substate surrounding open areas on the substrate surface for each of said FET elements; forming a relatively thin gate dielectric layer within said open areas; forming a gate electrode comprising a layer of conductive material of a predetermined shape and thickness into gate areas over said gate dielectric layer within said open areas; forming a layer of dielectric material on the sides and top of each said gate area of conductive material; forming, within each said open area surrounded by said field oxide doped silicon, source and drain regions of a second conductivity type material opposite to said first conductivity type, the boundaries of said source and drain regions being determined by the edges of said gate areas so that said source and drain regions are self-aligned with respect to the edges of said gate electrode; forming a relatively thin layer of protective dielectric material over substantially the entire surface of the device including all areas of conductive material in said open areas and said field oxide areas; covering said thin layer of protective material on said device with a relatively thick layer of insulating material; etching predetermined oversized access openings through said insulating material over said gate

electrode and over said source and drain regions and removing oxide and dielectric material from the surfaces of said source and drain regions and from predetermined portions of said gate electrode; depositing a predetermined metallic-type, high-electrical conductivity interconnection lines pattern extending into said access openings to make electrical connections with said source and drain regions and with said gate electrode.

2. A method as claimed in claim 1 wherein said protective layer is silicon nitride formed by vapour deposition to a thickness in the range of 150Å to 300Å.

3. A method as claimed in claim 2 wherein the upper surface of said silicon nitride protective layer is oxidized before application of said insulating material.

4. A method as claimed in claim 1 wherein said protective layer is silicon carbide.

5. A method as claimed in claim 1 wherein said protective layer is aluminium oxide.

6. A method as claimed in any one of the preceding claims wherein said gate dielectric layer is a sandwich of silicon nitride over silicon dioxide.

7. A method as claimed in any one of the preceding claims wherein said conductive gate electrodes are poly crystalline silicon covered on all sides and on top with an outer layer of silicon dioxide.

8. A method as claimed in claim 7 wherein said source and drain regions are formed by ion implantation.

9. A method as claimed in claim 7 or 8 wherein said silicon dioxide layer on said gate electrodes has a thickness of around 3000Å to 5000Å.

10. A method as claimed in any one of claims 1 to 6 wherein the conductive gate electrodes are poly crystalline silicon whose sides are covered with a layer of silicon dioxide and whose top is covered with a layer of silicon nitride.

11. A method as claimed in claim 10 wherein the thickness of the silicon dioxide layer on the sides of said gate electrode is substantially 3000Å to 5000Å and the thickness of said silicon nitride layer on top thereof is substantially 1000Å to 2000Å.

12. A method as claimed in claim 10 wherein said source and drain regions for each said FET are formed by a diffusion process.

13. A semiconductor device whenever fabricated by a method according to any one of claims 1 to 12.

14. An integrated circuit semiconductor device having an array of field effect transistor (FET) elements each with self-aligned electrical contacts on their source and drain regions and their gate electrodes for connection with the device interconnection lines, said device comprising: a doped semiconductive substrate of a first conductive type; field oxide regions above or recessed into said substrate surrounding open area on the substrate surface for each of said FET elements; a layer of conductive material of a predetermined shape and thickness forming said gate electrodes within said open areas; a layer of dielectric material on the sides and top of each said gate electrode; doped silicon source and drain regions of second conductivity type material opposite to said first conductivity type on opposite sides of said gate electrode, the boundaries of said source and drain regions being determined by the edges of said gate electrode; a relatively thin layer of protective dielectric material covering substantially the entire top portion of each said gate electrode; a relatively thick layer of insulating material covering said thin layer of protective material on said device and having oversized access openings located over said gate electrode and over said source and drain regions; and a predetermined metallic-type, high-electrical conductivity inter-connection line pattern on said device extending into said access openings to make electrical connections with said self-aligned source and drain regions and with said gate electrode.

15. A semiconductor device as claimed in claim 14, wherein said internal protective layer is silicon nitride having a thickness in the range of 150Å to 300Å.

16. A method for fabricating an integrated circuit semiconductor substantially as herein described with reference to Figures 2 and 3*a* to 14*a* of the accompanying drawings.

17. A method for fabricating an integrated circuit semiconductor substantially as herein described with reference to Figures 2 and 3*b* to 14*b* of the accompanying drawings.

18. An integrated circuit semiconductor whenever made by the method of claim 16.

19. An integrated circuit semiconductor whenever made by the method of claim 17.

20. An integrated circuit semiconductor substantially as herein described with reference to and as shown in Figures 2 and 3*a* to 14*a* of the accompanying drawings.

21. An integrated circuit semiconductor substantially as herein described with reference to and as shown in Figures 2 and 3*b* to 14*b* of the accompanying drawings.

22. Any novel feature or combination of features disclosed herein.

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