

May 14, 1968

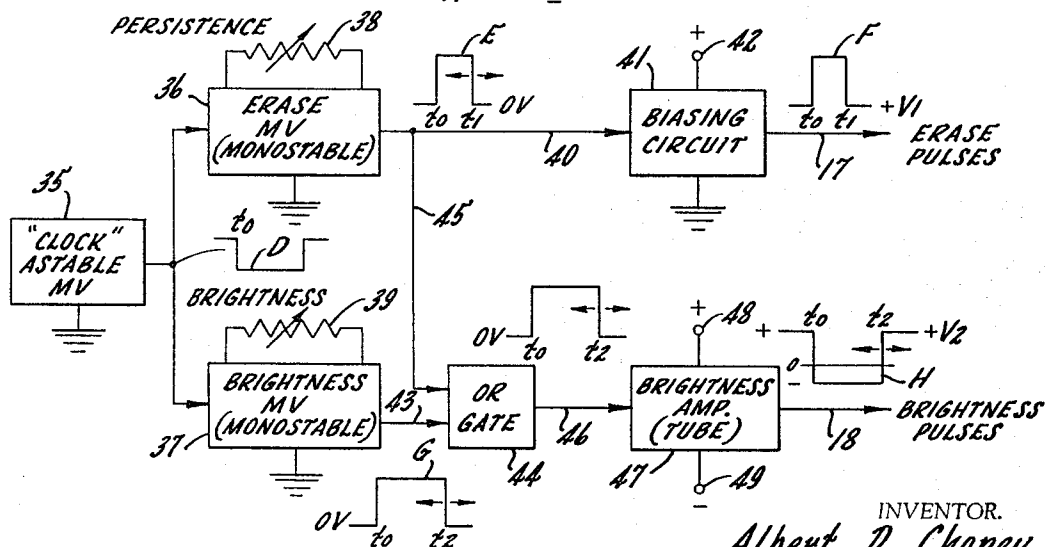
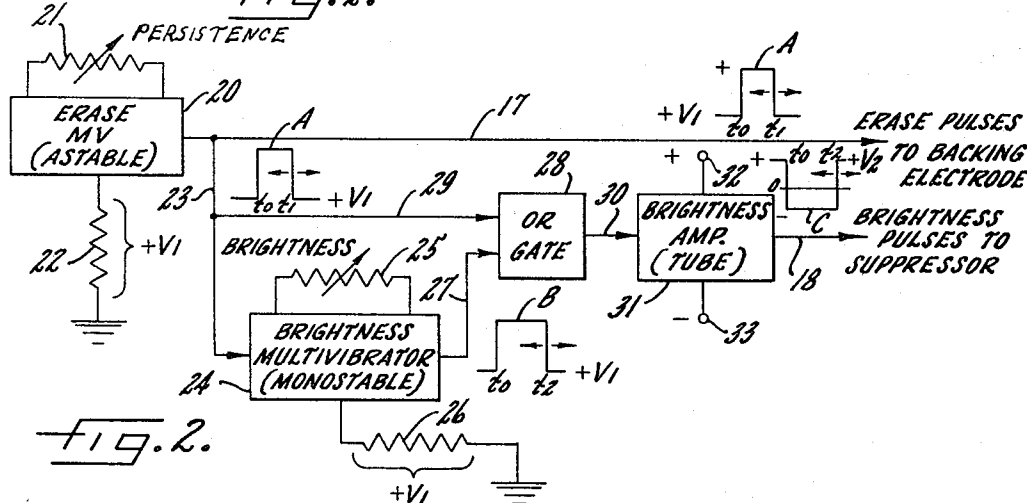
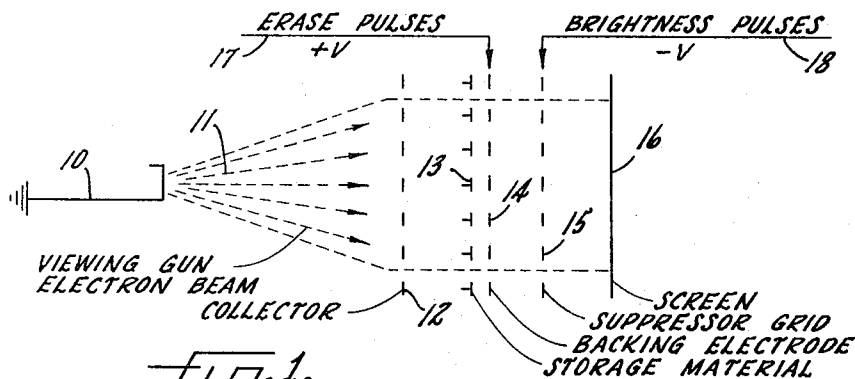
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3,383,546

BRIGHTNESS CONTROL CIRCUITRY FOR DIRECT VIEW STORAGE TUBES

Filed Jan. 15, 1965

2 Sheets-Sheet 1



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2 Sheets-Sheet 2

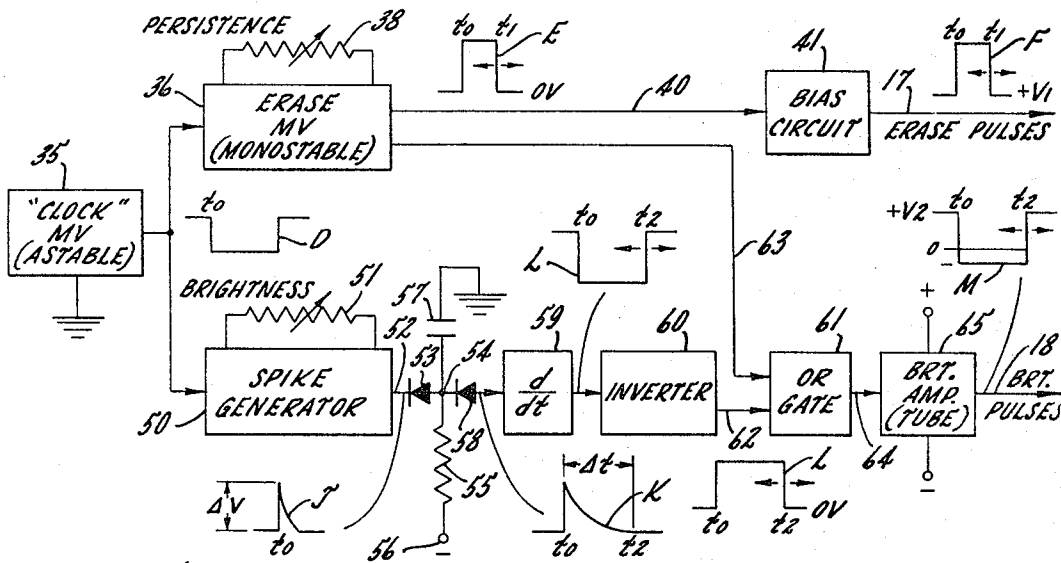


Fig. 4.

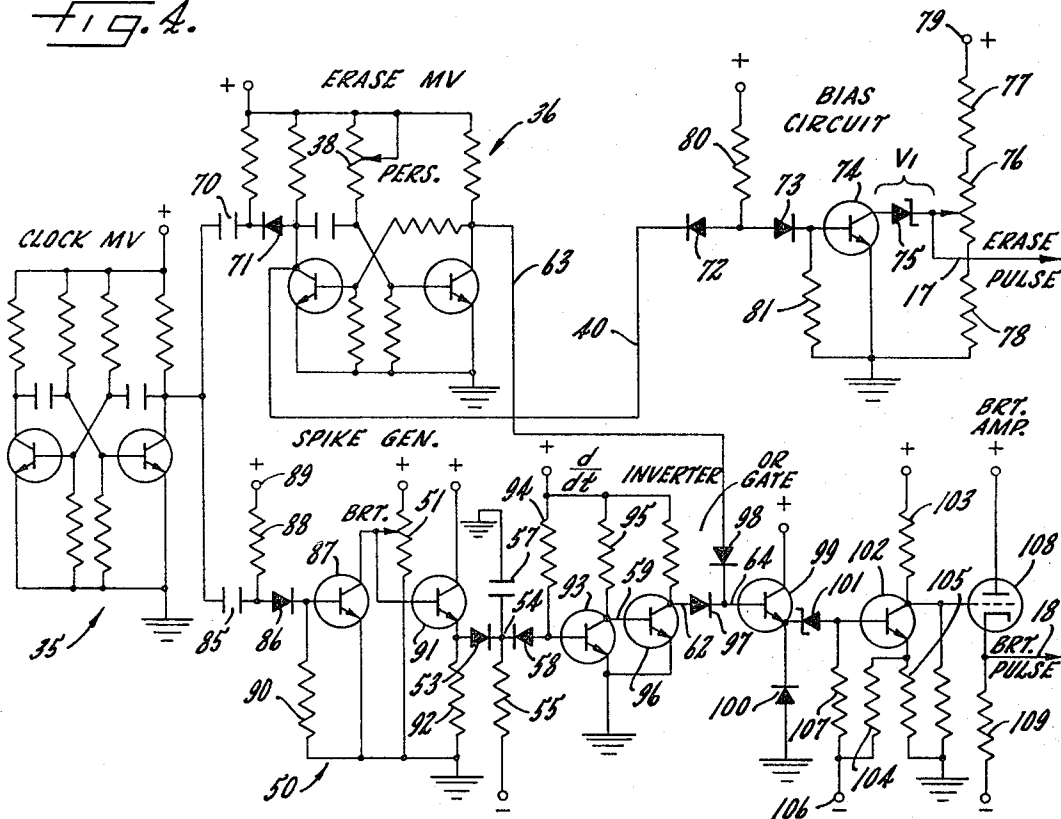


Fig. 5.

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## BRIGHTNESS CONTROL CIRCUITRY FOR DIRECT VIEW STORAGE TUBES

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4 Claims. (Cl. 315-12)

### ABSTRACT OF THE DISCLOSURE

A brightness control circuit for direct view storage tubes having parallel channels, one channel to develop erase pulses for the backing electrode of the storage tube and the other channel to develop brightness pulses, coincident in initial time and longer in duration than the erase pulses, for the suppressor grid of the storage tube to minimize the flashing effects of the erase pulses. The two channels have a common triggering pulse source and the channel developing the brightness pulse has a brightness pulse generator, the output of which is through an "OR" gate, together with the erase pulses, and through a brightness pulse amplifier to the suppressor grid to insure brightness pulse application although a brightness pulse fails to develop in its channel.

### Background of the invention

This invention relates to circuitry for controlling display intensity of direct view storage tubes (DVST) and more particularly to circuitry for producing voltage pulses coincident in time with erase pulses, and of opposite polarity and greater duration than the erase pulses, for application to the suppressor grid of the DVST to minimize or eliminate the flashing effects of the erase pulses.

Recent development in the storage tube industry has led to the addition of a suppressor grid in some DVST models. This new grid is located in the viewing or flooding gun system of the tube and is placed between the backing electrode to which the erase pulses are applied and the phosphorescent screen. By varying the direct current (D.C.) voltage applied to this suppressor grid, it is possible to control the flow of electrons striking the screen or the display of target information where the DVST is used in a radar system. The intensity or brightness of the display can be controlled by applying pulses to the suppressor grid and varying their duty cycle.

Operation of any DVST requires pulsing the backing electrode with "erase pulses." These pulses erase stored information in the form of charges on the storage surface adjacent to the backing electrode. Here again, duty cycle variation is used and determines display persistence. Erase pulses are normally in the form of positive pulses. Through electrostatic charging these pulses result in the addition of electrons to the storage surface which in turn nullify positively charged areas of information previously written by the DVST writing guns. In DVST's, which do not contain a suppressor grid, or which do contain suppressor grids of fixed bias, this positive pulsing of the backing electrode causes bursts of electrons to hit the phosphorescent screen. The result is a flashing display. Due to the duty cycle and frequency of the erase pulses the flashing manifests itself in a display with a bright background since the eye cannot resolve the individual flashes but rather averages the overall intensity level. Taking advantage of the suppressor grid in the newer DVST models and pulsing the suppressor grid in proper phase relation with the backing electrode by erase pulses, this flashing display can be minimized or controlled.

### Summary of the invention

In the present invention the pulse source which produces the erase pulses on the backing electrode of the DVST is utilized in a second channel for developing a brightness pulse coincident in time with the leading edge of the erase pulse but opposite in polarity and of equal or greater pulse width for application to the suppressor grid of the DVST. The erase pulses are ordinarily generated by an astable multivibrator having an adjustable pulse width control means therein to vary the duty cycle of the pulses which will control the DVST persistence on the display screen. This same astable multivibrator pulse source is applied to a monostable multivibrator having adjustable means therein to vary the duty cycle of the output brightness pulses produced thereby which will control the brightness of the DVST fluorescent screen upon the application of these pulses to the suppressor grid. The erase pulses and brightness pulses are coupled to the suppressor grid through an "OR" gate so that a brightness pulse will be applied to the suppressor grid even though the brightness monostable multivibrator fails to produce a brightness pulse. In both channels of the erase pulses and the brightness pulses, biasing circuitry is provided and inverters are provided, where necessary, to produce the brightness pulse on the suppressor grid of the DVST in an opposite polarity or phase relation with that of the erase pulse and of at least equal or greater pulse width than the erase pulse to eliminate the flashing effects produced by the erase pulse alone on the fluorescent screen of the DVST. It is therefore a general object of this invention to provide circuitry in conjunction with the erase pulse circuitry of a DVST having a suppressor grid which will minimize or eliminate the flashing effects produced by erased pulses on the DVST fluorescent screen.

### Brief description of the drawing

These and other objects and the attendant advantages, features, and uses of this invention will become more apparent to those skilled in the art as a more detailed description proceeds herein taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a simplified illustration of the gun, grids, and fluorescent screen of a DVST having a suppressor grid;

FIGURE 2 is a block schematic diagram of one embodiment of the invention;

FIGURE 3 is a block schematic diagram of a second embodiment of the invention;

FIGURE 4 is a block schematic and partially circuit schematic of a third embodiment of the invention; and

FIGURE 5 is a circuit schematic of the embodiment shown in FIGURE 4.

### Description of the preferred embodiments

Referring more particularly to FIGURE 1 where a simplified illustration is shown of a DVST, the gun portion is illustrated only by the cathode 10 producing viewing gun electron beams 11 toward a collector 12, a storage surface 13, a backing electrode 14, a suppressor grid 15, and a phosphorescent screen 16. As well understood by those skilled in the art of DVST's, the erase pulses are applied to the backing electrode, herein shown as being applied by the conductor means 17. In accordance with this invention, brightness pulses are used to eliminate the flashing effects on the fluorescent screen 16 caused by the application of erase pulses over conductor means 17. These brightness pulses are applied to the suppressor grid by way of the conductor means 18. The application of negative voltage brightness pulses by way of conductor 18, as will be disclosed below, will compensate for the

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positive voltage erase pulses applied by way of conductor means 17.

Referring more particularly to FIGURE 2, there is illustrated in block circuit schematic one means of developing negative voltage brightness pulses for the suppressor grid coincident with positive erase pulses for application to the backing electrode of the DVST shown in FIGURE 1. In this embodiment erase pulses are produced by an astable multivibrator 20 having variable resistance adjustable means 21 for varying the trailing edge of an output pulse identified by pulse A with trailing edge  $t_1$  at a voltage level V1 fixed by the bias of resistor 22. The erase pulse A will be conducted by the conductor means 17 to the backing electrode 14 of the DVST. This erase pulse A is likewise conducted by means of conductor 23 to a monostable multivibrator 24, referred to herein and in the drawings as the brightness multivibrator. The brightness multivibrator 24 has a variable resistance means 25 as a brightness control which varies the pulse width or the trailing edge, identified as  $t_2$  of the generated pulse B on the output thereof, and a fixed resistor 26 provides the bias on the output pulse, identified in FIGURE 2 as V1 voltage, corresponding to the voltage bias by the resistor 22 for the erase multivibrator 20. The output pulses B of the brightness multivibrator 24 are conducted by way of the output conductor 27 to an "OR" gate 28 to which is also applied the erase pulses by way of the branch conductor 23 and a branch conductor 29. The output of the "OR" gate 28 is applied by way of conductor means 30 to a brightness amplifier tube circuit 31 to produce the amplified brightness pulses C on the output conductor 18 which is coupled to the suppressor grid 15 of the DVST. The brightness amplifier tube circuit 31 has biasing voltages applied at terminals 32 and 33 to establish the +V2 voltage on the output pulse C. A tube is used in the brightness amplifier 31 to isolate the above-described circuitry from any arcs which may occur within the DVST thereby protecting this circuitry, which is preferably circuitry utilizing transistors to provide a compact and light weight package.

In the operation of FIGURE 1, the generation of erase pulses A by the astable multivibrator 20 will cause the brightness multivibrator 24 to generate similar pulses B for the suppressor grid 15 of the DVST. Since the brightness multivibrator 24 is triggered by the leading edge of the erase pulses A from the erase multivibrator 20, the erase pulses A and brightness pulses C are coincident in time, represented by  $t_0$ , for application to the backing electrode and suppressor grid, respectively. The control means 21 and 25 are adjustable to control the pulse width of A and the pulse width of C and, consequently, their duty cycles. The pulse width of C should always be at a time  $t_1$  or greater, herein shown to be  $t_2$ , to fully compensate or eliminate flashing of the DVST fluorescent screen by the erase pulses A.

Referring more particularly to FIGURE 3, an astable multivibrator or other equivalent clock pulse source 35 produces pulses D in common to an erase monostable multivibrator 36 and a brightness monostable multivibrator 37 in each of two channels to the backing electrode 14 and suppressor grid 15 of the DVST by way of conductor means 17 and 18, respectively. The erase pulse multivibrator 36 has a persistence variable resistance control means 38 while the brightness multivibrator 37 has a brightness variable resistor control means 39. The erase multivibrator 36 utilizes the leading edge  $t_0$  of the clock pulse D to generate the erase pulse E on its output conductor 40. Conductor 40 has a biasing circuit network 41 coupled thereto from a positive voltage source 42 and ground to bias the erase pulse F on the output conductor 17 at a voltage V1. The brightness multivibrator 37 produces the brightness pulse G on the output conductor 43 which is applied to an "OR" gate 44 together with the erase pulse E by way of the branch conductor 45 from the erase multivibrator 36. Here again, as in FIGURE 2,

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the "OR" gate 44 insures that a brightness pulse will exist at all times that an erase pulse is generated. The brightness pulse G is conducted through the "OR" gate 44 over the output conductor 45 through a brightness amplifier tube circuit 47 which includes bias networks from the positive voltage source 48 and the negative voltage source 49 to establish the brightness pulse H over the output conductor 18 at the desired voltage level V2. In like manner, the erase pulse F and the brightness pulse H will be conducted respectively over the output conductors 17 and 18 to the backing electrode 14 and suppressor grid 15, respectively, as in the case of the operation of FIGURE 2. As in FIGURE 1, the time duration of the brightness pulse H,  $t_0$  to  $t_2$ , should never be less than the time interval of the erase pulse F from  $t_0$  to  $t_1$  to eliminate the flashing effects caused by the erase pulse in the DVST. Since the adjusting means 38 is capable of adjusting the time  $t_0$  to  $t_1$  for the erase pulse F, or tube persistence on the screen of the DVST, and since the brightness on the screen 16 of the DVST is adjustable by the control means 39 to adjust the time interval  $t_0$  to  $t_2$  on the brightness pulse H, these two adjustments 38 and 39 are variable to obtain the optimum persistence and brightness results from the DVST shown in FIGURE 1.

Referring more particularly to FIGURE 4 where like reference characters refer to like parts in other figures, the astable multivibrator or clock pulse source 35 applies pulses to the erase multivibrator 36 to generate the erase pulses E over the output conductor 40 and through biasing circuitry 41 to establish the erase pulses F at the desired voltage level V1 in the same manner as shown in FIGURE 3. In this embodiment the clock pulses D also will be applied to a spike generator 50 having a brightness control 51 connected therewith to produce spike voltages J which is varied in amplitude  $\Delta V$  by the brightness control 51. The output of the spike generator 50 is applied over the conductor means 52 through a diode 53 to a terminal 54 to which is coupled a resistor 55 in series to a negative voltage source 56. Terminal 54 is also coupled to one plate of capacitor 57, the opposite plate of which is grounded. The network including the resistor 55 and capacitor 57 constitutes a charging network which stretches the spike J in time  $t_0$  to  $t_2$  proportional to the amplitude of  $\Delta V$  voltage. This stretched voltage waveform K, is conducted through a diode 58 to a differentiating network 59 which produces a square wave L on its output coextensive with  $\Delta t$  or in time relation  $t_0$  to  $t_2$  corresponding with that of the waveform K. The differentiating output 59 is coupled through an inverter 60 to an "OR" gate 61 by the conductor means 62, a second input to the "OR" gate 61 being the erase pulse E over the conductor 63 from the erase multivibrator 36. Here again the "OR" gate 61 is used to insure that a brightness pulse will pass to the output 64 whenever an erase pulse E is generated. The brightness pulse L is applied to a brightness amplifier tube circuit and biasing network 65 to produce on its output 18 the brightness pulse M at the desired voltage level V2. As in the prior FIGURES 2 and 3, the erase pulse F and brightness pulse M are generated and applied to the backing electrode 14 and suppressor grid 15, respectively, of the DVST of a pulse width and bias to minimize or eliminate flashing on the fluorescent screen 16 normally caused by the erase pulses. If it is desirable to change the duty cycle of the erase pulse F, it is only necessary to adjust the persistence control 38, whereas, if it is necessary to change the duty cycle of the brightness pulse M, it is only necessary to adjust the brightness control 51. The brightness control 51 varies the  $\Delta V$  amplitude which would vary  $\Delta t$  in the waveform K and thus control time  $t_2$  of the brightness of pulses L and M. As stated hereinbefore, the pulse width  $t_0$  to  $t_2$  of the brightness pulse M should always be equal to  $t_0$  to  $t_1$  or greater for good results of eliminating flashing on the fluorescent screen 16 of the DVST by the erase pulse F.

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Referring more particularly to FIGURE 5, which illustrates a preferred circuit schematic diagram of the block circuit shown in FIGURE 4, the clock pulse multivibrator 35 is herein illustrated as being an astable multivibrator utilizing two transistors, as well understood by those skilled in the art and, accordingly, will not be explained or described in detail. The clock pulses D are applied through a coupling capacitor 70 and a diode 71 to the erase multivibrator 36. The multivibrator 36 is monostable, its stable condition being while the right transistor is conducting to produce a zero voltage on the output conductor 63. When the negative clock pulse D is applied to the multivibrator 36, this negative clock pulse on the base of the right transistor renders it non-conductive and the left transistor conductive to produce a negative erase pulse E on the output 40 and a positive erase pulse E on the output 63. The duration of the erase pulse E is determined by the adjustment on the persistence control means 38 to vary the RC constant for recovery of the monostable multivibrator 36 from a condition of left transistor conduction back to right transistor conduction, as well understood by those skilled in the multivibrator art. The output from the collector of the left erase multivibrator transistor is a negative pulse that is conducted through the diodes 72 and 73 to the base of a transistor 74 which inverts the negative pulse to that of the erase pulse F, shown in FIGURE 4. The collector output is applied through a Zener diode 75 to the adjustable tap of a potentiometer 76 having the resistance element in series with resistors 77 and 78 from a positive voltage source 79 and ground. Input bias established on the base of transistor 74 is established by the resistors 80 and 81. The Zener diode 75 establishes the V<sub>I</sub> voltage level for the erase pulse F. The output conductor 17 is coupled directly to the movable tap of potentiometer 76.

Clock pulses D are also applied through a coupling capacitor 85 and a diode 86 to the base of a transistor 87 in the spike generator 50. The biases on the anode of the diode 86 and the base of transistor 87 are established by a resistor 88 from a voltage source 89 and by a resistor 90 coupled to ground. The collector of the transistor 87 is coupled to the adjustable tap of the potentiometer brightness control 51, the resistance element of which is coupled between a positive voltage source and ground. The brightness control adjustable tap is coupled directly to the base of a transistor 91 having its collector coupled directly to a positive voltage source and its emitter coupled through an emitter load resistor 92 to ground. The coupling capacitor 85 and biasing resistor 88 coupled to the diode 86 render only the leading edge of the clock pulses D effective to produce the spike voltage J which reaches an amplitude directly proportional to the brightness control 51 voltage setting. This spike voltage J is taken from the emitter of transistor 91 and applied through the diode 53 to the terminal 54 in the network 55, 57 to produce a sawtooth voltage K proportional to the amplitude of the spike voltage J. This sawtooth voltage K is applied through the diode 58 to the base of a transistor 93 operating as a differentiating network by the bias thereon from resistors 94 and 95 and the ground on the emitter terminal. The collector produces the pulse L over conductor 59 which is applied directly to the base of a transistor 96 which inverts the pulse L on its collector output 62. The positive pulse L on the inverter output 62 is applied to the "OR" gate consisting of diodes 97 and 98, the output 62 being through diode 97, while the output 63 from the erase multivibrator 36 is through the diode 98. The output 64 of the "OR" gate is applied directly to the base of transistor 99 having its collector coupled directly to a positive voltage source and its emitter coupled through a diode 100 to ground. The emitter is also coupled through a Zener diode 101 to the base of a transistor 102 having its collector coupled through a load resistor 103 to a positive voltage source and its emitter coupled through a

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voltage divider consisting of resistors 104 and 105 in series between a negative voltage source 106 and ground. The base of transistor 102 is biased from negative source 106 through a resistor 107. The transistor 102 operates as an inverter for the positive brightness pulse L conducted from the emitter of transistor 99 to the base of transistor 102 and taken from the collector of transistor 102. The collector of transistor 102 is coupled directly to the grid of a triode vacuum tube 108 having its anode coupled directly to a positive voltage source and its cathode coupled through a resistor 109 to a negative voltage source. The output conductor 18 for the brightness pulse is coupled directly to the cathode of the vacuum tube 108 operating as a cathode follower isolating any transient voltages on the output 18 which may attempt to feed back into the transistor circuitry from the DVST. The Zener diode 101 and the negative bias on the cathode of tube 108 through the resistor 109 establish the voltage bias level on the brightness pulse for application to the suppressor grid 15 of the DVST. Since the operation of the circuit of FIGURE 5 in conjunction with the operation explained for FIGURE 4 should be clear from the tracing of the various waveforms J, K, L, and M, through the circuitry, it is believed that further discussion and description of the operation is unnecessary. As may be seen from the circuitry of the preferred illustrated form of the invention in FIGURE 5 for the block circuit diagram in FIGURE 4, the erase and brightness pulses connected over the outputs 17 and 18, respectively, to the backing electrode 14 and suppressor grid 15 of the DVST will substantially eliminate or greatly minimize flashing on the fluorescent screen 16 of the DVST normally produced by erase pulses.

The embodiment shown in FIGURES 2 and 3 have a minor disadvantage of not being able to generate a brightness pulse with a 100 percent duty cycle due to the recovery time characteristics of the multivibrators. There is no such disadvantage in the embodiment shown in FIGURE 4 since the variable amplitude spike voltage generator triggered by the clock pulse circuit and the RC charging network to generate a sawtooth wave shape do not have the recovery time difficulties of multivibrators. Accordingly, it is possible to get a 100 percent duty cycle by generating a large positive spike or high amplitude spike voltage J in the circuit of FIGURES 4 and 5. When the circuits of FIGURES 4 and 5 are operated with 100 percent duty cycle brightness pulses, the DVST flooding gun of FIGURE 1 is essentially turned "off" and a black background display results with only writing gun "writing-through" being displayed.

While many modifications and changes may be made in the constructional details and features of this invention without departing from the spirit and scope of this invention for the intended purpose, it is to be understood that I desire to be limited only by the scope of the appended claims.

I claim:

1. In a direct view storage tube having a backing electrode and a suppressor grid, a control circuit for coupling to the backing electrode and suppressor grid thereof comprising:

generating means for generating voltage pulses over each of two channels in leading edge time coincidence;

first means in one said channel for developing each pulse in one polarity with adjustable means in said first means to vary pulse width to produce an erase pulse on an output thereof for application to the backing electrode of the direct view storage tube;

a second means in said other channel for developing each pulse in the opposite polarity to said erase pulse with adjustable means in said second means to vary pulse width to produce a brightness pulse of greater pulse width than said erase pulse on an output thereof;

an "OR" gate coupled to the outputs of said means of each channel to gate either said erase pulse and brightness pulse on an output thereof; and  
 a brightness amplifier coupled to the output of said "OR" gate and having an output for coupling to the suppressor grid of the direct view storage tube whereby the brightness of the direct view storage tube, with the control circuit coupled thereto, can be controlled upon the application of erase pulses.

2. Control circuitry for coupling to the backing electrode and the suppressor grid of a direct view storage tube having backing and suppressor grid electrodes comprising:

an astable multivibrator adjustable to produce erase pulses of variable width and biased at a predetermined level in one channel output;

a monostable multivibrator coupled to the output of said astable multivibrator to be triggered thereby and adjustable to produce brightness pulses of variable width on an output thereof in another channel;

an "OR" gate coupled to the outputs of said astable and monostable multivibrators to pass either pulse as said brightness pulse on an output thereof in leading edge time coincidence with said erase pulse;

a brightness amplifier coupled to the output of said "OR" gate to produce an amplified brightness pulse on an output thereof; and

means in said other channel to produce said brightness pulse in a polarity relation opposite to said erase pulse whereby erase and brightness pulse are produced by adjustably variable duty cycle to control the persistence and brightness voltages for the direct view storage tube during erase of stored information.

3. Control circuitry for coupling to the backing electrode and suppressor grid of a direct view storage tube having backing and suppressor grid electrodes comprising:

a generator of fixed frequency pulses conducted over two output channels;

a first monostable multivibrator in one channel having means therein to vary the output pulse width thereof produced by the triggering fixed frequency pulses;

a biasing circuit in said one channel coupled to the output of said first monostable multivibrator to bias the output pulses to produce erase pulses for the backing electrode;

a second monostable multivibrator in the other channel having means therein to vary the width of each brightness pulse produced by the triggering fixed frequency pulses;

an "OR" gate coupled to the outputs of said first and

second monostable multivibrators to conduct said brightness pulses on an output thereof; and

a brightness amplifier coupled to the output of said "OR" gate to amplify and bias said brightness pulses for the direct view storage tube suppressor grid, said erase and brightness pulses being in opposite polarity whereby said erase and brightness pulses are coincident and adjustable in duty cycle.

4. Control circuitry for coupling to the backing electrode and suppressor grid of a direct view storage tube having backing and suppressor grid electrodes comprising:

a generator of fixed frequency pulses conducted over two output channels;

a first monostable multivibrator in one channel producing erase pulses on an output thereof by triggering of said fixed frequency pulses, said multivibrator being adjustable to vary pulse width;

a biasing circuit coupled to the output of said first monostable multivibrator to bias said erase pulses to a predetermined level;

a spike generator coupled in the other channel to generate spike voltages upon being triggered by said fixed frequency pulses, said generator being adjustable to vary the spike voltage amplitude;

a resistor-capacitor network coupled to said spike generator to shape said spike voltage into a sawtooth voltage proportional to spike voltage amplitude;

a differentiator coupled to said resistor-capacitor network to produce a differentiated brightness pulse of a width proportional to input pulse amplitude;

an inverter coupled to the output of said differentiator to invert said brightness pulse;

an "OR" gate coupled to receive said erase and brightness pulses on inputs thereof to pass brightness pulses to the output thereof; and

a brightness amplifier coupled to said "OR" gate output to control the amplitude and bias level of said brightness pulses for the direct view storage tube suppressor grid whereby the duty cycle of said erase and brightness pulses are varied to control tube brightness during erase of voltage information therein.

## References Cited

## UNITED STATES PATENTS

|           |        |                    |         |
|-----------|--------|--------------------|---------|
| 3,088,048 | 4/1963 | Ogland et al. .... | 315—12  |
| 3,237,188 | 2/1966 | Shair et al. ....  | 340—347 |

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