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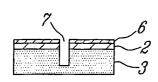
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(54) Title: FABRICATION PROCESS FOR HIGH RESOLUTION LITHOGRAPHY MASKS USING EVAPORATED OR PLASMA ASSISTED ELECTRON SENSITIVE RESISTS WITH PLATING IMAGE REVERSAL



(57) Abstract: The present invention relates to a method for fabricating a high resolution lithography mask, comprising providing a blank mask, coating the blank mask with a conductive layer, depositing a negative electron-sensitive resist layer on the conductive layer, applying an electron beam irradiation to the negative electron-sensitive resist layer to form patterns of non-soluble resist, dissolving the negative electron-sensitive resist layer to leave on the conductive layer only the patterns of non-soluble resist, plating an etchresistant material on the conductive layer to invert the patterns, and conducting a

directional etch through the patterns not protected by the plated etch-resistant material to transfer these patterns into the blank mask.





FABRICATION PROCESS FOR HIGH RESOLUTION LITHOGRAPHY MASKS USING EVAPORATED OR PLASMA ASSISTED ELECTRON SENSITIVE RESISTS WITH PLATING IMAGE REVERSAL

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FIELD OF THE INVENTION

The present invention relates to the field of fabricating high resolution lithography masks.

The present specification will make reference to many references of which the contents is herein incorporated by reference.

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BACKGROUND OF THE INVENTION

The fabrication of high speed integrated semiconductor devices requires efficient high resolution lithography techniques. For production of these semiconductor devices, it is also required that the lithography technique be capable of high throughput. For the fabrication of devices with sub-100 nm critical dimensions, several lithographic techniques are being studied as replacement techniques for the current deep ultraviolet technology (DUV) that is widely used in industry for integrated circuit fabrication on semiconductor wafers; DUV lithography being limited by the wavelength of the ultraviolet source, which is typically 248 nm or 193 nm. Several of the replacement technologies that are being developed use proximity or contact printing, which require very high resolution and image placement accuracy on the masks (original) that are used for pattern replication.

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In proximity X-ray lithography (PXL), a mask is placed in close proximity (10 to 50 μ m) to the exposed wafer. X-rays are projected through the mask to

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pattern the X-ray sensitive resist coating the semiconductor wafer. The mask is made of a transparent membrane (mostly 2 µm thick silicon carbide or diamond) on which thick absorber structures are patterned (300 to 500 nm thickness of tantalum (Ta) or tungsten (W) alloys). A major advantage of PXL lithography is the depth of focus of X-rays, which makes it possible to pattern extremely thick resists. This also makes it ideal to pattern via-holes for integrated circuits and high frequency transistor gates. PXL technology has demonstrated the potential for 50 nm resolutions in limited throughput conditions [Kise et al, 2002; Tsuboi et al., 2001], the resolution of PXL technology being mainly limited by the resolution of the masks. An important issue for this technology is to obtain masks with high resolution patterns and high contrast. Since there is no scale reduction factor between the mask and the projected pattern, the critical dimensions on the masks correspond to the critical dimensions of the circuit.

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To fabricate such masks, an electron beam lithography system can be used to pattern an electron sensitive resist layer, which is deposited on top of a blank mask. The patterns from the resist are then transferred using directional plasma etching such as reactive ion etching to an underlying layer of absorber, typically 300 to 500 nm thickness of tantalum (Ta) or tungsten (W) alloys. In previous work [Smith et al., 1998; Kimura et al., 1988] the electron sensitive resist was in liquid form and needed to be spin coated on top of the absorber layer. Spin coating is performed by depositing the resist in liquid form on top of the blank mask, then rotating the mask at several thousands of revolution per minutes. The mask being typically made from a 2 µm thick silicon carbide or diamond substrate, this process induces deformation of the membranes, which in turn causes image placement errors, i.e. errors in the position of the absorber patterns.

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In low energy electron proximity lithography (LEEPL), the mask is made of an absorber membrane with a thickness ranging from 200 nm to 500 nm [Nakasuji, M., 2001; Shimazu et al., 2002, Yoshizawa, M., 2002]. Holes are

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patterned in the membranes, which electrons can traverse unhindered. The membrane is brought in the vicinity of the silicon wafer (25 to 100 µm distance) and low energy electrons (typically 2 keV) are projected through the holes to form patterns on the sensitive coating of the semiconductor wafer. LEEPL has demonstrated resolutions up to 65 nm in non-production environment, the resolution of LEEPL technology being mainly limited by the resolution of the mask. Once again, there is no scale reduction factor between the mask and the projected pattern; the critical dimensions on the masks correspond to the critical dimensions of the circuit.

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To fabricate such masks, an electron beam lithography system can be used to pattern an electron sensitive resist layer which is deposited on top of a thin membrane (thinner than 2 µm of silicon, silicon carbide or diamond). The patterns from the resist are then transferred using directional plasma etching such as reactive ion etching, to form patterned holes in the membranes. In previous work, the electron sensitive resist was spin coated on top of the membrane. Spin coating is performed in similar conditions than for the X-ray mask fabrication. The membrane being in most cases even thinner than 2 µm, this process causes image placement errors. Moreover, during the fabrication of the mask, the membrane is sagging due to gravity. During the projection of the mask on the semiconductor wafer, the membrane is inverted, causing reverse sagging. This induces image placement errors in the order of 10-100 nm, which is not acceptable for high resolution semiconductor lithography.

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In nanoimprint lithography [Chou, S.Y., 1995], a mold fabricated to nanometer resolution is brought in direct contact with a soft material, which is typically made of a polymer layer on top of a semiconductor wafer. By applying pressure and some heating to the mold, it is possible to transfer the patterns from the mold to the soft material with nanometer scale resolution. Resolutions better than 50 nm have been demonstrated with this technique using molds with limited area. In this case also, the resolution of the nanoimprint technology is limited by the resolution of the mask.

To fabricate a nanoimprint mold, an electron beam lithography system is used to pattern an electron sensitive resist layer which is deposited on top of a hard substrate. This substrate is often quartz or silicon nitride on a silicon wafer. The patterns from the resist are then transferred to the substrate using directional plasma etching such as reactive ion etching, to obtain an embossed mold. In previous work, the electron sensitive resist was spin coated on top of hard substrate. However uniform spreading of the membrane cannot be achieved by spin coating on non planar surfaces. This makes it impossible to fabricate non planar molds. As an example, it is not currently possible to consider the fabrication of cylindrical molds that could be used for periodical patterning of large semiconductor wafers. Also, it is not currently possible to fabricate nanoimprint molds with deep non-contact regions and limited patterned regions.

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SUMMARY OF THE INVENTION

According to the present invention, there is provided a method for fabricating a high resolution lithography mask, comprising: providing a blank mask; coating the blank mask with a conductive layer; depositing a negative electron-sensitive resist layer on the conductive layer; applying an electron beam irradiation to the negative electron-sensitive resist layer to form patterns of non-soluble resist; dissolving the negative electron-sensitive resist layer to leave on the conductive layer only the patterns of non-soluble resist; plating an etch-resistant material on the conductive layer to invert the patterns; and conducting a directional etch through the patterns not protected by the plated etch-resistant material to transfer said patterns into the blank mask.

The method according to the present invention is capable of, in particular but not exclusively:

- fabricating masks for X-ray lithography and masks for electron projection lithography with achievable resolutions below 50 nm; and
- fabricating molds usable for nanoimprint lithography.

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The foregoing and other objects, advantages and features of the present invention will become more apparent upon reading of the following non restrictive description of an illustrative embodiment thereof, given by way of example only with reference to the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

In the appended drawings:

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Figure 1a is a side elevational view of a multi-layer substrate on which a metal seed layer and a negative electron sensitive resist layer have been deposited;

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Figure 1b is a side elevational view of the multi-layer substrate, the metal seed layer and the resist layer from Figure 1a showing the formation of a polymer structure from the resist layer by means of a controlled focused or shaped electron beam;

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Figure 1c is a side elevational view of the multi-layer substrate and metal seed layer from Figure 1a on which the non-reacted portion of the resist layer has been removed to leave only the polymer structure on the substrate;

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Figure 1d is a side elevational view of the multi-layer substrate and metal seed layer from Figure 1a, on which a metal layer is electro-plated on top of the metal seed layer, except in areas protected by the polymer structure; and

Figure 1e is a side elevational view of the multi-layer substrate from Figure 1a, on which the polymer structure has been removed and trenches have been etched by directional plasma etching.

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DETAILED DESCRIPTION OF THE ILLUSTRATIVE EMBODIMENT

In the different figures of the appended drawings, the corresponding elements are identified by the same reference numerals.

Appended Figures 1a, 1b, 1c and 1d illustrate the various steps of a non restrictive illustrative embodiment of the method according to the present invention, for fabricating etched structures 7 (Figure 1e) on a high resolution lithography mask 3. This method uses a controlled electron beam 4 (Figure 1b) to form polymer 5 from a layer of negative electron-sensitive resist 1. The illustrative embodiment of this method also uses plating to obtain an inverted pattern layer 6 (Figure 1d). The non-restrictive illustrative embodiment of this method further uses directional etching to transfer the patterns from the plated layer 6 to the substrate 3 as etched structures 7 (Figure 1e).

More specifically, the non-restrictive illustrative embodiment of the method according to the invention, for fabricating a high resolution lithography mask using a negative electron-sensitive resist layer, an inversion plating procedure and a directional etch to form the patterned structures 7 on a mask 3, can be summarized as follows:

Figure 1a:

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A seed layer of metal 2 and a layer of negative electron-sensitive resist 1 are deposited on a top face of the substrate 3 using, for example, two successive evaporation steps (Figure 1a).

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The substrate 3 is a blank mask for X-ray lithography, low energy electron proximity projection lithography, electron projection lithography or nanoimprint lithography.

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For X-ray lithography, the substrate 3 is a multi-layer substrate usually including an X-ray transparent membrane formed, for example, of a 2 µm thick diamond or SiC membrane, on which a 300 nm to 500 nm thick layer of X-ray absorbing material is deposited by sputtering. The X-ray absorbing material comprises, for example, a tantalum (Ta) compound such as a compound of tantalum and boron (TaB). The X-ray transparent membrane can be held flat and rigid through a mono-crystalline silicon ring located on the same side of the membrane as the layer of X-ray absorbing material.

For low energy electron proximity projection lithography or electron projection lithography, the substrate 3 is usually a 200 nm to 500 nm thick Si, SiC or diamond membrane.

For nanoimprint lithography, the substrate 3 is, for example, selected from the group consisting of a quartz plate, a silicon (Si) wafer with or without a layer of Si₃N₄ on top, a glass plate, and a glass cylinder.

The metal seed layer 2 is advantageously a highly conductive metal layer. It is deposited on the top face of the substrate 3 for example by evaporation or sputtering. For example, a typical deposition method is evaporation using a Joule effect evaporator, under a 10⁻⁷ torr vacuum, to deposit a 50 nm thick layer of silver (Ag). Aluminum (Al) could also be used to form the metal seed layer 2. The thickness of the metal seed layer 2 is located between 5 nm and 100 nm.

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After deposition of the metal seed layer 2, a negative electron-sensitive resist layer 1 is deposited on the top face of this metal seed layer 2. For

example, a typical resist deposition consists of evaporating a 30 nm thick sterol layer by organic Joule effect evaporation, at a controlled temperature of 130°C to 145°C, with a 10⁻⁷ torr pre-deposition vacuum (see Figure 1a). A plasma-assisted deposition of fluoropolymer could also be used for depositing the negative electron-sensitive resist layer 1.

Therefore, the negative electron-sensitive resist layer can be selected from the group consisting of: a sterol layer deposited by evaporation [Lavallee, E. et al., International published patent application WO 03/079112 A1] or of a fluoropolymer layer [Awad, Y. et al., International published patent application WO 03/087938 A1] deposited by plasma reaction.

Figure 1b:

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The layer of negative electron sensitive resist 1 is polymerized by applying an electron beam 4 to the layer 1 to locally break chemical bonds in the molecules, creating free radicals to form bonds between the molecules, thus forming patterned structures of non-soluble polymer 5. In other words, the negative electron-sensitive resist is cross-linked at the molecular level to make it less soluble. The electron beam 4 is either focused through a series of electromagnetic lenses or electrostatic lenses in order to achieve a minimal beam size on the surface of the layer 1, or shaped by projection through a stencil to project this shape on the surface of the resist layer. The electron beam is also displaced, for example under the control of a computer, to expose a desired pattern to be given by the completed mask.

For example, typical electron-beam lithography parameters with a sterol layer as the negative electron sensitive resist can use a 3 keV focused gaussian electron beam, with a 2 nA current, and with electron doses for the exposed areas of 200 μ C/cm². Alternatively, a 25 keV or 50 keV focused electron beam can be used, with currents up to 20 nA, to pattern the resist. According to another illustrative example, a low energy electron proximity

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projection lithography (LEEPL) system can be used to bombard the blank mask with 2 keV electrons at a dose of 200 μ C/cm² through a stencil opening in a membrane, thus transferring the patterns from the stencil opening to the blank mask (see Figure 1b).

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In general terms, the dose is between 20 mC/cm² and 400 mC/cm² at an energy level between 1 keV and 100 keV.

Figure 1c:

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After the completion of electron beam lithography, the sample of Figure 1b is immersed into a solvent solution (development solution) that is able to dissolve the negative electron-sensitive resist layer 1, but not the etchresistant polymer 5. After this wet dissolution, only the areas (etch-resistant polymer 5) having been exposed to the electron beam 4 will remain on the top face of the substrate metal seed layer 2. With a sterol layer as the negative electron sensitive resist 1, the wet solvent solution is typically a mixture of propanediol and another stronger solvent (see Figure 1c). The bland mask is then rinsed in de-ionized water in order to remove dust particles or residues from the development solution. For that purpose, the blank mask is fully immersed in de-ionized water.

The wet development solution cannot be brought into direct contact with the negative electron-sensitive resist layer only through full immersion of the blank mask in the wet development solution but also by spraying the wet development solution on the resist layer 1 while the blank mask rotates.

Oxygen plasma can also be used to remove the negative electronsensitive resist layer 1 except the etch-resistant polymer 5.

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Figure 1d:

The top face metal seed layer 2 of Figure 1c is electro-plated, using an alternating current between a metal electrode and the mask, both immersed in a wet plating solution, for example a wet nickel plating solution of nickel sulphamate or a wet copper plating solution.

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The reverse cycle of the current is adjusted in time duration and in voltage amplitude to remove the top portion of the metal deposited in the forward biasing cycle, thus reducing the grain size of the plated metallic layer 6. Plating is done by cycling a forward (plating) bias at a voltage superior or equal to the threshold plating voltage, with a reverse (removing) bias at a voltage which is larger than the forward bias by a factor of 3/2. Typically, square shaped electrical waveforms are used to produce this cycling, at a frequency in the range of 20 kHz to 100 kHz, with the reverse cycle shorter in time duration than the forward cycle. Therefore, the reverse bias cycles are adjusted in time duration and in voltage amplitude to remove during the reverse bias cycles the top portion of the material deposited during the forward bias cycles, in order to obtain a smooth uniform plated layer of etch-resistant material. Higher frequency is preferable as it limits the time the atoms, for example nickel atoms, plated in the forward cycle have to relax to a stable state, making it more difficult to remove in the reverse bias cycle (see Figure 1d).

Figure 1e:

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The sample of Figure 1d is inserted in a directional plasma etch system, in order to remove first the etch-resistant polymer 5, and to etch trenches such as 7 in the metal seed layer 2 and the substrate 3. The electroplated metallic layer 6 is etch-resistant to the selected etching gases, thus resulting in patterned trenches 7 in the multi-layer mask. A reactive ion etching system (RIE) can be used for this purpose, using an initial O_2 gas followed by a mixture of CH_4 and SF_6 . The pressure of gas in the chamber is of the order of 50 to 80 millitorr. The ratio of CH_4 over SF_6 is adjusted in order to control the

angle of the sides of the structures formed by the pattern transferred to the underlying layers. As a non limitative example, for the transfer in a 300 nm thick TaB alloy such as used for X-ray lithography masks, the proportion of gases is $CH_4:SF_6$ 2:1. Under these conditions, the etch time is approximately 60 minutes. Vertical pattern transfer from the Ni etch mask to the underlying TaB layer is then possible. Such vertical transfer is generally required by high resolution mask fabrication to avoid blurring during the exposure of the mask. To ensure adequate placement of the patterns once transferred to the absorber layer (not shown), the substrate 3 is usually placed in direct contact on a controlled temperature plate (not shown). This plate cools the substrate 3 during the etching process, in order to avoid distortion of the said substrate due to heating by the plasma bombardment (see Figure 1e).

In general terms:

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- the directional etch is selected from the group consisting of: reactive ion etching, electron cyclotron resonance reactive ion etching and inductively coupled plasma etching;
- the directional plasma etch can be created using gas selected from the group consisting of: O₂, CF₄, SF₆, CH₄, or a combination thereof;
 - when the substrate 3 is a multi-layer blank mask, the gas is selected so as to create a plasma gas capable of etching the patterns 5 of non-soluble resist, the metal layer 2, and at least one layer of the substrate 3, except in areas protected by the plated etch-resistant layer 6.

Non-restrictive illustrative example:

In this example, the non-restrictive, illustrative embodiment of the method according to the present invention will be applied to the production of masks for X-ray lithography.

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The X-ray lithography blank mask in this example consists of a multilayer substrate of diamond membrane, held flat and rigid by a silicon monocrystalline ring, the membrane being coated by a 300 nm thick TaB layer. The silicon ring applies a moderate tensile stress to the membrane, preventing it from curving. The TaB layer is deposited by sputter coating in controlled temperature conditions, so the membrane remains flat with the TaB layer on top. The TaB layer is coated on the same side of the membrane that stands the silicon ring, i.e. on the back side of the membrane, in order to obtain a blank mask for X-ray lithography. The top face of the TaB layer of the blank mask is subsequently first coated by a 50 nm thick silver layer, using deposition by Joule effect evaporation. The initial pressure during the evaporation is of the order of 10⁻⁷ torr. The silver layer is evaporated at the minimal temperature for silver evaporation in order to keep the grain size of this layer inferior to 20 nm. A sterol negative electron sensitive layer (resist layer) is then deposited on top of the silver and TaB layers, also by Joule effect evaporation. This resist layer is 30 nm thick.

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Electron beam lithography is performed to pattern this sterol layer, using a low energy electron beam lithography system. A 3 keV electron energy is chosen in order to achieve polymerization of the entire thickness of the resist layer during exposure, while keeping a minimal ratio of backscattered electrons (electrons that reach the TaB layer and are backscattered to the resist layer). Backscattered electrons in such a case would cause deformation of the patterns from electron beam lithography, since such electrons can cause reaction of the resist material in unwanted areas. The electron beam causes the molecules of the sterol layer to cross-link, making it non-soluble. The electron beam is displaced using a computer-controlled pattern generator. These patterns correspond to the desired patterns for the completed mask. Such patterns can be for example via-holes or gate levels for integrated circuits.

Once patterning is complete, the blank mask is taken out of the electron beam lithography system and immersed in a development solution, such as propanediol in combination with another stronger solvent. Such a solvent solution will dissolve the sterol layer, except in areas exposed to the electron beam. The blank mask is then immersed in water to clean the residues from the solvent solution.

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In order to obtain an inverted image on the mask of the exposed pattern, the mask is immersed in a standard nickel plating solution (such as used for plating in the disk or protective coating industries), with a nickel electrode. An alternating current is used for plating. The current biasing in the forward direction has to be greater than in the reverse direction, in order for a nickel layer to be plated on the surface. The reverse biasing is adjusted to be shorter in time period but higher in voltage amplitude compared to the forward biasing conditions. Thus, during the forward biasing cycle, nickel is deposited on top of the silver seed layer, and during the reverse biasing cycle, roughness of the nickel layer is reduced by removing protruding nickel atoms from the surface. Plating does not occur in the regions where there are patterned structures of sterol resist, the resist not being conductive. The plating therefore covers the silver layer, producing a nickel layer with inverted patterns from the sterol resist structures.

Once plating is completed, the sample is removed from the plating solution, dried and placed in a reactive ion etching plasma chamber. Vacuum is obtained in the reactive ion etching chamber by using a pumping system in order to eliminate contamination from gases present in the atmosphere from the process. An oxygen (O₂) plasma at 100W is used for 2 minutes to remove the non-soluble resist structures formed by resist exposure to the electron beam. A SF₆:CH₄ plasma, at 80W for 100 minutes is then used to etch through the silver layer and the TaB layer, except in areas protected by the plated nickel layer. These regions become transparent to X-rays, while the rest of the mask remains absorbent to X-rays.

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In a manner similar to this application, masks for electron projection lithography can be fabricated, by substituting the TaB layer by the appropriate layer absorption for the given technology.

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Although the present invention has been described in the foregoing description in relation to a non-restrictive illustrative embodiment thereof, this illustrative embodiment can be modified at will, within the scope of the appended claims without departing from the scope and spirit of the subject invention.

References:

Awad, Y., Lavallée, E., Beauvais, J., Drouin, D., "Plasma polymerized electron beam resist", International published patent application WO 03/087938 A1.

Chou, S.Y., "Nanoimprint lithography", US patent #5,772,905 (1995)

Kimura, T., Mochiji, K., Okamoto, H., Iwayanagi, T., Kudo, T., Kuniyoshi, S.,
"Mask for X-ray lithography and process for producing the same", US patent #4,719,161 (1988)

Kise, K., Watanabe, H., Itoga, K., Yabe, H., Sumitani, H., Amemiya, M., "Evaluation of secondary electron blur in x-ray lithography by using the pattern replication technique on the mask", Microprocesses and Nanotechnology conference, Tokyo, Japan (2002)

Lavallee, E., Beauvais, J., Drouin, D., Cloutier, M., "Method of producing an etch-resistant polymer structure using electron beam lithography", International published patent application WO 03/079112 A1

Nakasuji, M., "Charged-particle-beam transfer masks and methods of making",

US patent #6,284,415 (2001)

Shimazu, N., Utsumi, T., "Manufacturing method of mask for electron beam proximity exposure and mask", US patent #6,444,374 (2002)

5

Smith, H.I., Lim, M., Carter, J., Schattenburg, M., "X-ray lithography masking", US patent #5,809,103 (1998)

Tsuboi, S., Tanaka, Y., Iwamoto, T., Sumitani, H., Nakayama, Y., "Recent progress in 1x X-ray mask technology: Feasibility study using ASET-NIST format TaxN X-ray masks with 100 nm rule 4 Gbit dynamic random access memory test pattern", J. Vac. Sci. Technol. B, 19, pp. 2416-2422 (2001)

Yoshizawa, M., "Sub-50 nm stencil mask for low energy electron beam projection lithography", J. Vac. Sci. Technol. B, 20, pp. 3021-3024 (2002)

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WHAT IS CLAIMED IS:

1. A method for fabricating a high resolution lithography mask, 5 comprising:

providing a blank mask;

coating the blank mask with a conductive layer;

depositing a negative electron-sensitive resist layer on the conductive layer;

applying an electron beam irradiation to the negative electron-sensitive resist layer to form patterns of non-soluble resist;

dissolving the negative electron-sensitive resist layer to leave on the conductive layer only the patterns of non-soluble resist;

plating an etch-resistant material on the conductive layer to invert said patterns; and

conducting a directional etch through the patterns not protected by the plated etch-resistant material to transfer said patterns into the blank mask.

A method for fabricating a high resolution lithography mask as
 defined in claim 1, wherein depositing a negative electron-sensitive resist layer comprises:

evaporating electron-sensitive resist material on the conductive layer.

3. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein depositing a negative electron-sensitive resist layer comprises:

conducting a plasma assisted deposition of electron-sensitive material on the conductive layer.

4. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein applying an electron beam irradiation comprises: applying a focused or shaped electron beam to the negative electronsensitive resist layer in order to cross link the resist at the molecular level to make it less soluble; and

displacing the focused or shaped electron beam onto the negative electron-sensitive resist layer to form the patterns of non-soluble resist.

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5. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein dissolving the negative electron-sensitive resist layer comprises:

dissolving the negative electron-sensitive resist layer in a development solution.

6. A method for fabricating a high resolution lithography mask as defined in claim 1, further comprising:

rinsing the blank mask in de-ionized water in order to remove dust particles and/or residues from the development solution.

7. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein coating the blank mask comprises:

depositing on the blank mask a layer of highly conductive metal.

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8. A method for fabricating a high resolution lithography mask as defined in claim 7, wherein electro-plating an etch-resistant material on the conductive layer comprises:

plating an etch-resistant material on the conductive layer in a wet plating solution using the highly conductive metal layer as a seed for plating.

9. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein conducting a directional etch comprises:

using a directional plasma etch.

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10. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein providing a blank mask comprises:

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providing a multi-layer blank mask selected from the group consisting of: X-ray lithography blank mask, low energy electron proximity projection lithography blank mask, electron projection lithography blank mask, nanoimprint lithography blank mask.

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11. A method for fabricating a high resolution lithography mask as defined in claim 7, wherein depositing on the blank mask a layer of highly conductive metal comprises depositing on the blank mask a layer of highly conductive metal selected from the group consisting of silver and aluminum.

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12. A method for fabricating a high resolution lithography mask as defined in claim 7, wherein depositing on the blank mask a layer of highly conductive metal comprises:

depositing on the blank mask a layer of highly conductive metal having a thickness between 5 nm and 100 nm.

13. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein depositing a negative electron-sensitive resist layer comprises:

depositing on the conductive layer a sterol layer by evaporation.

14. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein depositing a negative electron-sensitive resist layer comprises:

depositing a negative electron-sensitive resist layer having a thickness between 5 nanometer and 100 nanometer.

15. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein displacing the focused or shaped electron beam onto the negative electron-sensitive resist layer comprises:

computer-controlling displacement of the electron beam on the layer of negative electron-sensitive resist.

- 16. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein applying an electron beam irradiation to the negative electron-sensitive resist layer comprises:
- exposing the negative electron-sensitive resist layer to an electron irradiation between 20 µC/cm² and 400 µC/cm².
 - 17. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein applying an electron beam irradiation to the negative electron-sensitive resist layer comprises:

applying to the negative electron-sensitive resist layer electrons at an energy of at least 1 keV.

18. A method for fabricating a high resolution lithography mask as
 defined in claim 5, wherein dissolving the negative electron-sensitive resist layer comprises:

bringing a wet development solution into direct contact with the negative electron-sensitive resist layer through full immersion of the blank mask in the wet development solution.

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- 19. A method for fabricating a high resolution lithography mask as defined in claim 5, wherein dissolving the negative electron-sensitive resist layer comprises:
- bringing a wet development solution into direct contact with the negative electron-sensitive resist layer through spraying of the wet development solution on the resist layer while the blank mask rotates.
- 20. A method for fabricating a high resolution lithography mask as defined in claim 6, wherein rinsing the blank mask in de-ionized water comprises:

fully immersing the blank mask in de-ionized water.

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21. A method for fabricating a high resolution lithography mask as defined in claim 8, wherein electro-plating an etch-resistant material on the conductive layer in a wet plating solution comprises:

electro-plating the etch-resistant material on the conductive layer in a wet nickel plating solution of nickel sulphamate.

22. A method for fabricating a high resolution lithography mask as defined in claim 8, wherein electro-plating the etch-resistant material on the conductive layer in a wet plating solution comprises:

using an alternating current in the wet plating solution.

23. A method for fabricating a high resolution lithography mask as defined in claim 22, wherein using an alternating current comprises:

producing the alternating current in the wet plating solution by
alternately cycling forward and reverse voltage bias between the mask and a
metal electrode both immersed in the wet plating solution.

- 24. A method for fabricating a high resolution lithography mask as defined in claim 22, further comprising adjusting the reverse bias cycles in time duration and in voltage amplitude to remove during the reverse bias cycles a top portion of the material deposited during the forward bias cycles, in order to obtain a smooth uniform plated layer of etch-resistant material.
- 25. A method for fabricating a high resolution lithography mask as defined in claim 1, comprising selecting the directional etch from the group consisting of: reactive ion etching, electron cyclotron resonance reactive ion etching and inductively coupled plasma etching.
- 26. A method for fabricating a high resolution lithography mask as defined in claim 9, wherein using a directional plasma etch comprises:

creating a plasma using gas selected from the group consisting of: O_2 , CF_4 , SF_6 , CH_4 , or a combination thereof.

27. A method for fabricating a high resolution lithography mask as defined in claim 26, wherein the blank mask is a multi-layer blank mask, and wherein said method comprises selecting as the gas used to create the plasma a gas capable of etching the patterns of non-soluble resist, the conductive layer, and at least one layer of the blank mask, except in areas protected by the plated etch-resistant material.

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28. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein providing a blank mask comprises:

producing an X-ray lithography blank mask comprising an X-ray transparent membrane coated by sputtering with a layer of X-ray absorbing material.

- 29. A method for fabricating a high resolution lithography mask as defined in claim 28, comprising selecting a material of the membrane from the group consisting of: SiC and diamond.
- 30. A method for fabricating a high resolution lithography mask as defined in claim 28, wherein the layer of X-ray absorbing material is 300 nm thick.
 - 31. A method for fabricating a high resolution lithography mask as defined in claim 28, wherein the X-ray absorbing material comprises a compound of tantalum and boron.
 - 32. A method for fabricating a high resolution lithography mask as defined in claim 28, comprising holding the X-ray transparent membrane flat and rigid through a mono-crystalline silicon ring located on the same side of the membrane as the layer of X-ray absorbing material.
 - 33. A method for fabricating a high resolution lithography mask as

defined in claim 32, comprising depositing the conductive layer and the negative electron-sensitive resist layer subsequently on a top face of the layer of X-ray absorbing material.

5 34. A method for fabricating a high resolution lithography mask as defined in claim 1, wherein providing a blank mask comprises:

providing a nanoimprint lithography blank mask selected from the group consisting of: a silicon wafer, a quartz plate, a glass plate, and a glass cylinder.

