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[Continued on next page]

(54) Title: OXIDE SEMICONDUCTOR FILM, SEMICONDUCTOR DEVICE, AND MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

FIG. 1A

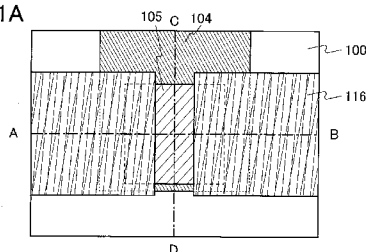


FIG. 1B

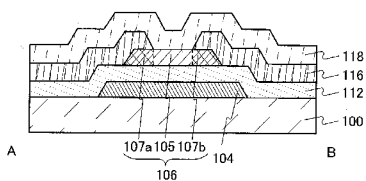
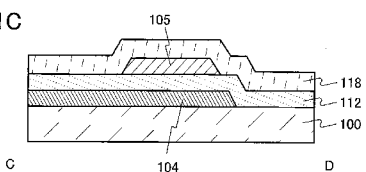


FIG. 1C



(57) Abstract: A highly reliable semiconductor device is manufactured by giving stable electric characteristics to a transistor in which an oxide semiconductor film is used. In a transistor using an oxide semiconductor film for an active layer, a microvoid is provided in a source region and a drain region adjacent to a channel region. By providing a microvoid in the source region and the drain region formed in an oxide semiconductor film, hydrogen contained in the channel region of an oxide semiconductor film can be captured in the microvoid.



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DESCRIPTION

OXIDE SEMICONDUCTOR FILM, SEMICONDUCTOR DEVICE, AND
MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

5

TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device which is provided with a circuit including a semiconductor element such as a transistor. Moreover, the present invention relates to an oxide semiconductor film used in the semiconductor device. For example, the present invention relates to an electronic device which includes, as a component, any of a power device mounted in a power circuit, a semiconductor integrated circuit including a memory, a thyristor, a converter, an image sensor, or the like, an electro-optical device typified by a liquid crystal display device, a light-emitting display device including a light-emitting element, and the like.

15

[0002]

In this specification, a semiconductor device generally refers to a device which can function by utilizing semiconductor characteristics; an electrooptic device, a light-emitting display device, a semiconductor circuit, and an electronic device are all included in semiconductor devices.

20

BACKGROUND ART

[0003]

Many transistors formed over a glass substrate or the like are manufactured using amorphous silicon, polycrystalline silicon, or the like, as typically seen in liquid crystal display devices. Although transistors including amorphous silicon have low field effect mobility, they can be formed over a larger glass substrate. On the other hand, although transistors including polycrystalline silicon have high field effect mobility, they are not suitable for being formed over a larger glass substrate.

25

[0004]

30

In addition to a transistor formed using silicon, a technique in which a transistor is manufactured using an oxide semiconductor and applied to an electronic device or an optical device has attracted attention. For example, a technique of

manufacturing a transistor by using zinc oxide or In-Ga-Zn-O-based oxide as oxide semiconductor, and of using the transistor for a switching element of a pixel of a display device and the like is disclosed in Patent Document 1 and Patent Document 2.

[0005]

- 5 In an oxide semiconductor, part of hydrogen serves as a donor to release electrons as carriers. When the carrier concentration in the oxide semiconductor becomes high, a channel is formed in the transistor without voltage application to a gate. That is, the threshold voltage of a transistor shifts in the negative direction. It is difficult to remove hydrogen in the oxide semiconductor completely; therefore, it is also
10 difficult to control the threshold voltage.

[0006]

- In Patent Document 3, it is disclosed that when hydrogen is added in an oxide semiconductor film, electrical conductivity of the oxide semiconductor is increased by four to five orders of magnitude approximately. Moreover, it is disclosed that
15 hydrogen is diffused into the oxide semiconductor film from an insulating film which is in contact with the oxide semiconductor film.

[Reference]

[0007]

[Patent Document 1] Japanese Published Patent Application No. 2007-123861

- 20 [Patent Document 2] Japanese Published Patent Application No. 2007-096055

[Patent Document 3] Japanese Published Patent Application No. 2008-141119

DISCLOSURE OF INVENTION

[0008]

- 25 An object of one embodiment of the present invention is to provide an oxide semiconductor film which can capture hydrogen efficiently.

[0009]

- Another object of one embodiment of the present invention is to manufacture a highly reliable semiconductor device in which a transistor including an oxide
30 semiconductor film has stable electric characteristics.

[0010]

A technical idea of one embodiment of the present invention is to form a

microvoid in the oxide semiconductor film.

[0011]

Another technical idea of one embodiment of the present invention is to form a microvoid in a source region and a drain region adjacent to a channel region in a transistor using an oxide semiconductor film.

[0012]

It is known that an oxide semiconductor generally has n-type conductivity and part of hydrogen in an oxide semiconductor film serves as a donor and causes release of an electron serving as a carrier. Thus, the use of an oxide semiconductor film for a transistor might cause a shift of the threshold voltage of the transistor in the negative direction. Then, it is necessary to form an oxide semiconductor film containing as little hydrogen as possible; however, it is difficult to suppress entry of a minute amount of hydrogen.

[0013]

According to one embodiment of the present invention, a microvoid is provided in a source region and a drain region formed in an oxide semiconductor film, so that hydrogen included in a channel region in an oxide semiconductor film can be captured.

[0014]

The microvoid can be formed by an ion implantation or an ion doping using at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$.

[0015]

By providing a microvoid, an oxide semiconductor film in which hydrogen can be captured efficiently can be provided.

[0016]

Hydrogen included in a channel region is captured in a source region and a drain region, whereby stable electric characteristics can be given to a transistor in which

an oxide semiconductor film is used, and thus a highly reliable semiconductor device can be manufactured.

BRIEF DESCRIPTION OF DRAWINGS

5 [0017]

In the accompanying drawings:

FIGS. 1A to 1C are a top view and cross-sectional views illustrating an example of a transistor according to one embodiment of the present invention;

10 FIGS. 2A to 2C are a top view and cross-sectional views illustrating an example of a transistor according to one embodiment of the present invention;

FIGS. 3A to 3C are a top view and cross-sectional views illustrating an example of a transistor according to one embodiment of the present invention;

FIGS. 4A to 4C are a top view and cross-sectional views illustrating an example of a transistor according to one embodiment of the present invention;

15 FIGS. 5A to 5C are a top view and cross-sectional views illustrating an example of a transistor according to one embodiment of the present invention;

FIGS. 6A to 6C are a top view and cross-sectional views illustrating an example of a transistor according to one embodiment of the present invention;

20 FIGS. 7A to 7C are a top view and cross-sectional views illustrating an example of a transistor according to one embodiment of the present invention;

FIG. 8 is a circuit diagram illustrating an example of a liquid crystal display device including a transistor according to one embodiment of the present invention;

25 FIGS. 9A and 9B are a circuit diagram illustrating an example of a semiconductor memory device including a transistor according to one embodiment of the present invention and a graph illustrating electrical characteristics;

FIGS. 10A and 10B are circuit diagrams illustrating an example of a semiconductor memory device including a transistor according to one embodiment of the present invention and a graph illustrating electrical characteristics;

30 FIG. 11 is a circuit diagram illustrating an example of a semiconductor memory device including a transistor according to one embodiment of the present invention;

FIGS. 12A to 12C are a block diagram illustrating a specific example of a CPU including a transistor according to one embodiment of the present invention and circuit

diagrams each illustrating part of the CPU;

FIGS. 13A to 13C are perspective views illustrating examples of electronic devices each including a semiconductor device that is one embodiment of the present invention;

5 FIGS. 14A to 14D are cross-sectional views each illustrating an example of a manufacturing method of a transistor according to one embodiment of the present invention;

10 FIGS. 15A to 15D are cross-sectional views each illustrating an example of a manufacturing method of a transistor according to one embodiment of the present invention;

FIGS. 16A to 16D are cross-sectional views each illustrating an example of a manufacturing method of a transistor according to one embodiment of the present invention;

15 FIGS. 17A to 17D are cross-sectional views each illustrating an example of a manufacturing method of a transistor according to one embodiment of the present invention;

FIGS. 18A to 18D are cross-sectional views each illustrating an example of a manufacturing method of a transistor according to one embodiment of the present invention;

20 FIGS. 19A to 19D are cross-sectional views each illustrating an example of a manufacturing method of a transistor according to one embodiment of the present invention;

25 FIGS. 20A to 20D are cross-sectional views each illustrating an example of a manufacturing method of a transistor according to one embodiment of the present invention;

FIGS. 21A and 21B are cross-section observation images obtained with a TEM;
FIGS. 22A and 22B are cross-section observation images obtained with the TEM;

30 FIGS. 23A and 23B are cross-section observation images obtained with the TEM;

FIG. 24A is a cross-section observation image obtained with the HAADF-STEM, and FIG. 24B is a cross-section observation image showing the

distribution of elements observed by EELS;

FIG. 25A is a cross-section observation image obtained with the HAADF-STEM, and FIG. 25B is a cross-section observation image showing the distribution of elements observed by EELS;

5 FIG. 26A is a cross-section observation image obtained with the HAADF-STEM, and FIG. 26B is a cross-section observation image showing the distribution of elements observed by EELS;

FIG. 27 shows XPS spectra;

10 FIGS. 28A and 28B are graphs showing the concentration distribution of hydrogen and nitrogen in the depth direction measured with SIMS;

FIGS. 29A and 29B are graphs showing the concentration distribution of hydrogen and nitrogen in the depth direction measured with SIMS; and

FIG. 30 is a cross-sectional view of an oxide semiconductor film which is one embodiment of the present invention.

15

BEST MODE FOR CARRYING OUT THE INVENTION

[0018]

Hereinafter, embodiments of the present invention are described in detail with reference to the accompanying drawings. However, the present invention is not
20 limited to the description below, and it is easily understood by those skilled in the art that modes and details thereof can be modified in various ways. Therefore, the present invention is not construed as being limited to description of the embodiments. In describing structures of the present invention with reference to the drawings, the same reference numerals are used in common for the same portions in different drawings.
25 Note that the same hatch pattern is applied to similar parts, and the similar parts are not especially denoted by reference numerals in some cases.

[0019]

Before the present invention is described, terms used in this specification are briefly explained. First, when one of a source and a drain of a transistor is called a
30 drain, the other is called a source in this specification. That is, the source and the drain are not distinguished depending on the potential level. Therefore, a portion called a source in this specification can be alternatively referred to as a drain.

[0020]

A voltage refers to a potential difference between a given potential and a reference potential (e.g., a ground potential) in many cases. Therefore, a voltage and a potential can be interchanged with each other.

5 [0021]

Even when it is written in this specification that "to be connected", there is the case where no physical connection is made in an actual circuit and a wiring is only extended.

[0022]

10 Note that the ordinal numbers such as "first" and "second" in this specification are used for convenience and do not denote the order of steps or the stacking order of layers. In addition, the ordinal numbers in this specification do not denote particular names which specify the present invention.

[0023]

15 (Embodiment 1)

In this embodiment, an example of an oxide semiconductor film which is one embodiment of the present invention is described with reference to FIG. 30.

[0024]

20 FIG. 30 is a cross-sectional view of an oxide semiconductor film 3006. The oxide semiconductor film 3006 has a microvoid 3010, and the microvoid 3010 contains at least one of nitrogen, hydrogen, and oxygen.

[0025]

For example, for the oxide semiconductor film 3006, an In-Sn-Ga-Zn-O-based material; an In-Ga-Zn-O-based material, an In-Sn-Zn-O-based material, an
25 In-Al-Zn-O-based material, a Sn-Ga-Zn-O-based material, an Al-Ga-Zn-O-based material, or a Sn-Al-Zn-O-based material; an In-Zn-O-based material, a Sn-Zn-O-based material, an Al-Zn-O-based material, a Zn-Mg-O-based material, a Sn-Mg-O-based material, an In-Mg-O-based material, or an In-Ga-O-based material; an In-O-based material; a Sn-O-based material; a Zn-O-based material; or the like may be used. Here,
30 for example, an In-Ga-Zn-O-based material means an oxide containing indium (In), gallium (Ga), and zinc (Zn), and there is no particular limitation on the atomic ratio. Further, the In-Ga-Zn-O-based material may contain an element other than In, Ga, and

Zn. In this case, the oxide semiconductor film 3006 preferably contains a larger amount of oxygen than the stoichiometric proportion. When the amount of oxygen is large, generation of carriers which results from oxygen deficiency in the oxide semiconductor film 3006 can be suppressed.

5 [0026]

For example, in the case where an In-Zn-O-based material is used as an example of the oxide semiconductor film 3006, the atomic ratio is set so that In/Zn is in a range of from 0.5 to 50, preferably from 1 to 20, more preferably from 3 to 15. When the atomic ratio of Zn is in the above range, the field effect mobility of the transistor can be improved. Here, when the atomic ratio of the compound is In:Zn:O =
10 X:Y:Z, the relation $Z > 1.5X + Y$ is satisfied.

[0027]

Further, a material represented by $\text{InMO}_3(\text{ZnO})_m$ ($m > 0$) may be used for the oxide semiconductor film 3006. Here, M represents one or more metal elements
15 selected from Ga, Al, Mn, and Co. For example, M may be Ga, Ga and Al, Ga and Mn, Ga and Co, or the like.

[0028]

The microvoid provided in the oxide semiconductor film 3006 has a low density as compared to the surrounding thereof or an empty space. The microvoid is
20 substantially a spherical region where the diameter is larger than or equal to 0.1 nm and smaller than or equal to 10 nm, preferably larger than or equal to 2 nm and smaller than or equal to 7 nm, or a region where a plurality of spherical regions overlaps each other. For example, such a spherical microvoid whose diameter is 10 nm can capture 1 to 20000 nitrogen molecules whose diameter is 0.375 nm and oxygen molecules whose
25 diameter is 0.364 nm, and 1 to 40000 hydrogen molecules whose diameter is 0.29 nm. In the oxide semiconductor film 3006, the region where the microvoid is provided has a low density as compared to the other region where the microvoid is not provided.

[0029]

A gas molecule such as nitrogen, oxygen, and hydrogen can be captured into
30 the microvoid provided in the oxide semiconductor film 3006. In order to capture more gas molecules such as nitrogen, oxygen, and hydrogen, for example, heat

treatment may be performed at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, preferably at a temperature higher than or equal to 300 °C and lower than or equal to 650 °C, after the microvoid is formed.

[0030]

5 An oxide semiconductor film 3006 is in a single crystal state, a polycrystalline (also referred to as polycrystal) state, an amorphous state, or the like.

[0031]

 An oxide semiconductor film 3006 is preferably a CAAC-OS (c-axis aligned crystalline oxide semiconductor) film.

10 [0032]

 The CAAC-OS film is not completely single crystal nor completely amorphous. The CAAC-OS film is an oxide semiconductor film having a crystal-amorphous mixed structure in which an amorphous phase includes a crystal portion and an amorphous portion. Note that in most cases, the crystal portion fits inside a cube whose one side
15 is less than 100 nm. From an observation image obtained with a transmission electron microscope (TEM), a boundary between an amorphous portion and a crystal portion in the CAAC-OS film is not clear. Further, with the TEM, a grain boundary in the CAAC-OS film is not found. Thus, in the CAAC-OS film, a reduction in electron mobility, due to the grain boundary, is suppressed.

20 [0033]

 In each of the crystal portions included in the CAAC-OS film, a c-axis is aligned in a direction parallel to a normal vector of a surface where the CAAC-OS film is formed or a normal vector of a surface of the CAAC-OS film, triangular or hexagonal atomic arrangement which is seen from the direction perpendicular to the a-b plane is
25 formed, and metal atoms are arranged in a layered manner or metal atoms and oxygen atoms are arranged in a layered manner when seen from the direction perpendicular to the c-axis. Note that, among crystal portions, the directions of the a-axis and the b-axis of one crystal portion may be different from those of another crystal portion. In this specification, a simple term "perpendicular" includes a range from 85° to 95°. In
30 addition, a simple term "parallel" includes a range from -5° to 5°.

[0034]

In the CAAC-OS film, distribution of crystal portions is not necessarily uniform. For example, in the formation process of the CAAC-OS film, in the case where crystal growth occurs from a surface side of the oxide semiconductor film, the proportion of crystal portions in the vicinity of the surface of the oxide semiconductor film is higher than that in the vicinity of the surface where the oxide semiconductor film is formed in some cases. Further, when an impurity is added to the CAAC-OS film, the crystal portion in a region to which the impurity is added becomes amorphous in some cases.

[0035]

Since the c-axes of the crystal portions included in the CAAC-OS film are aligned in the direction parallel to a normal vector of a surface where the CAAC-OS film is formed or a normal vector of a surface of the CAAC-OS film, the directions of the c-axes may be different from each other depending on the shape of the CAAC-OS film (the cross-sectional shape of the surface where the CAAC-OS film is formed or the cross-sectional shape of the surface of the CAAC-OS film). Note that when the CAAC-OS film is formed, the direction of c-axis of the crystal portion is the direction parallel to a normal vector of the surface where the CAAC-OS film is formed or a normal vector of the surface of the CAAC-OS film. The crystal portion is formed by film formation or by performing treatment for crystallization such as heat treatment after film formation.

[0036]

With use of the CAAC-OS film in a transistor, change in electric characteristics of the transistor due to irradiation with visible light or ultraviolet light can be reduced. Thus, the transistor has high reliability.

[0037]

The crystal portion included in the CAAC-OS film is more likely to be formed near the vicinity of the surface of the film. An oxide semiconductor film including a microvoid as in one embodiment of the present invention has many surfaces in the film, thereby a crystal portion as appeared in the CAAC-OS film is readily obtained.

[0038]

Note that the oxide semiconductor film is formed by a sputtering method, a plasma CVD method, a pulse laser deposition method (PLD), a molecular beam epitaxy

method (MBE), or an evaporation method, and after that, the microvoid 3010 is provided by adding an ion, so that the oxide semiconductor film 3006 can be formed. For ion addition, at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, or an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ is used. After a nitrogen ion or an oxygen ion is added, a hydrogen ion may be added. The addition of a nitrogen ion, a hydrogen ion, and/or an oxygen ion may be performed by an ion implantation method or an ion doping method; the ion doping method is preferably used. For example, when a nitrogen ion is added, an NH_X (X is a natural number) ion may be added by an ion doping method. An ion doping method is preferable in that it takes a time shorter than that by an ion implantation method.

[0039]

Next, by performing heat treatment at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, hydrogen can be captured into the microvoid 3010 from inside and outside the oxide semiconductor film 3006.

[0040]

According to this embodiment, an oxide semiconductor film having the microvoid which can capture hydrogen.

[0041]

This embodiment can be implemented in appropriate combination with the other embodiments.

[0042]

(Embodiment 2)

In this embodiment, an example of a transistor which is a semiconductor device according to an embodiment of the present invention is described with reference to FIGS. 1A to 1C.

[0043]

FIG. 1A is a top view of the transistor. A cross section along dashed-dotted line A-B in FIG. 1A and a cross section along dashed-dotted line C-D in FIG. 1A

correspond to a cross section A-B in FIG. 1B and a cross section C-D in FIG. 1C, respectively.

[0044]

Here, the cross section A-B in FIG. 1B is described in detail.

5 [0045]

The transistor includes a substrate 100, a gate electrode 104 over the substrate 100, a gate insulating film 112 covering the gate electrode 104, an oxide semiconductor film 106 including a channel region 105, a source region 107a, and a drain region 107b over the gate electrode 104 with the gate insulating film 112 provided therebetween, and
10 a pair of electrodes 116 over the oxide semiconductor film 106 to be partly in contact with the oxide semiconductor film 106. Note that it is preferable to have an interlayer insulating film 118 over the oxide semiconductor film 106 so that the channel region 105 in the oxide semiconductor film 106 is not exposed.

[0046]

15 The oxide semiconductor film 106 may have the same structure as the oxide semiconductor film 3006 described in Embodiment 1.

[0047]

Here, by adding at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion
20 having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ to a part of the oxide semiconductor film 106, a microvoid is provided in the oxide semiconductor film 106. A resist mask may be formed over the oxide semiconductor film 106 in order to add the ion selectively.

25 [0048]

The oxide semiconductor film 106 bonds to hydrogen, and may form an electron serving as a carrier. Therefore, when hydrogen is captured in the microvoid, the sheet resistance in a region around the microvoid is decreased approximately from $1 \times 10^5 \Omega/\text{sq}$ to $1 \times 10^7 \Omega/\text{sq}$ (preferably approximately from $1 \times 10^4 \Omega/\text{sq}$ to $1 \times 10^6 \Omega/\text{sq}$),
30 so that the source region 107a and the drain region 107b are formed. Moreover, the other region where no microvoid is formed functions as the channel region 105.

[0049]

At this time, hydrogen included in the channel region 105 and a film which is in contact with the oxide semiconductor film 106 is captured in the microvoid in the source region 107a and the drain region 107b. Thus, it is possible to lower the hydrogen concentration in the channel region 105 and the vicinity thereof as much as possible, so that the channel region 105 is highly purified.

[0050]

The hydrogen concentration in the channel region 105 is less than $5 \times 10^{18} \text{ cm}^{-3}$, preferably less than or equal to $1 \times 10^{18} \text{ cm}^{-3}$, more preferably less than or equal to $5 \times 10^{17} \text{ cm}^{-3}$, and still more preferably less than or equal to $1 \times 10^{16} \text{ cm}^{-3}$.

[0051]

Here, an alkali metal is not an element included in an oxide semiconductor, and therefore, is an impurity. In addition, an alkaline earth metal is also an impurity in the case where the alkaline earth metal is not included in an oxide semiconductor. An alkali metal, in particular, Na diffuses in an insulating film which is in contact with the oxide semiconductor film and Na becomes Na^+ . In addition, in the oxide semiconductor film, Na cuts or enters a bond between a metal and oxygen which are included in the oxide semiconductor. As a result, for example, deterioration of characteristics of the transistor such as a normally-on state of the transistor due to shift of a threshold voltage in the negative direction or a reduction in field-effect mobility occurs; in addition, variation in characteristics is also caused. Such deterioration of characteristics of the transistor and variation in characteristics due to the impurity remarkably appear when the concentration of hydrogen in the oxide semiconductor film is sufficiently low. Therefore, when the concentration of hydrogen in the oxide semiconductor film is less than or equal to $1 \times 10^{18} \text{ cm}^{-3}$, or less than or equal to $1 \times 10^{17} \text{ cm}^{-3}$, the concentration of impurity is preferably reduced. Specifically, the measurement value of Na concentration is lower than or equal to $5 \times 10^{16} \text{ cm}^{-3}$, preferably lower than or equal to $1 \times 10^{16} \text{ cm}^{-3}$, more preferably lower than or equal to $1 \times 10^{15} \text{ cm}^{-3}$. In addition, the measurement value of lithium (Li) concentration is preferably $5 \times 10^{15}/\text{cm}^{-3}$ or less, more preferably $1 \times 10^{15}/\text{cm}^{-3}$ or less. In addition, the measurement value of potassium (K) concentration is preferably less than or equal to 5

$\times 10^{15} \text{ cm}^{-3}$, more preferably less than or equal to $1 \times 10^{15} \text{ cm}^{-3}$.

[0052]

The off-state current of the above-described transistor in which the channel region 105 is formed is extremely small. For example, the off-state current of the transistor where the channel length is $3 \mu\text{m}$ and the channel width is $1 \mu\text{m}$ is less than or equal to $1 \times 10^{-18} \text{ A}$, less than or equal to $1 \times 10^{-21} \text{ A}$, or less than or equal to $1 \times 10^{-24} \text{ A}$.

[0053]

For the oxide semiconductor film 106, for example, a material containing two or more elements selected from In, Ga, Zn, and Sn may be used.

[0054]

As for the oxide semiconductor film 106, a material which has a band gap of 2.5 eV or more, preferably has a band gap of 3.0 eV or more, is selected in order to reduce the off-state current of the transistor. Instead of an oxide semiconductor film, any other semi conductive material which has a band gap within the above range may be used.

[0055]

For the gate insulating film 112 and the interlayer insulating film 118, silicon nitride, aluminum oxide, hafnium oxide, yttrium oxide, zirconium oxide, and the like may be used with a single layer or a stacked layer. For example, the gate insulating film 112 and the interlayer insulating film 118 may be formed by a plasma CVD method, a sputtering method, or the like. As each of the gate insulating film 112 and the interlayer insulating film 118, a film from which oxygen is released by heat treatment may be preferably used. With the use of such a film from which oxygen is released by heat treatment, defects generated in the channel region 105 can be repaired and deterioration in electric characteristics of the transistor can be suppressed.

[0056]

In this embodiment, as the gate insulating film 112 and the interlayer insulating film 118, an insulating film including hydrogen with a concentration which is higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ may be used. A transistor in which a conventional oxide semiconductor film is used in a channel region has been pointed that the hydrogen concentration in the vicinity of the oxide

semiconductor film needs to be small as much as possible. However, by applying an embodiment of the present invention, hydrogen can be captured in the source region 107a and the drain region 107b provided with a microvoid. Therefore, as the gate insulating film 112 and the interlayer insulating film 118, even an insulating film including hydrogen with a high concentration may be used, whereby the resistance in the source region 107a and the drain region 107b can be reduced by hydrogen which is supplied from the gate insulating film 112 and the interlayer insulating film 118. Such an insulating film including hydrogen with a concentration which is higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ can be formed, for example, by a plasma CVD method in an atmosphere in which silane and nitrous oxide are mixed. Alternatively, the insulating film can be formed by a sputtering method in an atmosphere in which argon, oxygen, and hydrogen are mixed.

[0057]

To release oxygen by heat treatment means that the amount of released oxygen which is converted to oxygen atoms is greater than or equal to $1.0 \times 10^{18} \text{ cm}^{-3}$, preferably greater than or equal to $1.0 \times 10^{20} \text{ cm}^{-3}$, in thermal desorption spectroscopy (TDS) analysis.

[0058]

Here, a method of the amount of released oxygen using TDS analysis is described.

[0059]

The amount of released gas in TDS analysis is proportional to the integral value of ion intensity. Therefore, the amount of released gas can be calculated from the ratio between the integral value of measured ion intensity and the reference value of a standard sample. The reference value of a standard sample refers to the ratio of the density of a predetermined atom contained in a sample to the integral value of ion intensity.

[0060]

For example, the number of the released oxygen molecules (N_{O_2}) from an insulating film can be found according to a Formula 1 with the TDS analysis results of a silicon wafer containing hydrogen at a predetermined density which is the standard

sample and the TDS analysis results of the insulating film. Here, all gases having a mass number of 32 which are obtained by the TDS analysis are assumed to originate from an oxygen molecule. CH_3OH , which is given as a gas having a mass number of 32, is not taken into consideration on the assumption that it is unlikely to be present.

5 Further, an oxygen molecule including an oxygen atom having a mass number of 17 or 18 which is an isotope of an oxygen atom is also not taken into consideration because the proportion of such a molecule in the natural world is minimal.

[0061]

$$N_{\text{O}_2} = N_{\text{H}_2}/S_{\text{H}_2} \times S_{\text{O}_2} \times \alpha \text{ (Formula 1)}$$

10 [0062]

N_{H_2} is the value obtained by conversion of the number of hydrogen molecules desorbed from the standard sample into densities. S_{H_2} is the integral value of ion intensity when the standard sample is subjected to TDS analysis. Here, the reference value of the standard sample is set to $N_{\text{H}_2}/S_{\text{H}_2}$. S_{O_2} is the integral value of ion intensity

15 when the insulating film is subjected to TDS analysis. α is a coefficient which influences ion intensity in TDS analysis. Refer to Japanese Published Patent Application No. H06-275697 for details of Formula 1. Note that the amount of released oxygen from the insulating film is measured with a thermal desorption spectroscopy apparatus produced by ESCO Ltd., EMD-WA1000S/W using a silicon

20 wafer containing hydrogen atoms at $1 \times 10^{16} \text{ cm}^{-3}$ as the standard sample.

[0063]

Further, in the TDS analysis, oxygen is partly detected as an oxygen atom. The ratio between oxygen molecules and oxygen atoms can be calculated from the ionization rate of the oxygen molecules. Note that, since the above α includes the

25 ionization rate of the oxygen molecules, the number of the released oxygen atoms can also be estimated through the evaluation of the number of the released oxygen molecules.

[0064]

Note that N_{O_2} is the number of the released oxygen molecules. The amount of

30 released oxygen when converted into oxygen atoms is twice the number of the released oxygen molecules.

[0065]

In the above structure, the film from which oxygen is released by heat treatment may be oxygen-excess silicon oxide (SiO_X ($X > 2$)). In the oxygen-excess silicon oxide (SiO_X ($X > 2$)), the number of oxygen atoms per unit volume is more than
5 twice the number of silicon atoms per unit volume. The number of silicon atoms and the number of oxygen atoms per unit volume are measured by Rutherford backscattering spectrometry (RBS).

[0066]

Oxygen is supplied to the channel region 105 from the gate insulating film 112
10 and the interlayer insulating film 118, thereby the interface state density between the channel region 105 and the gate insulating film 112, and the interface state density between the channel region 105 and the interlayer insulating film 118 can be reduced. As a result, carrier trapping at the interface between the channel region 105 and the gate insulating film 112, and the interface between the channel region 105 and the interlayer
15 insulating film 118 can be suppressed, and thus a transistor with less degradation in electric characteristics can be obtained.

[0067]

Further, in some cases, charge is generated due to oxygen deficiency in the channel region 105. In general, part of oxygen vacancy in an oxide semiconductor
20 film serves as a donor and causes release of an electron which is a carrier. As a result, the threshold voltage of a transistor shifts in the negative direction. Oxygen is sufficiently supplied from the gate insulating film 112 or the interlayer insulating film 118 to the channel region 105, whereby the oxygen vacancy in the channel region 105, which causes the negative shift of the threshold voltage, can be reduced.

25 [0068]

In other words, a film from which oxygen is released by heat treatment is provided for the gate insulating film 112 or the interlayer insulating film 118, the interface state density at an interface between the channel region 105 and the gate insulating film 112 or the interface state density at an interface between the channel
30 region 105 and the interlayer insulating film 118 and the oxygen vacancy in the channel region 105 can be reduced. Thus, the influence of carrier trapping at the interface between the channel region 105 and the gate insulating film 112 or at the interface

between the channel region 105 and the interlayer insulating film 118 can be reduced.

[0069]

Thus, the threshold voltage of the transistor may shift in the negative direction due to various causes. Therefore, it is preferable that the hydrogen concentration in the channel region 105 is reduced while oxygen deficiency is reduced.

[0070]

There is no particular limitation on the substrate 100 as long as it has heat resistance enough to withstand at least heat treatment performed later. For example, a glass substrate, a ceramic substrate, a quartz substrate, or a sapphire substrate may be used as the substrate 100. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like, a compound semiconductor substrate made of silicon germanium or the like, a silicon-on-insulator (SOI) substrate, or the like may be used as the substrate 100. Still alternatively, any of these substrates further provided with a semiconductor element may be used as the substrate 100.

[0071]

As the substrate 100, a flexible substrate may be used. In that case, the transistor may be formed directly over the flexible substrate. Note that to provide a transistor on the flexible substrate, there is also a method in which a transistor is formed over a non-flexible substrate, and the transistor is separated and transferred to the substrate 100 which is a flexible substrate. In that case, a separation layer is preferably provided between the non-flexible substrate and the transistor.

[0072]

The gate electrode 104 may be formed to have a single layer structure or a stacked structure, using at least one of the following materials: Al, Ti, Cr, Co, Ni, Cu, Y, Zr, Mo, Ag, Ta, and W; a nitride of any of these elements; an oxide of any of these elements; and an alloy of any of these elements. Further, in the case where an oxide is used as the gate electrode 104, the oxide may include nitrogen which is greater than or equal to $5 \times 10^{19} \text{ cm}^{-3}$ and less than or equal to 20 atomic%, preferably greater than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and less than or equal to 7 atomic%. For example, an oxide film which contains nitrogen at higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal

to 7 at.% and also contains In, Ga, and Zn may be used. Since an oxide film has higher resistance than a metal film, in the case of using an oxide film as the gate electrode 104, it is preferable to use a stacked structure of the oxide film and a low-resistance film with a sheet resistance of 10 Ω/sq or lower in order to reduce resistance of the whole gate electrode 104. The concentration which is represented by the unit cm^{-3} can be quantified by secondary ion mass spectrometry (SIMS), and the concentration which is represented by the unit atomic% can be quantified by X-ray photoelectron spectroscopy (XPS).

[0073]

In FIGS. 1A to 1C, the gate electrode 104 is larger than the oxide semiconductor film 106 in length and width, so that degradation and generation of electric charge due to light are suppressed in the oxide semiconductor film 106; however, the present invention is not limited to this structure. For example, the oxide semiconductor film 106 may be larger than the gate electrode 104 in length and width in the top view.

[0074]

The pair of electrodes 116 may be formed with a single layer structure or a stacked structure using a metal film, a metal nitride film, a metal oxide film, an alloy film, or the like given for the gate electrode 104.

[0075]

When a film containing Cu is used for the pair of electrodes 116, the resistance of a wiring can be reduced, and generation of wiring delays or the like even in a large-sized display device can be reduced. In the case of using Cu for the pair of electrodes 116, the adhesion depends on the material of the substrate 100; in such a case, it is preferable to employ a stacked-layer structure using a film having favorable adhesion property to the substrate 100. As a film with high adhesion to the substrate 100, a film containing Ti, Mo, Mn, Al, or the like may be used. For example, a Cu-Mn-Al alloy may be used.

[0076]

Next, a method for manufacturing the transistor illustrated in FIGS. 1A to 1C is described with reference to FIGS. 14A to 14D.

[0077]

First, a conductive film is formed over the substrate 100 by a sputtering method, an evaporation method, or the like, and is processed to form the gate electrode 104. Next, the gate insulating film 112 covering the gate electrode 104 is formed (see FIG. 14A).

[0078]

Next, an oxide semiconductor film is formed over the gate electrode 104 with the gate insulating film 112 provided therebetween, and is processed to form the oxide semiconductor film 106 (see FIG. 14B).

[0079]

Then, a resist mask or the like is formed over the oxide semiconductor film 106, and at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ is added to a part of the oxide semiconductor film 106. By the addition, a microvoid can be formed in the part of the oxide semiconductor film 106. Then, heat treatment at a temperature higher than or equal to 200°C and lower than or equal to 700°C , preferably at a temperature higher than or equal to 300°C and lower than or equal to 650°C is performed thereon, so that hydrogen is captured in the microvoid. In this manner, the channel region 105, the source region 107a, and the drain region 107b are formed (see FIG. 14C).

[0080]

Next, a conductive film is formed by a sputtering method, an evaporation method, or the like, and is processed to form a pair of electrodes 116 to be in contact with a part of the oxide semiconductor film 106. Moreover, the interlayer insulating film 118 may be formed over the oxide semiconductor film 106 and the pair of electrodes 116 (see FIG. 14D).

[0081]

As described above, a microvoid can be formed by adding an ion to a part of the oxide semiconductor film 106, and hydrogen can be captured in the microvoid by

heat treatment, thereby a resistance in the vicinity of a formation region of the microvoid is reduced to form the source region 107a and the drain region 107b. At the same time, hydrogen is removed from the region in the oxide semiconductor film 106 other than the source region 107a and the drain region 107b to form the channel region 105 which is high purified. Accordingly, a high reliability semiconductor device having stable electric characteristics, in which the off-state current of the transistor is extremely small, can be manufactured.

[0082]

Through the above-described process, the transistor illustrated in FIGS. 1A to 1C can be manufactured.

[0083]

This embodiment can be implemented in appropriate combination with the other embodiments.

[0084]

(Embodiment 3)

In this embodiment, a transistor having a structure different from that of the transistor described in Embodiments 2 is described.

[0085]

FIGS. 2A to 2C are a top view and cross-sectional views of the transistor. A cross section along dashed-dotted line A-B in FIG. 2A and a cross section along dashed-dotted line C-D in FIG. 2A correspond to a cross section A-B in FIG. 2B and a cross section C-D in FIG. 2C, respectively.

[0086]

The cross section A-B in FIG. 2B is described in detail below.

[0087]

The transistor includes a substrate 100, a gate electrode 104 over the substrate 100, a gate insulating film 112 covering the gate electrode 104, a pair of electrodes 216 over the gate insulating film 112, and an oxide semiconductor film 206 including a channel region 205, a source region 207a, and a drain region 207b, which is over the gate electrode 104 with the gate insulating film 112 provided therebetween and partly in contact with the pair of electrodes 216. Note that an interlayer insulating film 218 over the gate insulating film 112, the pair of electrodes 216, and the oxide

semiconductor film 206 is preferably provided, so that the oxide semiconductor film 206 is not exposed. Here, the pair of electrodes 216, the oxide semiconductor film 206, and the interlayer insulating film 218 may be referred to the pair of electrodes 116, the oxide semiconductor film 106, and the interlayer insulating film 118 described in Embodiment 2, respectively.

[0088]

The source region 207a and the drain region 207b are referred to the source region 107a and the drain region 107b described in Embodiment 2. That is, by adding at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ to a part of the oxide semiconductor film 206, a microvoid is provided in the oxide semiconductor film 206, and by capturing hydrogen in the microvoid, the source region 207a and the drain region 207b are formed. Further, hydrogen is removed from the region of the oxide semiconductor film 206 other than the source region 207a and the drain region 207b, so that the channel region 205 which is high purified can be formed.

[0089]

In FIGS. 2A to 2C, the gate electrode 104 is larger than the oxide semiconductor film 206 in length and width, so that degradation and generation of electric charge due to light are suppressed in the oxide semiconductor film 206; however, the present invention is not limited to this structure. For example, the oxide semiconductor film 206 may be larger than the gate electrode 104 in length and width in the top view.

[0090]

Next, a method for manufacturing the transistor illustrated in FIGS. 2A to 2C is described with reference to FIGS. 15A to 15D.

[0091]

First, a conductive film is formed over the substrate 100 by a sputtering method, an evaporation method, or the like, and is processed to form the gate electrode 104.

Then, the gate insulating film 112 covering the gate electrode 104 is formed. Next, a conductive film is formed over the gate insulating film 112 by a sputtering method, an evaporation method, or the like, and is processed to form the pair of electrodes 216 (see FIG. 15A).

5 [0092]

Next, an oxide semiconductor film is formed over the gate electrode 104 with the gate insulating film 112 provided therebetween, and is processed to form the oxide semiconductor film 206 which is partly in contact with the pair of electrodes 216 (see FIG. 15B).

10 [0093]

Then, a resist mask or the like is formed over the oxide semiconductor film 206, and at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ is added to a part of the oxide semiconductor film 206. By the addition, a microvoid can be formed in the part of the oxide semiconductor film 206. Then, heat treatment at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, preferably higher than or equal to 300 °C and lower than equal to 650 °C is performed thereon, thereby hydrogen can be captured in the microvoid. In this manner, the channel region 205, the source region 207a, and the drain region 207b are formed (see FIG. 15C).

[0094]

Moreover, the interlayer insulating film 218 can be formed over the oxide semiconductor film 206 and the pair of electrodes 216 (see FIG. 15D).

[0095]

Through the above-described process, the transistor illustrated in FIGS. 2A to 2C can be manufactured.

[0096]

30 This embodiment can be implemented in appropriate combination with the other embodiments.

[0097]

(Embodiment 4)

In this embodiment, a transistor having a structure which is different from the structures of the transistors described in Embodiments 2 and 3 is described.

5 [0098]

FIGS. 3A to 3C are a top view and cross-sectional views of a transistor. A cross section along dashed-dotted line A-B in FIG. 3A and a cross section along dashed-dotted line C-D in FIG. 3A correspond to a cross section A-B in FIG. 3B and a cross section C-D in FIG. 3C, respectively.

10 [0099]

The cross section A-B in FIG. 3B is described in detail below.

[0100]

The transistor includes a substrate 100, a base insulating film 302 over the substrate 100, an oxide semiconductor film 306 including a channel region 305, a source region 307a, and a drain region 307b over the base insulating film 302, a pair of electrodes 316 which is over the oxide semiconductor film 306 and partly in contact with the oxide semiconductor film 306, a gate insulating film 312 over the oxide semiconductor film 306 and the pair of electrodes 316, and a gate electrode 304 over the oxide semiconductor film 306 with the gate insulating film 312 provided therebetween.

20 Note that the base insulating film 302 is not necessarily provided, which depends on the surface condition of the substrate 100. Here, the pair of electrodes 316, the oxide semiconductor film 306, the gate electrode 304, and the gate insulating film 312 may be referred to the pair of electrodes 116, the oxide semiconductor film 106, the gate electrode 104, and the gate insulating film 112 described in Embodiment 2, respectively.

25 [0101]

The source region 307a and the drain region 307b are referred to the source region 107a and the drain region 107b described in Embodiment 2. That is, by adding at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than

30

or equal to $3 \times 10^{22} \text{ cm}^{-3}$ to a part of the oxide semiconductor film 306, a microvoid is provided in the oxide semiconductor film 306, and by capturing hydrogen in the microvoid, the source region 307a and the drain region 307b are formed. Further, hydrogen is removed from the region of the oxide semiconductor film 306 other than the source region 307a and the drain region 307b, so that the channel region 305 which is high purified can be formed.

[0102]

Further, the base insulating film 302 can have the same structure as the gate insulating film 312.

[0103]

In FIGS. 3A to 3C, the gate electrode 304 is larger than the oxide semiconductor film 306 in length and width, so that degradation and generation of electric charge due to light are suppressed in the oxide semiconductor film 306; however, the present invention is not limited to this structure. For example, the oxide semiconductor film 306 may be larger than the gate electrode 304 in length and width in the top view.

[0104]

Next, a method for manufacturing the transistor illustrated in FIGS. 3A to 3C is described with reference to FIGS. 16A to 16D.

[0105]

First, the base insulating film 302 is formed over the substrate 100. Next, an oxide semiconductor film is formed over the base insulating film 302, and is processed to form the oxide semiconductor film 306 (see FIG. 16A). Note that the base insulating film 302 is not necessarily provided, which depends on the surface condition of the substrate 100.

[0106]

Then, a resist mask or the like is formed over the oxide semiconductor film 306, and at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than

or equal to $3 \times 10^{22} \text{ cm}^{-3}$ is added to a part of the oxide semiconductor film 306. By the addition, a microvoid can be formed in the part of the oxide semiconductor film 306. Then, heat treatment at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, preferably higher than or equal to 300 °C and lower than or equal to 650 °C is performed thereon, thereby hydrogen can be captured in the microvoid. In this manner, the channel region 305, the source region 307a, and the drain region 307b are formed (see FIG. 16B).

[0107]

Next, a conductive film is formed over the oxide semiconductor film 306 by a sputtering method, an evaporation method, or the like, and is processed to form the pair of electrodes 316 which is partly in contact with the oxide semiconductor film 306 (see FIG. 16C).

[0108]

Then, a gate insulating film 312 is formed over the oxide semiconductor film 306 and the pair of electrodes 316. Next, a conductive film is formed by a sputtering method, an evaporation method, or the like, and is processed to form the gate electrode 304 overlapping with the oxide semiconductor film 306 with the gate insulating film 312 interposed therebetween (see FIG. 16D).

[0109]

Through the above-described process, the transistor illustrated in FIGS. 3A to 3C can be manufactured.

[0110]

This embodiment can be implemented in appropriate combination with the other embodiments.

[0111]

(Embodiment 5)

In this embodiment, a transistor having a structure partly different from that of the transistor described in Embodiments 4 is described.

[0112]

FIGS. 4A to 4C are a top view and cross-sectional views of a transistor. A cross section along dashed-dotted line A-B in FIG. 4A and a cross section along

dashed-dotted line C-D in FIG. 4A correspond to a cross section A-B in FIG. 4B and a cross section C-D in FIG. 4C, respectively.

[0113]

The cross section A-B in FIG. 4B is described in detail below.

5 [0114]

The transistor includes a substrate 100, a base insulating film 302 over the substrate 100, an oxide semiconductor film 406 including a region 405a, a region 405b, a region 405c, a region 407a, and a region 407b over the base insulating film 302, a pair of electrodes 316 which is over the oxide semiconductor film 406 and partly in contact
10 with the oxide semiconductor film 406, a gate insulating film 312 over the oxide semiconductor film 406 and the pair of electrodes 316, and a gate electrode 404 which is not overlapped with the pair of electrodes 316 and is over the oxide semiconductor film 406 with the gate insulating film 312 provided therebetween. Note that the base insulating film 302 is not necessarily provided, which depends on a surface condition of
15 the substrate 100. The oxide semiconductor film 406 and the gate electrode 404 are referred to the oxide semiconductor film 106 and the gate electrode 104 described in Embodiment 2.

[0115]

The region 407a and the region 407b each have a sheet resistance value higher
20 than or equal to that each of the source region 107a and the drain region 107b described in Embodiment 2 and lower than or equal to that each of the region 405a, the region 405b, and the region 405c. By adding at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and
25 lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ to a part of the oxide semiconductor film 406, a microvoid is provided in the oxide semiconductor film 406, and by capturing hydrogen in the microvoid, the region 407a and the region 407b are formed. Further, hydrogen is removed from the region of the oxide semiconductor
30 film 406 other than the region 407a and the region 407b (the region 405a, the region 405b, and the region 405c), so that the channel region which is high purified can be

formed.

[0116]

The resistance of the region 407a and the region 407b is higher than that of the source region 107a and the drain region 107b described in Embodiment 2, and lower than any concentration of the region 405a, the region 405b, and the region 405c, thereby deterioration caused by hot carriers or the like can be suppressed even when the transistor is miniaturized, and a short-channel effect can be reduced.

[0117]

Next, a method for manufacturing the transistor illustrated in FIGS. 4A to 4C is described with reference to FIGS. 17A to 17D.

[0118]

First, the base insulating film 302 is formed over the substrate 100. Next, an oxide semiconductor film is formed over the base insulating film 302 and is processed to form the oxide semiconductor film 406 (see FIG. 17A). Note that the base insulating film 302 is not necessarily provided, which depends on the surface condition of the substrate 100.

[0119]

Next, a conductive film is formed over the oxide semiconductor film 406 by a sputtering method, an evaporation method, or the like, and is processed to form the pair of electrodes 316 (see FIG. 17B).

[0120]

Then, a gate insulating film 312 is formed over the oxide semiconductor film 406 and the pair of electrodes 316. Next, a conductive film is formed thereon by a sputtering method, an evaporation method, or the like, and is processed to form a gate electrode 404 which overlaps with the oxide semiconductor film 406 with the gate insulating film 312 provided therebetween and does not overlap with the pair of electrodes 316 (see FIG. 17C).

[0121]

Then, with the use of the gate electrode 404 and the pair of the electrodes 316 as a mask, at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a

concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ is added to a part of the oxide semiconductor film 406. By the addition, a microvoid can be formed in the part of the oxide semiconductor film 406. Then, heat treatment at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, preferably at a temperature higher than or equal to 300 °C and lower than or equal to 650 °C is performed thereon, thereby hydrogen can be captured in the microvoid. In this manner, the region 405a, the region 405b, the region 405c, the region 407a, and the region 407b are formed (see FIG. 17D).

10 [0122]

Through the above-described process, the transistor illustrated in FIGS. 4A to 4C can be manufactured.

[0123]

This embodiment can be implemented in appropriate combination with the other embodiments.

15 [0124]

(Embodiment 6)

In this embodiment, a transistor having a structure different from that of the transistor described in Embodiments 2 to 5 is described.

20 [0125]

FIGS. 5A to 5C are a top view and cross-sectional views of a transistor. A cross section along dashed-dotted line A-B in FIG. 5A and a cross section along dashed-dotted line C-D in FIG. 5A correspond to a cross section A-B in FIG. 5B and a cross section C-D in FIG. 5C, respectively.

25 [0126]

The cross section A-B in FIG. 5B is described in detail below.

[0127]

The transistor includes a substrate 100, a base insulating film 302 over the substrate 100, a pair of electrodes 516 over the base insulating film 302, an oxide semiconductor film 506 including a channel region 505, a source region 507a, and a drain region 507b, which is over the pair of electrodes 516 and partly in contact with the

pair of electrodes 516, a gate insulating film 512 over the oxide semiconductor film 506 and the pair of electrodes 516, and a gate electrode 504 over the oxide semiconductor film 506 with the gate insulating film 512 provided therebetween. Note that the base insulating film 302 is not necessarily provided, which depends on a surface condition of the substrate 100. Here, the pair of electrodes 516, the oxide semiconductor film 506, the gate electrode 504, and the gate insulating film 512 may be referred to the pair of electrodes 116, the oxide semiconductor film 106, the gate electrode 104, and the gate insulating film 112 described in Embodiment 2, respectively.

[0128]

Here, the source region 507a and the drain region 507b are referred to the source region 107a and the drain region 107b described in Embodiment 2. That is, by adding at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ to a part of the oxide semiconductor film 506, a microvoid is provided in the oxide semiconductor film 506, and by capturing hydrogen in the microvoid, the source region 507a and the drain region 507b are formed. Further, hydrogen is removed from the region of the oxide semiconductor film 506 other than the source region 507a and the drain region 507b, so that the channel region 505 which is high purified can be formed.

[0129]

In FIGS. 5A to 5C, the gate electrode 504 is larger than the oxide semiconductor film 506 in length and width, so that degradation and generation of electric charge due to light are suppressed in the oxide semiconductor film 506; however, the present invention is not limited to this structure. For example, the oxide semiconductor film 506 may be larger than the gate electrode 504 in length and width in the top view.

[0130]

Next, a method for manufacturing the transistor illustrated in FIGS. 5A to 5C is described with reference to FIGS. 18A to 18D.

[0131]

First, the base insulating film 302 is formed over the substrate 100. Next, a conductive film is formed over the base insulating film 302 by a sputtering method, an evaporation method, or the like, and is processed to form the pair of electrodes 516 (see FIG. 18A). Note that the base insulating film 302 is not necessarily provided, which depends on a surface condition of the substrate 100.

[0132]

Next, an oxide semiconductor film is formed, and is processed to form the oxide semiconductor film 506, which is partly in contact with the pair of electrodes 516 (see FIG. 18B).

[0133]

Then, a resist mask or the like is formed over the oxide semiconductor film 506, and at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ is added to a part of the oxide semiconductor film 506. By the addition, a microvoid can be formed in the part of the oxide semiconductor film 506. Then, heat treatment at a temperature higher than or equal to 200°C and lower than or equal to 700°C , preferably at a temperature higher than or equal to 300°C and lower than or equal to 650°C is performed thereon, thereby hydrogen can be captured in the microvoid. In this manner, the channel region 505, the source region 507a, and the drain region 507b are formed (see FIG. 18C).

[0134]

Then, a gate insulating film 512 is formed over the oxide semiconductor film 506 and the pair of electrodes 516. Next, a conductive film is formed thereon by a sputtering method, an evaporation method, or the like, and is processed to form the gate electrode 504 overlapping with the oxide semiconductor film 506 with the gate insulating film 512 provided therebetween (see FIG. 18D).

[0135]

Through the above-described process, the transistor illustrated in FIGS. 5A to

5C can be manufactured.

[0136]

This embodiment can be implemented in appropriate combination with the other embodiments.

5 [0137]

(Embodiment 7)

In this embodiment, a transistor having a structure different from that of the transistor described in Embodiments 2 to 6 is described.

[0138]

10 FIGS. 6A to 6C are a top view and cross-sectional views of a transistor included in a semiconductor device in one embodiment of the present invention. A cross section along dashed-dotted line A-B in FIG. 6A and a cross section along dashed-dotted line C-D in FIG. 6A correspond to a cross section A-B in FIG. 6B and a cross section C-D in FIG. 6C, respectively.

15 [0139]

The cross section A-B in FIG. 6B is described in detail below.

[0140]

The transistor includes a substrate 100, a base insulating film 302 over the substrate 100, an oxide semiconductor film 606 including a channel region 605, a source region 607a, and a drain region 607b over the base insulating film 302, a gate insulating film 612 over the oxide semiconductor film 606, a gate electrode 604 overlapping with the channel region 605 with the gate insulating film 612 interposed therebetween, an interlayer insulating film 618 over the oxide semiconductor film 606 and the gate electrode 604, and a pair of electrodes 616 which is in contact with the oxide semiconductor film 606 through opening portions formed in the gate insulating film 612 and the interlayer insulating film 618. Note that the base insulating film 302 is not necessarily provided, which depends on a surface condition of the substrate 100. Here, the pair of electrodes 616, the oxide semiconductor film 606, the gate electrode 604, the interlayer insulating film 618, and the gate insulating film 612 may be referred to the pair of electrodes 116, the oxide semiconductor film 106, the gate electrode 104, the interlayer insulating film 118, and the gate insulating film 112 described in Embodiment 2, respectively.

20

25

30

[0141]

Although not illustrated, the gate insulating film 612 and the gate electrode 604 may have substantially the same shape seen from the top surface. The shape can be obtained by processing the gate electrode 604 and the gate insulating film 612 together with use of one mask. Alternatively, the shape can be obtained by processing the gate insulating film 612 with use of the gate electrode 604 as a mask.

[0142]

In FIGS. 6A to 6C, although the shape of the opening portion provided in the gate insulating film 612 and the interlayer insulating film 618 has a circular shape when seen from the above, the present invention is not limited thereto. There is no particular limitation on the shape of the opening portions, as long as the opening portions expose the source region 607a and the drain region 607b.

[0143]

The channel region 605 and the gate electrode 604 may have substantially the same shape when seen from the above. This shape is obtained by forming the source region 607a and the drain region 607b of the oxide semiconductor film 606 with the use of the gate insulating film 612 or the gate electrode 604 as a mask. Here, the gate electrode 604 is used as the mask, and at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ is added to a part of the oxide semiconductor film 406, whereby the oxide semiconductor film 606 is provided with a microvoid, and hydrogen is captured in the microvoid, so that the source region 607a and the drain region 607b are formed. At the same time, hydrogen is removed from the region of the oxide semiconductor film 606 other than the source region 607a and the drain region 607b, so that the channel region 605 which is high purified can be formed.

[0144]

Next, a method for manufacturing the transistor illustrated in FIGS. 6A to 6C is described with reference to FIGS. 19A to 19D.

[0145]

First, the base insulating film 302 is formed over the substrate 100. Next, an oxide semiconductor film is formed over the base insulating film 302, and is processed to form the oxide semiconductor film 606 (see FIG. 19A). Note that the base insulating film 302 is not necessarily provided, which depends on a surface condition of the substrate 100.

[0146]

Next, the gate insulating film 612 is formed by a sputtering method, a plasma CVD method, or the like. Then, a conductive film is formed by a sputtering method, an evaporation method, or the like. A resist mask or the like is formed over the conductive film, and the conductive film is processed, thereby the gate electrode 604 is formed (see FIG. 19B). Note that after formation of the gate electrode 604, the width of the gate electrode 604 may be narrowed by performing plasma treatment or chemical treatment.

[0147]

Then, with the use of the gate electrode 604 as a mask, at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ is added to a part of the oxide semiconductor film 606. By the addition, a microvoid can be formed in the part of the oxide semiconductor film 606. Then, heat treatment at a temperature higher than or equal to 200°C and lower than or equal to 700°C , preferably at a temperature higher than or equal to 300°C and lower than or equal to 650°C is performed thereon, thereby hydrogen can be captured in the microvoid. In this manner, the channel region 605, the source region 607a, and the drain region 607b are formed (see FIG. 19C).

[0148]

Next, the interlayer insulating film 618 is formed over the oxide semiconductor film 606 and the gate electrode 604, and the opening portions in which the source region 607a and the drain region 607b are exposed is formed in the gate insulating film

612 and the interlayer insulating film 618. Then, a conductive film is formed by a sputtering method, an evaporation method, or the like, and is processed to form the pair of electrodes 616 which is in contact with the oxide semiconductor film 606 (see FIG. 19D).

5 [0149]

In FIGS. 19A to 19D, although the shape of the opening portion provided in the gate insulating film 612 and the interlayer insulating film 618 has a circular shape when seen from the above, the present invention is not limited thereto. There is no particular limitation on the shape of the opening portion, as long as the opening portions expose
10 the source region 607a and the drain region 607b.

[0150]

Through the above-described process, the transistor illustrated in FIGS. 6A to 6C can be manufactured.

[0151]

15 This embodiment can be implemented in appropriate combination with the other embodiments.

[0152]

(Embodiment 8)

In this embodiment, a transistor having a structure different from that of the
20 transistor described in Embodiments 2 to 7 is described.

[0153]

FIGS. 7A to 7C are a top view and cross-sectional views of a transistor. A cross section along dashed-dotted line A-B in FIG. 7A and a cross section along dashed-dotted line C-D in FIG. 7A correspond to a cross section A-B in FIG. 7B and a
25 cross section C-D in FIG. 7C, respectively.

[0154]

The cross-section A-B of FIG. 7B is described in detail below.

[0155]

The transistor includes a substrate 100, a gate electrode 704 over the substrate
30 100, a gate insulating film 712 covering the gate electrode 704, an oxide semiconductor film 706 including a channel region 705, a source region 707a, and a drain region 707b over the gate electrode 704 with the gate insulating film 712 provided therebetween, the

interlayer insulating film 718 over the oxide semiconductor film 706 and the gate insulating film 712 including opening portions in which the source region 707a and the drain region 707b are exposed, and a pair of electrodes 716 which is in contact with the oxide semiconductor film 706 through the opening portions provided in the interlayer insulating film 718. Here, the pair of electrodes 716, the oxide semiconductor film 706, the gate electrode 704, the interlayer insulating film 718, and the gate insulating film 712 may be referred to the pair of electrodes 116, the oxide semiconductor film 106, the gate electrode 104, the interlayer insulating film 118, and the gate insulating film 112 described in Embodiment 2, respectively.

10 [0156]

In FIGS. 7A to 7C, the gate electrode 704 and the channel region 705 have substantially the same shape when seen from the above; however, the present invention is not limited thereto. The gate electrode 704 and the channel region 705 may have different shapes from each other.

15 [0157]

Here, a resist mask or the like is used, and at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ is added to the oxide semiconductor film 706, whereby the oxide semiconductor film 706 is provided with a microvoid, and hydrogen is captured in the microvoid, so that the source region 707a and the drain region 707b are formed. At the same time, hydrogen is removed from the region of the oxide semiconductor film 706 other than the source region 707a and the drain region 707b, so that the channel region 705 which is high purified can be formed. The resist mask or the like may be formed by a back exposure technique with the use of the gate electrode 704 as a mask. In that case, an area where the source region 707a overlaps with the gate electrode 704 and an area where the drain region 707b overlaps with the gate electrode 704 can be reduced, and thus the parasitic capacitance is reduced, so that the operation speed of the transistor can be increased. In addition, the number of photomasks used for forming a resist mask can be reduced,

whereby the manufacturing cost for the transistor can be reduced, which is preferable.

[0158]

Next, a method for manufacturing the transistor illustrated in FIGS. 7A to 7C is described with reference to FIGS. 20A to 20D.

5 [0159]

First, a conductive film is formed over the substrate 100 by a sputtering method, an evaporation method, or the like, and is processed to form the gate electrode 704. Then, the gate insulating film 712 covering the gate electrode 704 is formed (see FIG. 20A).

10 [0160]

Next, an oxide semiconductor film is formed, and is processed to form the oxide semiconductor film 706 (see FIG. 20B).

[0161]

Then, a resist mask is used, at least one of a nitrogen ion having a concentration higher than or equal to $1 \times 10^{19} \text{ cm}^{-3}$ and lower than or equal to $1 \times 10^{22} \text{ cm}^{-3}$, a hydrogen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$, and an oxygen ion having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$ is added to a part of the oxide semiconductor film 706. By the addition, a microvoid can be formed in a part of the oxide semiconductor film 706. Then, heat treatment performing at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, preferably at a temperature higher than or equal to 300 °C and lower than or equal to 650 °C, hydrogen can be captured in the microvoid, and the channel region 705, the source region 707a, and the drain region 707b are formed (see FIG. 20C).

25 [0162]

Next, the interlayer insulating film 718 is formed over the oxide semiconductor film 706 and the gate insulating film 712, and opening portions in which the source region 707a and the drain region 707b is exposed is formed. Then, a conductive film is formed by a sputtering method, an evaporation method, or the like, and the conductive film is processed to form the pair of electrodes 716 which is in contact with the oxide semiconductor film 706 (see FIG. 20D).

[0163]

Through the above-described process, the transistor illustrated in FIGS. 7A to 7C can be manufactured.

[0164]

5 This embodiment can be implemented in appropriate combination with the other embodiments.

[0165]

(Embodiment 9)

10 In this embodiment, a liquid crystal display device manufactured using any of the transistors described in Embodiments 2 to 8 is described. Note that an example in which one embodiment of the present invention is applied to a liquid crystal display device is described in this embodiment; however, the present invention is not limited to this embodiment. For example, application of one embodiment of the present invention to an electroluminescence (EL) display device is readily conceived by those skilled in the art.

[0166]

FIG. 8 is a circuit diagram of an active matrix liquid crystal display device. The liquid crystal display device includes source lines SL₁ to SL_a, gate lines GL₁ to GL_b, and a plurality of pixels 2200. The pixels 2200 each include a transistor 2230, a capacitor 2220, and a liquid crystal element 2210. The plurality of pixels 2200 with such a structure forms a pixel portion of the liquid crystal display device. In the case where the source line or the gate line is simply mentioned, it is denoted as the source line SL or the gate line GL.

[0167]

25 As the transistor 2230, any of the transistors described in Embodiments 2 to 8 is used. Since an oxide semiconductor is used for any transistor which is one embodiment of the present invention, the transistor has excellent electric characteristics, whereby a display device with high image quality can be provided.

[0168]

30 The gate line GL is connected to a gate of the transistor 2230, the source line SL is connected to a source electrode of the transistor 2230, and a drain electrode of the

transistor 2230 is connected to one capacitor electrode of the capacitor 2220 and one pixel electrode of the liquid crystal element 2210. The other capacitor electrode of the capacitor 2220 and the other pixel electrode of the liquid crystal element 2210 are connected to a common electrode. Note that the common electrode may be formed in the same layer as the gate line GL using the same material as the gate line GL.

[0169]

Further, the gate line GL is connected to a gate driver circuit. The gate driver circuit may include any of the transistors described in Embodiments 2 to 8.

[0170]

The source line SL is connected to a source driver circuit. The source driver circuit may include any of the transistors described in Embodiments 2 to 8.

[0171]

Note that either or both of the gate driver circuit and the source driver circuit may be formed separately and connected using a method such as chip on glass (COG), wire bonding, or tape automated bonding (TAB).

[0172]

Since a transistor is easily broken by static electricity or the like, a protection circuit is preferably provided. The protection circuit is preferably formed using a nonlinear element.

[0173]

When a voltage is applied to the gate line GL to be higher than or equal to the threshold voltage of the transistor 2230, electric charge supplied from the source line SL flows as a drain current of the transistor 2230 and is stored in the capacitor 2220. After charging for one row is performed, the transistors 2230 in the row are turned off, and the voltage is not given from the source line SL. However, the necessary voltage can be held by the electric charge stored in the capacitor 2220. Then, the capacitors 2220 in the next row are charged. In such a manner, charging for the first row to b -th row is performed.

[0174]

In the case of using a transistor having a small off-state current as the transistor 2230, the period for which the voltage can be kept can be lengthened. By this effect, the display rewriting frequency can be reduced in the case of displaying an image with

little motion (including a still image); accordingly, further reduction of the power consumption is possible. Further, the capacitance of the capacitor 2220 can be further reduced; accordingly, power consumed for charging can be reduced.

[0175]

5 As described above, according to one embodiment of the present invention, a liquid crystal display device with high image quality and low power consumption can be provided.

[0176]

10 This embodiment can be implemented in appropriate combination with the other embodiments.

[0177]

(Embodiment 10)

In this embodiment, an example of manufacturing a semiconductor memory device using the transistor described in Embodiments 2 to 8 is described.

15 [0178]

Typical examples of a volatile semiconductor memory device include a dynamic random access memory (DRAM) which stores data in such a manner that a transistor included in a memory element is selected and electric charge is accumulated in a capacitor, and a static random access memory (SRAM) which holds stored data using a circuit such as a flip-flop.

20 [0179]

A typical example of a nonvolatile semiconductor memory device includes a flash memory which has a node between a gate and a channel formation region of a transistor and stores data by holding electric charge in the node.

25 [0180]

Any of the transistors described in Embodiments 2 to 8 can be applied to part of transistors included in the above-described semiconductor memory device.

[0181]

30 First, a memory cell which is the semiconductor memory device to which the transistor described in Embodiments 2 to 8 is applied is described with reference to FIGS. 9A and 9B.

[0182]

The memory cell includes a bit line BL, a word line WL, a sense amplifier SAmpl, a transistor Tr, and a capacitor C (see FIG. 9A).

[0183]

It is known that the potential held in the capacitor is gradually decreased with time as shown in FIG. 9B owing to the off-state current of the transistor Tr. After a certain period of time, the potential originally charged from V_0 to V_1 is decreased to V_A which is a limit for reading data 1. This period is called a holding period T_1 . In the case of a two-level memory cell, refresh needs to be performed within the holding period T_1 .

[0184]

When the transistor described in Embodiments 2 to 8 is employed as the transistor Tr, the holding period T_1 can be made longer because the off-state current of the transistor is small. That is, frequency of the refresh operation can be reduced; thus, power consumption can be reduced. For example, when a memory cell is formed using a transistor in which the off-state current is less than or equal to 1×10^{-21} A, preferably less than or equal to 1×10^{-24} A, data can be held for several days to several decades without supply of power.

[0185]

As described above, using one embodiment of the present invention, a semiconductor memory device having high reliability and low power consumption can be provided.

[0186]

Next, a memory cell included in a semiconductor memory device to which any of the transistors described in Embodiments 2 to 8 is applied is described with reference to FIGS. 10A and 10B.

[0187]

FIG. 10A is a circuit diagram of a memory cell. The memory cell includes a transistor Tr₁, a gate line GL₁ connected to a gate of the transistor Tr₁, a source line SL₁ connected to a source of the transistor Tr₁, a transistor Tr₂, a source line SL₂ connected to a source of the transistor Tr₂, a drain line DL₂ connected to a drain of the transistor Tr₂, a capacitor C, a capacitor line CL connected to one of ends of the

capacitor C, and a node N connected to the other end of the capacitor C, a drain of the transistor Tr₁, and a gate of the transistor Tr₂.

[0188]

The semiconductor memory cell described in this embodiment utilizes variation in an apparent threshold voltage of the transistor Tr₂, which depends on the potential of the node N. For example, FIG. 10B shows a relation between a potential V_{CL} of the capacitor wiring CL and a drain current I_{ds_2} flowing through the transistor Tr₂.

[0189]

The voltage of the node N can be controlled through the transistor Tr₁. For example, the potential of the source line SL₁ is set to V_{DD} . In this case, when the voltage of the gate line GL₁ is set to be higher than or equal to the potential obtained by adding V_{DD} to the threshold voltage V_{th} of the transistor Tr₁, the potential of the node N can be HIGH. Further, when the potential of the gate line GL₁ is set to be lower than or equal to the threshold voltage V_{th} of the transistor Tr₁, the potential of the node N can be LOW.

[0190]

Thus, either a V_{CL} - I_{ds_2} curve (N = LOW) or a V_{CL} - I_{ds_2} curve (N = HIGH) can be obtained. That is, when N = LOW, the I_{ds_2} is small at a V_{CL} of 0V; accordingly, data 0 is stored. Further, when N = HIGH, the I_{ds_2} is large at a V_{CL} of 0V; accordingly, data 1 is stored. In this manner, data can be stored.

[0191]

Since the off-state current of any of the transistors described in Embodiments 2 to 8 can be made to be extremely small, if the transistor is used as the transistor Tr₁ here, unintentional leak of electric charge accumulated in the node N between the source and the drain of the transistor Tr₁ can be suppressed. Therefore, data can be held for a long period.

[0192]

Note that any of the transistors described in Embodiments 2 to 8 may also be applied to the transistor Tr₂.

[0193]

Next, the memory cell included in the semiconductor memory device shown in FIGS. 10A and 10B without the capacitor is described with reference to FIG. 11.

[0194]

FIG. 11 is a circuit diagram of a memory cell. The memory cell includes a transistor Tr₁, a gate line GL₁ connected to a gate of the transistor Tr₁, a source line SL₁ connected to a source of the transistor Tr₁, a transistor Tr₂, a source line SL₂ connected to a source of the transistor Tr₂, a drain line DL₂ connected to a drain of the transistor Tr₂, a gate of the transistor Tr₂ connected to a drain of the transistor Tr₁, and a node N connected to the drain of the transistor Tr₁ and the gate of the transistor Tr₂.

[0195]

In the case where the normally off transistor whose off-state current is extremely small is used as the transistor Tr₁, electric charge can be held in the node N which is between the drain of the transistor Tr₁ and the gate of the transistor Tr₂ without the capacitor. The structure without the capacitor makes it possible to reduce an area of a memory cell, so that the integration degree of a memory module using the memory cell can be more increased than that of the structure with a capacitor. However, in the case where the transistor Tr₁ is normally on or the off-state current is a little large, the threshold voltage of the transistor Tr₁ can be controlled by providing a backgate, a transistor, or a diode.

[0196]

Although the semiconductor memory device including four or five wirings is described in this embodiment, a structure of the nonvolatile memory is not limited thereto. For example, a structure in which one wiring functions as the source line SL₁ and the drain line DL₂ may be employed.

[0197]

As described above, according to one embodiment of the present invention, a semiconductor memory device with high reliability for a long period, low power consumption, and a high degree of integration can be obtained.

[0198]

This embodiment can be implemented in appropriate combination with the

other embodiments.

[0199]

(Embodiment 11)

A central processing unit (CPU) can be formed using a transistor including an
5 oxide semiconductor in an active layer for at least part of the CPU.

[0200]

FIG. 12A is a block diagram illustrating a specific structure of a CPU. The
CPU shown in FIG. 12A includes an arithmetic logic unit (ALU) 1191, an ALU
controller 1192, an instruction decoder 1193, an interrupt controller 1194, a timing
10 controller 1195, a register 1196, a register controller 1197, a bus interface (Bus I/F)
1198, a rewritable ROM 1199, and an ROM interface (ROM I/F) 1189 over a substrate
1190. A semiconductor substrate, an SOI substrate, a glass substrate, or the like is
used as the substrate 1190. The rewritable ROM 1199 and the ROM interface 1189
may be provided over a separate chip. Obviously, the CPU illustrated in FIG. 12A is
15 only an example in which the configuration is simplified, and an actual CPU may have
various configurations depending on the application.

[0201]

An instruction that is input to the CPU through the bus interface 1198 is input
to the instruction decoder 1193 and decoded therein, and then, input to the ALU
20 controller 1192, the interrupt controller 1194, the register controller 1197, and the
timing controller 1195.

[0202]

The ALU controller 1192, the interrupt controller 1194, the register controller
1197, and the timing controller 1195 conduct various controls in accordance with the
25 decoded instruction. Specifically, the ALU controller 1192 generates signals for
controlling the operation of the ALU 1191. While the CPU is executing a program, the
interrupt controller 1194 judges an interrupt request from an external input/output
device or a peripheral circuit on the basis of its priority or a mask state, and processes
the request. The register controller 1197 generates an address of the register 1196, and
30 reads/writes data from/to the register 1196 in accordance with the state of the CPU.

[0203]

The timing controller 1195 generates signals for controlling operation timings

of the ALU 1191, the ALU controller 1192, the instruction decoder 1193, the interrupt controller 1194, and the register controller 1197. For example, the timing controller 1195 includes an internal clock generator for generating an internal clock signal CLK2 based on a reference clock signal CLK1, and supplies the clock signal CLK2 to the
5 above circuits.

[0204]

In the CPU illustrated in FIG. 12A, a semiconductor memory device is provided in the register 1196. The semiconductor memory device described in Embodiment 10 can be used as the memory element provided in the register 1196.

10 [0205]

In the CPU illustrated in FIG. 12A, the register controller 1197 selects an operation of holding data in the register 1196 in accordance with an instruction from the ALU 1191. That is, the register controller 1197 selects whether data is held by a phase-inversion element or a capacitor in the memory element included in the register
15 1196. When data holding by the phase-inversion element is selected, a power supply voltage is supplied to the memory element in the register 1196. When data holding by the capacitor is selected, the data is rewritten in the capacitor, and supply of a power supply voltage to the memory element in the register 1196 can be stopped.

[0206]

20 The power supply can be stopped by providing a switching element between a memory element group and a node to which a power supply potential V_{DD} or a power supply potential V_{SS} is supplied, as illustrated in FIG. 12B or FIG. 12C. Circuits illustrated in FIGS. 12B and 12C are described below.

[0207]

25 FIGS. 12B and 12C each illustrate an example of a structure of a memory circuit including a transistor including an oxide semiconductor in an active layer as a switching element for controlling supply of a power supply potential to a memory element.

[0208]

30 The memory device illustrated in FIG. 12B includes a switching element 1141 and a memory element group 1143 including a plurality of memory elements 1142. Specifically, as each of the memory elements 1142, the memory element described in

Embodiment 5 can be used. Each of the memory elements 1142 included in the memory element group 1143 is supplied with the high-level power supply potential V_{DD} via the switching element 1141. Further, each of the memory elements 1142 included in the memory element group 1143 is supplied with a potential of a signal IN and the low-level power supply potential V_{SS} .

[0209]

In FIG. 12B, any of the transistors whose off-state current is extremely small described in Embodiments 2 to 8 is used as the switching element 1141, and the switching of the transistor is controlled by a signal SigA supplied to a gate electrode thereof.

[0210]

Note that FIG. 12B illustrates the structure in which the switching element 1141 includes only one transistor; however, without limitation thereto, the switching element 1141 may include a plurality of transistors. In the case where the switching element 1141 includes a plurality of transistors which serve as switching elements, the plurality of transistors may be connected to each other in parallel, in series, or in combination of parallel connection and series connection.

[0211]

Although the switching element 1141 controls the supply of the high-level power supply potential V_{DD} to each of the memory elements 1142 included in the memory element group 1143 in FIG. 12B, the switching element 1141 may control the supply of the low-level power supply potential V_{SS} .

[0212]

In FIG. 12C, an example of a memory device in which each of the memory elements 1142 included in the memory element group 1143 is supplied with the low-level power supply potential V_{SS} via the switching element 1141 is illustrated. The supply of the low-level power supply potential V_{SS} to each of the memory elements 1142 included in the memory element group 1143 can be controlled by the switching element 1141.

[0213]

When a switching element is provided between a memory element group and a node to which the power supply potential V_{DD} or the power supply potential V_{SS} is

supplied, data can be held even in the case where operation of a CPU is temporarily stopped and the supply of the power supply voltage is stopped; accordingly, power consumption can be reduced. Specifically, for example, while a user of a personal computer does not input data to an input device such as a keyboard, the operation of the CPU can be stopped, so that the power consumption can be reduced.

[0214]

Although the CPU is given as an example, the transistor can also be applied to an LSI such as a digital signal processor (DSP), a custom LSI, or a field programmable gate array (FPGA).

[0215]

This embodiment can be implemented in appropriate combination with the other embodiments.

[0216]

(Embodiment 12)

In this embodiment, examples of electronic devices to which any of Embodiments 2 to 11 is applied are described.

[0217]

FIG. 13A illustrates a portable information terminal, which includes a housing 9300, a button 9301, a microphone 9302, a display portion 9303, a speaker 9304, and a camera 9305, and has a function as a mobile phone. One embodiment of the present invention can be applied to the display portion 9303 and the camera 9305. Although not illustrated, one embodiment of the present invention can also be applied to an arithmetic unit, a wireless circuit, or a memory circuit inside the main body.

[0218]

FIG. 13B illustrates a display, which includes a housing 9310 and a display portion 9311. One embodiment of the present invention can be applied to the display portion 9311. When one embodiment of the present invention is employed, a display having high display quality can be provided even in the case where the size of the display portion 9311 is increased.

[0219]

FIG. 13C illustrates a digital still camera, which includes a housing 9320, a button 9321, a microphone 9322, and a display portion 9323. One embodiment of the

present invention can be applied to the display portion 9323. Although not illustrated, one embodiment of the present invention can also be applied to a memory circuit or an image sensor.

[0220]

5 By applying one embodiment of the present invention, the performance of an electric device can be improved and the reliability of the electric device can be improved.

[0221]

10 This embodiment can be implemented in appropriate combination with the other embodiments.

[Example 1]

[0222]

In this example, an oxide semiconductor film including a microvoid, which is one embodiment of the present invention is described.

15 [0223]

A sample used in this example has a structure in which a silicon oxide film is provided over a glass substrate and an In-Ga-Zn-O film is provided as an oxide semiconductor film over the silicon oxide film was used.

[0224]

20 The silicon oxide film was formed to have a thickness of 300 nm by a plasma CVD method.

[0225]

25 The oxide semiconductor film was formed with a thickness of 30 nm by a sputtering method. The other conditions were as follows: In-Ga-Zn-O ($\text{In}_2\text{O}_3:\text{Ga}_2\text{O}_3:\text{ZnO} = 1:1:2$ [molar ratio]) was used for a target; the electric power for the film formation was set to 500 W (DC); the pressure for the film formation was set to 0.4 Pa; the gas for the film formation was argon at 30 sccm and oxygen at 15 sccm; and the substrate temperature during the film formation was set to 400 °C.

[0226]

30 FIGS. 21A and 21B are cross-section observation images (four million-fold magnification) obtained with a transmission electron microscope (TEM): FIG. 21A is

the image of a sample in a state immediately after the oxide semiconductor film was formed; and FIG. 21B is the image of a sample on which heat treatment was performed at 650 °C for 1 hour in a nitrogen atmosphere after the formation of the oxide semiconductor film. Note that H-9000NAR manufactured by Hitachi, Ltd was used as the TEM, and the images were observed with the acceleration voltage of 300 kV.

[0227]

It is found that the sample on which heat treatment was performed at 650 °C after the film formation has c-axis alignment perpendicularly to the surface on the surface side of the oxide semiconductor film.

[0228]

FIGS. 22A and 22B are cross-section observation images (four million-fold magnification) obtained with the TEM: FIG. 22A is the image of a sample to which N⁺ ion was added after the formation of the oxide semiconductor film; and FIG. 22B is the image of a sample to which N⁺ ion was added after the formation of the oxide semiconductor film and on which heat treatment was performed at 650 °C for 1 hour in a nitrogen atmosphere. In this example, by an ion implantation method, N⁺ ions were added under the following condition: the concentration of N⁺ ions was $5.0 \times 10^{16} \text{ cm}^{-2}$; an accelerating voltage was 10kV; a tilt angle was 7 °C; and a twist angle was 72 °C.

[0229]

It is found that both of the samples include microvoids with almost a spherical shape (portions displayed brightly in the cross-section observation images obtained with the TEM) in the oxide semiconductor film. In particular, in the sample on which heat treatment was performed at 650 °C for 1 hour in a nitrogen atmosphere, the peripheral portion of microvoids are clearly seen. Moreover, on a surface side in the oxide semiconductor film, c-axis alignment perpendicular to the surface is formed, and a region with high crystallinity can be seen in the vicinity of the microvoid in the oxide semiconductor film. Crystal portions which are in contact with peripheral portions of the microvoids are c-axis aligned to the normal direction of the surface which is in contact with the peripheral portion of the microvoid.

[0230]

FIG. 23A is a cross-section observation image obtained, with the TEM (four

million-fold magnification), of a sample to which N^+ ion was added after the formation of the oxide semiconductor film and on which heat treatment was performed at 650 °C for 1 hour in an oxygen atmosphere. FIG. 23B is a cross-section observation image obtained, with the TEM (eight million-fold magnification), of the same sample.

5 [0231]

It is found that the sample includes microvoids with almost a spherical shape in the oxide semiconductor film. The peripheral portion of microvoids of this sample is observed more clearly the sample on which heat treatment was performed in a nitrogen atmosphere. Moreover, on a surface side in the oxide semiconductor film, c-axis
10 alignment perpendicular to the surface is formed, and a region with high crystallinity can be seen in the vicinity of the microvoid in the oxide semiconductor film. Crystal portions which are in contact with peripheral portions of the microvoids are c-axis aligned to the normal direction of the surface which is in contact with the peripheral portion of the microvoid.

15 [0232]

Next, the microvoid was observed in more detail with use of a high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM). A Hitachi scanning transmission electron microscope HD-2700 was used as the HAADF-STEM, and the microvoid was observed with an acceleration voltage of 200
20 kV.

[0233]

FIG. 24A is a cross-section observation image obtained, with the HAADF-STEM (1.5 million-fold magnification), of a sample to which N^+ ion was added after the formation of the oxide semiconductor film and on which heat treatment
25 was performed at 650 °C for 1 hour in an oxygen atmosphere. By using the HAADF-STEM, the sample can be observed to emphasize gradation. In addition, distribution of In in the observation portion was examined by electron energy loss spectroscopy (EELS), and the examined portion is shown in FIG. 24B.

[0234]

30 In the same manner, FIG. 25A is a cross-section observation image obtained, with the HAADF-STEM (1.5 million-fold magnification), of a sample to which N^+ ion

was added after the formation of the oxide semiconductor film, and on which heat treatment was performed at 650 °C for 1 hour in an oxygen atmosphere. Further, distribution of O in the observation portion was examined by EELS, and the examined portion is shown in FIG. 25B.

5 [0235]

In the same manner, FIG. 26A is a cross-section observation image, obtained with the HAADF-STEM (1.5 million-fold magnification), of a sample to which N⁺ ion was added after the formation of the oxide semiconductor film, and on which heat treatment was performed at 650 °C for 1 hour in an oxygen atmosphere. Further, distribution of N in the observation portion was examined by EELS, and the examined portion is shown in FIG. 26B.

[0236]

According to FIGS. 24A and 24B and FIGS. 25A and 25B, it is found that the microvoid in the oxide semiconductor film are brighter than the surrounding part, and In and O which are main components of the oxide semiconductor film are hardly included. That is, it is found that the microvoid has a low density as compared to the surrounding part or an empty space. According to FIGS. 26A and 26B, it is found that the microvoid is darker than the surrounding part, and N is included in the microvoid.

[0237]

20 Next, XPS was used to examine a state of added N⁺ in the oxide semiconductor film.

[0238]

FIG. 27 shows XPS spectra including a spectrum 5001 of a sample without heat treatment, a spectrum 5002 of a sample on which heat treatment was performed at 300 °C for 1 hour in a nitrogen atmosphere, a spectrum 5003 of a sample on which heat treatment was performed at 450 °C for 1 hour in a nitrogen atmosphere, and a spectrum 5004 of a sample on which heat treatment was performed at 650 °C for 1 hour in a nitrogen atmosphere. In all the samples, heat treatment was performed after addition of N⁺ ions to an oxide semiconductor film.

30 [0239]

In all spectra in FIG. 27, a peak of N₂ or -NO_x appears in the vicinity of a

binding energy of 403 eV, and a peak of metal-N appears in the vicinity of a binding energy of 397 eV. That is, it is found that N exists in a bonding state of N_2 , $-NO_x$, or metal-N in a sample to which N^+ ion is added. Here, according to distribution of In and O shown in FIG. 24B and FIG. 25B, it is found that a bonding of $-NO_x$ and metal-N are hardly exist in the microvoid, and N exists as N_2 in the microvoid.

[0240]

According to this example, it is found that the microvoid is formed in the oxide semiconductor film by adding N^+ ion to the oxide semiconductor film. In addition, it is found that N_2 exists in the microvoid.

[Example 2]

[0241]

In this example, a relationship between H and N when N^+ ion is added to an oxide semiconductor film is described.

[0242]

A sample used in this example has a structure in which an In-Ga-Zn-O film is formed as an oxide semiconductor film over a silicon wafer was used.

[0243]

The oxide semiconductor film was formed to have a thickness of 300 nm by a sputtering method. The other conditions were as follows: In-Ga-Zn-O ($In_2O_3:Ga_2O_3:ZnO = 1:1:2$ [molar ratio]) was used for a target; the electric power for the film formation was set to 500 W (DC); the pressure for the film formation was set to 0.4 Pa; the gas for the film formation was argon at 30 sccm and oxygen at 15 sccm; and the substrate temperature during the film formation was set to 200 °C.

[0244]

FIG. 28A shows the distribution of a hydrogen concentration in the depth direction measured by SIMS, of a sample without heat treatment (a solid line 5011) and a sample on which heat treatment was performed at 450 °C for 1 hour in hydrogen atmosphere (a solid line 5012). In both of the samples, N^+ ion was added after H^+ ion had been added. Further, FIG. 28B shows the distribution of a nitrogen concentration in the depth direction measured by SIMS of a sample without heat treatment (a solid line 5021) and a sample on which heat treatment was performed at 450 °C for 1 hour in

nitrogen atmosphere (a solid line 5022). In both of the samples, N^+ ion was added after H^+ ion had been added. By an ion implantation method, H^+ ion was added under the following condition: the concentration of H^+ ions was $1.0 \times 10^{16} \text{ cm}^{-2}$; an accelerating voltage was 22kV; a tilt angle was 7°C ; and a twist angle was 72°C .

5 Further, by an ion implantation method, N^+ ion was added under the following condition: the concentration of N^+ ions was $1.0 \times 10^{16} \text{ cm}^{-2}$; an accelerating voltage was 35kV; a tilt angle was 7°C ; and a twist angle was 72°C .

[0245]

According to FIG. 28B, there was little difference between the distribution of a
10 nitrogen concentration in the depth direction in the oxide semiconductor film examined after N^+ ion and H^+ ion had been added to the oxide semiconductor film and the distribution of a nitrogen concentration in the depth direction in the oxide semiconductor film examined after heat treatment had been performed at 450°C for 1 hour in nitrogen atmosphere. On the other hand, according to FIG. 28A, in the sample
15 without heat treatment, a hydrogen concentration has a peak at a depth in the vicinity of 200 nm, whereas in the sample on which heat treatment was performed at 450°C for 1 hour in nitrogen atmosphere, a hydrogen concentration has a peak at a depth in the vicinity of 70 nm. This peak position at a depth of the vicinity of 70 nm approximately corresponds to the peak position of a nitrogen concentration in the depth
20 direction shown in FIG. 28B.

[0246]

FIGS. 29A and 29B show examples in which the concentration of added N^+ ions is different from that in FIGS. 28A and 28B. FIG. 29A shows, H^+ ion was added to an oxide semiconductor film, then N^+ ion was added to the oxide semiconductor film,
25 distribution of a hydrogen concentration in the depth direction measured by SIMS of a sample without heat treatment (a solid line 5013) and a sample on which heat treatment was performed at 450°C for 1 hour in a hydrogen atmosphere (a solid line 5014). Further, FIG. 29B shows, after N^+ ion and H^+ ion are added to the same sample, distribution of a nitrogen concentration in the depth direction measured by SIMS of a
30 sample without heat treatment (a solid line 5023) and a sample on which heat treatment was performed at 450°C for 1 hour in nitrogen atmosphere (a solid line 5024). By an

ion implantation method, H^+ ion is added under the condition of the concentration of H^+ ions is $1.0 \times 10^{16} \text{ cm}^{-2}$, and N^+ ion is added under the condition of the concentration of N^+ ions is $5.0 \times 10^{16} \text{ cm}^{-2}$. For the other conditions of addition, the explanation of FIGS. 28A and 28B can be referred to.

5 [0247]

According to FIG. 29B, there was little difference between the distribution of a nitrogen concentration in the depth direction in the oxide semiconductor film examined after N^+ ion and H^+ ion had been added to the oxide semiconductor film and the distribution of a nitrogen concentration in the depth direction in the oxide semiconductor film examined after heat treatment had been performed at 450°C for 1 hour in nitrogen atmosphere. On the other hand, according to FIG. 29A, in the sample without heat treatment, a hydrogen concentration has a peak at a depth of the vicinity of 200 nm, whereas in the sample on which heat treatment was performed at 450°C for 1 hour in nitrogen atmosphere, a hydrogen concentration has a peak at a depth in the vicinity of 70 nm. Note that the hydrogen concentration at this peak position is higher than that in FIGS. 28A and 28B.

15 [0248]

According to this example, by adding N^+ ion to an oxide semiconductor film and performing heat treatment, it is found that the hydrogen concentration of a region where N^+ ion is added in the oxide semiconductor film is increased.

REFERENCE NUMERALS

[0249]

100: substrate, 104: gate electrode, 105: channel region, 106: oxide semiconductor film, 107a: source region, 107b: drain region, 112: gate insulating film, 116: a pair of electrodes, 118: interlayer insulating film, 205: channel region, 206: oxide semiconductor film, 207a: source region, 207b: drain region, 216: a pair of electrodes, 218: interlayer insulating film, 302: base insulating film, 304: gate electrode, 305: channel region, 306: oxide semiconductor film, 307a: source region, 307b: drain region, 312: gate insulating film, 316: a pair of electrodes, 404: gate electrode, 405a: region, 405b: region, 405c: region, 406: oxide semiconductor film, 407a: region, 407b: region, 504: gate electrode, 505: channel region, 506: oxide semiconductor film, 507a: source

region, 507b: drain region, 512: gate insulating film, 516: a pair of electrodes, 604: gate electrode, 605: channel region, 606: oxide semiconductor film, 607a: source region, 607b: drain region, 612: gate insulating film, 616: a pair of electrodes, 618: interlayer insulating film, 704: gate electrode, 705: channel region, 706: oxide semiconductor film, 707a: source region, 707b: drain region, 712: gate insulating film, 716: a pair of electrodes, 718: interlayer insulating film, 1141: switching element, 1142: memory element, 1143: memory element group, 1189: ROM interface, 1190: substrate, 1191: ALU, 1192: ALU controller, 1193: instruction decoder, 1194: interrupt controller, 1195: timing controller, 1196: register, 1197: register controller, 1198: bus interface, 1199: ROM, 2200: pixel, 2210: liquid crystal element, 2220: capacitor, 2230: transistor, 3006: oxide semiconductor film, 3010: microvoid, 5001: spectrum, 5002: spectrum, 5003: spectrum, 5004: spectrum, 5011: solid line, 5012: solid line, 5013: solid line, 5014: solid line, 5021: solid line, 5022: solid line, 5023: solid line, 5024: solid line, 9300: housing, 9301: button, 9302: microphone, 9303: display portion, 9304: speaker, 9305: camera, 9310: housing, 9311: display portion, 9320: housing, 9321: button, 9322: microphone, 9323: display portion.

This application is based on Japanese Patent Application serial no. 2011-060152 filed with Japan Patent Office on March 18, 2011, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. An oxide semiconductor film comprising a microvoid,
wherein at least one of nitrogen, hydrogen, and oxygen is included in the
5 microvoid, and
wherein a concentration of at least one of nitrogen, hydrogen, and oxygen in
the microvoid is higher than that a concentration of at least one of nitrogen, hydrogen,
and oxygen outside of the microvoid in the oxide semiconductor film.
- 10 2. An oxide semiconductor film according to claim 1,
wherein a diameter of the microvoid is larger than or equal to 0.1 nm and
smaller than or equal to 10 nm.
- 15 3. An oxide semiconductor film according to claim 1, further comprising a
crystal portion in contact with a peripheral portion of the microvoid.
4. A semiconductor device comprising:
a gate electrode;
a gate insulating film covering the gate electrode;
20 a pair of electrodes over the gate insulating film; and
an oxide semiconductor film overlapping with the gate electrode with the gate
insulating film provided therebetween, being partly in contact with the pair of electrodes,
including a channel region, a source region, and a drain region,
wherein densities of the source region and the drain region are lower than a
25 density of the channel region.
5. A semiconductor device according to claim 4,
wherein the source region and the drain region contain hydrogen having a
concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to 3×10^{22}
30 cm^{-3} .
6. A semiconductor device according to claim 5,

wherein a hydrogen concentration in the channel region is lower than 5×10^{18} cm⁻³.

7. A semiconductor device according to claim 4,
wherein the source region and the drain region include a microvoid.

8. A semiconductor device according to claim 7,
wherein the microvoid includes at least one of nitrogen, hydrogen, and oxygen more than the outside of the microvoid includes.

9. A semiconductor device according to claim 7,
wherein a diameter of the microvoid is larger than or equal to 0.1 nm and smaller than or equal to 10 nm.

10. A semiconductor device according to claim 7,
wherein a crystal portion is included in contact with a peripheral portion of the microvoid.

11. A semiconductor device comprising:

an oxide semiconductor film including a channel region, a source region, and a drain region;

a pair of electrodes being partly in contact with the oxide semiconductor film;

a gate insulating film over the oxide semiconductor film; and

a gate electrode overlapping with the oxide semiconductor film with the gate

insulating film provided therebetween,

wherein densities of the source region and the drain region are lower than a density of the channel region.

12. A semiconductor device according to claim 11,

wherein the source region and the drain region contain hydrogen having a concentration higher than or equal to 1×10^{20} cm⁻³ and lower than or equal to 3×10^{22}

cm⁻³.

13. A semiconductor device according to claim 12,
wherein a hydrogen concentration in the channel region is lower than 5×10^{18}

5 cm⁻³.

14. A semiconductor device according to claim 11,
wherein the source region and the drain region include a microvoid.

10 15. A semiconductor device according to claim 14,
wherein the microvoid includes at least one of nitrogen, hydrogen, and oxygen
more than the outside of the microvoid includes.

15 16. A semiconductor device according to claim 14,
wherein a diameter of the microvoid is larger than or equal to 0.1 nm and
smaller than or equal to 10 nm.

17. A semiconductor device according to claim 14,
wherein a crystal portion is included in contact with a peripheral portion of the
20 microvoid.

18. A semiconductor device comprising:
an oxide semiconductor film including a channel region, a source region, and a
drain region;

25 a gate insulating film over the oxide semiconductor film;
a gate electrode overlapping with the channel region with the gate insulating
film provided therebetween;

an interlayer insulating film over the gate insulating film and the gate
electrode; and

30 a pair of electrodes over the interlayer insulating film,
wherein the gate insulating film and the interlayer insulating film include
opening portions exposing the source region and the drain region,

wherein the pair of electrodes is in contact with the source region and the drain region through the opening portions, and

wherein densities of the source region and the drain region are lower than a density of the channel region.

5

19. A semiconductor device according to claim 18,

wherein the source region and the drain region contain hydrogen having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$.

10

20. A semiconductor device according to claim 19,

wherein a hydrogen concentration in the channel region is lower than $5 \times 10^{18} \text{ cm}^{-3}$.

15

21. A semiconductor device according to claim 18,

wherein the source region and the drain region include a microvoid.

22. A semiconductor device according to claim 21,

wherein the microvoid includes at least one of nitrogen, hydrogen, and oxygen more than the outside of the microvoid includes.

20

23. A semiconductor device according to claim 21,

wherein a diameter of the microvoid is larger than or equal to 0.1 nm and smaller than or equal to 10 nm.

25

24. A semiconductor device according to claim 21,

wherein a crystal portion is included in contact with a peripheral portion of the microvoid.

30

25. A semiconductor device comprising:

a gate electrode;

a gate insulating film covering the gate electrode;

an oxide semiconductor film overlapping with the gate electrode with the gate insulating film interposed therebetween and including a channel region, a source region, and a drain region;

5 an interlayer insulating film including opening portions exposing the source region and the drain region and provided over the gate insulating film and the oxide semiconductor film; and

a pair of electrodes being in contact with the oxide semiconductor film through the opening portions,

10 wherein densities of the source region and the drain region are lower than a density of the channel region.

26. A semiconductor device according to claim 25,

15 wherein the source region and the drain region contain hydrogen having a concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to $3 \times 10^{22} \text{ cm}^{-3}$.

27. A semiconductor device according to claim 26,

20 wherein a hydrogen concentration in the channel region is lower than $5 \times 10^{18} \text{ cm}^{-3}$.

28. A semiconductor device according to claim 25,

wherein the source region and the drain region include a microvoid.

25 29. A semiconductor device according to claim 28,

wherein the microvoid includes at least one of nitrogen, hydrogen, and oxygen more than the outside of the microvoid includes.

30. A semiconductor device according to claim 28,

30 wherein a diameter of the microvoid is larger than or equal to 0.1 nm and smaller than or equal to 10 nm.

31. A semiconductor device according to claim 28,
wherein a crystal portion is included in contact with a peripheral portion of the
microvoid.

5

32. A semiconductor device comprising:
an oxide semiconductor film;
a pair of electrodes being partly in contact with the oxide semiconductor film;
a gate insulating film over the oxide semiconductor film; and
10 a gate electrode overlapping with the oxide semiconductor film with the gate
insulating film provided therebetween, and not overlapping with the pair of electrodes,
wherein a density of a region in the oxide semiconductor film, which does not
overlap with the pair of electrodes and the gate electrode is lower than densities of
regions overlapping with the pair of electrodes or the gate electrode.

15

33. A semiconductor device according to claim 32,
wherein the source region and the drain region contain hydrogen having a
concentration higher than or equal to $1 \times 10^{20} \text{ cm}^{-3}$ and lower than or equal to 3×10^{22}
 cm^{-3} .

20

34. A semiconductor device according to claim 33,
wherein a hydrogen concentration in the channel region is lower than 5×10^{18}
 cm^{-3} .

25

35. A semiconductor device according to claim 32,
wherein the source region and the drain region include a microvoid.

36. A semiconductor device according to claim 35,
wherein the microvoid includes at least one of nitrogen, hydrogen, and oxygen
30 more than the outside of the microvoid includes.

37. A semiconductor device according to claim 35,

wherein a diameter of the microvoid is larger than or equal to 0.1 nm and smaller than or equal to 10 nm.

5 38. A semiconductor device according to claim 35,

wherein a crystal portion is included in contact with a peripheral portion of the microvoid.

39. A manufacturing method of a semiconductor device, the method
10 comprising the steps of:

forming a gate electrode over a substrate;

forming a gate insulating film covering the gate electrode;

forming an oxide semiconductor film over the gate electrode with the gate
insulating film provided therebetween;

15 forming a microvoid by adding any one or more of nitrogen, oxygen, and
hydrogen to a part of the oxide semiconductor film;

forming a pair of electrodes being partly in contact with the oxide
semiconductor film;

forming an interlayer insulating film over the oxide semiconductor film and the
20 pair of electrodes; and

performing heat treatment at a temperature higher than or equal to 200 °C and
lower than or equal to 700 °C after forming the interlayer insulating film.

40. A manufacturing method of a semiconductor device, the method
25 comprising the steps of:

forming a gate electrode over a substrate;

forming a gate insulating film covering the gate electrode;

forming a pair of electrodes over the gate insulating film;

forming an oxide semiconductor film being partly in contact with the pair of
30 electrodes and provided over the pair of electrodes;

forming a microvoid by adding any one or more of nitrogen, oxygen, and

hydrogen to a part of the oxide semiconductor film;

forming an interlayer insulating film over the oxide semiconductor film and the pair of electrodes; and

performing heat treatment at a temperature higher than or equal to 200 °C and
5 lower than or equal to 700 °C after forming the interlayer insulating film.

41. A manufacturing method of a semiconductor device, the method comprising the steps of:

forming an oxide semiconductor film over a substrate;

10 forming a microvoid by adding any one or more of nitrogen, oxygen, and hydrogen to a part of the oxide semiconductor film;

forming a pair of electrodes being partly in contact with the oxide semiconductor film;

forming a gate insulating film over the oxide semiconductor film and the pair
15 of electrodes;

forming a gate electrode overlapping with the oxide semiconductor film with the gate insulating film provided therebetween; and

performing heat treatment at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C after forming the gate electrode.
20

42. A manufacturing method of a semiconductor device, the method comprising the steps of:

forming a pair of electrodes over a substrate;

forming an oxide semiconductor film being partly in contact with the pair of
25 electrodes and provided over the pair of electrodes;

forming a microvoid by adding any one or more of nitrogen, oxygen, and hydrogen to a part of the oxide semiconductor film;

forming a gate insulating film over the oxide semiconductor film and the pair of electrodes;

30 forming a gate electrode overlapping with the oxide semiconductor film with the gate insulating film provided therebetween; and

performing heat treatment at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C after forming the gate electrode.

43. A manufacturing method of a semiconductor device, the method comprising the steps of:

forming an oxide semiconductor film over a substrate;

forming a gate insulating film over the oxide semiconductor film;

forming a gate electrode overlapping with the oxide semiconductor film with the gate insulating film provided therebetween;

forming a microvoid by adding any one or more of nitrogen, oxygen, and hydrogen to a part of the oxide semiconductor film using the gate electrode as a mask;

forming an interlayer insulating film over the gate insulating film and the gate electrode;

forming an opening portion exposing the oxide semiconductor film in the gate electrode and the interlayer insulating film;

performing heat treatment at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C; and

forming a pair of electrodes being in contact with the oxide semiconductor film through the opening portion.

44. A manufacturing method of a semiconductor device, the method comprising the steps of:

forming a gate electrode over a substrate;

forming a gate insulating film covering the gate electrode;

forming an oxide semiconductor film over the gate electrode with the gate insulating film provided therebetween;

forming a microvoid by adding any one or more of nitrogen, oxygen, and hydrogen to a part of the oxide semiconductor film;

forming an interlayer insulating film over the gate insulating film and the oxide semiconductor film;

performing heat treatment at a temperature higher than or equal to 200 °C and

lower than or equal to 700 °C;

forming an opening portion exposing the oxide semiconductor film to the interlayer insulating film; and

5 forming a pair of electrodes being in contact with the oxide semiconductor film through the opening portion.

45. A manufacturing method of a semiconductor device, the method comprising the steps of:

10 forming an oxide semiconductor film and a pair of electrodes being partly in contact with the oxide semiconductor film;

forming a gate insulating film over the oxide semiconductor film and the pair of electrodes;

15 forming a gate electrode overlapping with the oxide semiconductor film with the gate insulating film interposed between, and not overlapping with the pair of electrodes;

forming a microvoid by adding any one or more of nitrogen, oxygen, and hydrogen to part of the oxide semiconductor film using the pair of electrodes and the gate electrode as a mask; and

20 performing heat treatment at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C.

46. A manufacturing method of a semiconductor device, the method comprising the steps of:

25 forming a gate electrode over a substrate;
forming a gate insulating film covering the gate electrode;
forming an oxide semiconductor film over the gate electrode with the gate insulating film provided therebetween;

reducing a density of a region of the oxide semiconductor film by performing ion implantation to the region of the oxide semiconductor film;

30 forming a pair of electrodes being partly in contact with the region where the density of the oxide semiconductor film is reduced;

forming an interlayer insulating film over the oxide semiconductor film and the pair of electrodes; and

performing heat treatment at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C after forming the interlayer insulating film, so that
5 hydrogen is captured in the region where the density of the oxide semiconductor film is reduced.

47. A manufacturing method of a semiconductor device, the method comprising the steps of:

10 forming a gate electrode over a substrate;
forming a gate insulating film covering the gate electrode;
forming a pair of electrodes over the gate insulating film;
forming an oxide semiconductor film being partly in contact with the pair of electrodes and provided over the pair of electrodes;
15 reducing a density of a region of the oxide semiconductor film by performing ion implantation to the region of the oxide semiconductor film;
forming an interlayer insulating film over the oxide semiconductor film and the pair of electrodes; and
performing heat treatment at a temperature higher than or equal to 200 °C and
20 lower than or equal to 700 °C after forming the interlayer insulating film, so that hydrogen is captured in the region where the density of the oxide semiconductor film is reduced.

48. A manufacturing method of a semiconductor device, the method
25 comprising the steps of:

forming an oxide semiconductor film over a substrate;
reducing a density of a region of the oxide semiconductor film by performing ion implantation to the region of the oxide semiconductor film;
forming a pair of electrodes being partly in contact with the region where the
30 density of the oxide semiconductor film is reduced;
forming a gate insulating film over the oxide semiconductor film and the pair

of electrodes;

forming a gate electrode overlapping with the oxide semiconductor film with the gate insulating film provided therebetween; and

performing heat treatment at a temperature higher than or equal to 200 °C and
5 lower than or equal to 700 °C after forming the gate electrode, so that hydrogen is captured in the region where the density of the oxide semiconductor film is reduced.

49. A manufacturing method of a semiconductor device, the method comprising the steps of:

10 forming a pair of electrodes over a substrate;

forming an oxide semiconductor film being partly in contact with the pair of electrodes and provided over the pair of electrodes;

reducing a density of a region of the oxide semiconductor film by performing ion implantation to the region of the oxide semiconductor film;

15 forming a gate insulating film over the oxide semiconductor film and the pair of electrodes;

forming a gate electrode overlapping with the oxide semiconductor film with the gate insulating film provided therebetween; and

performing heat treatment at a temperature higher than or equal to 200 °C and
20 lower than or equal to 700 °C after forming the gate electrode, so that hydrogen is captured in the region where the density of the oxide semiconductor film is reduced.

50. A manufacturing method of a semiconductor device, the method comprising the steps of:

25 forming an oxide semiconductor film over a substrate;

forming a gate insulating film over the oxide semiconductor film;

forming a gate electrode overlapping with the oxide semiconductor film with the gate insulating film provided therebetween;

reducing a density of a region of the oxide semiconductor film by performing
30 ion implantation to the region of the oxide semiconductor film using the gate electrode as a mask;

forming an interlayer insulating film over the gate insulating film and the gate electrode;

forming an opening portion exposing the oxide semiconductor film in the gate electrode and the interlayer insulating film;

5 performing heat treatment at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, so that hydrogen is captured in the region where the density of the oxide semiconductor film is reduced; and

forming a pair of electrodes being in contact with the oxide semiconductor film through the opening portion.

10

51. A manufacturing method of a semiconductor device, the method comprising the steps of:

forming a gate electrode over a substrate;

forming a gate insulating film covering the gate electrode;

15 forming an oxide semiconductor film over the gate electrode with the gate insulating film provided therebetween;

reducing a density of a region of the oxide semiconductor film by performing ion implantation to the region of the oxide semiconductor film;

20 forming an interlayer insulating film over the gate insulating film and the oxide semiconductor film;

performing heat treatment at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, so that hydrogen is captured in the region where the density of the oxide semiconductor film is reduced;

25 forming an opening portion exposing the oxide semiconductor film to the interlayer insulating film after capturing hydrogen in the region where the density is reduced; and

forming a pair of electrodes being in contact with the oxide semiconductor film through the opening portion.

FIG. 1A

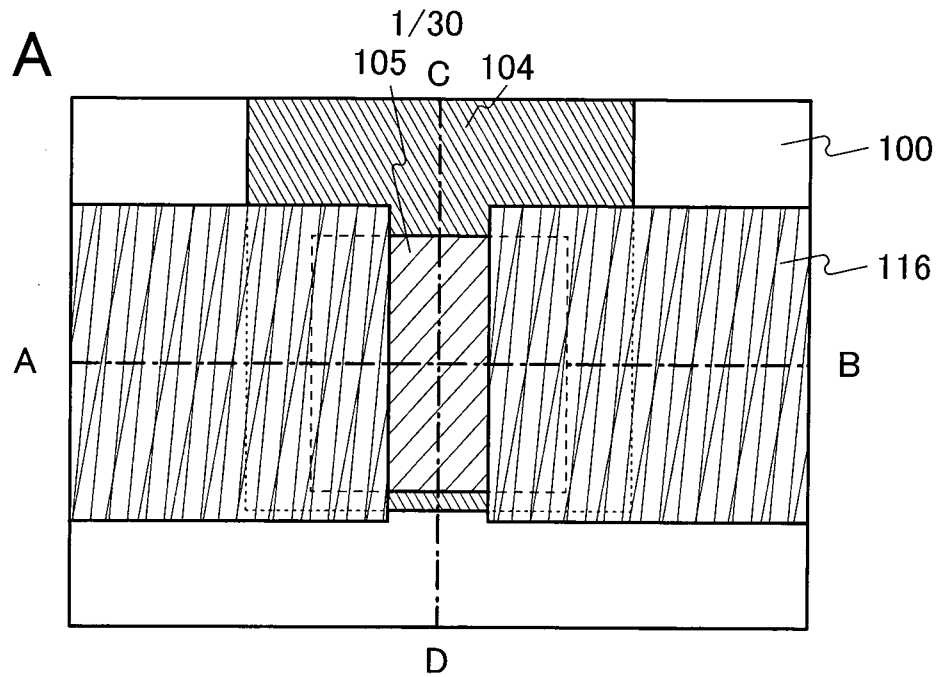


FIG. 1B

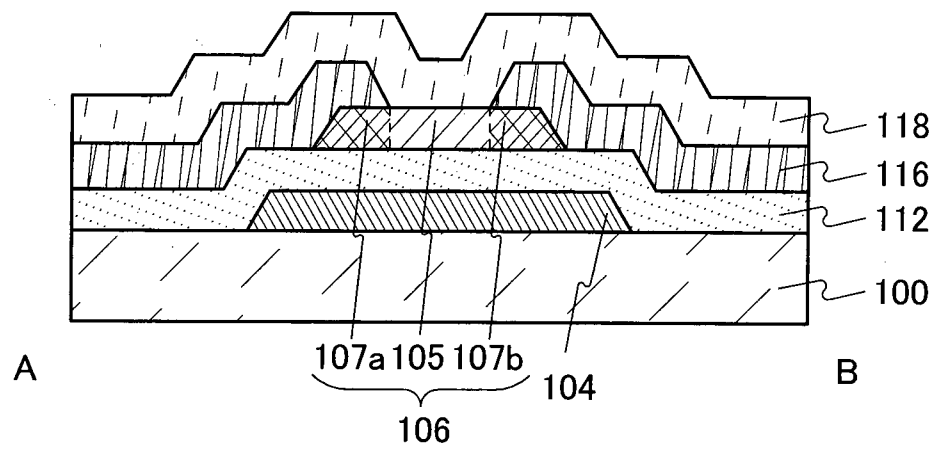


FIG. 1C

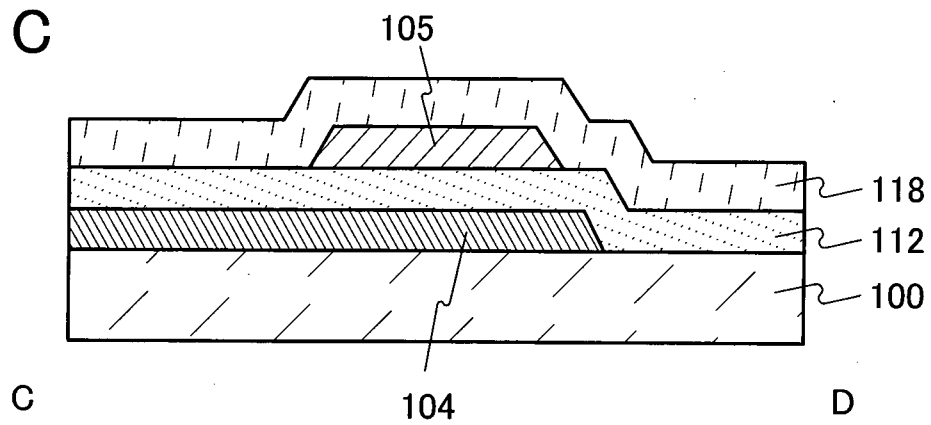


FIG. 2A

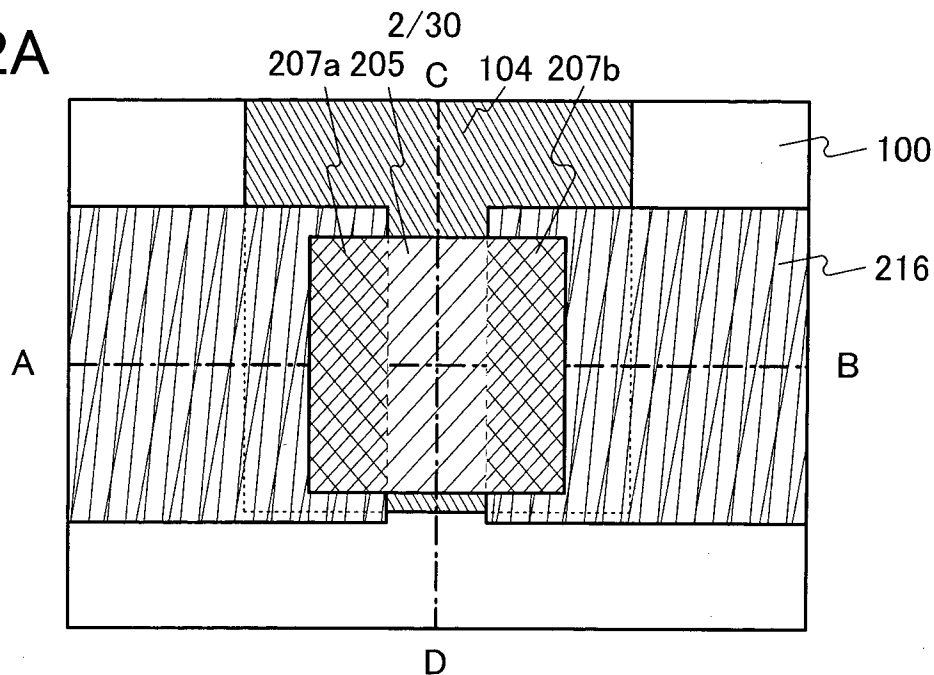


FIG. 2B

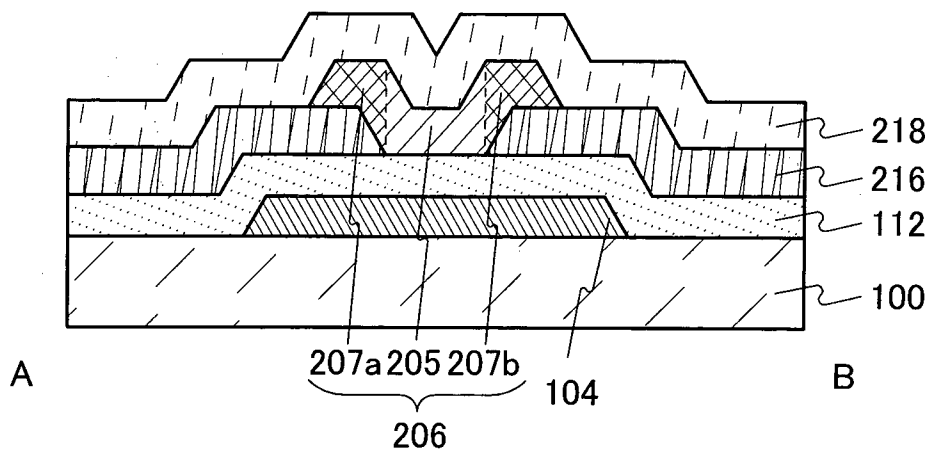


FIG. 2C

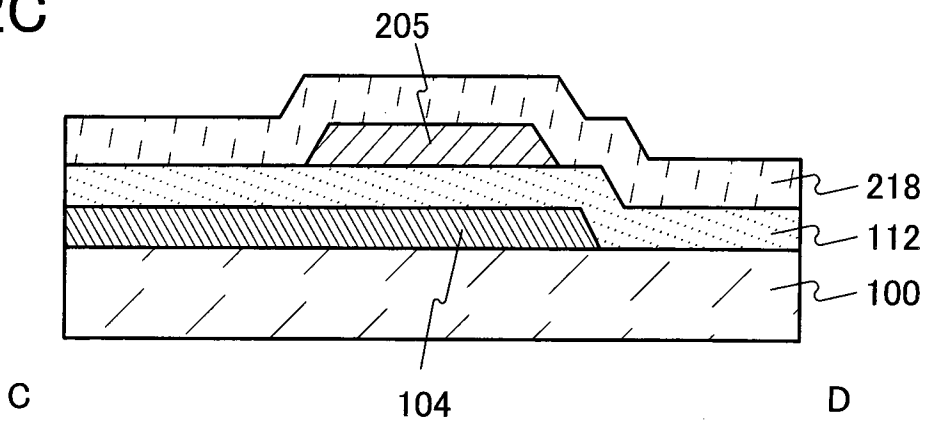


FIG. 3A

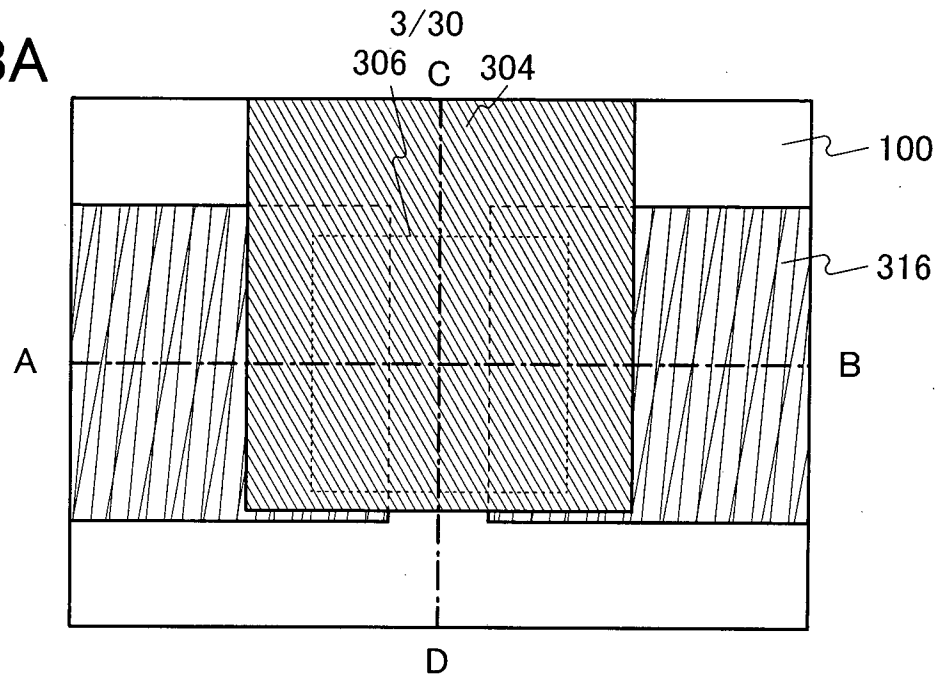


FIG. 3B

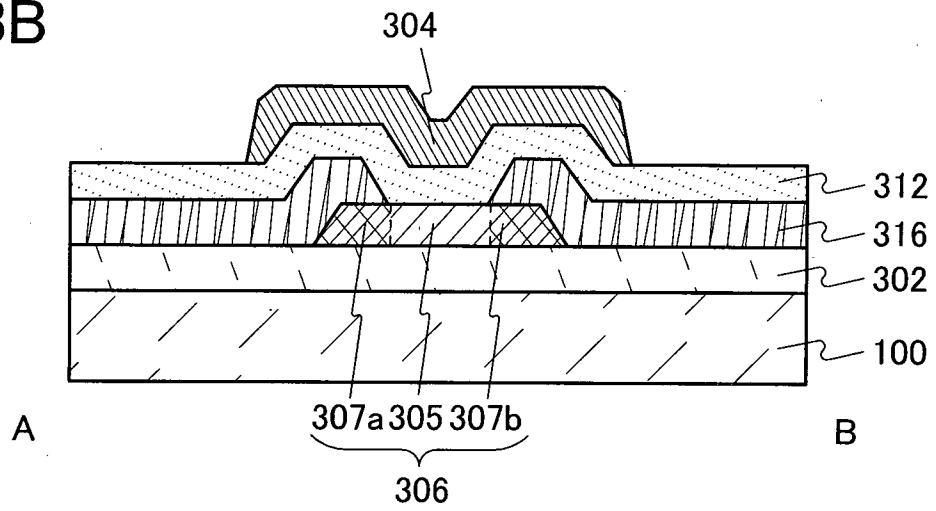


FIG. 3C

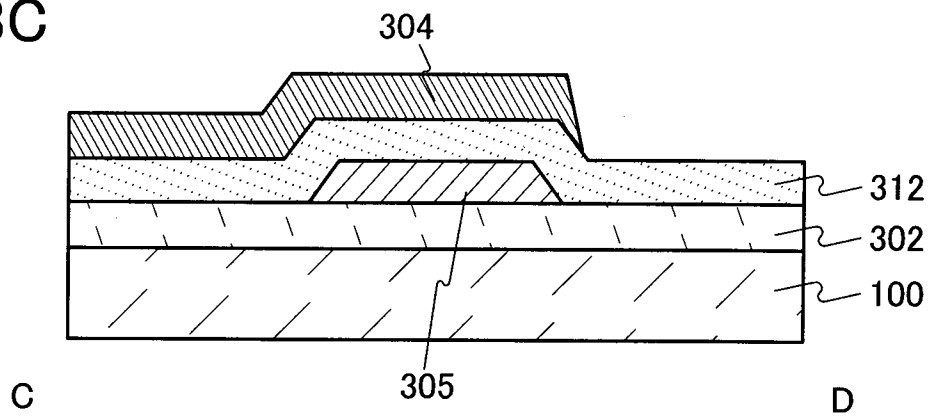


FIG. 4A

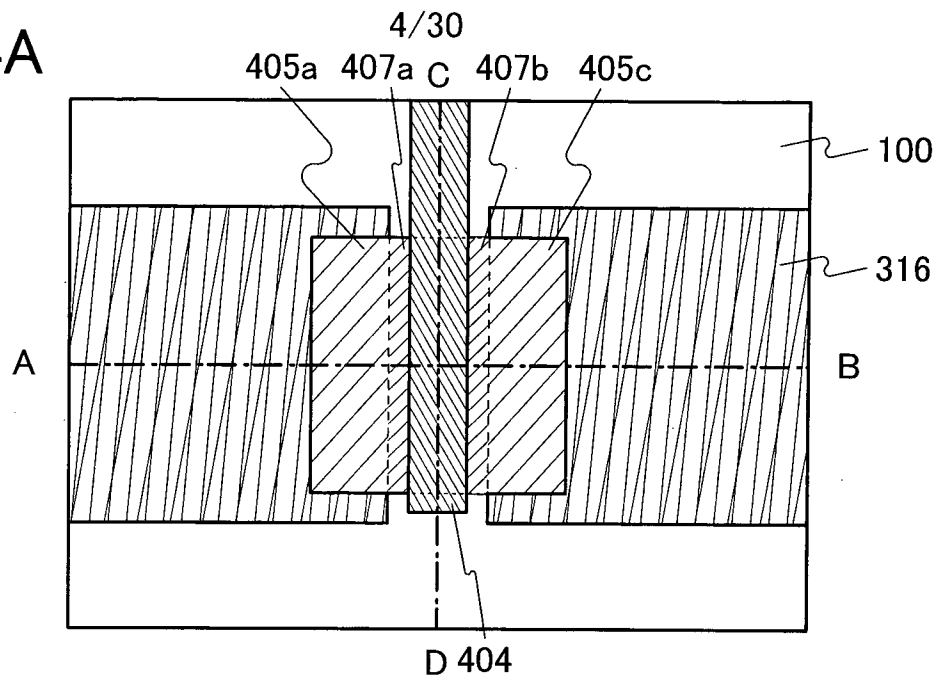


FIG. 4B

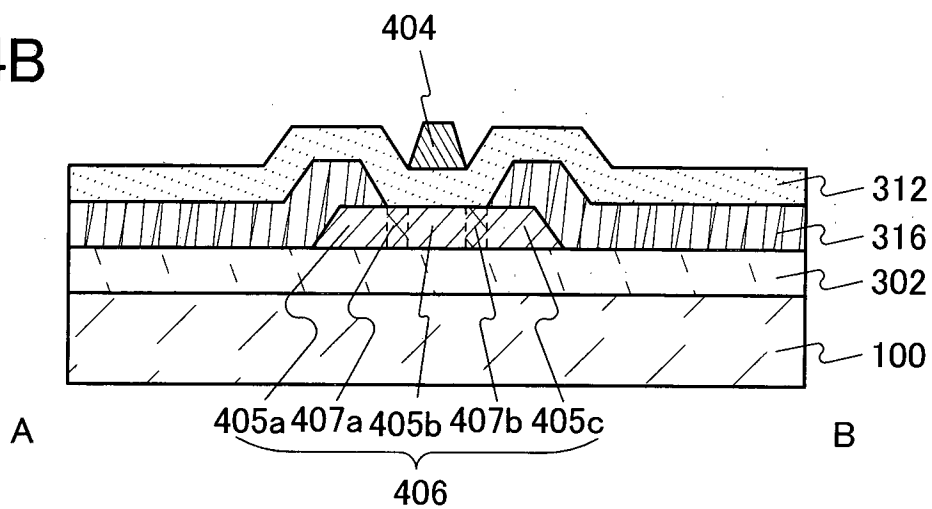


FIG. 4C

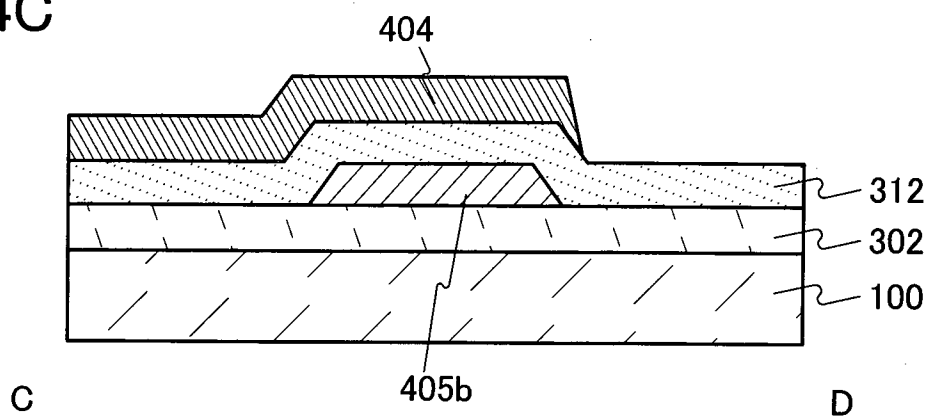


FIG. 5A

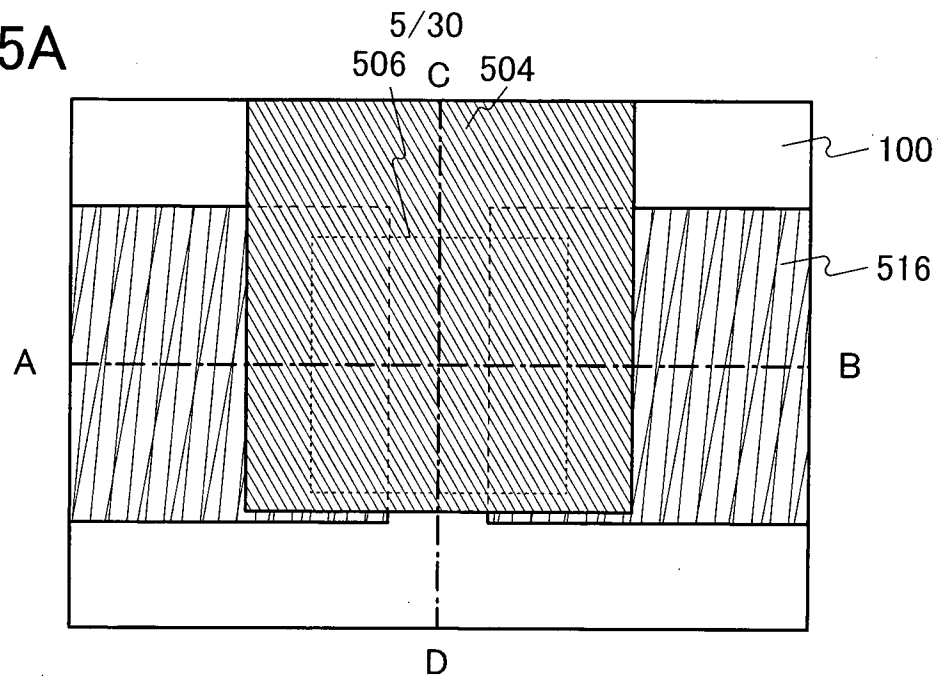


FIG. 5B

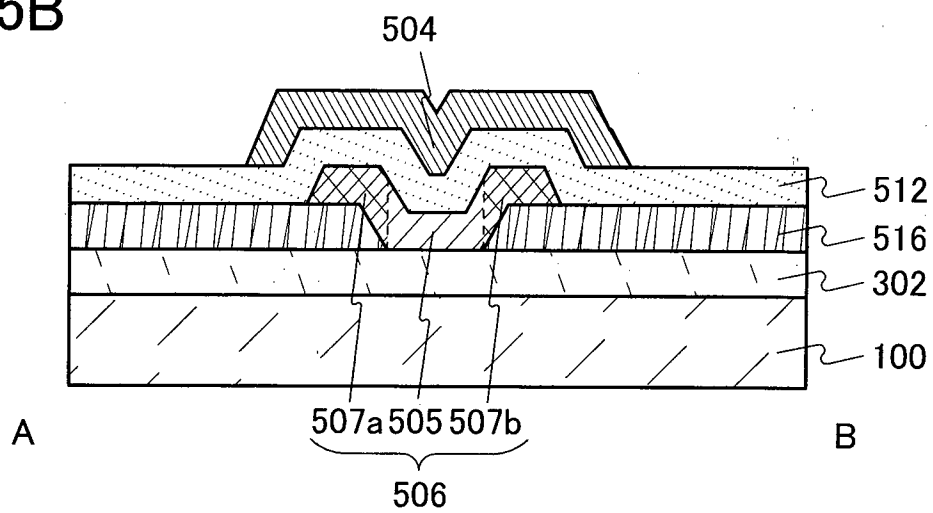


FIG. 5C

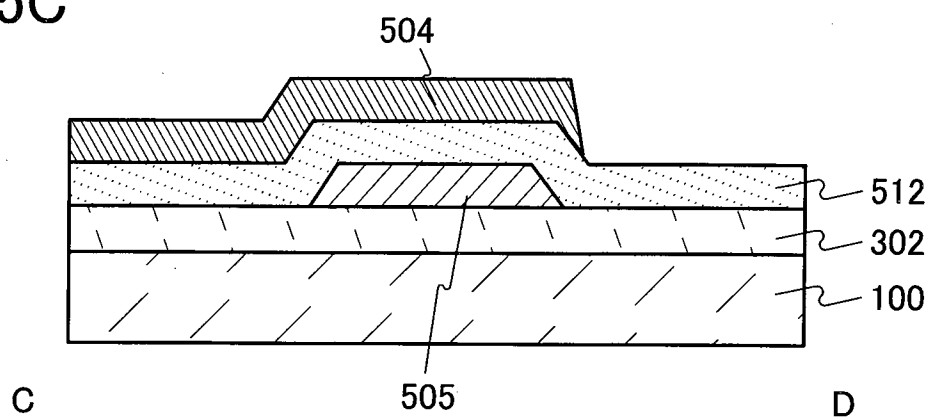


FIG. 6A

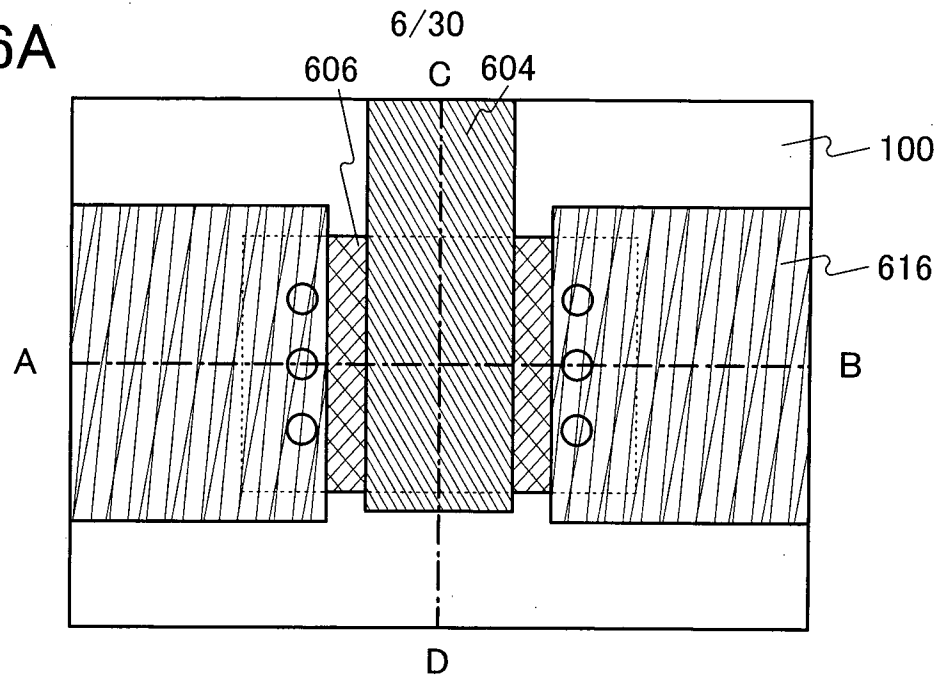


FIG. 6B

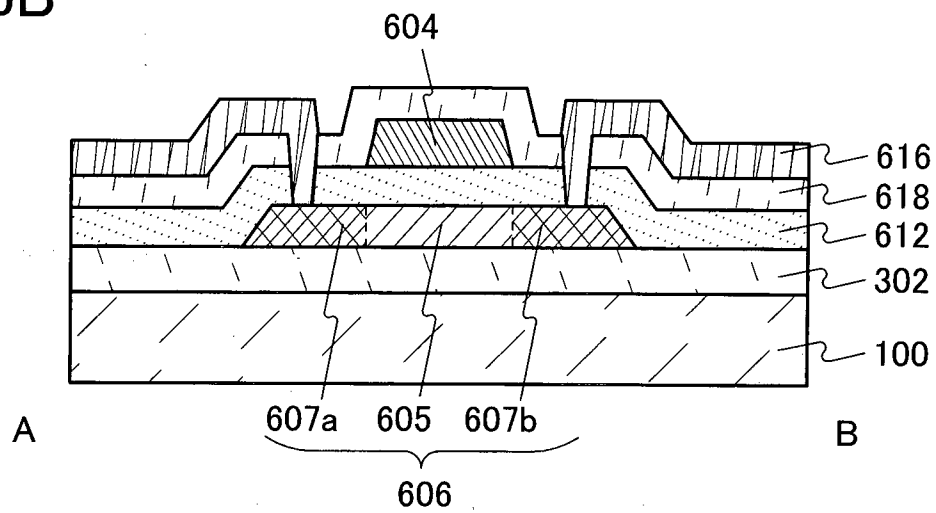
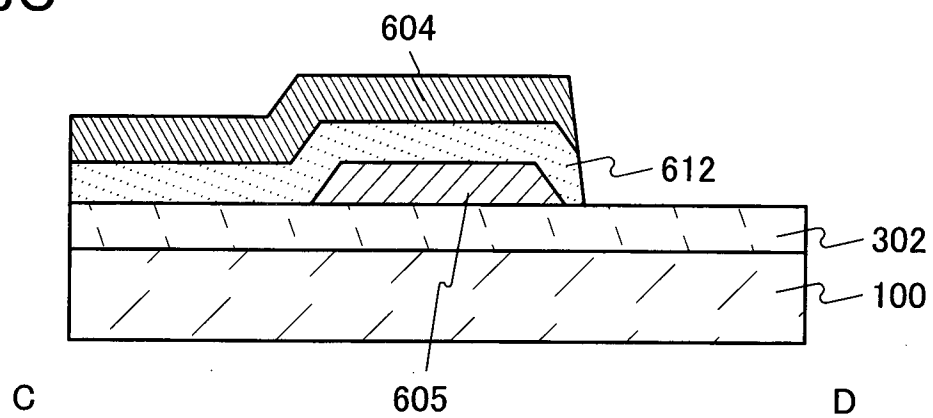


FIG. 6C



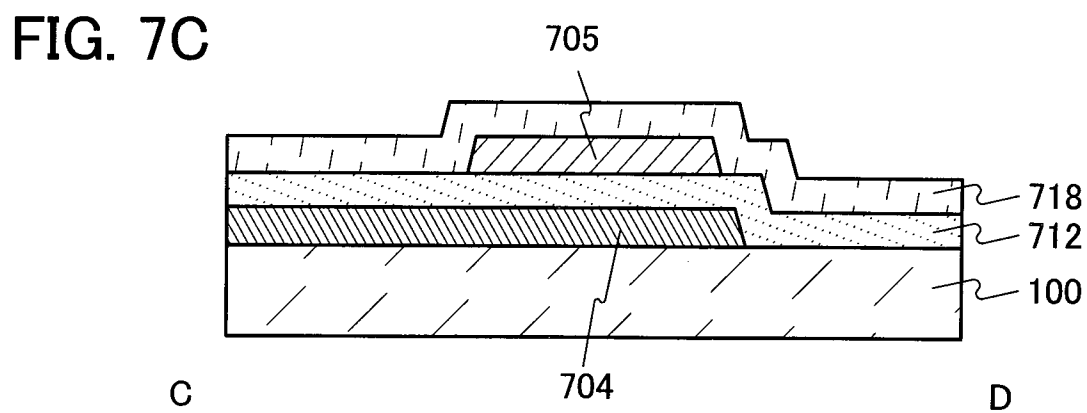
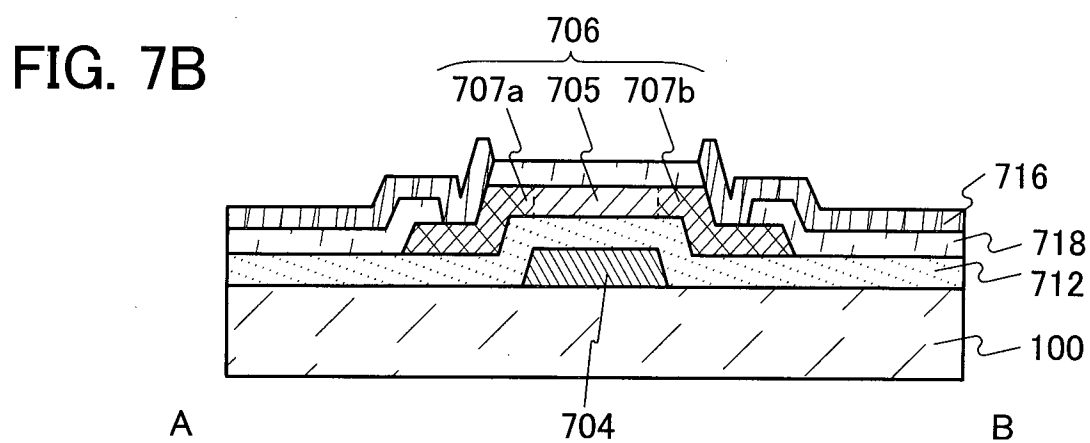
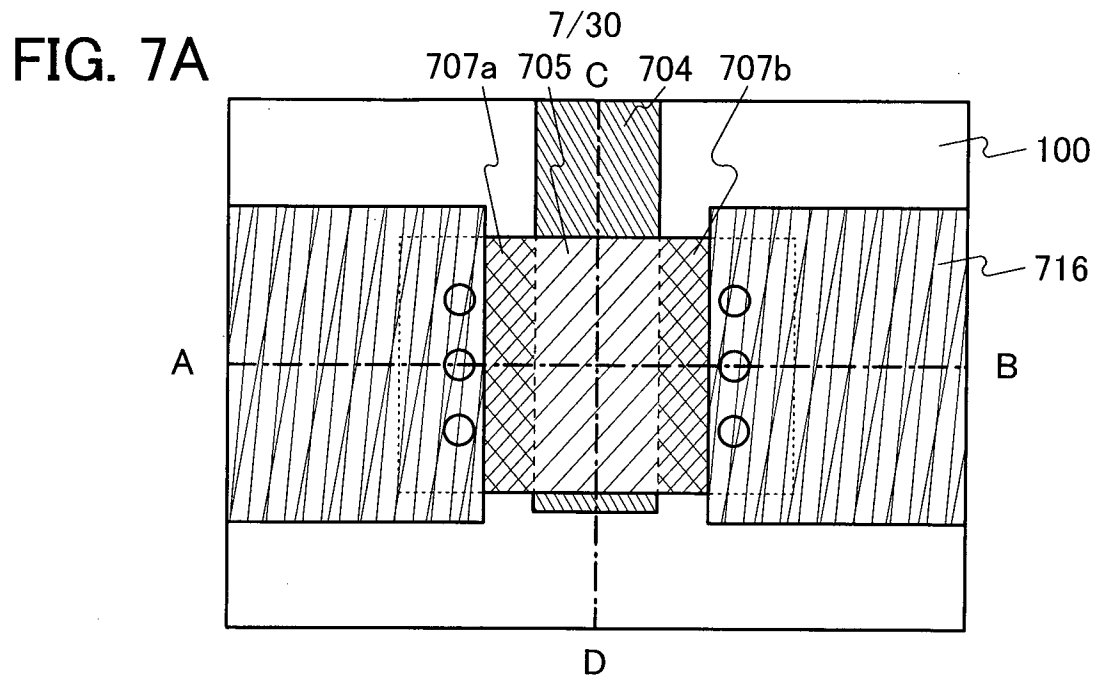
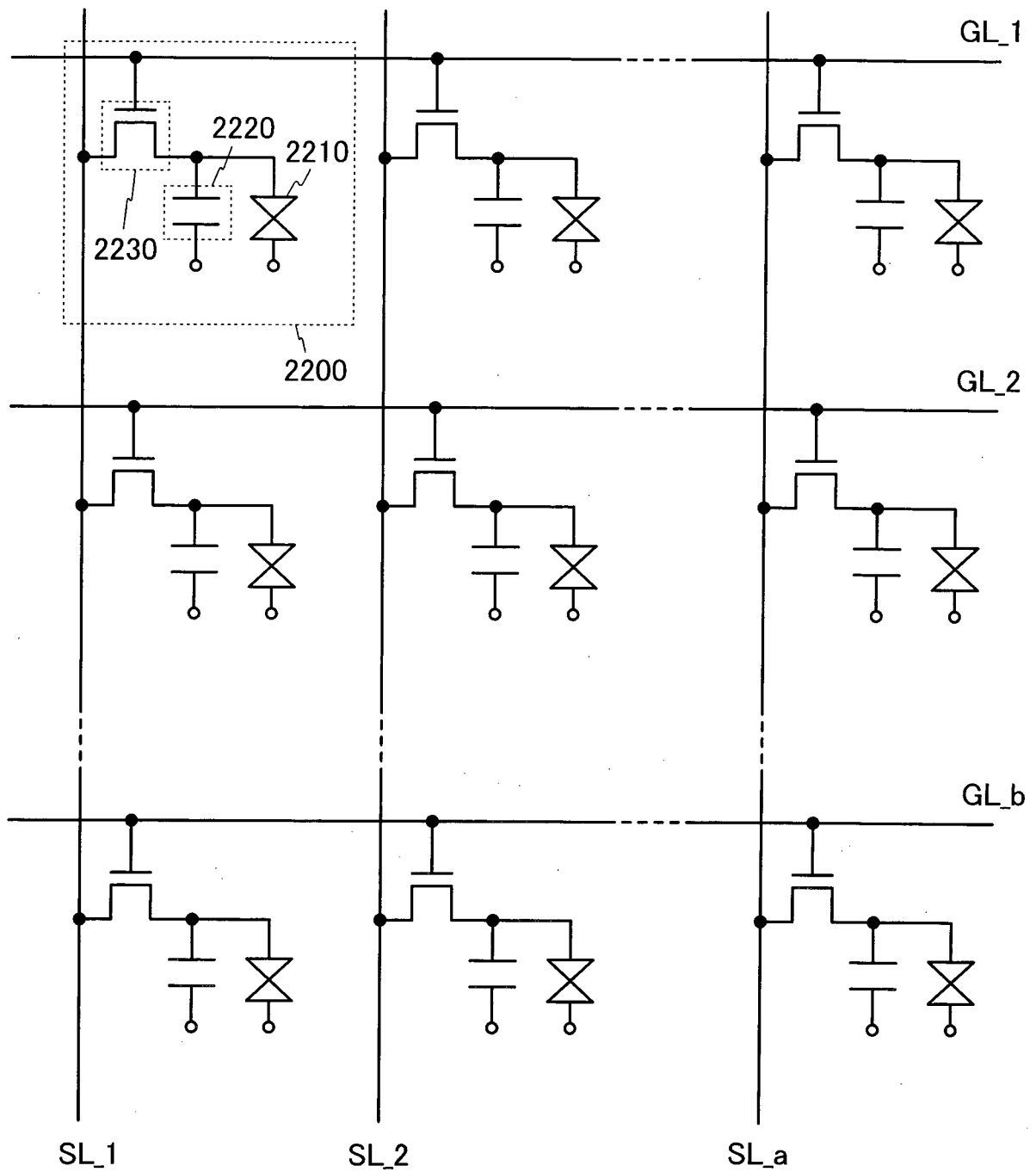


FIG. 8

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FIG. 9A

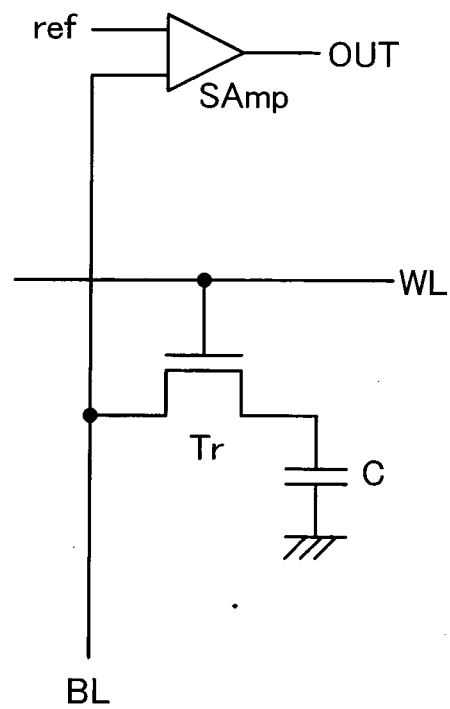
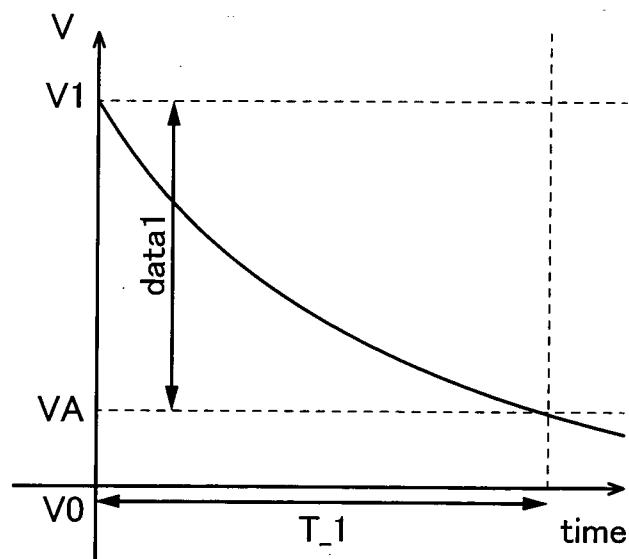


FIG. 9B



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FIG. 10A

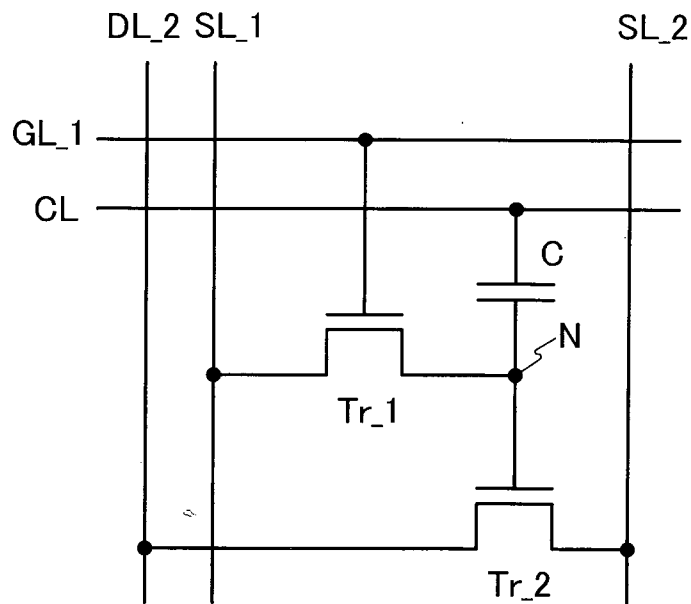


FIG. 10B

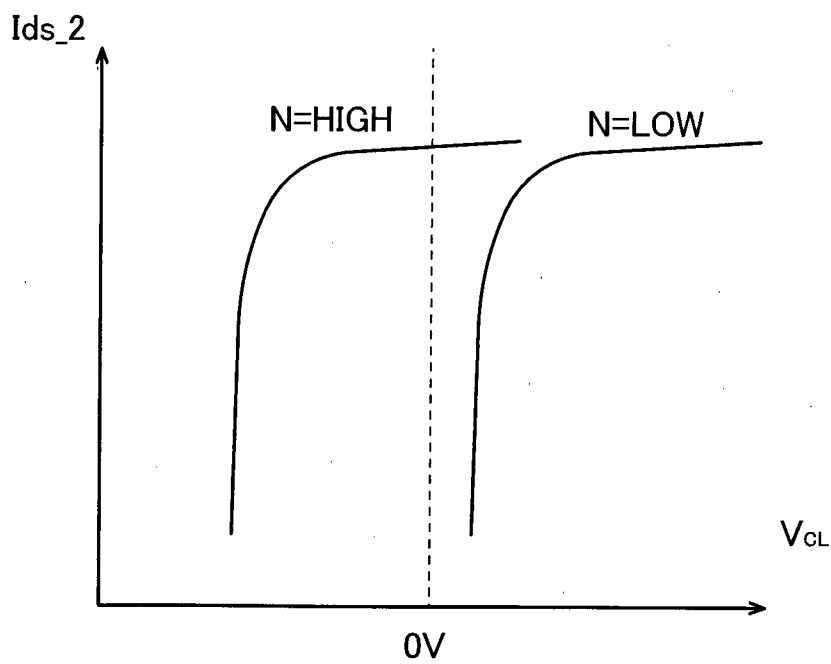
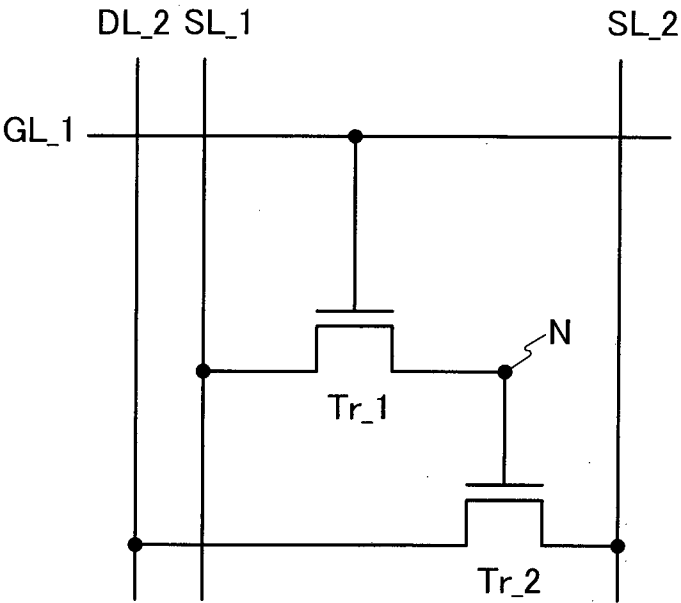


FIG. 11



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FIG. 12A

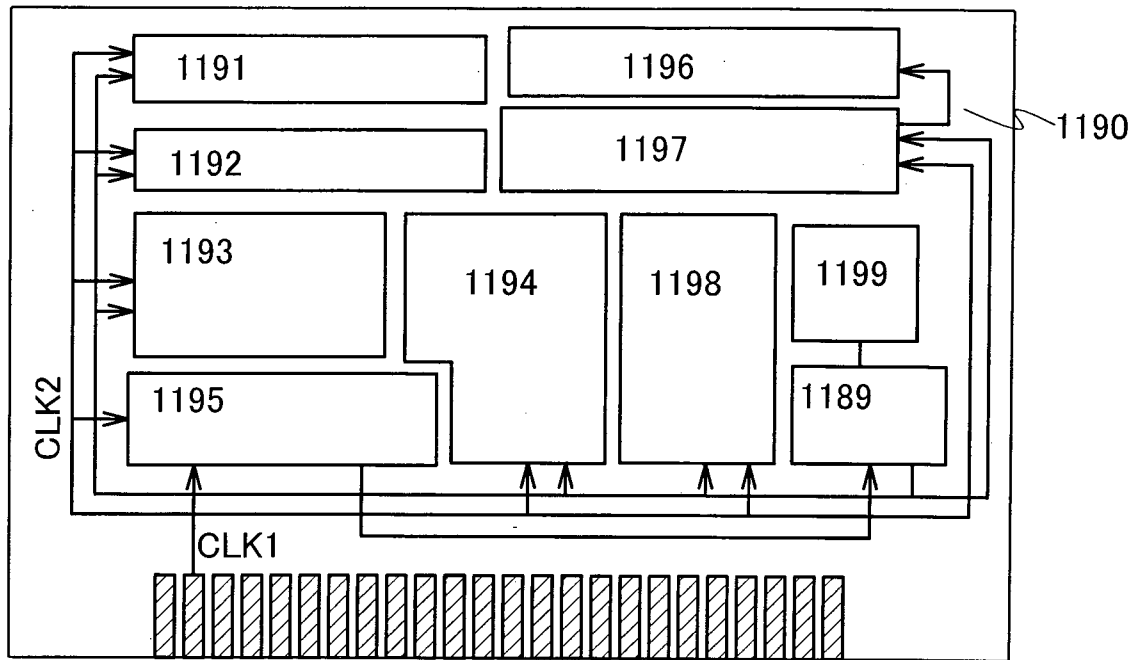


FIG. 12B

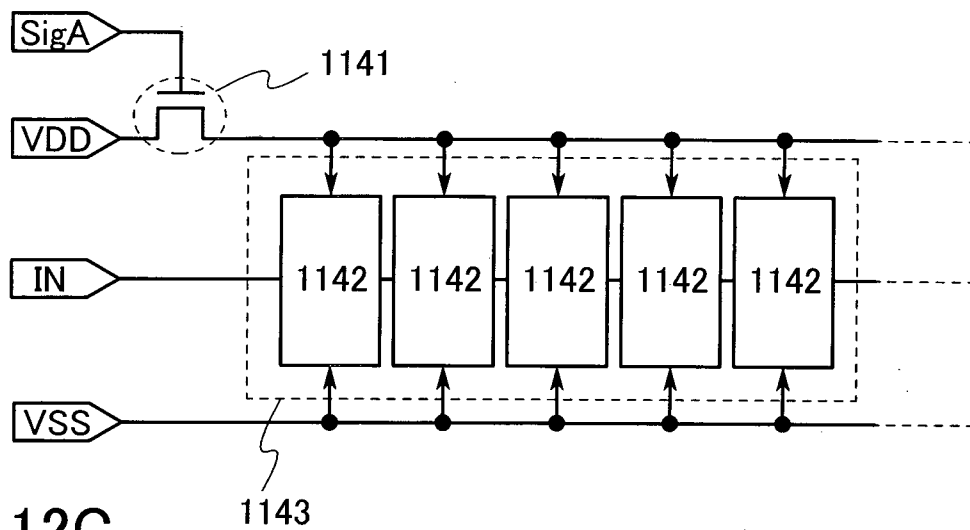
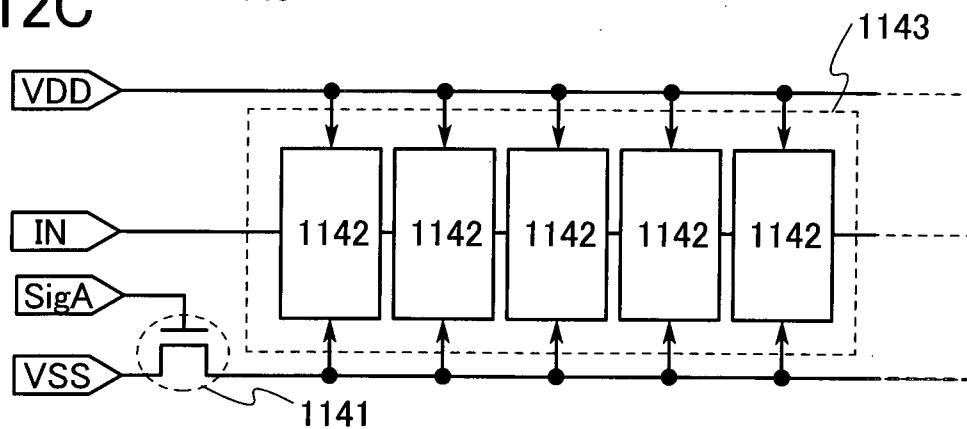


FIG. 12C



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FIG. 13A

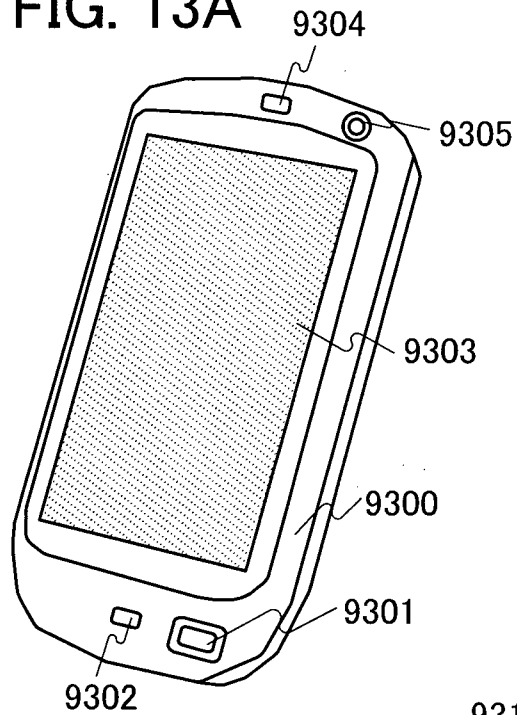


FIG. 13B

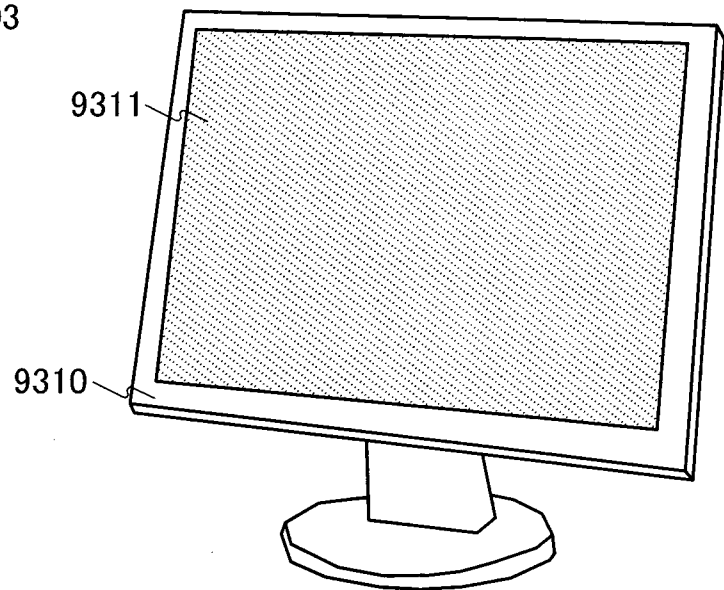
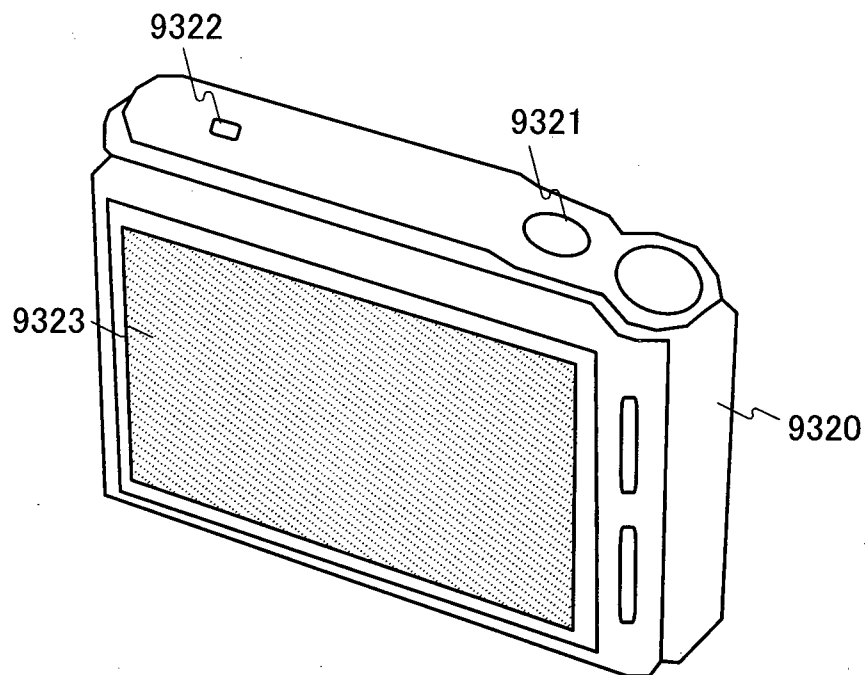


FIG. 13C



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FIG. 14A

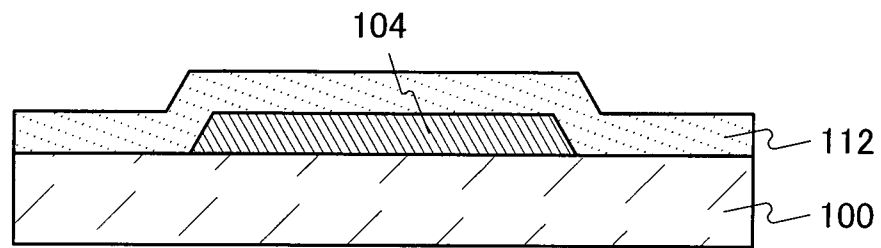


FIG. 14B

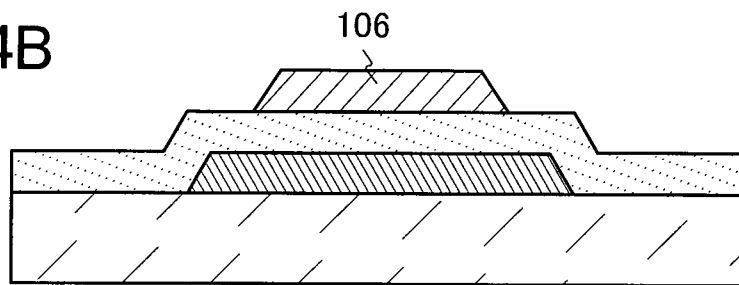


FIG. 14C

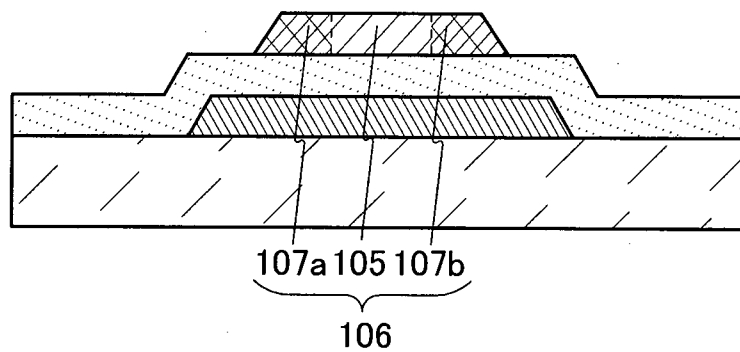


FIG. 14D

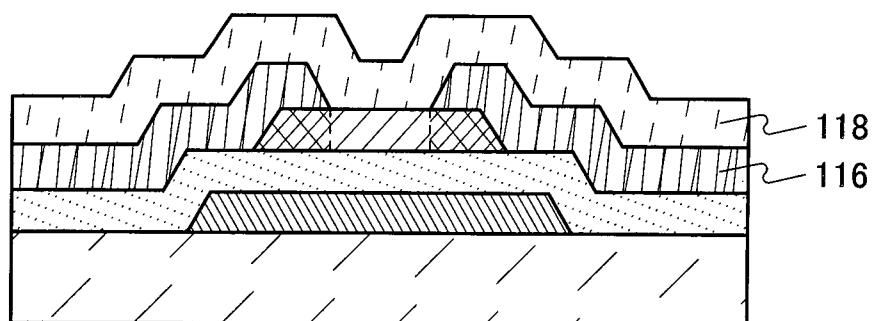


FIG. 15A

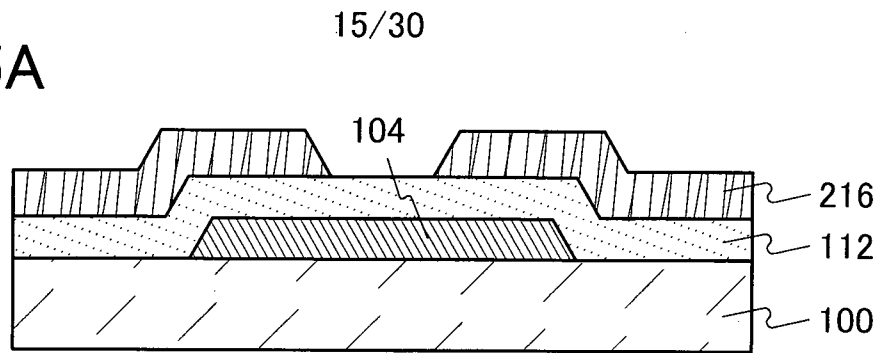


FIG. 15B

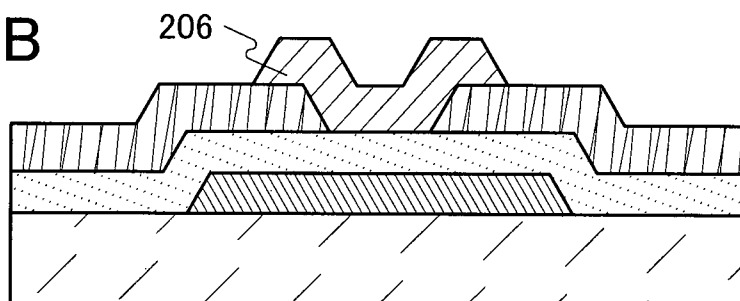


FIG. 15C

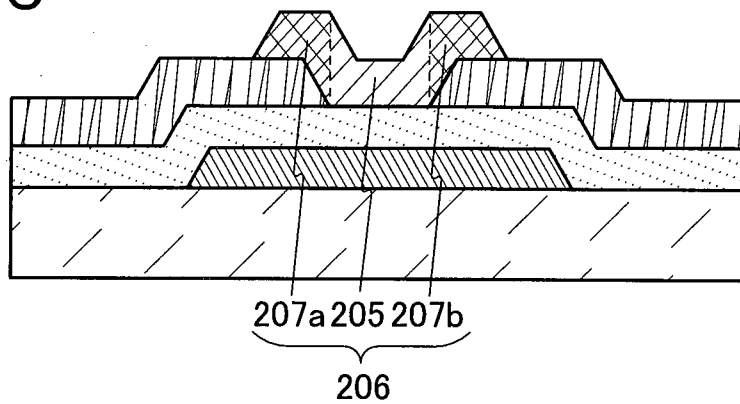
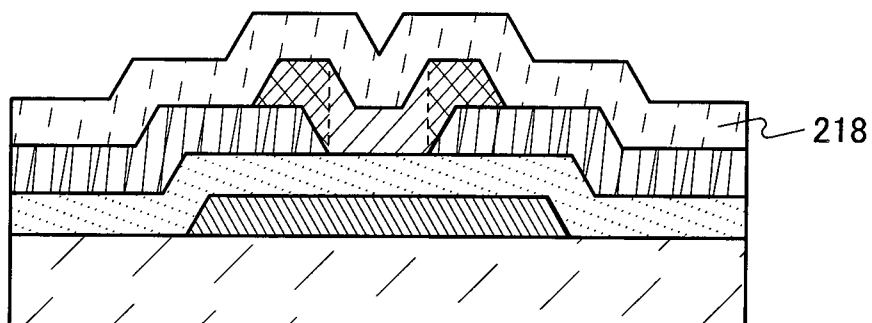


FIG. 15D



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FIG. 16A

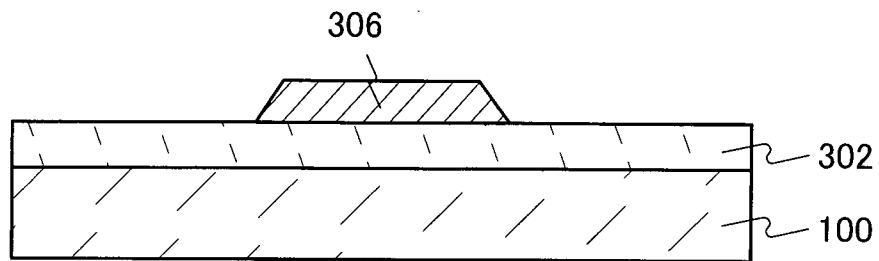


FIG. 16B

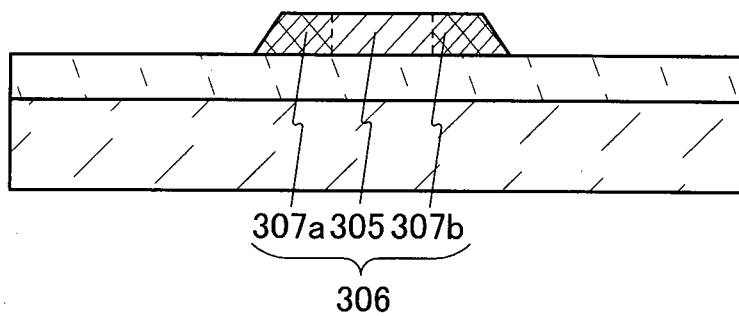


FIG. 16C

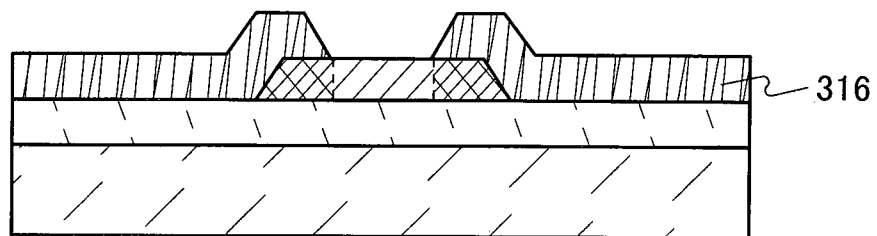
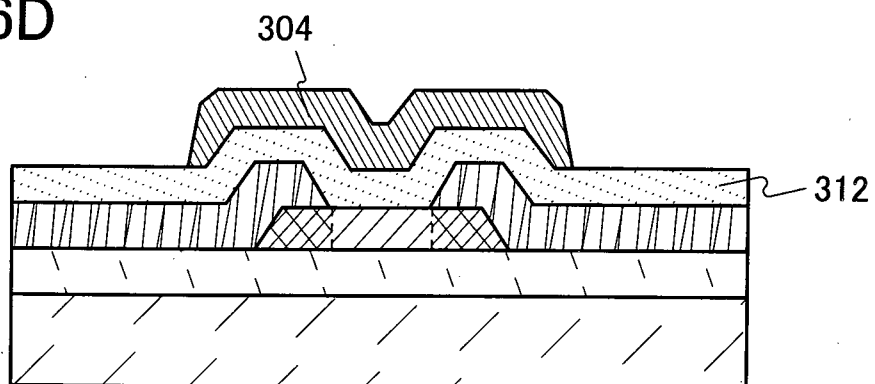


FIG. 16D



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FIG. 17A

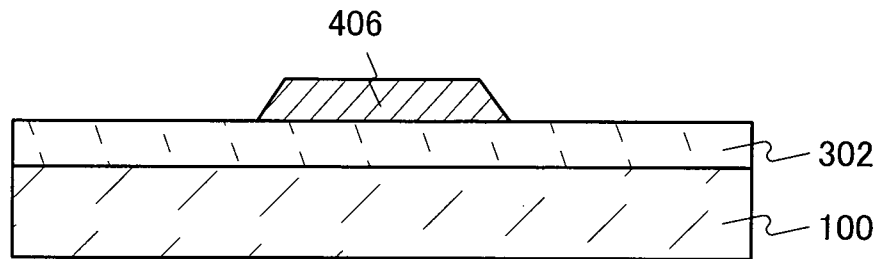


FIG. 17B

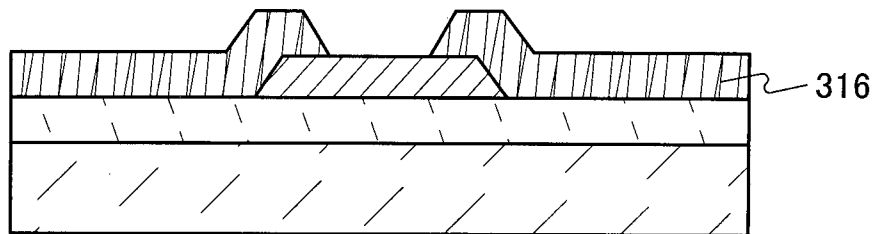


FIG. 17C

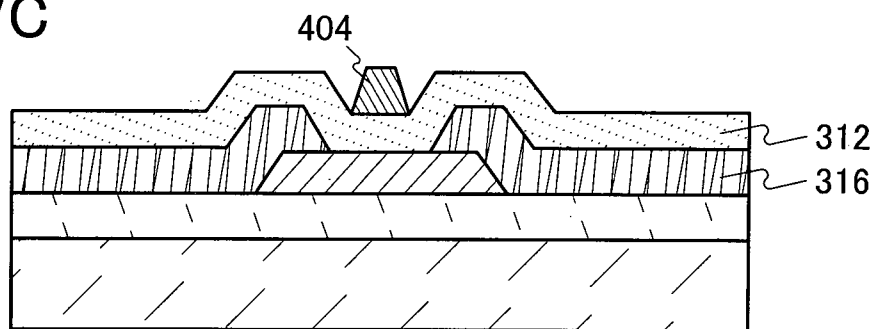
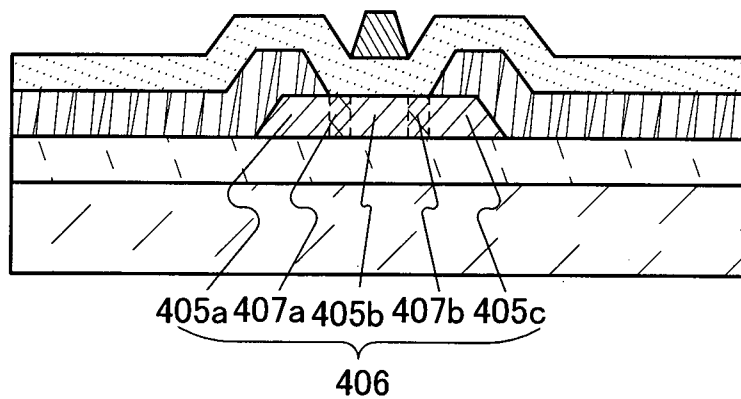


FIG. 17D



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FIG. 18A

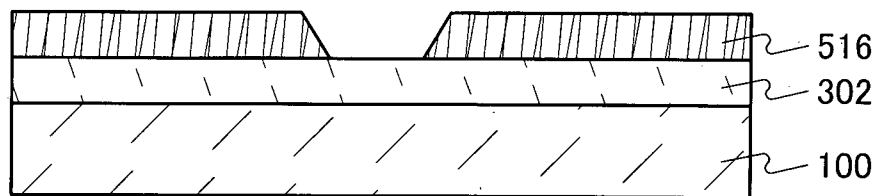


FIG. 18B

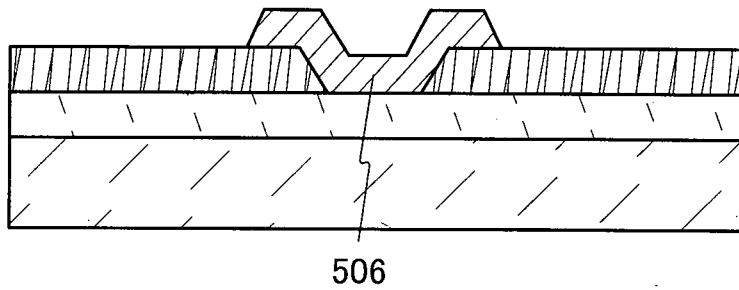


FIG. 18C

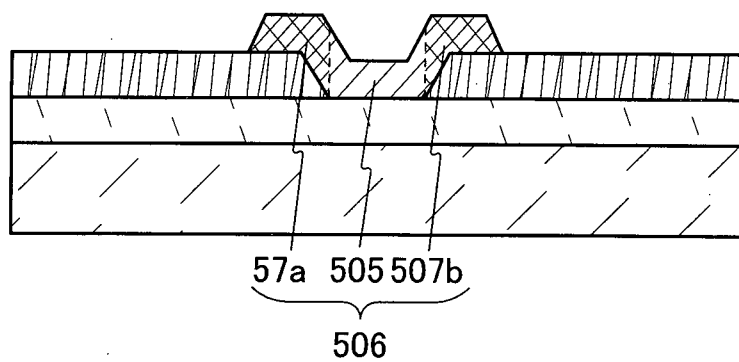
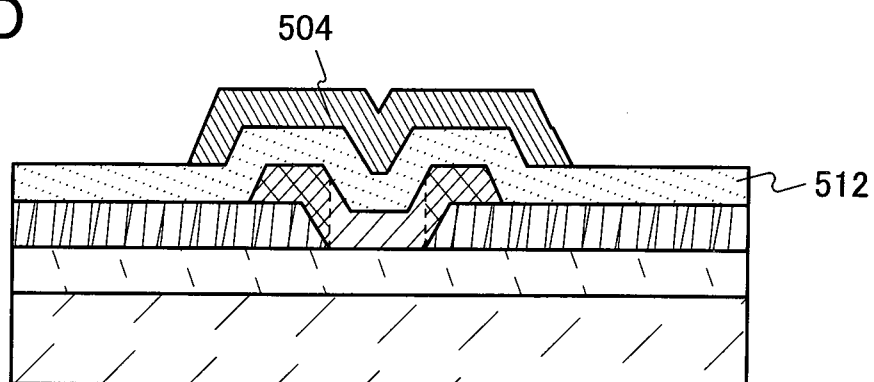


FIG. 18D



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FIG. 19A

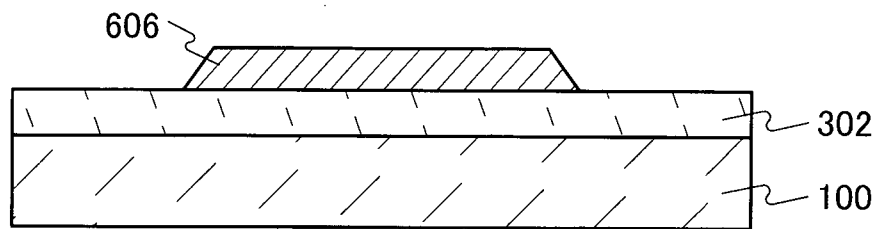


FIG. 19B

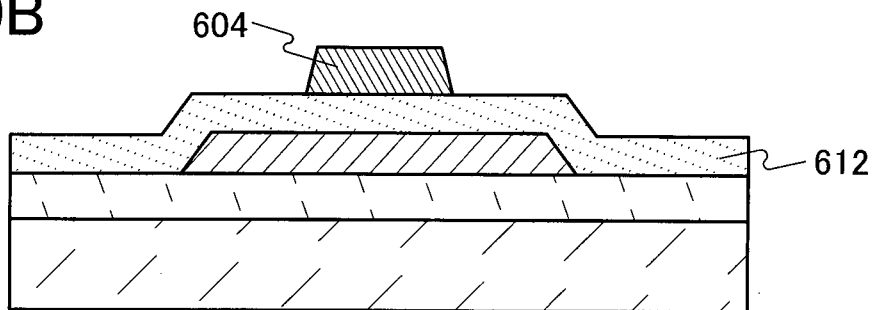


FIG. 19C

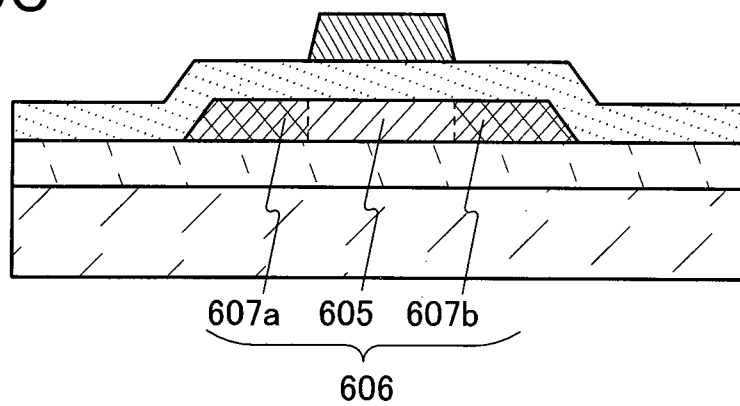
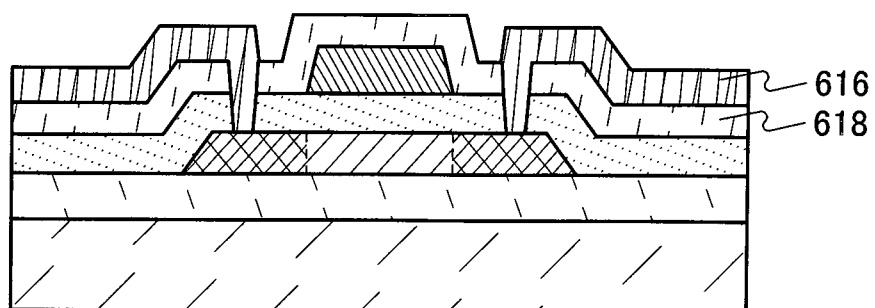


FIG. 19D



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FIG. 20A

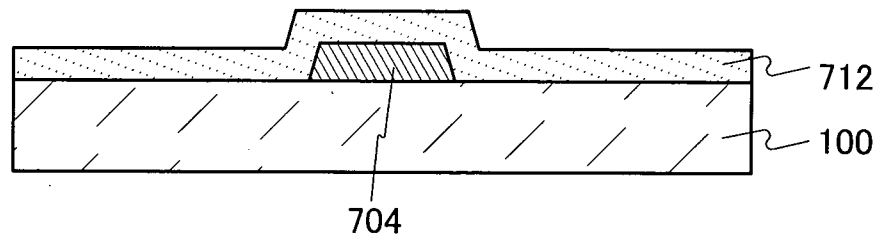


FIG. 20B

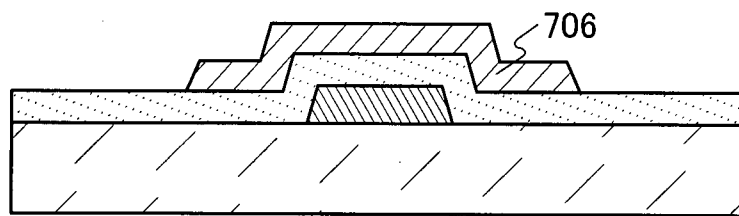


FIG. 20C

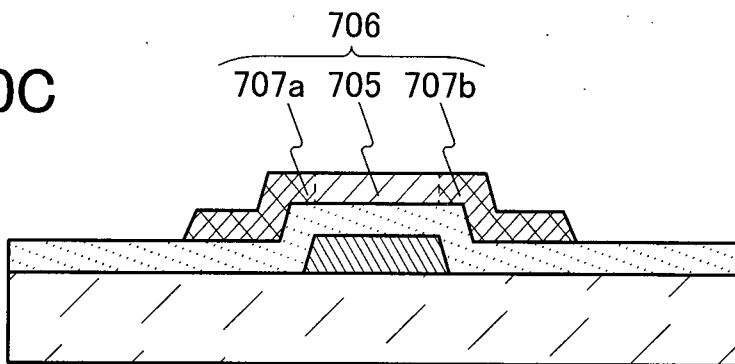
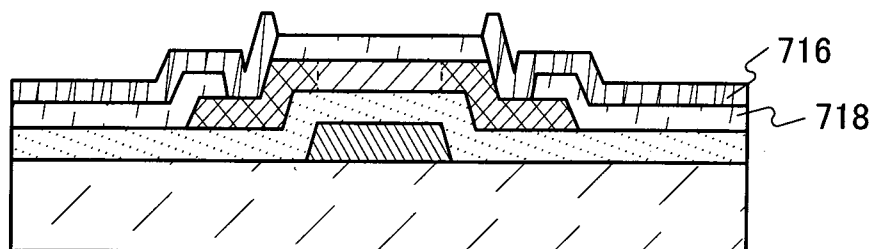


FIG. 20D



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FIG. 21A

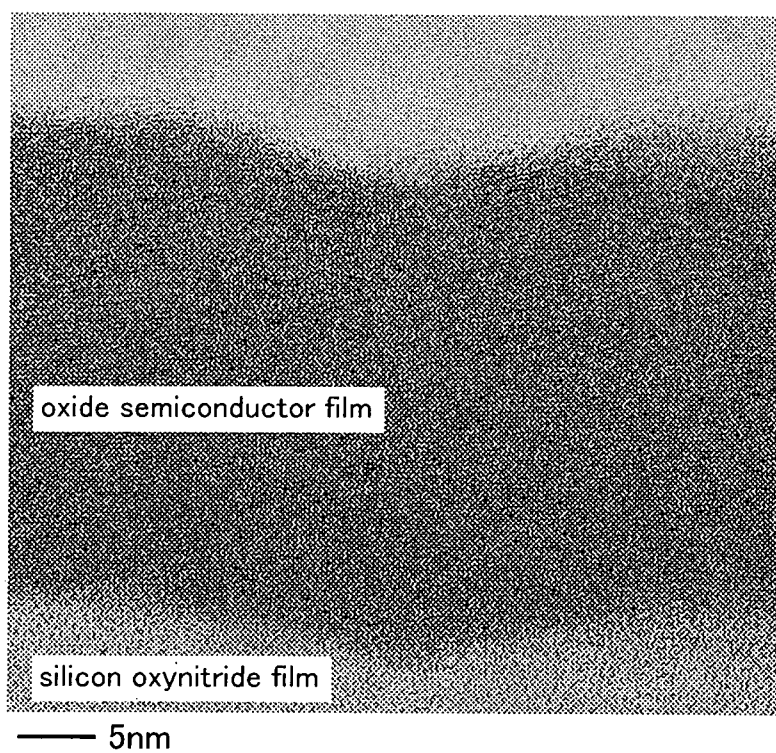
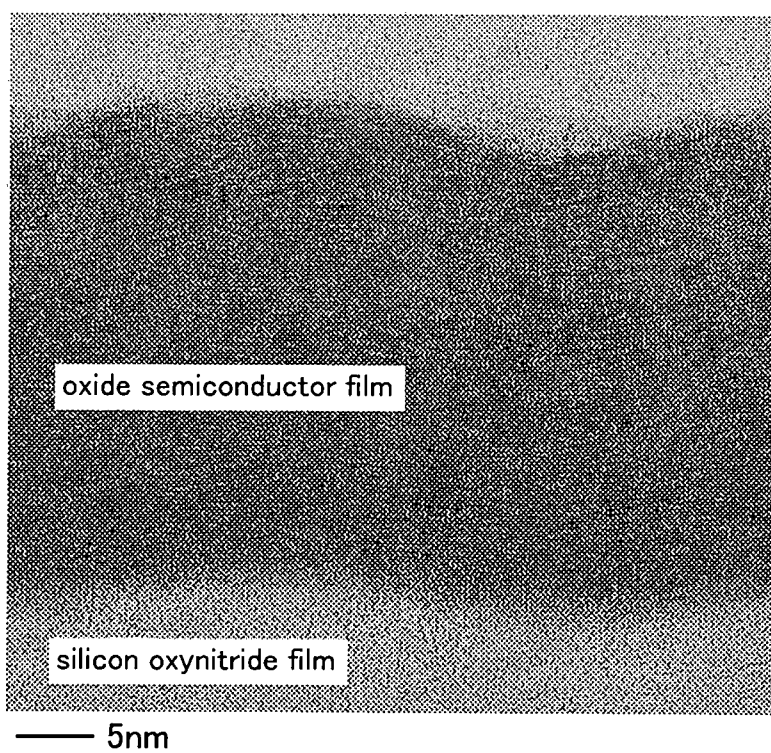


FIG. 21B



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FIG. 22A

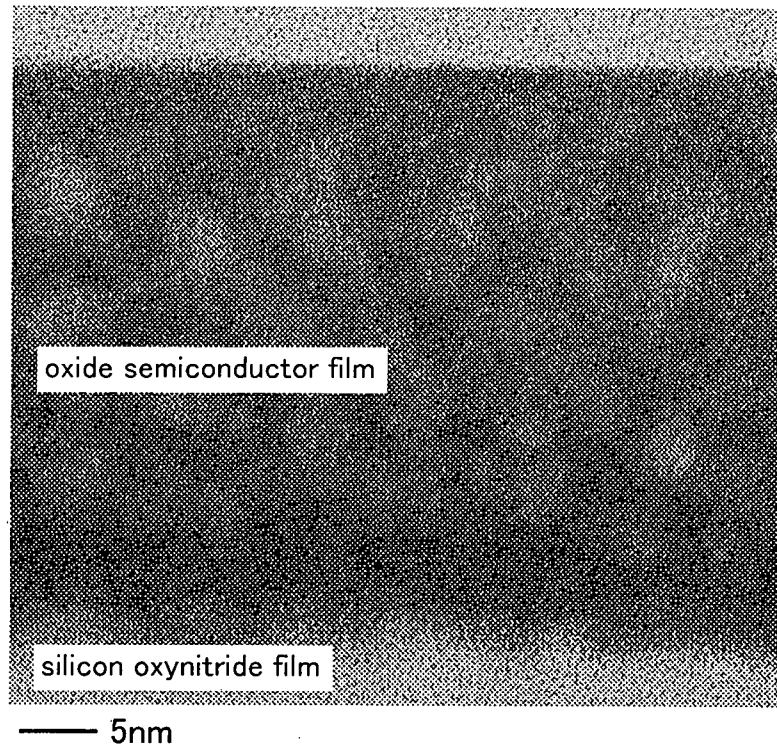
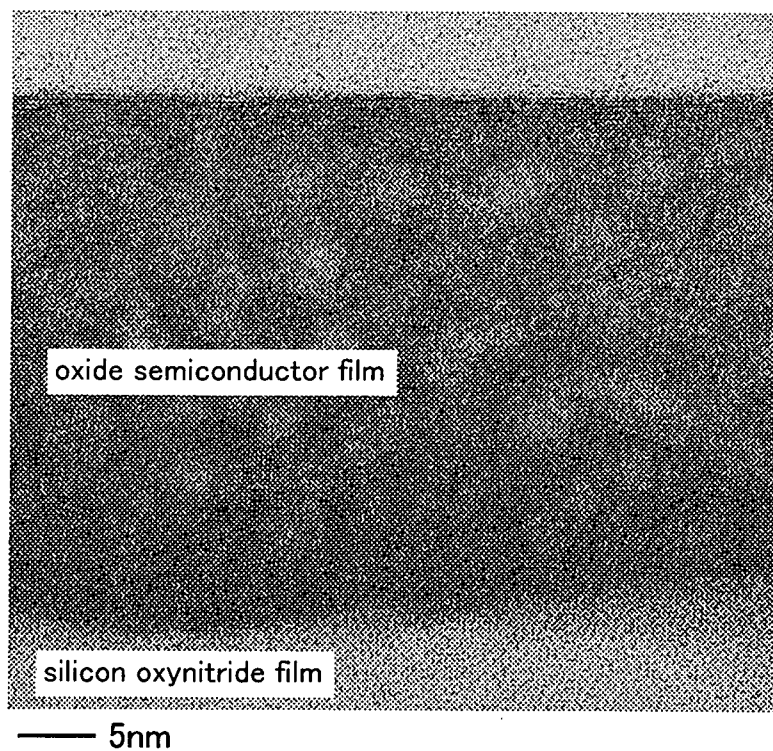


FIG. 22B



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FIG. 23A

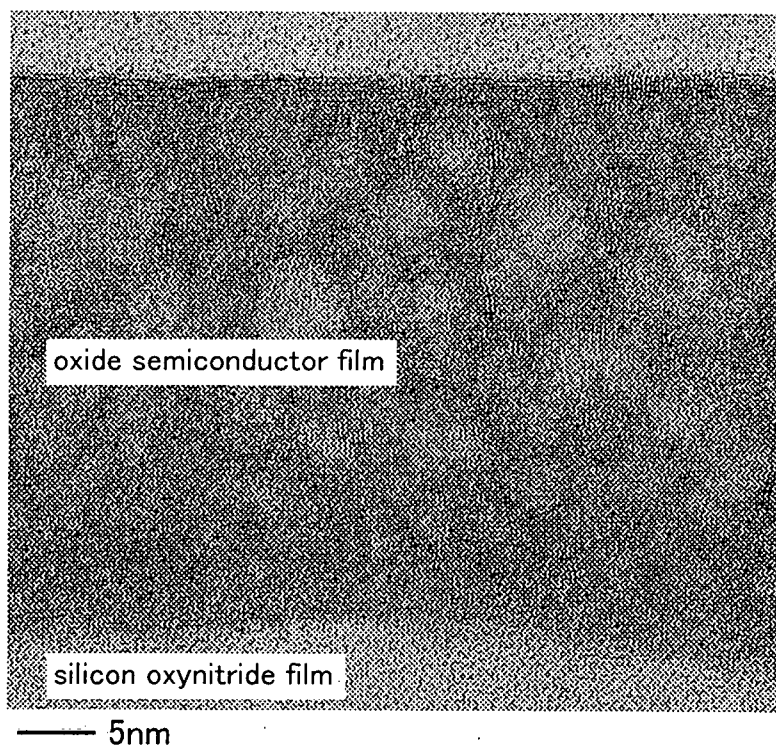
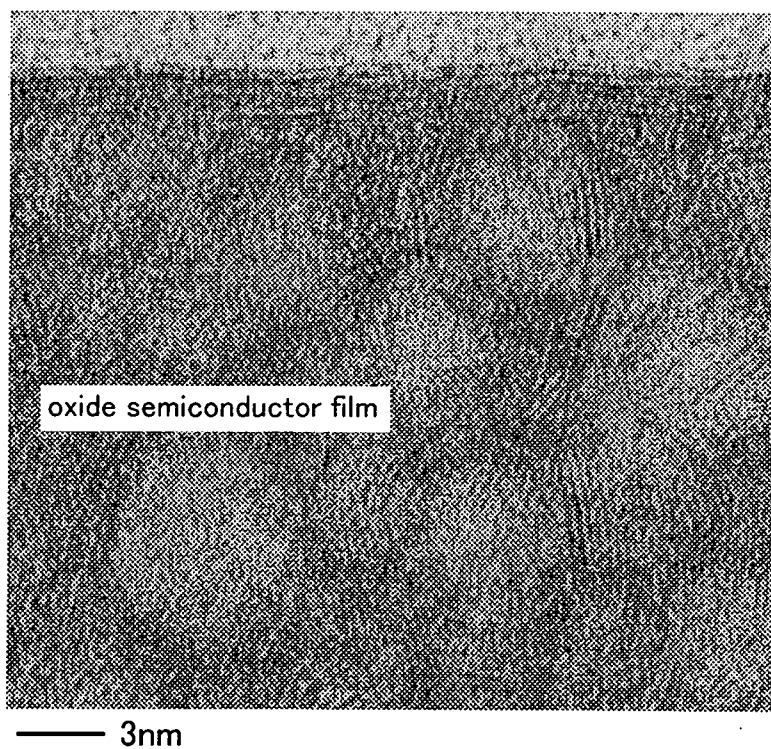


FIG. 23B



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FIG. 24A

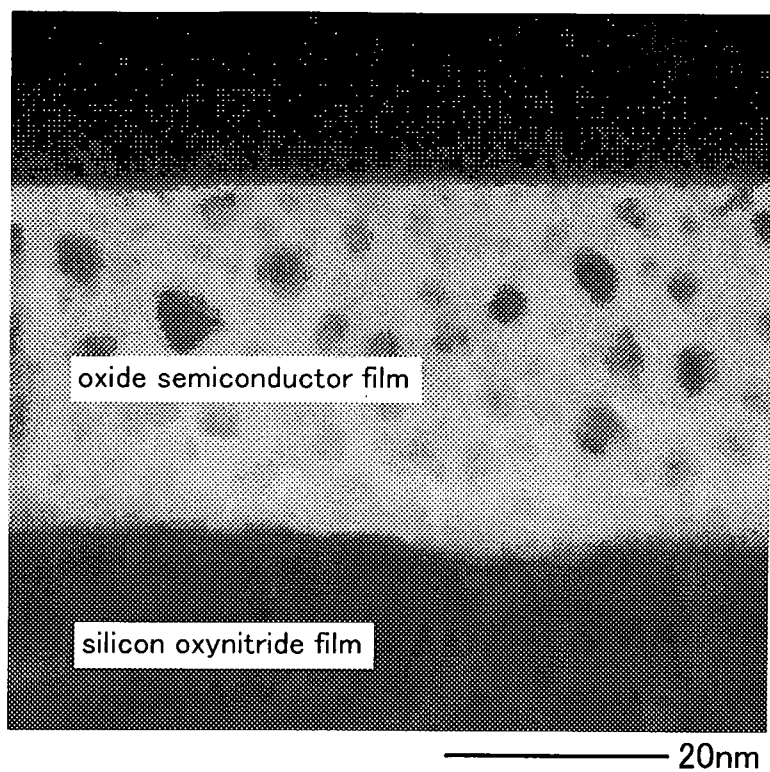
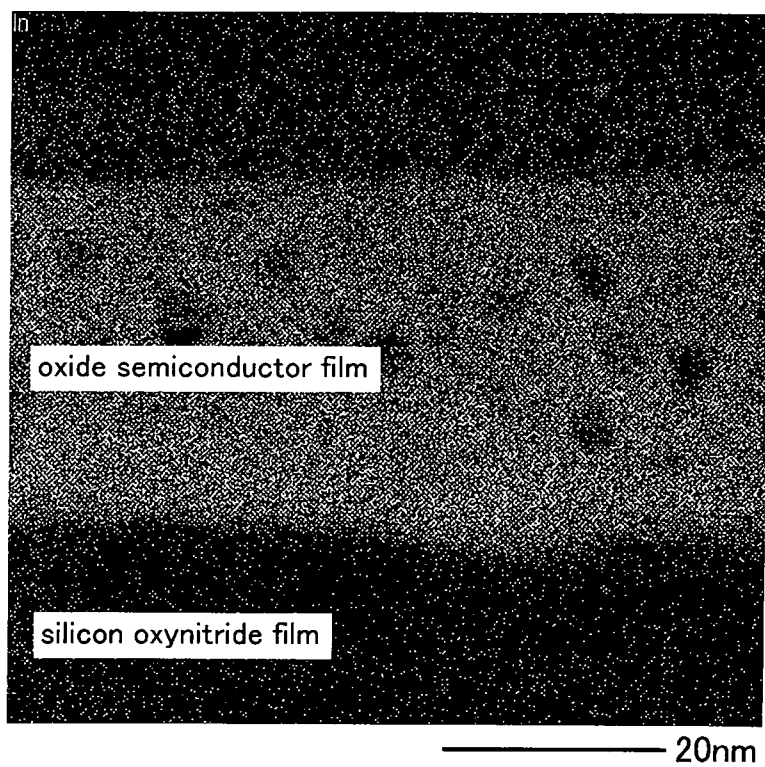


FIG. 24B



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FIG. 25A

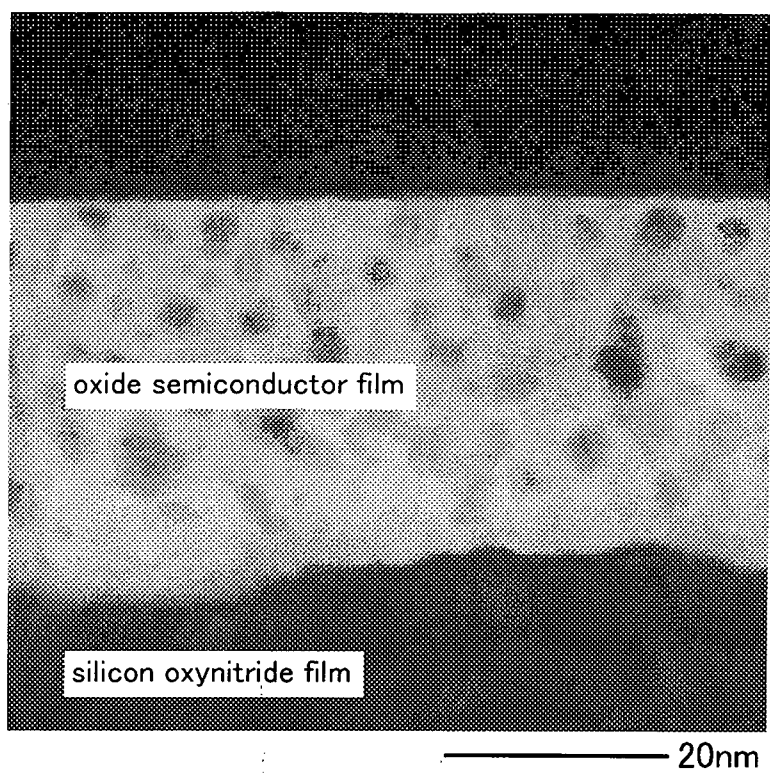
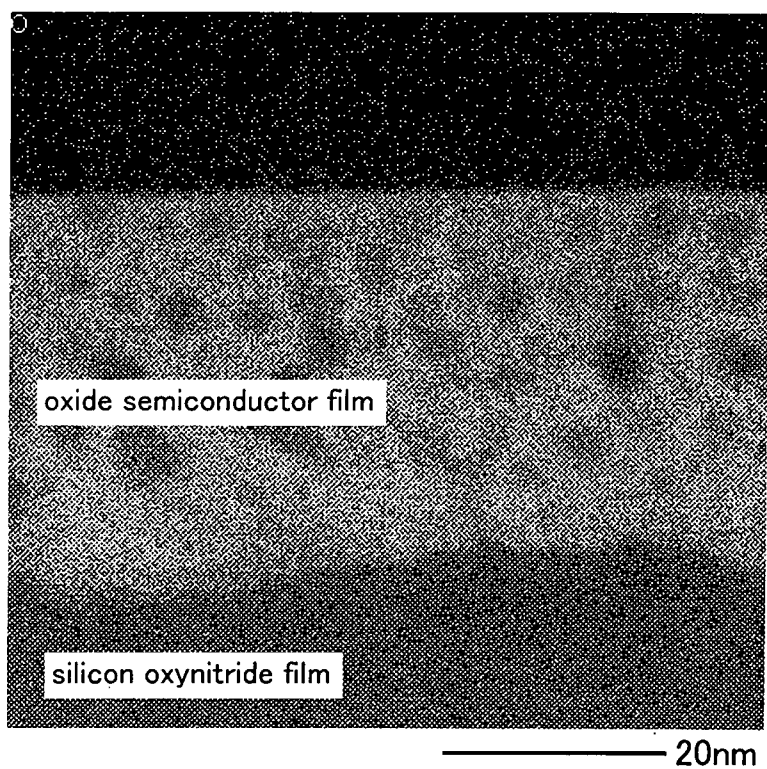


FIG. 25B



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FIG. 26A

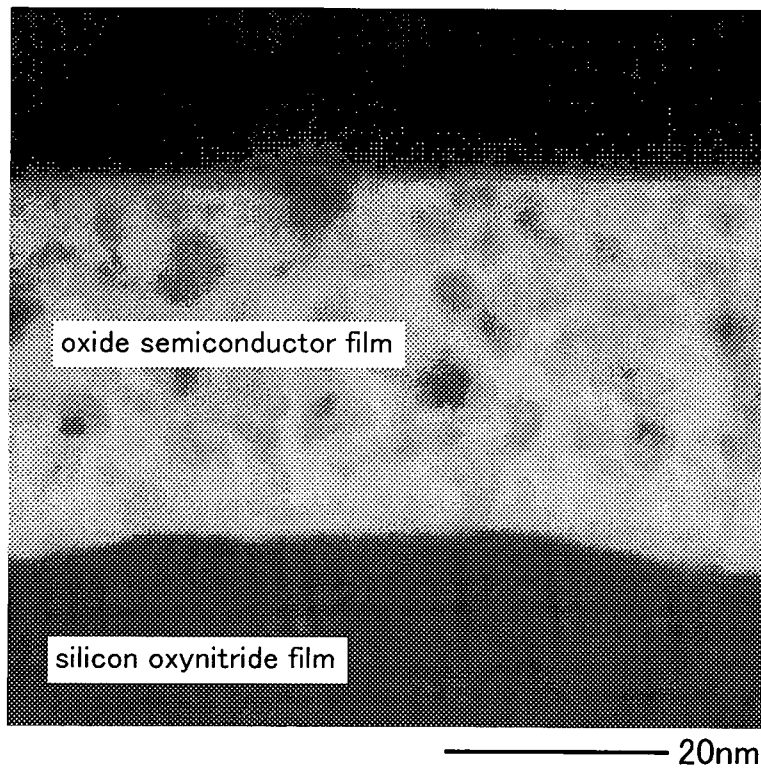
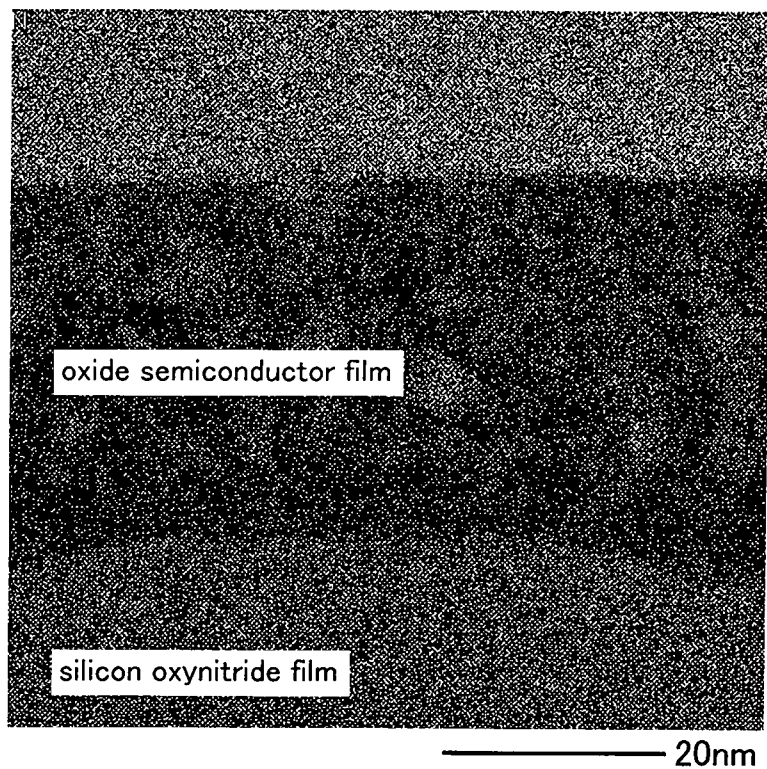
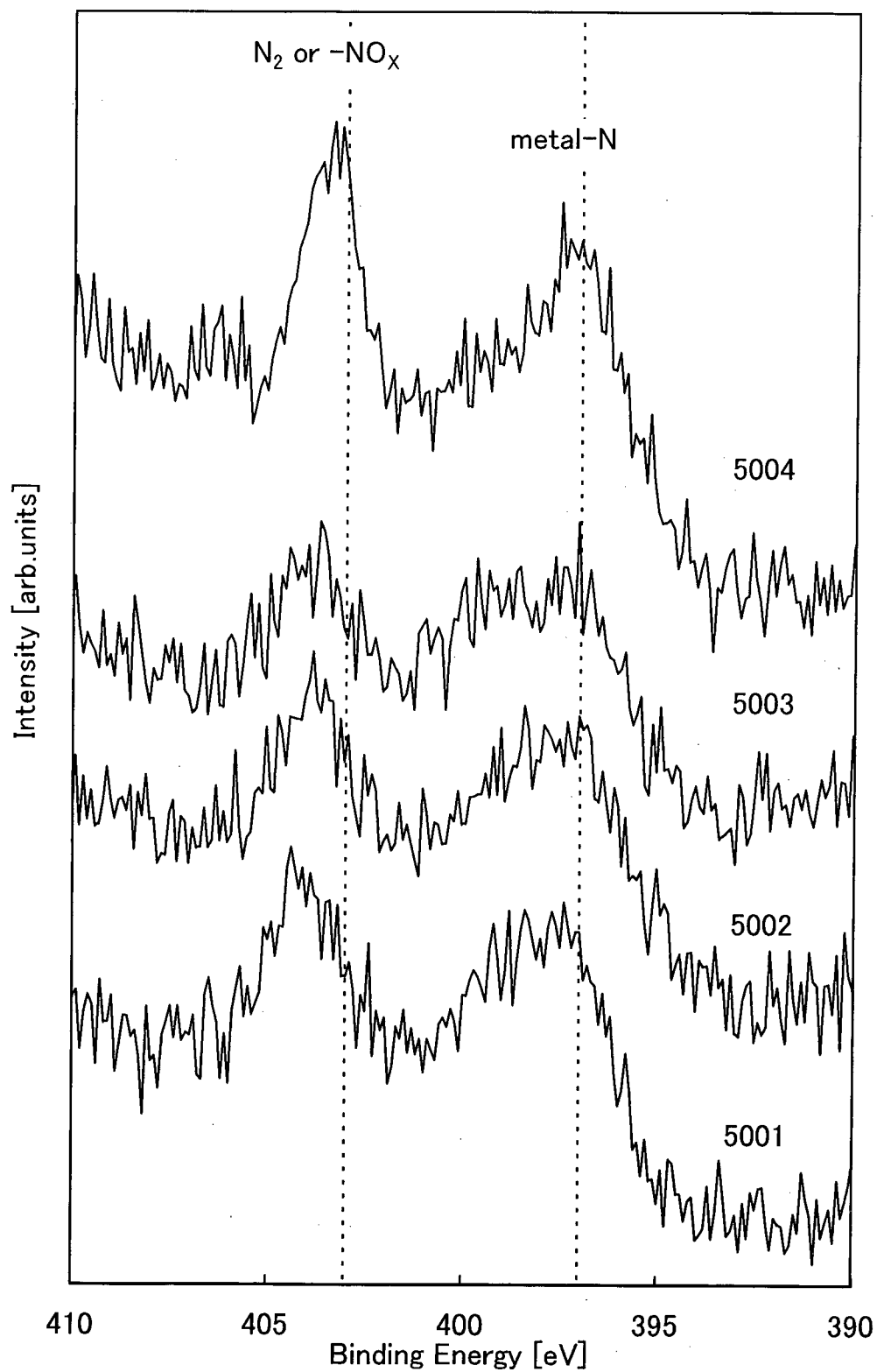


FIG. 26B



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FIG. 27



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FIG. 28A

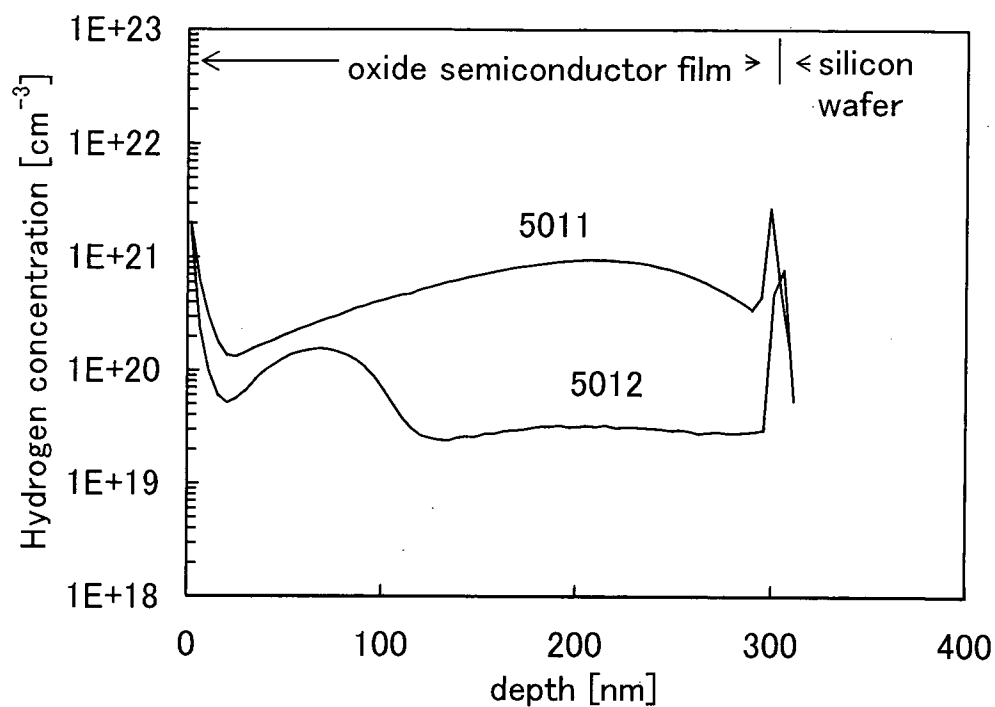
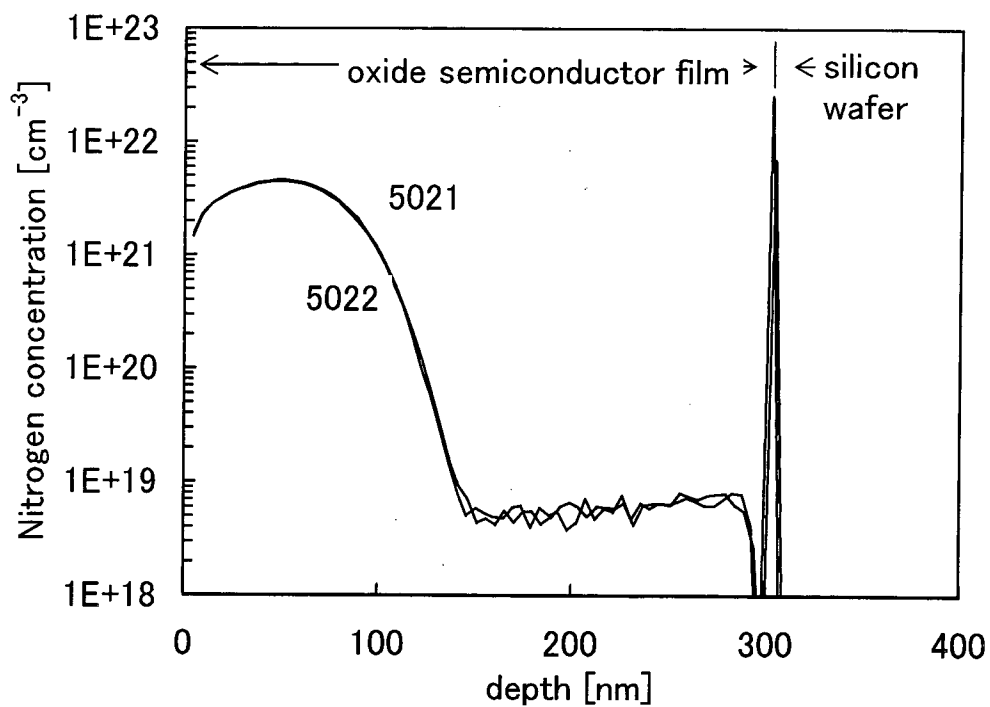


FIG. 28B



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FIG. 29A

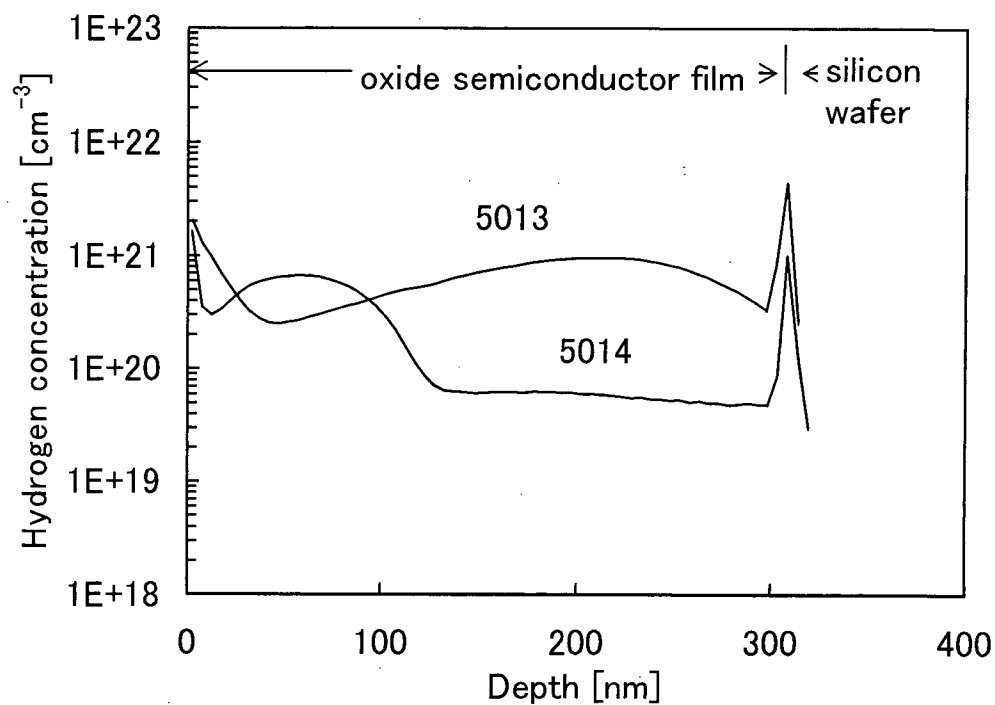
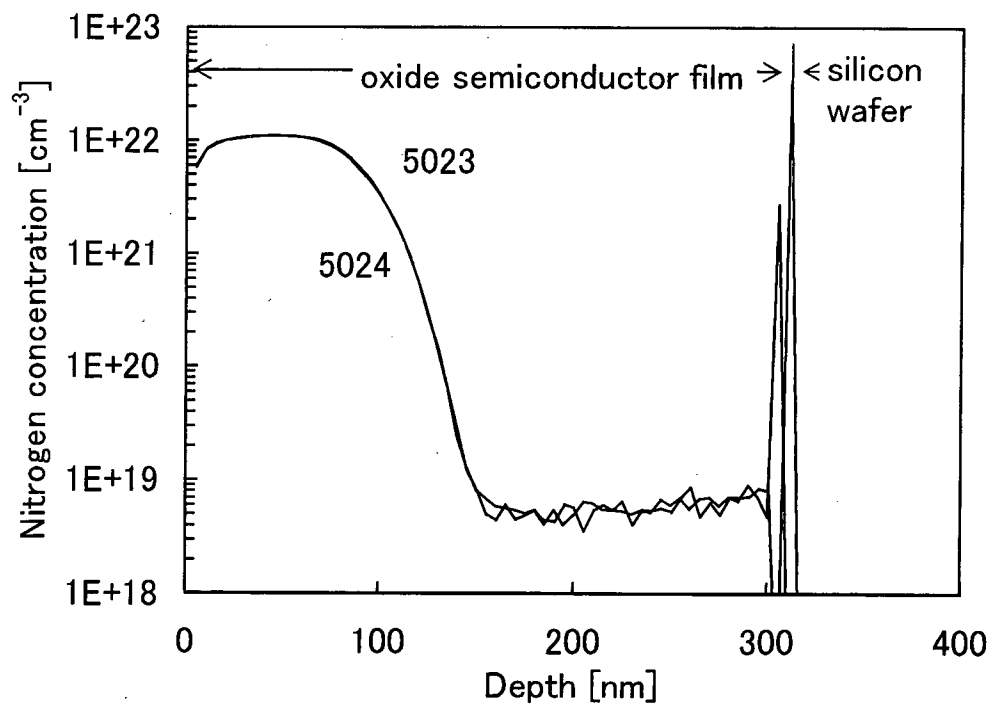
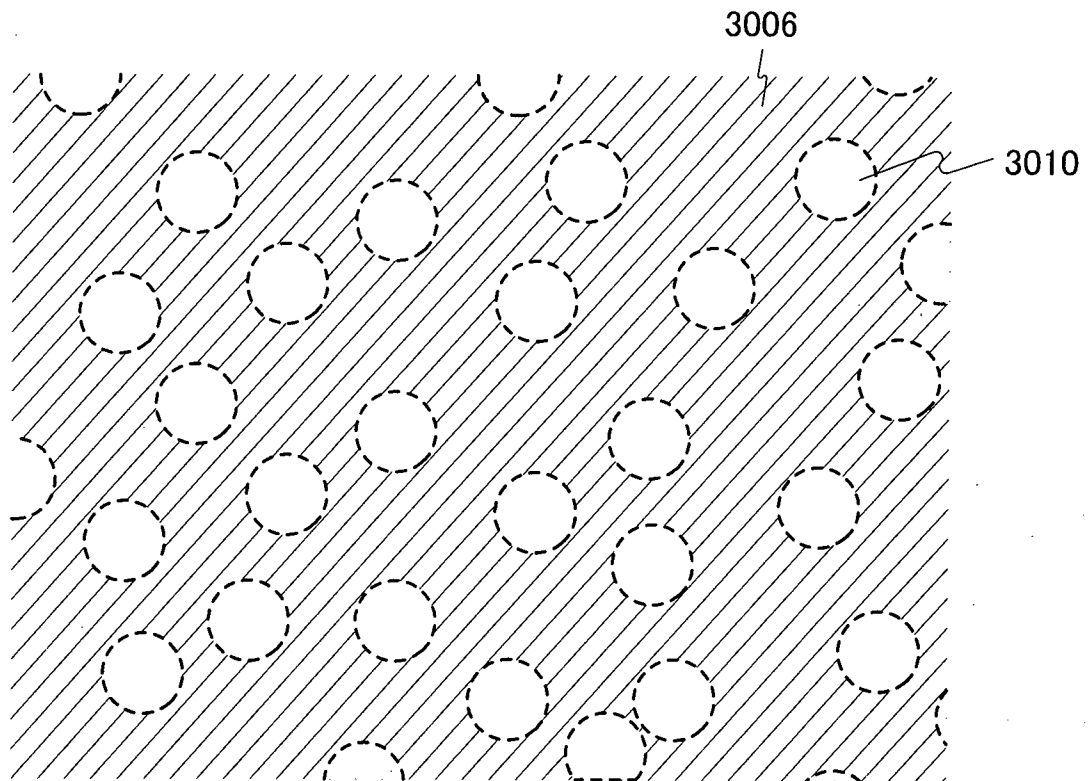


FIG. 29B



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FIG. 30



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2012/055734

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, H01L21/265, H01L21/336, H01L21/8242, H01L21/8247, H01L27/10, H01L27/108, H01L27/115, H01L29/788, H01L29/792

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
 Published unexamined utility model applications of Japan 1971-2012
 Registered utility model specifications of Japan 1996-2012
 Published registered utility model applications of Japan 1994-2012

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	JP 2010-093070 A (CANON KABUSHIKI KAISHA) 2010.04.22, Paragraphs 0034-0036, Fig.7 & US 2010/0084655 A1 & EP 2175493 A1 & CN 101719514 A	1, 2 3-31, 39-44, 4 6-51 32-38, 45
Y A	JP 2007-123861 A (Semiconductor Energy Laboratory Co, Ltd.) 2007.05.17, Page 2, lines 1-7 & US 2007/0072439 A1 & EP 1770788 A2 & CN 1941299 A	3 32-38, 45
Y A	JP 2009-260254 A (ELECTRONICS AND TELECOMMUNICATIONS RESEARCH INSTITUTE) 2009.11.05, Figs.1-4 & US 2009/0261389 A1	4-31, 39-42, 46 -49 32-38, 45



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

28.03.2012

Date of mailing of the international search report

10.04.2012

Name and mailing address of the ISA/JP

Japan Patent Office

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2012/055734

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	JP 2009-099953 A (CANON KABUSHIKI KAISHA) 2009.05.07, Fig.1 & US 2010/0203673 A1 & WO 2009/041713 A2 & CN 101809748 A	43, 44, 50, 51 32-38, 45

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2012/055734

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

D1 discloses an oxide semiconductor film added nitrogen $2 \times 10^{19} \text{ cm}^{-3}$ by ion implantation. And it is obvious that the oxide semiconductor film includes microvoid. Therefore, claim 1 lacks novelty over D1, and involves no special technical features. Thus, the requirement of unity of invention is not complied with.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2012/055734

CLASSIFICATION OF SUBJECT MATTER

H01L29/786(2006.01) i, H01L21/265(2006.01) i, H01L21/336(2006.01) i,
H01L21/8242(2006.01) i, H01L21/8247(2006.01) i, H01L27/10(2006.01) i,
H01L27/108(2006.01) i, H01L27/115(2006.01) i, H01L29/788(2006.01) i,
H01L29/792(2006.01) i