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Momoi et al.(10) **Pub. No.: US 2009/0085196 A1**(43) **Pub. Date: Apr. 2, 2009**(54) **INTEGRATED CIRCUIT CHIP
MANUFACTURING METHOD AND
SEMICONDUCTOR DEVICE**(30) **Foreign Application Priority Data**

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Publication Classification(75) Inventors: **Kazutaka Momoi**, Hiratsuka-shi
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Sagamihara-shi (JP)(51) **Int. Cl.**
H01L 23/12 (2006.01)(52) **U.S. Cl.** **257/707; 257/E23.005**(57) **ABSTRACT**

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NEW YORK, NY 10112 (US)**(73) Assignee: **CANON KABUSHIKI KAISHA**,
Tokyo (JP)(21) Appl. No.: **12/328,182**(22) Filed: **Dec. 4, 2008****Related U.S. Application Data**(62) Division of application No. 11/149,145, filed on Jun.
10, 2005, now Pat. No. 7,473,617.

This invention moderates the difficulty in chip formation or packaging which accompanies thinning of a semiconductor region where an integrated circuit is formed. An integrated circuit chip manufacturing method includes a first bonding step of bonding a first support member to a first surface of a semiconductor substrate which has the first surface and a second surface and has a semiconductor region including an integrated circuit on a first surface side thereof, a thinning step of removing a second surface-side portion of the semiconductor substrate bonded to the first support member to leave the semiconductor region, thereby thinning the semiconductor substrate, a second bonding step of bonding a second support member to the second surface side of the thinned semiconductor substrate, and a chip forming step of forming chips by cutting the semiconductor region.

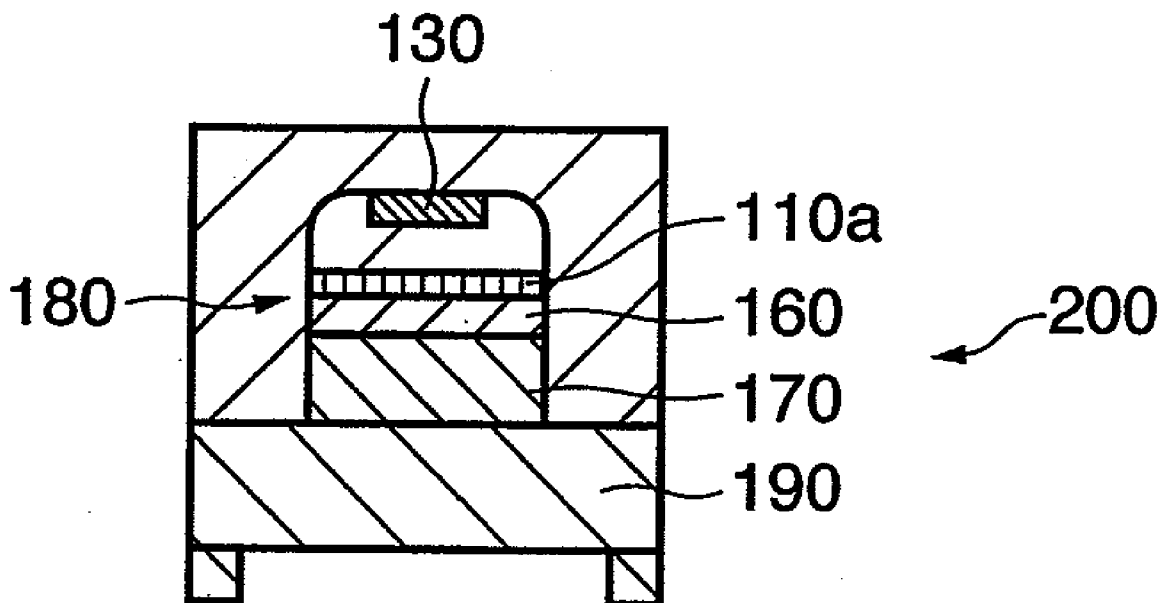


FIG. 1A

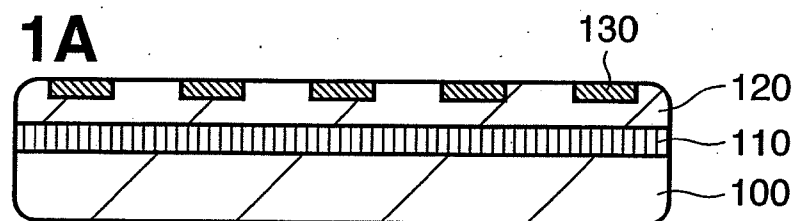


FIG. 1B

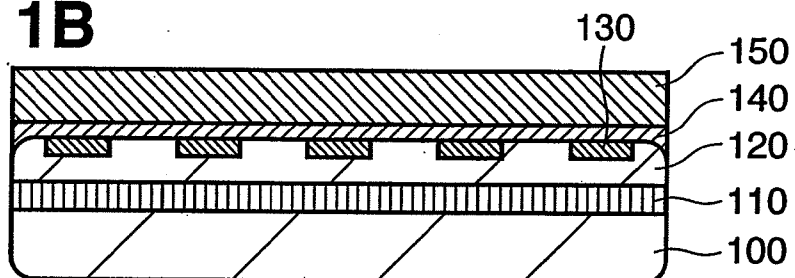


FIG. 1C

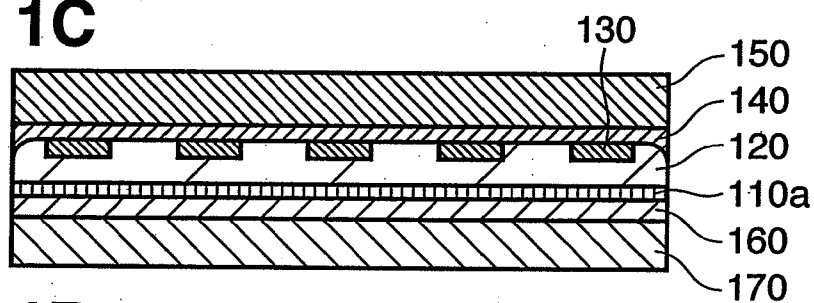


FIG. 1D

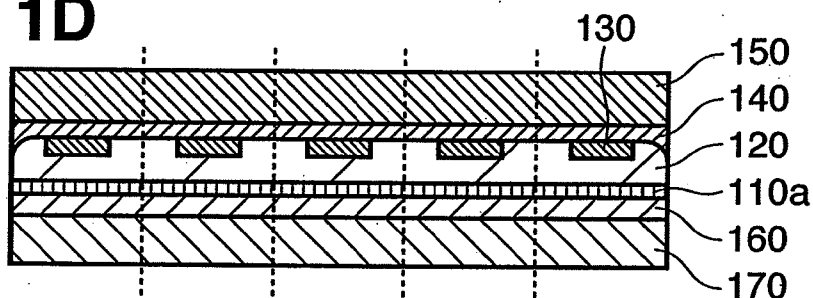


FIG. 1E

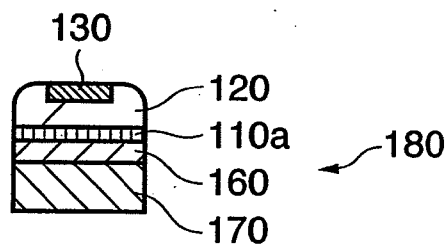


FIG. 1F

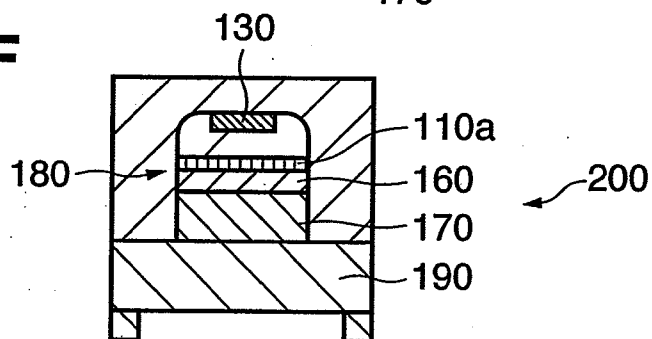


FIG. 2A

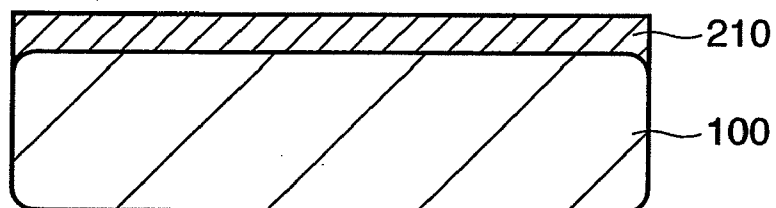


FIG. 2B

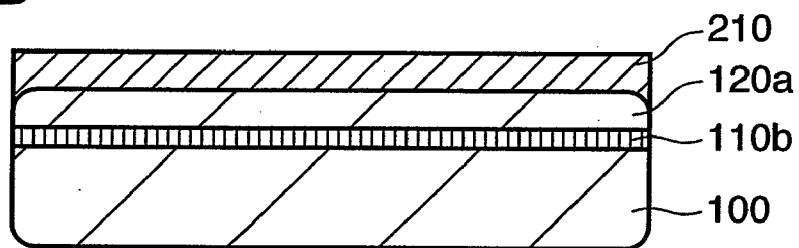
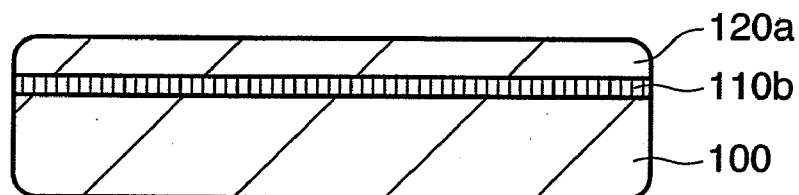


FIG. 2C



INTEGRATED CIRCUIT CHIP MANUFACTURING METHOD AND SEMICONDUCTOR DEVICE

FIELD OF THE INVENTION

[0001] The present invention relates to an integrated circuit chip manufacturing method and semiconductor device.

BACKGROUND OF THE INVENTION

[0002] In recent years, a technique which thins a semiconductor device attracts attention. According to the technique disclosed in patent reference 1, a protection film, protection insulating layer, and thin film layer are sequentially formed on the first substrate. The second substrate is adhered to the thin film layer with an adhesive. After that, the first substrate is removed by etching. The protection film is further removed to expose the protection insulating layer. A protection substrate is adhered to the protection insulating layer with an adhesive. After that, flexible cables are connected to the electrode portions of the thin film layer to manufacture an active matrix type organic electroluminescence display. Patent reference 1 is aimed at manufacturing a large-area thin film layer which is to be used as a display, and is not aimed at forming chips from a panel obtained by adhering a protection substrate.

[0003] According to the technique disclosed in patent reference 2, a semiconductor device is formed on a semi-insulating GaAs substrate by molecular beam epitaxy. The semiconductor device is separated by epitaxial lift-off from the substrate on which it is formed, and placed on a diamond substrate having a high thermal conductivity. However, patent reference 2 does not disclose forming chips from the semiconductor device placed on the diamond substrate.

[0004] According to the technique disclosed in patent reference 3, a semiconductor film having a semiconductor device is formed on a separation layer to form a substrate. The substrate is adhered to a support member. The resultant member is divided by using the separation layer. After that, the semiconductor film is formed into chips.

Patent Reference 1:

[0005] Japanese Patent Laid-Open No. 2003-323132

Patent Reference 2:

[0006] Japanese Patent Laid-Open No. 2000-58562

Patent Reference 3:

[0007] Japanese Patent Laid-Open No. 2002-231909

[0008] In the viewpoint of improving the flexibility, enabling multilayer formation, and increasing heat radiation, a demand has arisen for thinning a semiconductor device. Thinning of the semiconductor device can lead to damages of the semiconductor device during dicing, and make it difficult to hold a chip during die bonding.

SUMMARY OF THE INVENTION

[0009] The present invention has been made on the recognition of the above problems, and has as its object to moderate the difficulty in chip formation or packaging which accompanies thinning of a semiconductor region where an integrated circuit is formed and, more particularly, facilitate dicing, die bonding, and the like.

[0010] According to the first aspect of the present invention, there is provided an integrated circuit chip manufacturing method comprising a first bonding step of bonding a first support member to a first surface of a semiconductor substrate which has the first surface and a second surface and has a semiconductor region including an integrated circuit on a first surface side thereof, a thinning step of thinning the semiconductor substrate by removing a second surface-side portion of the semiconductor substrate bonded to the first support member such that the semiconductor region is left, a second bonding step of bonding a second support member to the second surface side of the thinned semiconductor substrate, and a chip forming step of forming chips by cutting the semiconductor region.

[0011] According to a preferred embodiment of the present invention, the chip forming step can be performed after the second bonding step.

[0012] The manufacturing method preferably further comprises, after the chip forming step, a removing step of removing the first support member from the semiconductor region which has been formed into the chips. In the chip forming step, the semiconductor region may be cut together with the second support member to form chips, or the semiconductor region may be cut together with the first and second support members to form chips.

[0013] Alternatively, the manufacturing method may further comprise, after the second bonding step and before the chip forming step, a step of removing the first support member from a bonded body which is formed by bonding the first support member, semiconductor region, and second support member. In the chip forming step, the semiconductor region can be cut together with the second support member to form chips.

[0014] According to another preferred embodiment of the present invention, the chip forming step can be performed after the thinning step and before the second bonding step. The manufacturing method preferably further comprises, after the first bonding step, a removing step of removing the first support member from the semiconductor region which has been formed into the chips.

[0015] According to still another preferred embodiment of the present invention, preferably, the semiconductor substrate has a separation layer under the semiconductor region, and in the thinning step, the semiconductor substrate bonded to the first support member is divided by using the separation layer to remove the second surface-side portion of the semiconductor substrate. The separation layer is preferably formed by anodization or ion implantation. The portion removed in the thinning step can be used again as a material to form the semiconductor substrate.

[0016] According to still another preferred embodiment of the present invention, the manufacturing method can further comprise a step of packaging the semiconductor region which has been formed into the chips.

[0017] According to still another preferred embodiment of the present invention, the first support member is preferably made of any one material selected from the group consisting of a plastic material, glass, a ceramic material, a metal, and a semiconductor.

[0018] According to still another preferred embodiment of the present invention, the second support member is preferably formed of a member having a higher thermal conductivity than that of the semiconductor substrate.

[0019] According to still another preferred embodiment of the present invention, in the second bonding step, the thinned semiconductor region and the second support member are preferably bonded through a conductive member (e.g., solder).

[0020] According to still another preferred embodiment of the present invention, the semiconductor region is preferably made of any one material selected from the group consisting of silicon, germanium, and a compound semiconductor.

[0021] According to still another preferred embodiment of the present invention, the second support member can comprise a light-transmitting member. The term light is not limited to visible light but includes infrared light and ultraviolet light.

[0022] According to still another preferred embodiment of the present invention, the thinned semiconductor region and the second support member may be bonded through a light-transmitting member.

[0023] According to the second aspect of the present invention, there is provided a semiconductor device which is formed by packaging an integrated circuit chip and a support member bonded to one surface of the integrated circuit chip, wherein the integrated circuit chip and support member have substantially the same size.

[0024] According to still another preferred embodiment of the present invention, the support member preferably comprises a member having a higher thermal conductivity than that of a substrate of the integrated circuit chip.

[0025] According to still another preferred embodiment of the present invention, the support member may comprise a light-transmitting member. The term light is not limited to visible light but includes infrared light and ultraviolet light.

[0026] According to still another preferred embodiment of the present invention, the integrated circuit chip and support member are preferably obtained by cutting both a semiconductor substrate having a plurality of integrated circuit chips and a support member bonded to the semiconductor substrate.

[0027] According to the present invention, chip formation which accompanies thinning of the semiconductor region where the integrated circuits are formed can moderate a difficulty in packaging, more specifically, facilitate dicing or die bonding.

[0028] Other features and advantages of the present invention will be apparent from the following description taken in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the figures thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0030] FIGS. 1A to 1F are views for schematically describing a semiconductor chip manufacturing method; and

[0031] FIGS. 2A to 2C are views for describing another example of a separation layer forming method.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0032] The preferred embodiments of the present invention will be described with reference to the accompanying drawings.

[0033] As the integration density and operation speed of semiconductor devices increase, heat generated by the semiconductor devices becomes very high. An increase in temperature of a semiconductor device caused by heat generation adversely affects the device characteristics considerably, and an increase in heat radiation performance is accordingly sought for. While the heat radiation performance can be increased by thinning the semiconductor device, if the semiconductor device is merely thinned, the semiconductor device or chip can be damaged during dicing, and it becomes difficult to hold the chip during die bonding.

[0034] In view of this, according to this embodiment, a semiconductor layer or semiconductor region where semiconductor devices are formed is supported by the first support member and then thinned to improve the heat radiation performance. The thinned semiconductor layer or semiconductor region is supported by a second support member, and cut or divided to form chips. By cutting or dividing the thinned semiconductor layer or semiconductor region to form chips, damages to the semiconductor layer or semiconductor region are prevented. Furthermore, the heat radiation performance can be improved by employing as the second support member a member having a high heat radiation performance. The first support member may be removed before cutting the semiconductor layer or semiconductor region, or after cutting.

[0035] The semiconductor layer or semiconductor region may be cut (divided) while it is supported by only the first support member (i.e., before it is supported by the second support member). In this case, after cutting, before the support member is removed, the second support member can be adhered to the semiconductor layer or semiconductor region which has been formed into chips by cutting.

First Embodiment

[0036] The first embodiment of the present invention will be described with reference to FIGS. 1A to 1F.

[0037] First, in the step shown in FIG. 1A, a separation layer 110 and semiconductor layer (semiconductor region) 120 are formed on a semiconductor substrate 100 serving as a seed substrate. Then, integrated circuits 130 including semiconductor devices are formed in the semiconductor layer 120.

[0038] More specifically, a porous layer 110 including two layers having different porosities is formed as a separation layer on the silicon substrate (semiconductor substrate) 100 serving as the seed substrate by an anodizing process. The porous layer 110 including the two layers having the different porosities can be formed by changing conditions (e.g., current conditions) for the anodizing process. When the porous layer 110 including the two layers having the different porosities is formed, the interface between the two layers can be used as a separation interface in a later separating step.

[0039] For example, the conditions for the anodizing process can be determined in the following manner.

[0040] Semiconductor substrate:

[0041] P⁻ substrate, resistivity=16 mΩ·cm

[0042] Anodizing process: HF:IPA=42.5:9.2 (wt. %) Current conditions (first porous layer):

[0043] 5.12 A, 150 sec

[0044] Current conditions (second porous layer):

[0045] 9.2 A, 60 sec

[0046] The resistivity and impurities of the semiconductor substrate are not particularly limited, and can be set arbitrarily as far as a porous layer serving as a separation layer can be formed. If epitaxial growth is to be employed in the subse-

quent step, to form a good epitaxial growth layer (semiconductor layer), it is preferable to employ a P-type substrate having a resistivity of 6 m Ω ·cm to 20 m Ω ·cm. It is more preferable to employ a P-type substrate having a resistivity of 14 m Ω ·cm to 17 m Ω ·cm.

[0047] The porous layer need not have a two-layer structure, but can have a single layer structure or a multilayer structure with three or more layers.

[0048] Preferably, the silicon substrate 100 on which the porous layer 110 serving as the separation layer is formed is oxidized (e.g., at 400° C. for 1 hr) in an oxygen atmosphere to cover the pore walls with a thermal oxide film. Subsequently, an aqueous solution of dilute hydrofluoric acid (HF) is preferably brought into contact with the surface of the porous layer 110 to remove the oxide film on the surface of the porous layer 110 to leave oxide films on the inner walls of the pores. This process is sufficient as far as it can remove only the oxide film on the surface of the porous layer, and can use, e.g., hydrofluoric acid (HF) vapor in place of the aqueous solution of hydrofluoric acid.

[0049] Subsequently, the pores in the surface of the porous layer 110 are preferably closed by baking the silicon substrate 100 in a hydrogen containing ambient.

[0050] Subsequently, the single-crystal silicon layer (semiconductor layer) 120 is epitaxially grown on the porous layer 110. For example, the single-crystal silicon layer 120 having a thickness of 2 μ m can be grown with the following conditions:

Source gas:	SiH ₂ Cl ₂ /H ₂
Flow rate of gas:	0.5/180 l/min
Pressure of gas:	80 Torr
Temperature:	950° C.

[0051] The epitaxial growth is not limited to vapor phase growth, but liquid phase growth can also be employed. As the semiconductor layer 120, instead of the silicon layer, another semiconductor layer such as germanium layer, or a compound semiconductor layer such as SiGe layer can be formed.

[0052] Subsequently, the integrated circuits 130 such as microprocessors, logic ICs, and memories are formed in the semiconductor layer 120 by lithography. The step of forming the integrated circuits is identical to the step of forming the integrated circuits in a bulk substrate. With the above steps, the substrate schematically shown in FIG. 1A is obtained. The semiconductor layer 120 side surface of the substrate shown in FIG. 1A will be referred to as the first surface, and a surface opposite to the first surface will be referred to as the second surface hereinafter.

[0053] In the step shown in FIG. 1B, the semiconductor substrate (FIG. 1A) in which the integrated circuits 130 are formed in the semiconductor layer 120 is bonded to a first support member 150 such that its semiconductor layer 120 side (first surface side) becomes inside. For this bonding, for example, an adhesive 140 such as epoxy adhesive can be used.

[0054] As the first support member 150, for example, a plastic material, glass, a ceramic material, a metal, a semiconductor, or the like can be employed, and can be appropriately selected in accordance with the required adhesion strength, the type of the adhesive that can be used, the strength required for the first support member, and the like. A method

with which the adhesion surface will not separate in the latter step before the separation interface in the porous layer does should be employed.

[0055] In the step shown in FIG. 1C, the silicon substrate 100 (the second surface side-portion) serving as the seed substrate is separated (removed) from the substrate shown in FIG. 1B at the separation interface (the interface in the porous layer including the two layers having the different porosities) in the porous layer 110 as the boundary (separation interface). A second support member 170 is adhered to the semiconductor layer 120 side of, of the two separate substrates, the substrate which has the semiconductor layer 120.

[0056] To separate (remove) the silicon substrate 100, a separation method employing a fluid is suitable. More specifically, a method of blowing a liquid such as water or alcohol or a gas such as air or nitrogen to the separation interface or its vicinity in the porous layer 110 is preferable.

[0057] When necessary, a porous layer 110a which is left in the semiconductor layer 120 in which the integrated circuits 130 are formed may be removed. As the method of removing the remaining porous layer 110a, a method which uses a chemical solution (e.g., aqueous hydrogen peroxide, a liquid mixture of nitric acid and hydrofluoric acid) that oxidizes silicon or a mechanical grinding method is suitable.

[0058] The method of removing the silicon substrate 100 using the porous layer 120 serving as the separation layer is excellent in that the silicon substrate 100 can be used again as the material substrate in this manufacturing method, that the silicon layer 110 can be removed within a short period of time, and that damages to the semiconductor layer 120 are small. To use the silicon substrate 100 again, it is processed at required and then subjected to the step which has been described with reference to FIG. 1A.

[0059] The second support member 170 is bonded to the semiconductor layer 120 side (second surface side) of, of the two separate substrates, the substrate which has the semiconductor layer 120. Then, a structure including the second support member 170/(remaining porous layer 110a; only when it is not removed)/semiconductor layer 120/adhesive 140/first support member 150 is obtained.

[0060] The second support member 170 is preferably a heat conductive member having a high thermal conductivity (e.g., a member having a thermal conductivity higher than that of the semiconductor substrate serving as the seed substrate). In adhesion, e.g., an adhesive 160 having a high thermal conductivity or a solder (conductive member) may be used. It is also suitable to plate the pore walls of the remaining porous layer 110a with copper or the like and adhere the porous layer 110a to a plate having a high thermal conductivity.

[0061] A heat sink such as one for an LSI may be used in place of the second support member 170. Also, a heat sink may be bonded to the second support member 170. When a conductive plate having a high thermal conductivity and a heat sink are to be used in combination, the conductive plate having the high thermal conductivity is preferably made of a material that can be bonded to both the semiconductor layer 120 or remaining porous layer 110a and the heat sink (made of e.g., Cu or Al) through an adhesive or solder (conductive member). For example, this material is preferably a metal, particularly copper or gold, which has a higher thermal conductivity than that of a semiconductor material which forms the integrated circuits.

[0062] Subsequent to the step shown in FIG. 1C, in the step shown in FIG. 1D, the semiconductor layer 120 supported by

the second support member 170 is diced (cut) to obtain integrated circuit chips 180 each of which is schematically shown in FIG. 1E. The semiconductor layer 120 may be cut together with the second support member 170, or together with both the first and second support members 150 and 170. When a plurality of members which are formed into chips (by cutting or separated) in accordance with the chip size of the semiconductor layer 120 are to be used as the second support member 170, when cutting the semiconductor layer 120, only the semiconductor layer 120 may be cut, or only the semiconductor layer 120 and first support member 150 may be cut.

[0063] The integrated circuit chip 180 includes the semiconductor layer 120 which is formed into a chip, and the second support member 170 which is formed into a chip having substantially the same size as that of the semiconductor layer 120 which is formed into the chip.

[0064] Conventionally, the semiconductor layer has a thickness that only corresponds to approximately the epitaxial growth and is very thin. For this reason, during dicing, the semiconductor layer may be damaged, and it is difficult to hold the chip during die bonding. In view of this, according to this embodiment, prior to dicing, the semiconductor layer 120 is supported by the second support member 170, e.g., a conductive plate having a high thermal conductivity. Thus, the semiconductor layer 120 has a sufficiently high strength against dicing, and the chip can be held easily during die bonding.

[0065] In the step shown in FIG. 1F, the integrated circuit chip 180 is packaged. During packaging, the thermal conductive plate having a high thermal conductivity and serving as the second support member 170 is adhered to a package base 190. Then, the integrated circuit 130 is wire-bonded to the lead frame of the package base 190.

[0066] Typically, prior to the packaging, the first support member 150 can be removed from the chip 180 or semiconductor layer 120. The first support member 150 may be removed from the chip 180 or semiconductor layer 120 before or after dicing (cutting) as far as the second support member 170 is already bonded to the semiconductor layer 120. Preferably, the first support member 150 is removed after dicing. With the method of removing the first support member 150 from the chip 180 after dicing, as the adhesion area is small, the first support member 150 can be removed from the chip 180 with a small force.

[0067] As the method of removing the first support member 150 from the chip 180 or semiconductor layer 120, a method of dipping the entire chip or substrate in an adhesive removing liquid (organic solvent) is suitable. Alternatively, a method of mechanically grinding the first support member or a method of removing the first support member by using the difference in thermal stress will do.

[0068] The integrated circuit chip 180 which is schematically shown in FIG. 1F and obtained with the above steps has a thickness of a fraction of several hundreds the thickness of an integrated circuit chip which uses a conventional bulk silicon substrate, and accordingly has a remarkably excellent heat radiation performance. As the semiconductor layer is formed into chips (divided) while it is supported by the second support member, damages to the semiconductor layer during the process such as dicing can be prevented. Furthermore, when a member having an excellent heat radiation performance is employed as the second support member, the heat radiation performance can be further improved. When

the semiconductor layer chip is supported by the second support member chip, the integrated circuit chip can be held easily during die bonding.

[0069] In the above embodiment, the second support member is bonded to the semiconductor layer 120, and after that the semiconductor layer 120 is cut. In place of this, the semiconductor layer 120 which is bonded to the first support member 150 may be cut into chips, the second support member 170 may be bonded to the semiconductor layer 120 which forms a chip, and thereafter the first support member 150 may be removed from the semiconductor layer 120 which forms the chip. With this method, the semiconductor layer 120 is cut while it is supported by the first support member 150. Therefore, the damages to be applied to the semiconductor layer 120 during cutting can be decreased. The second support member 170 is bonded to the semiconductor layer 120 before the first support member 150 is removed from the semiconductor layer 120 which forms the chip. Therefore, the semiconductor layer 120 which forms the chip can be protected from an impact or the like. Thus, for example, the semiconductor layer 120 which forms the chip can be held easily during die bonding.

[0070] When bonding the second support member 170 to the semiconductor layer 120 which forms the chips, the second support member 170 which is cut into the chip size may be bonded to the chip formed by cutting the semiconductor layer 120. Alternatively, the non-cut second support member 170 may be bonded to the semiconductor layer 120 which forms the chip, and thereafter the second support member 170 may be cut into a chip size.

[0071] When forming the semiconductor layer 120 into chips, the first support member 150 may be cut together with the semiconductor layer 120. Alternatively, only the semiconductor layer 120 may be cut without cutting the first support member 150.

Second Embodiment

[0072] According to the second embodiment, the method of forming the separation layer of the first embodiment is changed.

[0073] First, in the step shown in FIG. 2A, an insulating layer (e.g., a SiO₂ layer) serving as a protection film 210 is formed on a silicon substrate (semiconductor substrate) 100 serving as a seed substrate. In the step shown in FIG. 2B, ions such as hydrogen ions are implanted in the silicon substrate 100 to form an ion-implanted layer serving as a separation layer (ion-implanted layer) 110b in a region at a predetermined depth from the surface of the silicon substrate 100. For example, the implantation amount of the hydrogen ions can be set to the order of 10¹⁶ to 10¹⁷ (atoms/cm²).

[0074] After that, the protection film 210 is removed in the step shown in FIG. 2C. Thus, a substrate which has a semiconductor layer 120a on the separation layer 110b can be formed. The substrate obtained in this manner is subjected to the steps shown in FIGS. 1B to 1F to form integrated circuit chips having a thin semiconductor layer in the same manner as in the first embodiment.

[0075] The step of forming a protection film, which is performed prior to ion implantation, is not necessary. Alternatively, the separation film may be formed by implanting ions in the seed substrate (silicon substrate) 100 without forming a protection film on it.

Third Embodiment

[0076] This embodiment provides an optical card manufacturing method as well as a method of removing a seed substrate without using a separation layer.

[0077] First, integrated circuits including, e.g., a light-receiving element and amplification circuit, are formed on a silicon substrate serving as a seed substrate. After that, the first support member is bonded to the silicon substrate such that the integrated circuit side (first surface side) becomes inside.

[0078] Subsequently, the silicon substrate is thinned from the lower surface (second surface side) by grinding and abrasion using a grinder to leave a semiconductor layer (semiconductor region) having a predetermined thickness (e.g., 50 μm) as a region that includes integrated circuits.

[0079] Subsequently, a light-transmitting substrate (quartz substrate) serving as the second support member is bonded to the integrated circuit side (second surface side) of the obtained substrate. In this case, annealing (e.g., at 400° for 1 hr) is preferably performed to increase the bonding strength.

[0080] The light-transmitting substrate is not limited to the quartz substrate. The material of the light-transmitting substrate is not particularly limited as far as it transmits light, and can be, e.g., glass. As the light-transmitting substrate, for example, a substrate which has a higher light transmittance than that of the semiconductor substrate serving as the seed substrate can be employed.

[0081] Subsequently, the substrate is diced and wires are connected to it. After that, each diced substrate portion is packaged using a plastic material to obtain a transparent optical card (a card having a light-transmitting portion).

[0082] In the first embodiment as well, a card or package which employs a light-transmitting member as the second support member and has a light-transmitting portion can be manufactured.

[0083] As many apparently widely different embodiments of the present invention can be made without departing from the spirit and scope thereof, it is to be understood that the invention is not limited to the specific embodiments thereof except as defined in the appended claims.

CLAIM OF PRIORITY

[0084] This application claims priority from Japanese Patent Application No. 2004-183961 filed on Jun. 22, 2004, the entire contents of which are hereby incorporated by reference herein.

1-19. (canceled)

20. A semiconductor device which is formed by packaging an integrated circuit chip and a support member bonded to one surface of said integrated circuit chip, wherein said integrated circuit chip and support member have substantially the same size.

21. The device according to claim **20**, wherein said support member comprises a member having a higher thermal conductivity than that of a substrate of said integrated circuit chip.

22. The device according to claim **20**, wherein said support member comprises a light transmitting member.

23. The device according to claim **20**, wherein said integrated circuit chip and support member are obtained by cutting both a semiconductor substrate having a plurality of integrated circuit chips and a support member bonded to said semiconductor substrate.

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