A system for synthesizing a plurality of mutually coherent electrical signals with means for selecting the frequency of each signal.

44 Claims, 8 Drawing Figures
Fig. 3.

1 MHz

2 MHz

3 MHz

4 MHz

5 MHz

6 MHz

7 MHz

8 MHz

9 MHz

E1

\(E_1\)

\(E_2\)

\(E_3\)

\(E_4\)

\(E_5\)

\(E_6\)

\(E_7\)

\(E_8\)

\(E_9\)
FREQUENCY SELECTOR AND SYNTHESIZER

BACKGROUND OF THE INVENTION

In certain applications it is desirable to generate coherent sinusoidal waveforms of frequencies that can be easily selected from a wide range of frequencies so that the frequency difference between any two of the selected frequencies always remains constant. For example, by using coherent synthesized frequencies for animation signals as described in Lee Harrison III patent application, Ser. No. 882,125, filed Dec. 4, 1969, the generated image can be made to rotate at a constant rate, and that rate can be set within a wide range of rates by appropriately selecting the frequencies of the animation signals. This invention provides a system for generating such signals.

SUMMARY OF THE INVENTION

The system of this invention includes a master oscillator which is preferably a crystal type oscillator, for generating a master frequency from which the synthesized frequencies are generated. The frequency of the master oscillator depends on the highest synthesized frequency desired. As an example, the preferred embodiment hereinafter described uses a 10 MHz master oscillator. The master frequency is fed into a master synthesizer which generates nine separate frequencies. Where the master frequency is 10 MHz the master synthesizer generates frequencies in 1 MHz increments from 1 to 9 MHz. The master synthesizer includes a decade counter which generates signals corresponding to the 1's bit, 2's bit, 4's bit, and 8's bit of the Binary Coded Decimal (BCD) encoded count. These signals are then combined in a logic circuit to generate the nine synthesized frequencies.

The synthesized frequencies are fed into a digital frequency selector which includes a plurality of logic switches each having switch positions zero through 9. All of the synthesized frequencies from 1 to 9 MHz are fed as inputs into the logic switches; hence, each of the logic switches may be set to gate any one of the nine frequencies to its output. With the exception of the first logic switch, the output signal of each of the logic switches is fed into a division network which divides the output signal by some factor of 10; the output of the second logic switch being divided by 10; the output of the third logic switch being divided by 100; and so on, to the output of the last logic switch which is divided by 10 to the n-1 where n is the total number of logic switches. The outputs of the first logic switch and the division networks are added together to give the resultant synthesized frequency which corresponds to the frequency selected on the logic switches. For example, if the master frequency is 10 MHz, and seven logic switches are used, any frequency from 1 Hz to 9,999,999 MHz can be selected. The resultant synthesized frequency can be used as the input to an up-down counter to generate a triangular wave which can then be fed into a digital-to-analog converter to generate a synthesized sine wave.

The adder circuitry represents a novel feature of this invention in providing a means for adding the various frequency components together to generate the synthesized frequency. The adder circuit makes use of complement and enable signals which are generated by the master synthesizer simultaneously with the generalization of the other master synthesizer signals. The complement signals provide the pulses to be added, and the enable signals tell the system when the pulses should be added.

Any number of digital frequency selectors can be used in conjunction with the master synthesizer to generate a plurality of mutually coherent synthesized frequencies, each frequency different from another of the frequencies by a constant. Hence, this invention provides a novel system for generating a plurality of mutually coherent signals selected from a wide range of frequencies.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a general block diagram of the system of this invention;
FIGS. 2 and 2A are logic diagrams of the master synthesizer of this invention;
FIG. 3 is a drawing of the waveform generated by the network of FIGS. 2 and 2A;
FIG. 4 is a block diagram of the digital frequency selector of this invention;
FIG. 5 is a schematic diagram of the frequency adder of this invention;
FIG. 6 shows waveforms used in explaining the operation of the network of FIG. 5; and
FIG. 7 is a schematic diagram of the network for producing stair step and sinusoidal waveforms from the synthesized digital signals from the digital frequency selector of this invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 1 of the drawing there is shown a general block diagram of the system of this invention. A crystal oscillator 10 generates a fixed frequency which will be referred to as the master frequency. While the master oscillator frequency depends on the maximum synthesized frequency desired from the system, this embodiment will be described using a 10 MHz master frequency. Other frequencies could be used depending on the requirements of the system. The signal from the master oscillator is fed into a master synthesizer 12. The master synthesizer 12, which will be hereinafter described in detail, produces frequencies at its output at 1 MHz intervals from 1 to 9 MHz. The synthesized output frequencies are fed into frequency selectors 14, 16 and 18. While only three frequency selectors are shown, any number can be connected in parallel, the number of selectors depending on the number of coherent synthesized frequencies required. As the frequency selectors are identical, only the frequency selector 16 will be further described.

The synthesized frequencies from the master synthesizer 12 are fed into a digital frequency selector 20, the output of which is a series of digital pulses of the frequency selected. The digital output from the digital frequency selector 20 is fed into an up-down counter 22 which generates a set of binary weighted outputs that are fed into a digital-to-analog converter 24. The output of the digital-to-analog converter 24 is fed into an operational amplifier 25 (See FIG. 7) the output of which is a staircase waveform which approximates a triangular wave. This waveform is fed into a sine-shaping network 26 to generate a sinusoidal waveform having a
frequency coherent with the output frequencies of the other frequency selectors.

MASTER SYNTHESIZER

The logic diagram of the master synthesizer 12 is shown in FIG. 2. The 10 MHz signal from the master oscillator 10 is fed through a conductor 30 to an inverter 32. The output from the inverter 32 is fed through a conductor 34 and a conductor 36 to the input of an inverter 38. The output from the inverter 38 is fed through a conductor 40 and a conductor 42 to the input of a binary coded decimal (BCD) counter, having outputs Q₁, Q₂, Q₃, and Q₄. The waveforms of these outputs are shown in FIG. 3. The master frequency waveform is shown by the waveform 50, the Q₁ waveform is shown by the waveform 52, the Q₂ waveform is shown by the waveform 54, the Q₃ waveform is shown by the waveform 56, and the Q₄ waveform is shown by the waveform 58. The Q₁ through Q₄ waveforms represent the 1’s bit, 2’s bit, 4’s bit, and 8’s bit, respectively. The Q₂ output is not used in this system. As will be seen, it is from the waveforms 50–58 that the frequencies of 1 through 9 MHz are synthesized.

The re-inverted output on the conductor 40 is also fed through a conductor 60 and a conductor 62 to the input of an inverter 64. The output of the inverter 64 represents the inverse of the 10 MHz master frequency which is fed through a conductor 66. The signal on the conductor 60 is also fed through a conductor 68 and a conductor 70 to the input a of a NAND gate 72. The signal on the conductor 68 is also fed through a conductor 74 and a conductor 76 to the input a of a NAND gate 78. The signal on the conductor 74 is also fed through a conductor 80 and a conductor 82 to the input a of a NAND gate 84. The signal on the conductor 80 is also fed through a conductor 86 to the input a of a NAND gate 88.

The signal at the output Q₁ of the BCD counter 44, represented by the waveform 52, is fed through a conductor 90, a conductor 92, and a conductor 94 to the input a of a NAND gate 96. The signal on the conductor 92 is also fed through a conductor 98, and a conductor 100 to the input a of a NAND gate 102. The signal on the conductor 98 is also fed through a conductor 104 and a conductor 106 to the input a of a NAND gate 108. The signal on the conductor 104 is also fed through a conductor 110 to the input b of a NAND gate 112.

The Q₁ output from the BCD counter 44, represented by the waveform 58, is fed through a conductor 120, a conductor 122, and a conductor 124 to the input a of the NAND gate 112. The NAND gate 112 NANDs the waveforms Q₁ and Q₂ with the resultant output being fed through a conductor 126 and a conductor 128 to the input of an inverter 130. The output of the inverter 130 is fed through a conductor 132 to the input b of the NAND gate 72 which NANDs the signal on the conductor 132 with the master oscillator waveform 50. The output of the NAND gate 72 which is an inverted 1 MHz signal shown by the waveform 136 of FIG. 3, is fed through a conductor 137.

The Q₂ signal from the BCD counter 44, represented by the waveform 54 of FIG. 3, is fed through a conductor 140, a conductor 142 and a conductor 144 to the input b of the NAND gate 108. The output of the NAND gate 108 is fed through a conductor 146 and a conductor 148 to the input of an inverter 150. The output from the inverter 150 is fed through a conductor 152 to the input b of the NAND gate 78 which NANDs the signal on the conductor 152 with the master oscillator signal. The output from the NAND gate 78 which is an inverted 2 MHz signal shown by the waveform 154 of FIG. 3, is fed through a conductor 156.

The Q₃ signal on the conductor 140 is also fed through a conductor 158 to the input of an inverter 160. The output from the inverter 160 represents the inverse of the Q₃ signal or Q₃. The Q₄ signal from the inverter 160 is fed through a conductor 162 and a conductor 164 to the input b of the NAND gate 102. The NAND gate 102 NANDs the Q₃ and Q₄ signals. The output of the NAND gate 102 is fed through a conductor 166 and a conductor 168 to the input of an inverter 170. The output from the inverter 170 is fed through a conductor 172 to the input b of the NAND gate 84 which NANDs the signal on the conductor 172 with the master oscillator signal to produce at its output an inverted 3 MHz signal as shown by the waveform 180 of FIG. 3. This inverted 3 MHz signal is fed through a conductor 182.

The Q₄ signal on the conductor 120 is also fed through a conductor 186 to the input of an inverter 188. The output of the inverter 188 represents the inverse of the Q₄ waveform or Q₄ and is fed through a conductor 190 and a conductor 192 to the input b of the NAND gate 96 which NANDs the Q₃ and Q₄ signals. The output from the NAND gate 96 is fed through a conductor 194 and a conductor 196 to the input of an inverter 198. The output of the inverter 198 is fed through a conductor 200 to the input b of the NAND gate 88 which NANDs the signal on the conductor 200 with the master oscillator signal to produce at its output an inverted 4 MHz signal as shown by the waveform 202 of FIG. 3. This signal is fed through a conductor 204.

The signal on the conductor 34 from the inverter 32, which is an inverted master oscillator signal, is also fed through a conductor 210 and a conductor 212 to the input of an inverter 214, the output of which is fed through a conductor 216 and a conductor 218 to the input a of a NAND gate 220. The signal on the conductor 216 is also fed through a conductor 222 and a conductor 224 to the input a of a NAND gate 226. The signal on the conductor 222 is also fed through a conductor 228 to the input a of the NAND gate 230. The signal on the conductor 216 is also fed through a conductor 232 and a conductor 234 to the input a of a NAND gate 236. The signal on the conductor 232 is also fed through a conductor 238 and a conductor 240 to the input a of a NAND gate 242. The signal on the conductor 238 is also fed through a conductor 244 to the input a of a NAND gate 246. The Q₄ signal from the BCD counter 44 on the conductor 90 is also fed through a conductor 250 to the input b of the NAND gate 230 which NANDs the Q₁ signal and the master oscillator signal to produce an inverted 5 MHz signal at its output as shown by the waveform 252 of FIG. 3.

The waveform 252 is fed through a conductor 254. The signal from the NAND gate 96 on the conductor
194 is also fed through a conductor 256 to the input b of the NAND gate 226 to produce at its output an inverted 6 MHz signal as shown by the waveform 258 of Fig. 3. This signal is fed through a conductor 260. The signal from the NAND gate 102 on the conductor 166 is also fed through a conductor 262 to the input b of the NAND gate 220 to produce at its output an inverted 7 MHz signal as shown by the waveform 264 in Fig. 3. This signal is fed through a conductor 266. The signal from the output of the NAND gate 108 on the conductor 146 is also fed through a conductor 268 to the input b of the NAND gate 236 to produce an inverted 8 MHz signal at its output as shown by the waveform 270 of Fig. 3. This signal is fed through a conductor 272. The output signal from the NAND gate 112 on the conductor 126 is also fed through a conductor 274 to the input b of the NAND gate 242 to produce at its output an inverted 9 MHz signal as shown by the waveform 276 of Fig. 3. This signal is fed through a conductor 278.

It can be seen that the frequencies of 1 through 9 MHz have been synthesized from a single master oscillator signal of 10 MHz by the circuit of Fig. 2.

For reasons which will be hereinafter described, 1 through 9 MHz waveforms are generated with their pulses advanced in time by one master oscillator pulse. These waveforms are also shown in Fig. 3 and are used as Enable signals. Hence, the waveform 300 is an inverted 1 MHz signal corresponding to the waveform 136 advanced one master oscillator pulse; the waveform 301 is an inverted 2 MHz signal corresponding to the waveform 154 advanced one master oscillator pulse; the waveform 302 is an inverted 3 MHz signal corresponding to the waveform 180 advanced one master oscillator pulse; the waveform 303 is an inverted 4 MHz signal corresponding to the waveform 202 advanced one master oscillator pulse; the waveform 304 is an inverted 5 MHz signal corresponding to the waveform 252 advanced one master oscillator pulse; the waveform 305 is an inverted 6 MHz signal corresponding to the waveform 258 advanced one master oscillator pulse; the waveform 306 is an inverted 7 MHz signal corresponding to the waveform 264 advanced one master oscillator pulse; the waveform 307 is an inverted 8 MHz signal corresponding to the waveform 270 advanced one master oscillator pulse; and the waveform 308 is an inverted 9 MHz signal corresponding to the waveform 276 advanced one master oscillator pulse. The waveforms 300-308 are labeled E₁ through E₈, respectively, and are used as enable signals for telling the system when a pulse should be added. This will be explained in more detail in describing the frequency adders of this system.

The E₁ through E₈ waveforms are generated by inverting the Q₁ waveform which advances the 1 through 9 MHz waveforms by one master oscillator pulse. Hence, the Q₁ waveform on the conductor 90 at the Q₁ output of the BCD counter 44 is also fed through a conductor 322 and a conductor 320 to the input a of a NAND gate 336. The signal on the conductor 326 is also fed through a conductor 332 and a conductor 334 to the input a of the NAND gate 336. The signal on the conductor 322 is also fed through a conductor 338 and a conductor 340 to the input a of a NAND gate 342. The signal on the conductor 338 is also fed through a conductor 344 to the input a of a NAND gate 346.

The inverted master oscillator signal at the output of the inverter 32 which is fed through the conductors 34 and 210 is also fed through a conductor 362 to the input of an inverter 364. The output of the inverter 364 is fed through a conductor 366 and a conductor 368 to the input a of a NAND gate 369. The signal on the conductor 366 is also fed through a conductor 370 and a conductor 372 to a NAND gate 374. The signal on the conductor 370 is also fed through a conductor 376 and a conductor 378 to the input a of the NAND gate 380. The signal on the conductor 376 is also fed through a conductor 382 and a conductor 384 to the input a of a NAND gate 386. The signal on the conductor 382 is also fed through a conductor 388 and a conductor 390 to the input a of a NAND gate 392. The signal on the conductor 388 is also fed through a conductor 394 and a conductor 396 to the input a of a NAND gate 398. The signal on the conductor 394 is also fed through a conductor 400 and a conductor 402 to the input a of a NAND gate 404. The signal on the conductor 400 is also fed through a conductor 406 and a conductor 408 to the input a of a NAND gate 410.

The Q₁ output from the BCD counter 44 on the conductor 122 is also fed through a conductor 411 to the input b of the NAND gate 330 which NANDs the Q signal with the Q₁ signal. The output of the NAND gate 330 is fed through a conductor 412 and a conductor 413 to the input of an inverter 414. The output from the inverter 414 is fed through a conductor 415 to the input b of the NAND gate 369. The NAND gate 369 NANDs the signal on the conductor 415 with the master oscillator signal of the conductor 368 to produce at its output conductor 420 the inverted 1 MHz signal, E₁, shown by the waveform 300 of Fig. 3.

The Q₂ output from the BCD counter 44 on the conductor 142 is also fed through a conductor 422 to the input b of the NAND gate 336 which NANDs the Q₂ signal with the Q₁ signal. The output from the NAND gate 336 is fed through a conductor 424 and a conductor 426 to the input of an inverter 428. The output from the inverter 428 is fed through a conductor 430 to the input b of the NAND gate 374 which NANDs the signal on the conductor 430 with the master oscillator signal to produce at its output an inverted 2 MHz signal, E₂, represented by the waveform 301.

The Q₃ signal at the output of the inverter 160 which is fed through the conductor 162 is also fed through a conductor 434 to the input b of the NAND gate 342 which NANDs the Q₁ signal with the Q₃ signal. The output of the NAND gate 342 is fed through a conductor 436 and a conductor 438 to the input of an inverter 440. The output of the inverter 440 is fed through a conductor 442 to the input b of the NAND gate 380 which NANDs the Q₁ signal on the conductor 442 with the master oscillator signal to produce at its output conductor 444 the inverted 3 MHz signal, E₃, represented by the waveform 302.

The Q₄ signal from the inverter 188 which is fed through the conductor 190 is also fed through a conductor 446 to the input b of the NAND gate 346 which
NANDs the Q signal with the Q̄ signal. The output from the NAND gate 346 is fed through a conductor 448 and a conductor 450 to the input of an inverter 452. The output from the inverter 452 is fed through a conductor 454 to the input b of the NAND gate 386 which NANDs the signal on the conductor 454 with the master oscillator signal to produce at its output conductor 456 the inverted 4 MHz signal, E₄, represented by the waveform 303.

The Q̄ signal on the conductor 320 is also fed through a conductor 460 to the input of an inverter 462. The output of the inverter 462 is fed through a conductor 464 to the input b of the NAND gate 246 which NANDs the Q̄ signal with the master oscillator signal to produce at its output conductor 466 the inverted 5 MHz signal, E₅, represented by the waveform 304.

The output from the NAND gate 346 which is fed through the conductor 448 is also fed through a conductor 470 to the input b of the NAND gate 392 which NANDs the signal on the conductor 470 with the master oscillator signal to produce at its output conductor 472 the inverted 6 MHz signal, E₆, represented by the waveform 305. The output of the NAND gate 342 which is fed through the conductor 436 is also fed through a conductor 474 to the input b of the NAND gate 398 to produce at its output conductor 476 the inverted 7 MHz signal, E₇, represented by the waveform 306. The output of the NAND gate 336 which is fed through the conductor 424 is also fed through a conductor 478 to the input b of the NAND gate 404 which NANDs the signal on the conductor 478 with the master oscillator signal to produce at its output conductor 480 the inverted 8 MHz signal, E₈, represented by the waveform 307. The output from the NAND gate 330 which is fed through the conductor 412 is also fed through a conductor 482 to the input b of the NAND gate 410 which NANDs the signal on the conductor 482 with the master oscillator signal to produce at its output conductor 484 the inverted 9 MHz signal, E₉, represented by the waveform 308.

**DIGITAL FREQUENCY SELECTOR**

In FIG. 4 there is shown the block diagram of the digital frequency selector of this invention. The circuit of FIG. 4 makes possible the selection of any of a wide range of frequencies. In this embodiment seven logic switches — 501, 502, 503, 504, 505, 506 and 507 — are used. As the logic switches 501-507 are identical, only switches 501, 502, 503, and 507 are shown in the drawing.

The waveforms 136, 154, 180, 202, 252, 258, 264, 270 and 276 from the NAND gates 72, 78, 84, 88, 90, 226, 220, 236 and 242, respectively, are fed by the conductors 137, 156, 182, 204, 254, 260, 266, 272 and 278 into each of the logic switches 501-507. Each of the switches 501-507 has suitable selection means for gating any one of its inputs through to its output conductor. Hence, the switch 501 has an output conductor 510, to which any one of its inputs can be selectively gated; the switch 502 has an output conductor 512 to which any one of its inputs can be selectively gated, the switch 503 has an output conductor 513 to which any one of its inputs can be selectively gated; and so on, to the switch 507 which has an output conductor 522 to which any one of its inputs can be selectively gated.

The selected signal F₄ at the output of the switch 501 is fed through the conductor 510 to the input a of a frequency adder 530. The selected signal at the output of the switch 502 is fed through the conductor 512 to the input a a divide by 10⁴ network 532. The network 532 divides the selected frequency on the conductor 512 by a factor of 10. The frequency F₅ at the output of the division network 532 is fed through a conductor 534 to the input b of the frequency adder 530. The frequency adder 530 which will be hereinafter described in detail, is a circuit which generates at its output the sum of the frequencies at its inputs a and b. The output of the frequency adder 530 is fed through a conductor 536 to the input a of a frequency adder 540. The selected signal at the output of the switch 503 is fed through the conductor 513 to the input of a divide by 10⁶ network 538. The network 538 divides the selected frequency on the conductor 513 by a factor of 100. The frequency F₆ at the output of the division network 538 is fed through a conductor 539 to the input b of a frequency adder 540. The output of the frequency adder 540, which is the sum of the frequencies F₅ and F₆, is fed into the input a of the next frequency adder (not shown), and so on. Progressively, for the switches 501 through 507, the division network increases by factors of 10 to 10⁶ for the switch 507. The frequencies, therefore, are continuously added by the series of frequency adders until finally, the selected output of the switch 507 is fed through the conductor 522 to the input of a division network 541 which divides the selected frequency at the output of the switch 507 by 10⁹.

The output frequency F₇ from the division network 541 is fed through a conductor 542 to the input b of a frequency adder 544. The output from the preceding network adder is fed into the input a of the frequency adder 544. The output of the frequency adder 544 is the sum of all of the frequencies selected on the switches 501-507 and is fed through a conductor 546 to the up-down counter 22.

The frequency adder 530 has two additional inputs which are necessary to perform the required additions. Referring again to FIG. 4, it should be noted that a pulse may be added to any one of the waveforms only where there is a space available. For example, referring to the waveform 136 pulses may be added anywhere on this waveform except at the end where there is already a pulse. In other words, nine pulses may be added to the waveform 136; eight pulses to the waveform 154; seven pulses to the waveform 180; six pulses to the waveform 202; five pulses to the waveform 252; four pulses to the waveform 258; three pulses to the waveform 264; two pulses to the waveform 270; and one pulse to the waveform 276. In this regard it should also be noted that except for the 5 MHz waveform 252 each of the other waveforms has a complement waveform. Complement waveforms are those where one has a pulse where the other has a space; therefore, the waveforms 136 and 276, 154 and 270, 180 and 264, and 202 and 258 are complement waveforms. Although the 5 MHz waveform 252 has no complement among the nine waveforms it is noted that the E₉ waveform 304 is the complement of the waveform 252 since its pulses are advanced by one master oscillator pulse. Therefore, the E₉ waveform 304 can be used as the complement of the waveform.
252. Because of these complementary relationships the complement waveform is used to supply the pulses to be added.

Referring again to FIG. 4, the switch 501, which gates the selected millionths digit frequency F7, also automatically gates the F1, complementary waveform to an output conductor 550. Therefore, whatever frequency is selected on the switch 501, that frequency is gated to the output conductor 510, and the complementary frequency is gated to the output conductor 550. The complementary waveform on the conductor 550 is fed into an inverter 552. The output from the inverter 552, is fed through a conductor 554, to an input 556 of the frequency adder 530, from the frequency adder 530 by a conductor 557 to an input 558 of the frequency adder 540, and so on to a conductor 559 which feeds the signal to an input 560 of the last frequency adder 544. It is the complementary waveform pulses which are actually added to the selected frequency F1, by the frequency adders. The complementary waveforms are referred to as F4 signals.

The system must also know when vacancies in the frequency waveform will occur. By using the waveforms 300–308, the system can detect when the next Fs pulse will occur and, hence, when the next vacancy in the F1 waveform, will occur, which is one master oscillator pulse later. When the millionths digit frequency F1 is selected by the switch 501, the appropriate E waveform is automatically gated through the switch 501 and an output conductor 561 to the input of an inverter 562. The output from the inverter 562 is fed through a conductor 564 to an input 566 of the frequency adder 530 from the frequency adder 530 by a conductor 567 to an input 568 of the frequency adder 540, and so on to a conductor 569 which feeds the signal to an input 570 of the last frequency adder 544. The signal at the output of the inverter 562 is referred to as the F1 signal.

Therefore, the switch 501 selects the millionths digit frequency, and the switches 502 and so on to 507 select the 100,000ths, 10,000ths, 1,000ths, 100ths, 1ths, and units digit frequencies to be added. Automatically with the setting of the switch 501 to a selected Fs frequency, there is gated the appropriate F1 and F2 signals. In other words, the switches 502–507 tell the system how many pulses to add, the F3 signal provides the pulses to be added, and the F1 signal tells the system when to add the pulses.

**FREQUENCY ADDER**

In FIG. 5 there is shown a detailed drawing of the frequency adders 530, 540, and so on, to 544 of this invention. In this embodiment six such frequency adders are used, although it is to be understood that the number used depends on the frequency range desired. Referring to the frequency adder 530, the selected millionths digit output frequency F1 on the conductor 510 is fed to the input a of a NOR gate 650. The selected hundredth digit frequency F2 on the switch 502, which is to be added to the millionths digit frequency F1, is fed through the conductor 534 to the input of a differentiator circuit 652. The output from the differentiator circuit 652 is fed through a conductor 654 to the T input of a flip-flop 656. The flip-flop 656 has Q and Q outputs and a clear input c. When the flip-flop 656 is triggered by a signal at its input T the output of the flip-flop changes state with a zero level at its Q output and a 1 level at its Q output. The Q output of the flip-flop 656 is connected by a conductor 658 to the K input of a flip-flop 660. The 1 level Q output signal from the flip-flop 656 is fed through a conductor 662 to the J input of the flip-flop 660.

The F3 signal on the conductor 564 is fed through a conductor 670 to the T input of the flip-flop 660. Since the J input of the flip-flop 660 has been placed at a 1 level by the flip-flop 656, the flip-flop 660 will change state when the F2 signal appears on the T input, producing a zero level at its Q output and a 1 level at its Q output. The F4 signal on the conductor 564 is also fed through a conductor 672 to the input b of a NAND gate 674. The 1 level Q output from the flip-flop 660 is fed through a conductor 676 to the input b of a NAND gate 678. The Q output of the flip-flop 660 is connected by the conductor 680 and a conductor 682 to the input b of a NAND gate 684, and by a conductor 686 to the input a of the NAND gate 674.

The F5 signal on the conductor 554 is fed through a conductor 690 to the input a of the NAND gate 678. The F6 signal on the conductor 554 is also fed through a conductor 692 to the input a of the NAND gate 684. With the input b of the NAND gate 678 at 1 level, the output of the NAND gate 678 will go to a zero level when its input a receives the next positive pulse of the F5 signal. The negative output signal from the NAND gate 678, which is one master oscillator pulse in width, is fed through a conductor 700 and a conductor 702 to the input b of the NOR gate 650. Because the F6 is the complement of the F5 waveform, the negative pulse at the input b of the NOR gate 650 occurs at precisely the same time a blank space occurs on the F5 waveform at the input a of the NOR gate 650. The output of the NOR gate 650 is a waveform equal to the sum of the pulses at its input a and the pulses at its input b. The output from the NOR gate 650 is fed through a conductor 710 to the input of an inverter 712. The negative pulse at the output of the NAND gate 678 which is fed through the conductor 700 is also fed through the conductor 714 to the input of an inverter 716. The output of the inverter 716 is fed through a conductor 718 to the input of a differentiator circuit 720, the output of which is fed through a conductor 722 and a conductor 724 to the clear input C of the flip-flop 660. The signal on the conductor 722 is also fed through a conductor 726 to the clear input C of the flip-flop 656. The output signal from the differentiator circuit 720 clears the flip-flops 656 and 660 with the Q and Q outputs of the flip-flops 656 resetting to a zero level and a 1 level, respectively. With the Q output of the flip-flop 656 at a 1 level, the 1 level signal is fed through the conductor 658 to the K input of the flip-flop 660. With the flip-flop 660 cleared and a 1 level at its input K, its Q output will go to a 1 level and its Q output to a zero level. The 1 level signal from the Q output is fed through the conductors 680 and 682 to the input b of the NAND gate 684.

Assuming that a pulse on the F4 signal occurs before the next F6 pulse on the conductor 534, the F4 pulse is fed through the conductor 554 and 692 to the input a of the NAND gate 684. With both inputs a and b of the NAND gate 684 at 1 levels, a zero level signal will be
generated at the output for the duration of the Fp pulse. This pulse is fed through a conductor 730 to the input of an inverter 732. The 1 level signal at the Q output of the flip-flop 660 which is fed through the conductor 680 also is fed through the conductor 686 to the input a of the NAND gate 674.

Assuming that a pulse on the Fp waveform occurs prior to the next pulse on the Fq waveform on the conductor 534, the positive Fq pulse is fed through the conductors 654 and 672 to the input b of the NAND gate 674. With both inputs a and b at 1 level a zero level signal of a width equal to the width of the Fp pulse is fed through a conductor 734 to the input of an inverter 736. The outputs from the inverters 712, 732 and 736 are passed on to the next frequency adder 540 where the 10,000th digit frequency Fq set by the switch 503 is added. Hence, the added signal from the inverter 712 is fed through the conductor 536 to the input a of a NOR gate like the NOR gate 650; the output from the inverter 732 is fed through a conductor 750 to the a inputs of a NAND gate like the NAND gates 678 and 684; and the output from the inverter 736 is fed through a conductor 756 to the T input of a flip-flop like the flip-flop 660; and the input b of a NAND gate like the NAND gate 674.

The frequency adder network 540, and in fact, all of the frequency adders except the frequency adder 544, are identical to the frequency adder network 530. The frequencies added by the frequency adder 540 will be the output frequency Fp + Fq from the frequency adder 530 and the 10,000th digit frequency Fq set by the switch 503 which is fed through the conductor 539 to the frequency adder 540.

As an analysis of the frequency adder network will show, the NAND gates 684 and 674 operate to insure higher frequencies take precedence over the lower frequencies. In other words, the 100,000th digit frequency Fq takes precedence over the 10,000th digit frequency Fq and so on. Whenever a Fq waveform pulse occurs output conductor 534 will trigger the flip-flop 656. The next occurring Fq waveform will trigger the flip-flop 660, disabling the NAND gates 684 and 674 so that the Fq and Fp pulses cannot feed through to the frequency adder network 540. In this way the pulses of the Fq waveform of the frequency adder 530 will be added to the Fq waveform before the Fp, Fq, and so on, pulses are added. Without Fp and Fq pulses, the frequency adder network 540 will not operate, nor will the other frequency adders in the system.

The last frequency adder network 544 adds in the units frequency Fq selected by the switch 507. The frequency adder 544 is identical to the frequency adder 530 except that the NAND gates 684 and 674 and the inverters 732 and 736 and associated conductors are eliminated, there being no need for them in the last frequency adder. Hence, the Fq frequency is fed through the conductor 542 to the input b of the frequency adder 544; the Fq output from the previous frequency adder is fed through the conductor 569 to the input 570 of the frequency adder 544; the Fq signal from the previous adder circuit is fed through the conductor 559 to the input 560 of the frequency adder 544; and the frequency output signal from the previous adder representing the sum of the frequencies Fq through Fp is fed through a conductor 780 to the input of the frequency adder 544. The signal at the output conductor 546 of the frequency adder 544 is the sum of all of the frequencies Fq through Fp and is a coherent, synthesized signal of a frequency selected on the switches 501 through 507. With this embodiment of the invention, any frequency between 1 Hz and 9,999,999 MHz can be selected.

Because there are more spaces than pulses to be added, the resultant synthesized waveform will contain one or more spaces causing the waveform to be non-symmetrical. The lower the frequency the greater the number of spaces. This non-symmetry is called phase jitter. The phase jitter can be greatly reduced by dividing the resultant frequency by a factor of 10 or a factor of 100. While this divides the frequency by 100, it also divides the phase jitter by 100, which gives a much smoother waveform. If, for example, the resultant frequency is divided by 100 then the maximum frequency obtainable by this embodiment is 99,999.99 Hz.

UP-DOWN COUNTER AND DIGITAL TO ANALOG CONVERTER

Referring to FIG. 7 there is shown the network for producing a staircase waveform output from the synthesized digital signal from the digital frequency selector 20. The synthesized digital frequency on the conductor 546 is fed through a conductor 850 to the input a of a NAND gate 852. The signal on the conductor 546 is also fed through a conductor 854 to the input a of a NAND gate 856. When the NAND gate 852 is enabled the digital signal on the conductor 850 is fed through the NAND gate 852 and a conductor 858 to the U input of the Up-down counter 22, causing the counter 22 to count up. When the NAND gate 856 is enabled the digital signal on the conductor 854 is fed through the NAND gate 856 and a conductor 862 to the D input of the up-down counter 22, causing the counter 22 to count down.

In this embodiment of the invention the up-down counter 22 has outputs corresponding to the 1's, 2's, 4's, 8's, 16's, 32's, 64's, 128's and 256's bits. The number of outputs required depends on the desired relationship between the frequency of the digital input and the triangular output. With the circuit of FIG. 7, the up-down counter 22 counts continuously up and down between counts of 6 and 506 so that for each 1,000 pulses fed to its input the up-down counter will count one full cycle, the staircase wave output having a frequency of one one-thousandth of that of the digital input. Other staircase wave frequencies could be produced by simply changing the number of input pulses necessary for the up-down counter to complete one cycle. For example, if the up-down counter 22 had six binary weighted outputs corresponding to the 1's, 2's, 4's, 8's, 16's, and 32's bits, the counter could be made to count continuously up and down between counts of 7 and 57 so that for each 100 pulses fed to its input the counter would count one full cycle, the staircase output having a frequency of one one-hundredth of that of the digital input.

In this embodiment the up-down counter 22 has nine bits to produce necessary binary weighted output. As shown in FIG. 7, the 1's bit is connected by a conductor 864, an inverter 866, a conductor 868, a conductor...
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870, and a conductor 872 to the input a of a NAND gate 874, and by a conductor 876 to the input a of a NAND gate 878, and by a conductor 880 to the 1's bit input of the digital to analog converter 24. The 2's bit output of the up-down counter 22 is connected by a conductor 884 and a conductor 886 to the input b of the NAND gate 874, and a conductor 888 and a conductor 890 to the input b of the NAND gate 878, and a conductor 892, an inverter 894 and a conductor 896 to the 2's bit input of the digital to analog converter 24. The 4's bit output of the up-down counter 22 is connected by a conductor 898 and a conductor 900 to the input c of the NAND gate 878, and a conductor 902, an inverter 904, a conductor 906, and a conductor 908 to the input c of the NAND gate 874, and a conductor 910 to the 4's bit input of the digital to analog converter 24. The 8's bit output of the up-down counter 22 is connected by a conductor 912 and a conductor 914 to the input d of the NAND gate 874, and by a conductor 916, an inverter 918, a conductor 920 and a conductor 922 to the input d of the NAND gate 878, and by a conductor 924 to the 8's bit input of the digital to analog converter 24. The 16's bit output of the up-down counter 22 is connected by a conductor 926 and a conductor 928 to the input e of the NAND gate 874, and by a conductor 930, an inverter 932, a conductor 934, and a conductor 936 to the input e of the NAND gate 878, and by a conductor 938 to the 16's bit input of the digital to analog converter 24. The 32's bit output of the up-down counter 22 is connected by a conductor 940 and a conductor 942 to the input f of the NAND gate 874, and by a conductor 944, an inverter 946, a conductor 948, and a conductor 950 to the input f of a NAND gate 878 and by a conductor 952 to the 32's bit input of the digital to analog converter 24. The 64's bit output of the up-down counter 22 is connected by a conductor 954, and a conductor 956 to the input g of the NAND gate 874 and by a conductor 958, an inverter 960, a conductor 962, and a conductor 964 to the input g of the NAND gate 878, and by a conductor 966 to the 64's bit input of the digital to analog converter 24. The 128's bit output of the up-down counter 22 is connected by a conductor 968 and a conductor 970 to the h input of the NAND gate 874, and by a conductor 972, an inverter 974, a conductor 976, and a conductor 978 to the input h of the NAND gate 878, and by a conductor 980 to the 128's bit input of the digital to analog converter 24. The 256's bit output of the up-down counter 22 is connected by a conductor 982 and a conductor 984 to the input i of the NAND gate 874, and by a conductor 986, an inverter 988, a conductor 990, and a conductor 992 to the input i of the NAND gate 878, and by a conductor 994 to the 256's bit input of the digital to analog converter 24. The NAND gate 874 detects the count of 506, and the NAND gate 878 detects the count of 6 from the up-down counter 22.

The output of the NAND gate 874 is connected by a conductor 1000 and a conductor 1002 to the S input of a flip-flop 1004, and by a conductor 1006 to the input s of the NAND gate 852. The output of the NAND gate 878 is connected by a conductor 1008 and a conductor 1010 to the R input of the flip-flop 1004, and by a conductor 1012 to the input c of the NAND gate 856. The flip-flop 1004 has outputs Q and $\bar{Q}$. The Q output is connected by a conductor 1014 to the input b of the NAND gate 856, and the Q output is connected by a conductor 1016 to the input b of the NAND gate 852. As will be hereinafter described, the outputs from the NAND gates 874 and 878 control the state of the flip-flop 1004, which controls the NAND gates 852 and 856, which control the direction of count of the up-down counter 22.

The digital to analog converter 24, is a current summing device which produces a current at its output proportional to the binary code at its input. Hence, the greater the count at its input, the greater the current at its output. The output of the digital to analog converter 882 is connected by a conductor 1020, a conductor 1022, a resistor 1024, and a potentiometer 1026 to a conductor 1028 that carries a positive DC voltage. The potentiometer 1026 is set so that the output current is zero when the binary input is a count of 256. In so doing, the output current level of the digital to analog converter 24 increases from zero as the binary coded input increases from 256, and decreases from zero as the binary coded input decreases from 256, producing an alternating current signal on the conductor 1020. This alternating current signal is fed through a conductor 1030 to the operational amplifier 25 to produce at its output a voltage proportional to the binary number at the input of the digital to analog converter 24. Hence, the output of the operational amplifier 25 is a waveform that increases from zero at the binary count of 256 in a staircase manner to some positive peak voltage at the count of 506, then decreases in a staircase manner to some negative peak voltage at the count of 6, and then increases in a staircase manner back up to zero at the count of 256 and so on. In this way, a continuous staircase wave is generated at the output of the operational amplifier 25. Because the steps of the wave are very small, one for each count, the waveform approximates a triangular waveform. The triangular waveform at the output of the operational amplifier 25 is fed through a conductor 1034 to the sine shaping network 26 to produce a sine wave of the same frequency as the triangular wave.

**OPERATION**

To explain the operation of the system suppose that it is desired to produce a signal at the output conductor 546 with a frequency of 9.932678 MHz. The millionth digit switch 501 is set on 9 to gate the 9 MHz signal $F_s$ through to the conductor 510. The 100,000th digit switch 502 is set on 9 to gate the 9 MHz signal $F_s$ through to the conductor 512, and into the division network 532, where it is divided by 10 to produce a frequency of 900 KHz on the conductor 534. In this same manner the switches 503 through 507 are set to produce 30 KHz, 2 KHz, 600 Hz, 70 Hz, and 8 Hz, signals at the outputs from their dividers 538 through 541, respectively. The 9 MHz signal is gated by the switch 501 by setting the switch 501 in the 9 position. With the switch 501 in the 9 position the complementary 1 MHz signal is fed through the conductor 550, the inverter 552, and the conductor 554 to form the $F_s$ signal. Also the $F_s$ signal, which is a 1 MHz signal advanced one full master oscillator pulse relative to the $F_s$ signal, is fed through the conductor 561, the inverter.
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562, and the conductor 564 to form the \( F_{e} \) signal. The \( F_{f}, F_{g}, F_{a}, \) and \( F_{e} \) signals are all inputs to the frequency adder 530.

The \( F_{f} \) signal, which is the 30 KHz signal, is fed through the conductor 539 to the input \( b \) of the frequency adder 540. Although the frequency adders for adding the 2 KHz, 600 Hz, and 70 Hz signals \( F_{a}, F_{g}, \) and \( F_{e} \), respectively, are not shown, these adders have suitable inputs \( b \) for introducing these frequencies. Finally, the \( F_{g} \) signal, which is the 8 Hz signal and the last in the series, is fed through the conductor 542 to the input \( b \) of the frequency adder 544.

FIG. 6 shows the waveforms of the adder circuit 530. The waveform 800 is the 9 MHz signal \( F_{e} \) to the conductor 510. The waveform 802 is the complement of the waveform 800 and is the 1 MHz signal \( F_{a} \) to the conductor 554. The waveform 804 is the 1 MHz signal \( F_{g} \) which is advanced one full master oscillator pulse relative to the \( F_{a} \) waveform 802. The waveform 806 is the 900 KHz signal \( F_{e} \) which is set by the switch 502 and which is fed through the conductor 534. It is the frequency of the \( F_{e} \) waveform 806 that is added to the frequency of the \( F_{a} \) waveform 800 by the adder network 530.

When the differentiator circuit 652 detects the trailing edge of the first pulse of the \( F_{g} \) waveform 806 it produces at its output a negative going spike as shown by the waveform 808. This negative going spike triggers the flip-flop 656 which places a 1 level at the \( j \) input of the flip-flop 660 as shown by the waveform 810. The trailing edge of the next \( F_{a} \) pulse that comes along at the \( T \) input of the flip-flop 660, triggers the flip-flop 660, placing its \( Q \) output at a 1 level as shown by the waveform 812. This 1 level is fed through the conductor 676 to the input \( b \) of the NAND gate 678. Exactly one master oscillator pulse later a pulse on the \( F_{a} \) waveform appears at the input \( a \) of the NAND gate 678. With both inputs \( a \) and \( b \) of the NAND gate 678 at a 1 level, a zero level pulse is generated at its output having a width equal to the width of the \( F_{a} \) pulse. This negative pulse is shown by the waveform 814. The negative pulse is fed to the NOR Input \( b \) of the NOR gate 650. Because \( F_{a} \) is a complement of \( F_{e} \), the negative pulse at the input \( b \) of the NOR gate 650 occurs simultaneously with a blank space on the \( F_{a} \) waveform. The NOR gate 650 adds the negative pulse at its input \( b \) in the blank space to produce at the output of the inverter 712 the sum of the two waveforms 800 and 814 as shown by the waveform 816 of FIG. 6. The negative pulse at the output of the NAND gate 678 which is added to the waveform \( F_{e} \) is also fed through the inverter and differentiator circuit 716 and 720 to produce a spike generated at the trailing edge of the \( F_{e} \) pulse to clear the flip-flops 656 and 660. With the 656 and 660 cleared, the input \( b \) of the NAND gate 678 goes to a zero level, the input \( b \) of the NAND gate 684 goes to a 1 level, and the input \( a \) of the NAND gate 674 goes to a 1 level as heretofore described. Hence, the NAND gate 678 is disabled and the NAND gates 684 and 674 are enabled.

What happens next depends on which of the waveforms \( F_{a} \) through \( F_{g} \) the next pulse occurs. Because the \( F_{g} \) frequency is considerably higher than the frequencies of the waveforms \( F_{a} \) through \( F_{g} \), it is most likely that several pulses on the \( F_{g} \) waveform will occur before an \( F_{f} \) frequency pulse occurs. Each time the pulse on the \( F_{f} \) frequency occurs the operation heretofore described of the frequency adder 530 will repeat to add a \( F_{f} \) waveform pulse to the \( F_{f} \) waveform, each time the flip-flops 656 and 660 resetting, and the NAND gates 684 and 674 enabling. However, eventually a \( F_{f} \) waveform pulse will occur prior to an \( F_{e} \) waveform pulse. With the NAND gates 684 and 674 enabled, the \( F_{a} \) and \( F_{e} \) waveforms are gated through the NAND gates 684 and 674 and the inverters 732 and 736 to the frequency adder 540. The frequency adder 540 operates in response to the \( F_{f} \) waveform pulse in exactly the same manner as the frequency adder 530, with the pulse on the \( F_{g} \) waveform triggering a flip-flop like the flip-flop 656 to add an \( F_{f} \) pulse to the output waveform from the frequency adder 530, this waveform being the sum of the waveforms \( F_{e} \) and \( F_{g} \). After the pulse is added the frequency adder 540 is reset as heretofore described with NAND gates like the NAND gate 674 and 684 being enabled to gate the \( F_{a} \) and \( F_{e} \) waveforms through to the next frequency adder network. If a pulse on the \( F_{g} \) waveform is the next to occur, this adder will add a \( F_{g} \) pulse to the output waveform from the adder 540 in response to the \( F_{g} \) pulse. This process continues through to the last frequency adder 544 where \( F_{e} \) waveform pulses are added in response to pulses occurring on the \( F_{f} \) waveform, it being remembered that the NAND gates 674, 684, and 678 in each of the frequency adders insure that the higher frequencies take precedence over the lower frequencies. Therefore, in this example, over a one second period, the frequency adder 530 adds 900,000 pulses to the \( F_{f} \) waveform; the next frequency adder 540 adds 30,000 pulses to the \( F_{e} \) waveform; the next frequency adder adds 2,000 pulses to the \( F_{g} \) waveform; the next frequency adder adds 600 pulses to the \( F_{e} \) waveform; and the last frequency adder 544 adds eight pulses to the \( F_{e} \) waveform, giving a resultant frequency at the output adder 546 of 9.932678 MHz.

To explain the operation of the network of FIG. 7 assume that the synthesized digital frequency is being fed through the conductor 554 to the inputs \( a \) of the NAND gates 852 and 856. Also assume that the NAND gate 852 is enabled which means that each of its inputs \( a, b \) and \( c \) are at a 1 level, and that the NAND gate 856 is disabled which means that one or more of its inputs \( a, b \) and \( c \) are at a 0 level. With the NAND gate 852 enabled the digital signal is fed to the \( U \) input of the up-down counter 22 causing the up-down counter 22 to begin counting up one digit for each pulse fed to the input \( U \).

When the up-down counter 22 has counted to a count of 506 the signals at its outputs will be such as to enable the NAND gate 874, producing at its output a 0 signal which is fed through the conductors 1000 and 1006 to the input \( c \) of the NAND gate 852, disabling the NAND gate 852 which disables the input \( U \) of the up-down counter 22 causing the counter to stop counting. The 0 level signal on the conductor 1000 is also fed through the conductor 1002 to the \( S \) input of the flip-flop 1004 placing its \( Q \) output at a 1 level and its \( \overline{Q} \) output at a 0 level. The 1 level \( Q \) output from the flip-flop 1004 is fed through the conductor 1014 to the input \( b \) of the NAND gate 856. The zero level \( \overline{Q} \) output from
the flip-flop 1004 is fed through the conductor 1016 to the input b of the NAND gate 852, holding the NAND gate 852 in the disabled condition.

Since the output of the NAND gate 878 is at a 1 level except where the up-down counter 22 is at a 6 count, the 1 level output from the NAND gate 878 is fed through the conductors 1008 and 1012 to the input c of the NAND gate 856. With the inputs a, b, and c of the NAND gate 856 each at a 1 level, the NAND gate 856 is enabled allowing the digital signal on the conductor 854 to be fed through the NAND gate 856 and the conductor 862 to the input D of the up-down counter 22 causing the up-down counter 22 to count down from a count of 506. As the digital pulses on the conductor 854 continue to feed into the input D, the up-down counter 22 continues to count down until it gets to a 6 count. When it gets to a 6 count its binary encoded output pulses are such as to enable the NAND gate 878 producing at its output a 0 level signal which is fed through the conductors 1008 and 1012 to the input c of the NAND gate 856, disabling the NAND gate 856 which disables the input D of the up-down counter 22 causing the counter to stop counting.

The 0 level signal on the conductor 1008 is also fed through the conductor 1010 to the R input of the flip-flop 1004 causing the flip-flop 1004 to change state with a 1 level at its Q output and a 0 level at its Q output. The 1 level at its Q output is fed through the conductor 1016 to the input b of the NAND gate 852, and the 0 level at its Q output is fed through the conductor 1014 to the input b of the NAND gate 856 holding the NAND gate 856 in the disabled condition. As soon as the up-down counter 22 counted down from the count 506 the NAND gate 874 became disabled producing a 1 level at its output which was fed through the conductors 1000 and 1006 to the input c of the NAND gate 852.

With each of the inputs a, b and c of the NAND gate 852 at a 1 level, the NAND gate 852 is enabled, allowing the digital signal on the conductor 850 to pass through the NAND gate 852, and the conductor 858 to the U input of the up-down counter 22 causing the up-down counter 22 to count up from the 6 count to the 506 count. This process of counting up and down between counts of 6 and 506 continues with the binary weighted outputs from the up-down counter 22 being fed through inverters to the inputs of the digital to analog converter 24.

With the potentiometer 1026 adjusted as heretofore described to produce a zero voltage for the count of 256, the output of the sine shaping network 26 is an AC sinusoidal waveform having a positive peak voltage corresponding to the count of 506 and a negative peak voltage corresponding to the count of 6.

Because it takes 1,000 digital pulses to produce one cycle of the sine wave, the sine wave frequency will be one one-thousandth of the frequency of the synthesized digital signal on the conductor 546, so that with a digital frequency of 9.932678 MHz, the sine wave frequency is 9,932.678 Hz. The waveforms from the master synthesizer 12, can be fed into any number of frequency selectors to generate a plurality of frequencies. Because these frequencies are synthesized from the same source they are mutually coherent, so that the difference between any one frequency and any other frequency always remains constant.

In summary, a system has been described to generate a plurality of coherent synthesized frequencies each of which may be selected from a wide range of frequencies.

Various changes and modifications may be made within the invention as will be readily apparent to those skilled in the art. Such changes and modifications are within the scope and teaching of this invention as defined by the claims appended hereto.

What is claimed is:

1. A system for synthesizing an electrical signal having a frequency selected from a range of frequencies comprising a master synthesizer responsive to a constant frequency input for generating a plurality of output waveforms of frequencies extending over a prescribed band of frequencies, means for selecting from the output waveforms a frequency to represent each digit of a selected synthesized frequency, and means for adding the selected frequencies to produce the selected synthesized frequency.

2. The system of claim 1 wherein the master synthesizer includes means for generating a first set of waveforms from the constant frequency input, and means for generating the plurality of output waveforms from the first set of waveforms.

3. The system of claim 2 wherein the first set of waveforms includes three waveforms of frequencies representing the 1's, 2's, and 8's bits of a binary coded decimal counter, and the means for generating the output waveforms from the first set of waveforms includes logic means for generating the output waveforms from various combinations of the first set of waveforms.

4. The system of claim 1 including means for generating a complement waveform for each of the output waveforms, and wherein the adding means includes means for adding pulses of the waveform complementary to the highest digit waveform in response to pulses of the other digit waveforms.

5. The system of claim 4 wherein the pulses of the complementary waveform are added to the highest digit waveform in response to pulses of the other digit waveforms with higher digit waveform frequencies taking precedence over lower digit waveform frequencies.

6. The system of claim 4 including means for generating a third set of waveforms of frequencies equal to the frequencies of the complementary waveforms but at a prescribed phase shift ahead of the complementary waveforms, and wherein the adding means is further responsive to the waveform of the third set of waveforms equal in frequency to the waveform complementary to the highest digit waveform.

7. The system of claim 1 wherein the output waveforms include frequencies representing the numbers 1 through 9 multiplied by a factor of 10.

8. The system of claim 7 wherein the factor of 10 is the same for each of the waveforms.

9. The system of claim 1 wherein the means for selecting a frequency to represent each digit includes a plurality of division networks for dividing the frequencies of the output waveforms selected to represent the digits of the selected synthesized frequency by a factor of 10, the factor of 10 by which each selected frequency is divided depending on the digit it represents.

10. The system of claim 1 wherein the adding means includes a series of adding networks, one for each of
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the frequencies to be added to the highest digit frequency, and means for giving the addition of a higher frequency precedence over addition of a lower frequency.

11. The system of claim 1 wherein the selected synthesized signal is a pulse signal, and including means for generating a staircase waveform from the selected synthesized frequency.

12. The system of claim 11 wherein the staircase waveform generating means includes counter means for producing a binary coded decimal encoded count between a predetermined upper count and a predetermined lower count in response to the pulses on the selected synthesized signal, and means for converting each count to a voltage level proportional to the count to produce a staircase waveform approximating a triangular wave.

13. The system of claim 12 including means for shaping the staircase waveform to produce a sinusoidal waveform.

14. A system for synthesizing a plurality of mutually coherent electrical signals where the difference between the frequencies of any two of the signals remains constant over time, each of the signals being of a frequency selected from a range of frequencies comprising a master synthesizer responsive to a constant frequency input for generating a plurality of output waveforms of frequencies extending over a prescribed band of frequencies, and a plurality of frequency selectors, each frequency selector comprising means for selecting from the output waveforms a frequency to represent each digit of a selected synthesized frequency, and means for adding the selected frequencies to produce the selected synthesized frequency, whereby slight changes in frequency of the constant frequency input produces corresponding changes in the frequencies synthesized therefrom with the synthesized signals being mutually coherent.

15. The system of claim 14 wherein the master synthesizer includes means for generating a first set of waveforms from the constant frequency input, and means for generating the output waveforms from the first set of waveforms.

16. A system for synthesizing an electrical signal comprised of pulses of a frequency selected from a range of frequencies, the system comprising a master oscillator for generating a pulse signal of a single frequency, the frequency of the master oscillator depending on the frequency of the signal to be synthesized, means for generating a plurality of output pulse signals from the single master oscillator pulse signal, the plurality of output pulse signals being of frequencies extending over a prescribed band of frequencies, means to select from the plurality of output pulse signals a signal for each digit of the selected synthesized signal, and means for adding the signals representing each digit to generate the selected synthesized signals.

17. The system of claim 16 wherein the digit selection means includes a plurality of logic switches, the plurality of output pulse signals generated from the master oscillator signal being fed as inputs to each of the logic switches, and means for selectively gating an input signal through selective ones of the logic switches, the output signals from the logic switches representing the digits of the selected synthesized signal.

18. The system of claim 17 including a plurality of division networks for dividing the frequencies of the output signals from the logic switches by factors of 10, the factor of 10 by which each frequency is divided depending on the digit it represents.

19. The system of claim 16 including means for generating a first set of pulse signals from the single master oscillator pulse signal and means for generating the plurality of output pulse signals from the first set of pulse signals.

20. The system of claim 16 including means for generating a complement pulse signal for each of the plurality of output pulse signals generated from the master oscillator signal, the complementary pulse signal having pulses where its complement has no pulses, and means for adding pulses of the signal complementary with the highest digit signal to the highest digit signal in response to pulses of the lower digit signals.

21. The system of claim 20 including means for generating a third set of signals of frequencies equal to the frequencies of the complementary signals but whose pulses are at a prescribed phase shift ahead of the pulses of the complementary waveforms, and wherein the adding means is further responsive to the signal of the third set of signals equal in frequency to the signal complementary to the highest digit signal.

22. The system of claim 21 wherein the phase shift is one master oscillator pulse.

23. The system of claim 22 wherein the adding means includes gating means responsive to the pulses on the signal of the third set of signals equal in frequency to the signal complementary to the highest digit signal for gating the pulses on the complementary signal for addition to the highest digit signal, the gating means being also responsive to the pulses of the lower digit signals, the number of pulses added being equal to the number of pulses of the lower digit signals, and the timing of the pulses added being determined by the signal of the third set of signals.

24. The system of claim 23 including gating means for adding a pulse in response to a higher digit signal pulse before adding a pulse in response to a lower digit signal pulse.

25. A system for synthesizing a plurality of mutually coherent signals, each signal comprising pulses of a frequency selected from a range of frequencies, the system comprising a master oscillator for generating a pulse signal of a single frequency, the frequency of the master oscillator depending on the maximum frequency to be synthesized, means for generating a first set of pulse signals from the master oscillator pulse signal, means for generating a second set of pulse signals from the first set of pulse signals of frequencies representing a multiple of the numbers 1 through 9, the multiple depending on the maximum frequency to be synthesized, means for generating a complementary pulse signal for each of the second set of pulse signals, means for generating a third set of pulse signals equal in frequency to the complementary signals but at a prescribed phase shift ahead of the complementary signals, a plurality of frequency selectors, the number of frequency selectors depending on the number of coherent signals to be synthesized, each frequency selector comprising a plurality of logic switches, the number of logic switches depending on the number of digits in the signal to be synthesized, each of the second set of signals being fed
as inputs to each of the logic switches, means for gating a selective signal from the second set of signals through selective ones of the logic switches, means into which the outputs of the logic switches are fed to divide each of the outputs from the logic switches separately by a factor of 10 to produce signals representing each of the digits of a selected synthesized frequency, whereby each logic switch is set to gate a selected signal to represent a digit of the selected synthesized signal, and means for adding pulses on the signal complementary with the highest digit signal to the highest digit signal at times determined by the signal from the third set of signals equal in frequency to the complementary signal and in numbers determined by the number of pulses on the signals representing the remaining digits of the selected synthesized signal, and gating means to add a pulse in response to a higher digit signal pulse before adding a pulse in response to a lower digit signal pulse, whereby slight changes in frequency of the master oscillator signal produces corresponding changes in the frequencies synthesized therefrom with the synthesized frequency being mutually coherent.

26. A method of synthesizing an electrical signal having a frequency selected from a range of frequencies comprising the steps of generating a first signal of constant frequency, synthesizing a set of second signals from the first signal of frequencies extending over a prescribed band of frequencies, each signal of the second set of signals being of a constant frequency, selecting from the frequencies of the second set of signals a frequency for each digit of the selected synthesized signal, and adding the selected frequencies together to produce the selected synthesized signal.

27. The method of claim 26 wherein the generating step there is included the step of generating a first set of signals from the first constant frequency signal, and the step of synthesizing a set of second signals includes synthesizing the set of second signals from the first set of signals.

28. The system of claim 26 including the step of generating a complement signal for each of the second set of signals, and wherein the adding step includes adding pulses on the signal complementary with the highest digit signal to the highest digit signal in response to pulses on the lower digit signals.

29. The method of claim 28 including the step of generating a third set of waveforms of frequencies equal to the frequencies of the complementary waveforms but at a prescribed phase shift ahead of the complementary waveforms, and wherein the adding step further includes adding pulses on the waveform complementary with the highest digit waveform in response to the waveform of the third set of waveforms equal in frequency to the waveform complementary to the highest digit waveform.

30. The method of claim 26 wherein the selecting step further includes dividing the frequencies of the second set of signals selected to represent the digits of the selected synthesized signal by a factor of 10, the factor of 10 by which each selected frequency is divided depending on the digit it represents.

31. The method of claim 27 wherein the step of synthesizing the second set of signals from a first set of signals includes combining selective ones of the first set of signals in a logic circuit to synthesize the second set of signals.

32. A method of synthesizing a plurality of mutually coherent electrical signals where the difference between the frequencies of any two of the signals remains constant over time, each of the signals being of a frequency selected from a range of frequencies, comprising the steps of generating a first waveform of constant frequency, synthesizing a set of second waveforms from the first waveform of frequencies extending over a prescribed band of frequencies, the frequency of each waveform in the second set of waveforms being constant, selecting from the second set of waveforms a frequency to represent each digit of a plurality of selected synthesized signals, and adding the selected frequencies for producing each selected synthesized signal, whereby slight changes in frequency of the first waveform produces corresponding changes in the frequencies of the signals synthesized therefrom with the selected synthesized signals being mutually coherent.

33. The method of claim 32 wherein after the generating step there is included the step of generating a first set of waveforms from the first waveform, and wherein the synthesizing step includes synthesizing the second set of waveforms from the first set of waveforms.

34. The method of claim 31 wherein the selected synthesized signals are pulse signals, and including the step of generating a plurality of mutually coherent sinusoidal waveforms from the selected synthesized signals.

35. The method of claim 34 wherein the last mentioned step includes for each selected synthesized signal, generating signals corresponding to a binary coded decimal encoded count between a predetermined upper limit and a predetermined lower limit in response to the pulses on the selected synthesized frequency, generating a series of voltage levels in response to and in proportion to each count to produce a staircase waveform having a positive peak value corresponding to the predetermined upper count and a negative peak value corresponding to the predetermined lower count, and shaping the staircase waveform into a sinusoidal waveform.

36. A method of synthesizing an electrical signal comprised of pulses of a frequency selected from a range of frequencies, comprising the steps of generating a first pulse signal of a single frequency, the frequency of the first pulse signal depending on the frequency of the signal to be synthesized, generating a second set of pulse signals from the single pulse signal of frequencies extending over a prescribed band of frequencies, each of the signals in the second set of signals being of constant frequency, selecting from the second set of pulse signals a signal for each digit of a selected synthesized signal, and adding the signals representing each digit to produce the selected synthesized signal.

37. The method of claim 36 including the steps of feeding the second set of signals as inputs to each of a plurality of logic switches, and wherein the selecting step includes selectively gating an input signal through selective ones of the logic switches.

38. The method of claim 37 including the step of dividing the frequencies of the gated signals at the outputs of the logic switches by factors of 10, the factors of 10 by which each frequency is divided depending on the digit it represents.
39. The method of claim 36 including the step of generating a complement pulse signal for each of the second set of pulse signals, and wherein the adding step includes adding pulses of the signal complementary with the highest digit signal in response to pulses of the lower digit signals to the highest digit signal.

40. The method of claim 39 including the step of generating a third set of signals with frequencies equal to the frequencies of the complementary signals but whose pulses are at a prescribed phase shift ahead of the pulses of the complementary waveform, and wherein the adding step further includes adding pulses of the complementary signal in response to the signal in the third set of signals equal in frequency to the complementary signal.

41. The method of claim 40 wherein the adding step further includes gating pulses on the complementary signal for addition to the highest digit signal in response to pulses on the signal of the third set of signals equal in frequency to the signal complementary to the highest digit signal, and to pulses on the lower digit signals, the number of pulses added being equal to the number of pulses on the lower digit signals, and the timing of the pulses added being determined by the pulses on the signal of the third set of signals.

42. The method of claim 39 wherein a pulse is added in response to a higher digit signal before a pulse is added in response to a lower digit signal pulse.

43. A method for synthesizing a plurality of mutually coherent signals each signal comprising pulses of a frequency selected from a range of frequencies, comprising the steps of generating a first signal of constant frequency, the frequency of the first signal depending on the maximum frequency of the mutually coherent signals to be synthesized, generating a first set of pulse signals from the first signal, generating a second set of pulse signals from the first set of pulse signals, the second set of pulse signals being of frequencies representing a multiple of the numbers 1 through 9, the multiple depending on the maximum frequency of the mutually coherent signals to be synthesized, generating a complementary pulse signal for each of the second set of pulse signals, generating a third set of pulse signals equal in frequency to the complementary pulse signals but at a prescribed phase shift ahead of the complementary signals, feeding each of the second set of signals as inputs to each of a plurality of logic switches, the number of logic switches depending on the number of digits in the signals to be synthesized, gating a selective signal from the second set of signals through selected ones of the logic switches, dividing each of the gated signals separately by a factor of 10 to produce signals representing each of the digits of the selected synthesized signals, whereby each logic switch is set to gate a selected signal to represent a digit of each of the selected synthesized signals, and adding pulses of the signals complementary with the highest digit signals of the selected synthesized signals at times determined by signals of the third set of signals equal in frequency to the complementary signals and in numbers determined by the number of pulses on the signals representing the remaining digits of each of the selected synthesized signals, so that in synthesizing each selected signal a pulse is added in response to a pulse on a higher digit signal before a pulse on a lower digit signal, whereby slight changes in frequency of the first signal produces corresponding changes in the frequencies synthesized therefrom with the synthesized signals being mutually coherent.

44. A method of synthesizing an electrical signal having a frequency selected from a range of frequencies comprising the steps of generating a first signal of constant frequency, generating a set of second signals from the first signal, the set of second signals being of frequencies extending over a prescribed band of frequencies, generating a complementary signal for each of the second set of signals, generating a set of enable signals equal in frequency to the complementary signals but at a prescribed phase shift ahead of the complementary signals, selecting from the second set of signals a frequency for each digit of the selected synthesized signal, and adding each of the selected frequencies representing the lower digits to the highest digit frequency in a plurality of adding networks, the adding step further comprising the steps of recognizing each pulse on the signals to be added to the highest digit frequency, for each pulse recognized, recognizing the next pulse on the enable signal equal in frequency to the signal complementary to the highest digit signal, enabling a gate in response to the pulse on the enable signal, with the gate enabled, gating the next pulse on the signal complementary to the highest digit signal to an adding gate, adding the pulse on the complementary signal to the highest digit signal, and blocking the recognition of a pulse on a lower digit signal whenever a pulse on a higher digit signal appears giving higher digit signals precedence over lower digit signals, whereby over a time span of one second all of the pulses that appear on the lower digit signals will be added to the highest digit signal.