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61/937,594 9 February 2014 (09.02.2014) US(71) Applicant: **THE TRUSTEES OF COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK** [US/US]; 412 Low Memorial Library, 535 West 116th Street, New York, NY 10027 (US).(72) Inventors: **ZHU, Jianxun**; 400 West 119th Street, Apt. 2E, New York, NY 10027 (US). **KINGET, Peter, R.**; 11 Franklin Place, Summit, NJ 07901 (US). **KRISHNASWAMY, Harish**; 601 W. 115th Street, #65, New York, NY 10025 (US).(74) Agents: **BYRNE, Matthew, T.** et al.; Byrne Poh LLP, 11 Broadway, Suite 1115, New York, NY 10004 (US).

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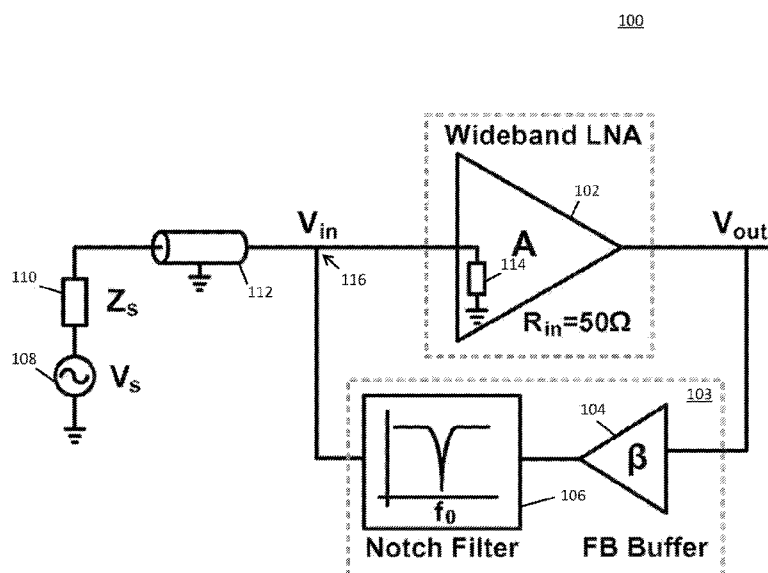


FIG. 1

(57) Abstract: Circuits for low noise amplifiers with interferer reflecting loops are provided. In some embodiments, circuits for a low noise amplifier with an interferer reflecting loop are provided, the circuits comprising: a low noise amplifier (LNA) having an input and an output; a buffer having an input coupled to the output of the LNA and an output; and notch filter having an input coupled to the output of the buffer and an output coupled to the input of the LNA.

CIRCUITS FOR LOW NOISE AMPLIFIERS WITH INTERFERER REFLECTING LOOPS

Cross Reference to Related Application

[0001] This application claims the benefit of United States Provisional Patent Application No. 61/937,594, filed February 9, 2014, which is hereby incorporated by reference herein in its entirety.

Statement Regarding Government Funded Research

[0002] This invention was made with government support under contract HR0011-12-1-0006 by the Defense Advanced Research Projects Agency (DARPA). The government has certain rights in the invention.

Background

[0003] The growth of wireless communications has resulted in a large number of different standards operating in different portions of the spectrum. Software defined radios (SDRs) have been proposed so a single device can operate with different standards or frequencies. Their implementation remains an active area of research given the challenging performance requirements in terms of noise figure (NF), linearity, and power dissipation. Multi-standard receivers are often designed to meet the worst-case combination of requirements which leads to increased power dissipation. Given the continued growth in usage and data rates of wireless devices, the amount of interference that receivers need to tolerate keeps increasing, while the spectral conditions can also vary significantly from location to location and from time to time.

Therefore it is becoming more and more desirable to design radio frequency (RF) front ends that can dynamically adjust to the specific spectral operating conditions and standards.

[0004] Accordingly, new circuits for radio receivers are desirable.

Summary

[0005] In accordance with some embodiments, circuits for low noise amplifiers with interferer reflecting loops are provided. In some embodiments, circuits for a low noise amplifier with an interferer reflecting loop are provided, the circuits comprising: a low noise amplifier (LNA) having an input and an output; a buffer having an input coupled to the output of the LNA and an output; and notch filter having an input coupled to the output of the buffer and an output coupled to the input of the LNA

Brief Description of the Drawings

[0006] FIG. 1 is a block diagram of a low noise amplifier with an interferer reflecting loop in accordance with some embodiments.

[0007] FIG. 2 is a schematic diagram of a low noise amplifier with an interferer reflecting loop in accordance with some embodiments.

[0008] FIG. 3 is a schematic diagram of a notch filter that can be used with the interferer reflecting loop of FIG. 2 in accordance with some embodiments.

[0009] FIG. 4 is a diagram showing timing diagrams of, and circuits for creating, different phases of a clock signal that can be used to control the notch filter of FIG. 3 in accordance with some embodiments.

[0010] FIG. 5 is a schematic diagram of another notch filter that can be used with the interferer reflecting loop of FIG. 2 in accordance with some embodiments.

[0011] FIG. 6 is a schematic diagram of yet another notch filter that can be used with the interferer reflecting loop of FIG. 2 in accordance with some embodiments.

Detailed Description

[0012] In accordance with some embodiments, circuits for low noise amplifiers with interferer reflecting loops are provided. These circuits can provide receiver components that can amplify desired in-band signals while reflecting out-of-band signals back to the signal source (e.g., one or more antennas).

[0013] Turning to FIG. 1, an example 100 of a circuit for a low noise amplifier with an interferer reflecting loop is illustrated. As shown, circuit 100 includes a low noise amplifier (LNA) 102, an interferer reflecting loop 103, a signal source V_S 108, a source impedance Z_S 110, and a transmission line 112.

[0014] LNA 102 can be any suitable LNA, such as a wideband LNA, and may have an input impedance R_{in} 114, which can have any suitable value, such as an impedance equal to that of source impedance Z_S , in some embodiments. Interferer reflecting loop 103 can include a feedback buffer 104 (which can be any suitable RF signal buffer in some embodiments) and a notch filter 106 (which can be any suitable notch filter in some embodiments). Signal source 108 can be any suitable source of a signal to be amplified by LNA 102. For example, in some embodiments, signal source 108 can be one or more antennas that provide RF signals. Source impedance Z_S 110 can be any suitable source impedance and may be part of signal source 108 in some embodiments. For example, source impedance Z_S 110 may be the impedance of one or

more antennas. Transmission line 112 can be any suitable transmission line, such as a coaxial cable, or combination of transmission lines, and can have any suitable characteristics, in some embodiments. For example, transmission line 112 can have a characteristic impedance equal to that of Z_S in some embodiments.

[0015] During operation of circuit 100, for in-band signals (which can be those signals at or around a desired receiver frequency) received at V_{in} , the loop gain resulting from feedback loop 103 can be small and therefore the presence of the feedback loop can be ignored. Under such conditions, the input impedance at V_{in} is generally set by the LNA input impedance (R_{in}), which can be matched to the source impedance (Z_S).

[0016] For out-of-band interferers (which can be those signals not at or around a desired receiver frequency), however, the gain from feedback loop 103 can be large and therefore the feedback loop can alter the input impedance at V_{in} . Under such conditions, the input impedance V_{in} is reduced below that of R_{in} and Z_S and hence low impedance signal reflection of the out-of-band interferers occurs.

[0017] To the first order, the voltage swings at the LNA input are dominated by the in-band signals. Out-of-band signals are shorted through the notch filter and its low impedance driver and the interferer power is reflected back to source 108 (e.g., the antenna(s)).

[0018] FIG. 2 shows a detailed schematic of an example 200 of a circuit including a low noise amplifier 202 with an interferer reflecting loop 203. As in circuit 100, circuit 200 also includes a signal source V_S 208, a source impedance Z_S 210, and a transmission line 212, which are substantially similar to signal source V_S 108, source impedance Z_S 110, and transmission line 112 in FIG. 1. Circuit 200 further includes DC blocking capacitors 230 and 232 (which can have

any suitable values, such as 33 pF, in some embodiments) and RF chokes 234 and 236 (which can have any suitable values, such as 82 nH, in some embodiments).

[0019] Within a device package including LNA 202, bondwires 238 and 240 may be provided to connect pins of the device package to a semiconductor chip on which the LNA is implemented.

[0020] As shown in FIG. 2, common gate transconductor 250 can be provided within LNA 202 in some embodiments. Transconductor 250 can be formed from transistors M1, M2, M3, and M4 in the configuration shown. $V_{bp,Gm}$ and $V_{bn,Gm}$ are bias voltages that can be supplied to the transconductor and can have any suitable values. V_{casp} and V_{casn} are control signals for turning transconductor 250 off by pulling V_{casn} to V_{SS} and V_{casp} to V_{DD} .

[0021] A common source transconductor 252 can also be provided within LNA 202 in some embodiments. As illustrated, in some embodiments, transconductor 252 can be a multi-slice transconductor having any suitable number of slices, such as 16 slices as shown in FIG. 2. In some embodiments, these slices can be individually turned off by pulling the respective V_{casn} to V_{SS} and V_{casp} to V_{DD} . Turning off slices allows power consumption by the LNA to be reduced in the field at the expense of a higher noise factor. As shown, each slice of the common source transconductor can include transistors M5, M6, M7, and M8 connected as shown.

[0022] Although not shown in FIG. 2, in some embodiments, common gate transconductor 250 can be implemented as a multi-slice transconductor having any suitable number of switchable slices in a manner similar to transconductor 252.

[0023] DC blocking capacitors 242 and 244 and shunt resistors 246 and 248 are also provided at the inputs to the common source transconductor to provide proper bias voltages.

[0024] In some embodiments, the signal currents I_{CG} and I_{CS} from common gate transconductor 250 and common source transconductor 252, respectively, are pushed into radio-frequency trans-impedance amplifiers (RF-TIAs) 276 and 274, respectively. RF-TIA 274 can be formed from any suitable number of switchable slices (such as two slices as shown in FIG. 2) and each slice can include transistors M11 and M12 connected as shown in FIG. 2, in some embodiments. To make the slices of RF-TIA switchable, switches (not shown) can be provided at the gates of transistors M11 and M12 that break them away from the signal path and pull them to V_{SS} and V_{DD} respectively. RF-TIA 276 can include transistors M9 and M10 connected as shown in FIG. 2, in some embodiments. Although not shown in FIG. 2, in some embodiments, RF-TIA 276 can be implemented as a multi-slice RF-TIA having any suitable number of switchable slices in a manner similar to RF-TIA 274.

[0025] DC blocking capacitors 258, 266, 268, and 260 can be provided at the inputs to RF-TIAs 274 and 276.

[0026] In some embodiments, the RF-TIAs can include resistive shunt-shunt feedback with digitally programmable resistors. More particularly, as shown, a feedback mechanism can be formed from digitally programmable resistors 262 and 264 and transistor slices 274 and 276. Sense resistors 280 and 282, shunt resistors 254, 270, 272, and 256, and operational amplifier 278 set the common-mode voltage at output nodes 284 and 286 to the desired value of $V_{CM,ref}$. This feedback mechanism allows one to independently program the gain of LNA 202 in the field and to adjust the weighted combination of the common source signals (from RF-TIAs 274) and the common gate signals (from RF-TIA 276) at output nodes 284 and 286 in the field.

[0027] Like interferer reflecting loop 103 described above in connection with FIG. 1, interferer reflecting loop 203 of FIG. 2 includes a feedback buffer 204 and a notch filter 206.

[0028] Feedback buffer 204 can be implemented using a class-AB complementary source follower including transistors M13 and M14 in some embodiments. Using a source follower topology can provide a low output impedance in some embodiments. The complementary structure can be biased by a bias circuit (e.g., as described below) with a low quiescent current (e.g., 1.1 mA) to save DC power, but when large out-of-band signals are present, the feedback buffer can sink large currents through the notch filter from source 208. To minimize the body effect, triple-well transistors can be used for transistors M13 and M14.

[0029] DC blocking capacitors 288 and 290 can be provided at the gates of transistors M14 and M13, respectively.

[0030] A bias circuit can be provided in buffer 204 using operational amplifier 296, current source 298, transistor 299, transistors M15, M16, M17, and M18, and resistors 292 and 294. In the bias circuit, the signal transistors are replicated as diodes (M16 and M17) while the DC bias current and the DC voltage at the sources of M16 and M17 can be controlled to $V_{CM,ref}$ with a feedback loop formed by M17, M18 and operational amplifier 296. Matching between M13, M16, M14, and M17 keep the DC output voltage of buffer 204 close to $V_{CM,ref}$.

[0031] In some embodiments, the user can disable the IR loop around the LNA by putting the feedback buffer in a high impedance state by appropriately pulling the gate biases of transistors M14 and M13 to V_{SS} and V_{DD} , respectively, by opening switches 289 and 291 and closing switches 293 and 295.

[0032] Any suitable parameters can be used for the components of FIG. 2 in some embodiments. For example, in some embodiments, the parameters in the following tables can be used:

MOSFETs	W(μm)	L(μm)
M1	32	0.08
M2	32	0.08
M3	64	0.08
M4	64	0.08
M5	16	0.08
M6	16	0.08
M7	32	0.08
M8	32	0.08
M9	48	0.08
M10	96	0.08
M11	48	0.08
M12	96	0.08
M13	80	0.08
M14	40	0.08
M15	8	0.5
M16	8	0.08
M17	4	0.08
M18	16	0.5
M19(299)	8	0.5

Resistors	R ($\text{k}\Omega$)
246	28
248	28
254	60
262	0.05-2.4
270	60
272	60
264	0.16-2.4
256	60
280	15.5
282	15.5

Capacitors	C (pF)
242	2
244	2
258	1.3
266	1.3
268	1.3
260	1.3
288	1.3
290	1.3

Current Source	I(μ A)
298	50

[0033] In accordance with some embodiments, any suitable notch filter can be used for notch filter 206 of FIG. 2. For example, in some embodiments, the notch filter can be implemented using: a switched-capacitor N-path notch filter; an LC filter with on-chip switchable capacitors and a spiral inductor; or an LC filter with on-chip switchable capacitors with bondwires as high Q inductors.

[0034] Turning to FIG. 3, an example of a circuit 300 for implementing a notch filter using a switched-capacitor N-path notch filter is shown. N-path filters translate a baseband impedance to RF frequencies realizing RF filters with high selectivity and tunable center frequency. An 8-path switched capacitor filter can be equivalent to a high-Q RLC resonator (where $R > 1k \text{ Ohm}$ when loaded with 25 Ohm) and can be used directly in interferer reflecting loop 203 to realize a narrowband filtering characteristic that is tunable in some embodiments. The N-path notch filter shown in FIG. 3 can use 4 pF MiM capacitors for capacitors 318, 320, 322, 324, 326, 328, 330, and 332, and $50 \text{ }\mu\text{m}/65 \text{ nm}$ switches with an $R_{ON} = 15 \text{ Ohm}$ for switches 302, 304, 306, 308, 310, 312, 314, and 316, in some embodiments.

[0035] As shown by timing diagram 402 in FIG. 4, a set of 8-phase 25% duty cycle overlapping clocks can be used to control switches 302, 304, 306, 308, 310, 312, 314, and 316, in some embodiments. The eight capacitors 318, 320, 322, 324, 326, 328, 330, and 332 can be sequentially selected by the overlapping phases of the two switches on either side of each capacitor (e.g., switches 302 and 310 for capacitor 318, and switches 304 and 310 for capacitor 320). The clock signals on the same side of the filter need to be non-overlapping to prevent discharging the capacitors during switch over time.

[0036] In some embodiments, as also shown in FIG. 4, to generate clocks ϕ_0 , ϕ_1 , ϕ_2 , ϕ_3 , ϕ_4 , ϕ_5 , ϕ_6 , and ϕ_7 , a divide-by-four, dual-edge-triggered latch divider 404 operating at half the frequency of a traditional divide-by-eight divider can be used to generate the signals in timing diagram 406. The clock frequency f_{clk} can be tuned between 0.8 GHz to 6.4 GHz corresponding to a 0.2 GHz to 1.6 GHz frequency tuning range for the frequency f_0 of the notch filter, in some embodiments. The signals a_0 , a_1 , a_2 , a_3 , a_4 , a_5 , a_6 , and a_7 produced by divider 404 can then be combined by logic 408 to produce clocks ϕ_0 , ϕ_1 , ϕ_2 , ϕ_3 , ϕ_4 , ϕ_5 , ϕ_6 , and ϕ_7 .

[0037] FIG. 5 shows an example of a circuit 500 for implementing a notch filter using an LC filter with on-chip switchable capacitors and a spiral inductor. As illustrated, circuit 500 can include an AC coupling capacitor 502, a switchable array of capacitors 504, and a spiral inductor 506 in some embodiments. In some embodiments, the spiral inductor can have any suitable value, such as 1.1 nH, and the switchable array of capacitors can be implemented using any suitable number of parallel-connected, switchable MiM capacitors having any suitable values, such as a value of 4.2 pF to 6 pF.

[0038] Turning to FIG. 6, an example of a circuit 600 for implementing a notch filter using an LC filter with on-chip switchable capacitors with bondwires as high Q inductors is shown. As

illustrated, circuit 600 can include an AC coupling capacitor 602, a switchable array of capacitors 604, and an inductor formed from bondwires 608 in some embodiments. In some embodiments, the switchable array of capacitors can be implemented using any suitable number of parallel-connected, switchable MiM capacitors having any suitable values, such as a value of 4.2 pF to 6 pF.

[0039] Bondwires can offer a high Q (e.g., $Q > 20$) alternative to other inductor types to realize an inductor. At packaging time, the wire length of the bondwires can be set to program the frequency of the notch filter, while the on-chip capacitors can be programmed in the field (e.g., from 4.2 pF to 6 pF) for fine tuning. As shown in FIG. 6, the bondwires can be connected to a floating bondpad 610 to provide mechanical support, in some embodiments. FIG. 7 illustrates an example of an approach to implementing an inductor for a QFN package 700 where a floating pin 704 is used as an intermediate landing point for a bondwires 702.

[0040] The provision of the examples described herein (as well as clauses phrased as "such as," "e.g.," "including," and the like) should not be interpreted as limiting the claimed subject matter to the specific examples; rather, the examples are intended to illustrate only some of many possible aspects.

[0041] Although the invention has been described and illustrated in the foregoing illustrative embodiments, it is understood that the present disclosure has been made only by way of example, and the numerous changes in the details of implementation of the invention can be made without departing from the spirit and scope of the invention, which is only limited by the claims which follow. Features of the disclosed embodiments can be combined and rearranged in various ways.

What is claimed is:

1. A circuit for a low noise amplifier with an interferer reflecting loop, comprising:
a low noise amplifier (LNA) having an input and an output;
a buffer having an input coupled to the output of the LNA and an output; and
a notch filter having an input coupled to the output of the buffer and an output coupled to the input of the LNA.
2. The circuit of claim 1, wherein LNA is a wideband LNA.
3. The circuit of claim 1, where a gain of the LNA can be changed in the field.
4. The circuit of claim 1, wherein the LNA comprises:
a common gate transconductor having an input coupled to the input of the LNA and an output;
a common source transconductor having an input coupled to the input of the LNA and an output;
a first radio frequency trans-impedance amplifier (RF-TIA) having an input coupled to the output of the common gate transconductor and having an output coupled to the output of the LNA; and
a second RF-TIA having an input couple to the output of the common source transconductor and having an output coupled to the output of the LNA.

5. The circuit of claim 4, wherein the common source transistor is a multi-slice common source transistor.
6. The circuit of claim 5, wherein each slice of the multi-slice common source transistor is switchable.
7. The circuit of claim 4, wherein the second RF-TIA is a multi-slice RF-TIA.
8. The circuit of claim 7, wherein each slice of the multi-slice RF-TIA is switchable.
9. The circuit of claim 4, wherein a ratio of a contribution of an output signal of the first RF-TIA to an output signal of the second RF-TIA in the output of the LNA is controllable in the field.
10. The circuit of claim 1, wherein the buffer comprises a class-AB complementary source follower.
11. The circuit of claim 1, wherein the notch filter is a switched-capacitor N-path notch filter.
12. The circuit of claim 11, wherein the notch filter comprises:
 - a first terminal;
 - a second terminal;
 - a plurality of capacitors each having a first side and a second side; and

a plurality of switches each having a first side and a second side,

wherein the first side of each of a first half of the plurality of switches are connected to the first terminal, the second side of each of the first half of the plurality of switches are connected to the first side of each of two unique ones of the plurality of capacitors, the first side of each of a second half of the plurality of switches are connected to the second terminal, and the second side of each of the second half of the plurality of switches are connected to the second side of each of two unique ones of the plurality of capacitors.

13. The circuit of claim 12, wherein the plurality of switches are formed from transistors.

14. The circuit of claim 12, wherein a multiphase clock signal controls the plurality of switches.

15. The circuit of claim 14, further comprising a divide-by-four, dual-edge-triggered latch divider and a plurality of NAND gates to create the multiphase clock signal.

16. The circuit of claim 1, wherein the notch filter comprises switchable capacitors and a spiral inductor.

17. The circuit of claim 1, wherein the notch filter comprises switchable capacitors and an inductor formed from bondwires.

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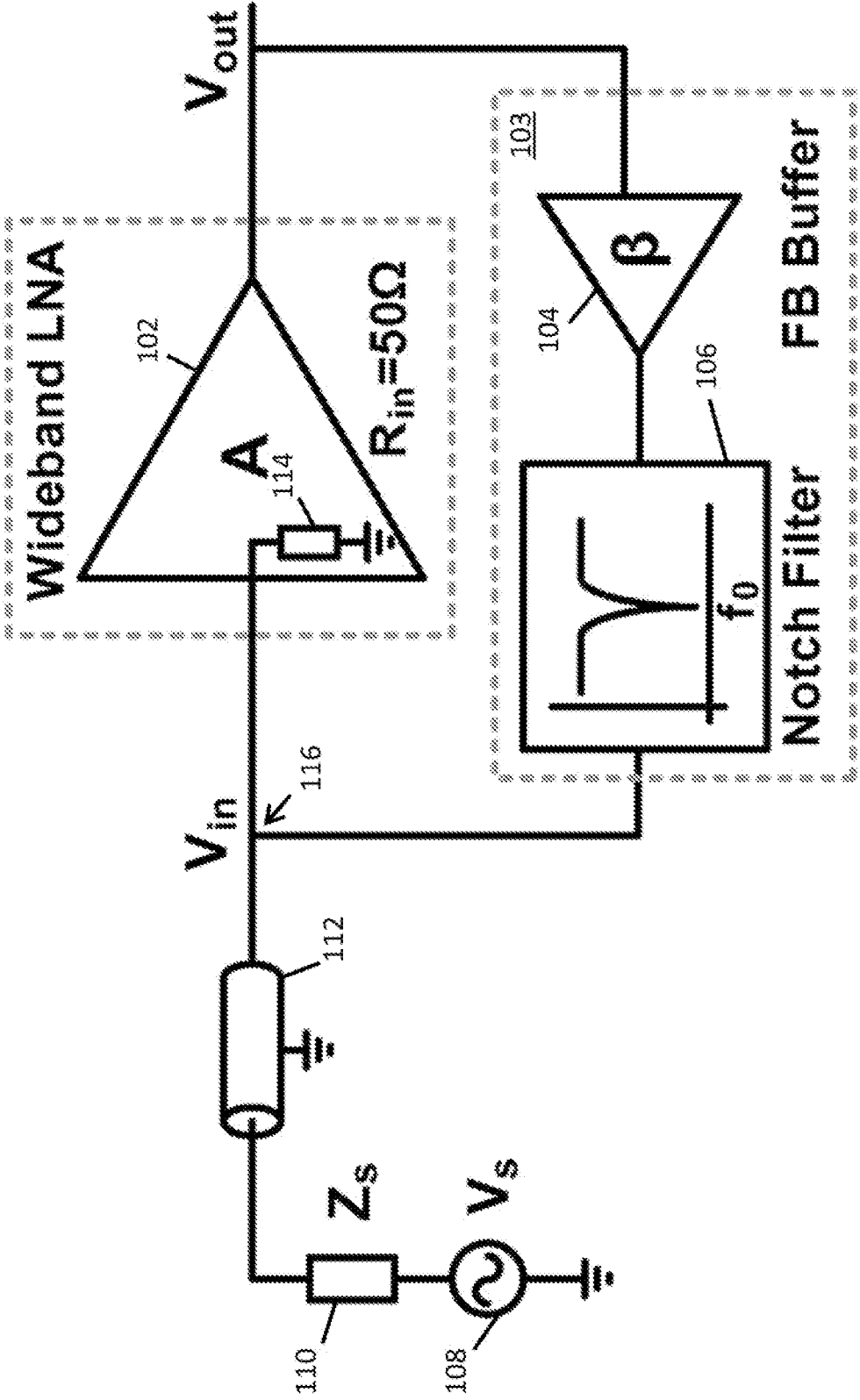


FIG. 1

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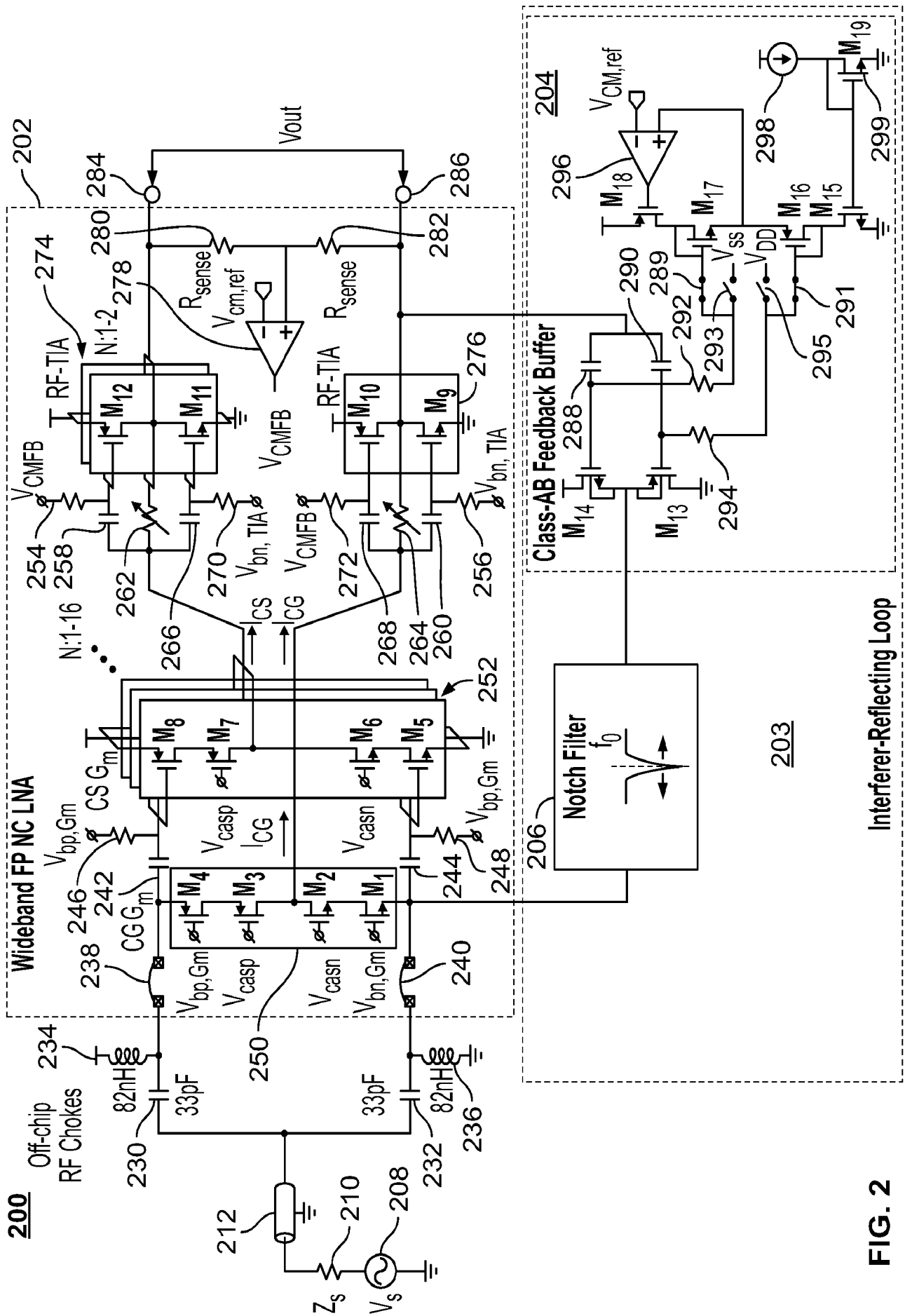


FIG. 2

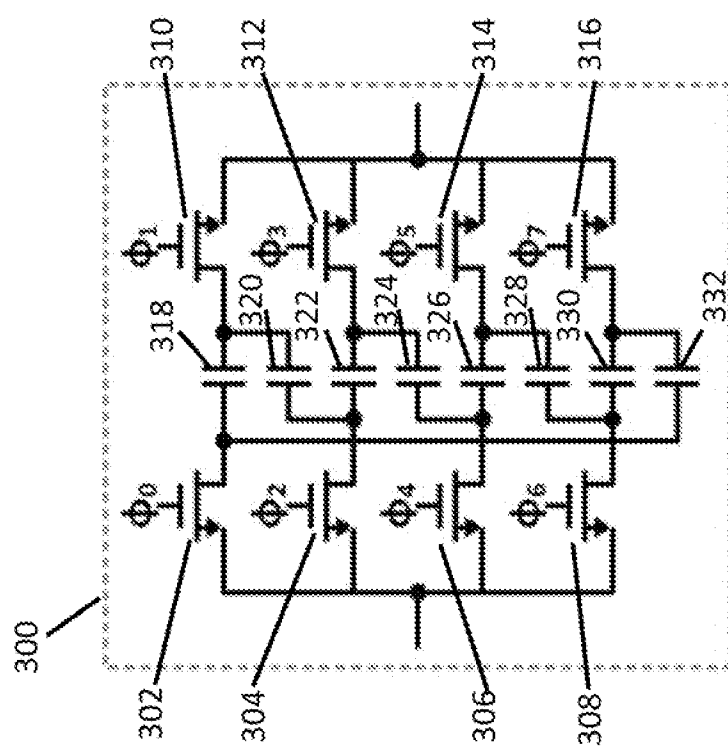


FIG. 3

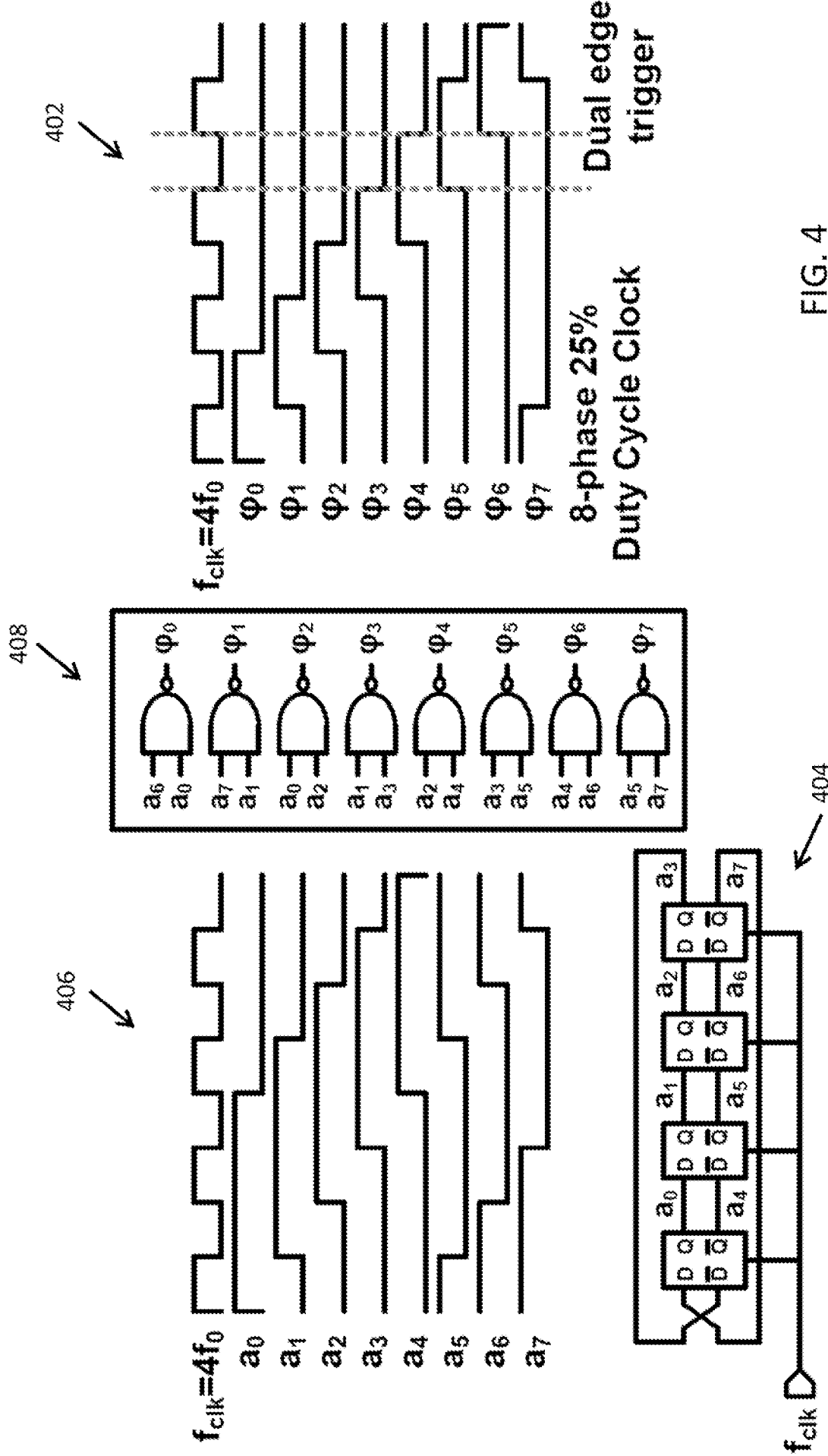


FIG. 4

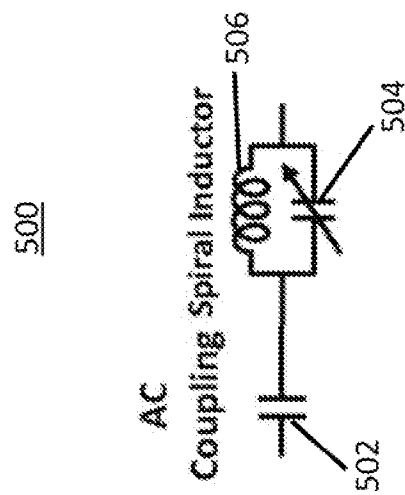


FIG. 5

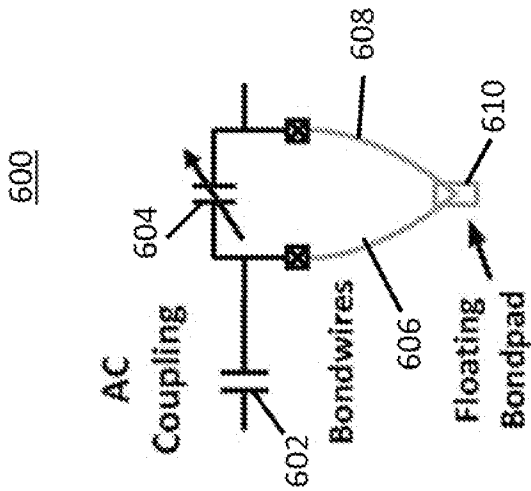


FIG. 6

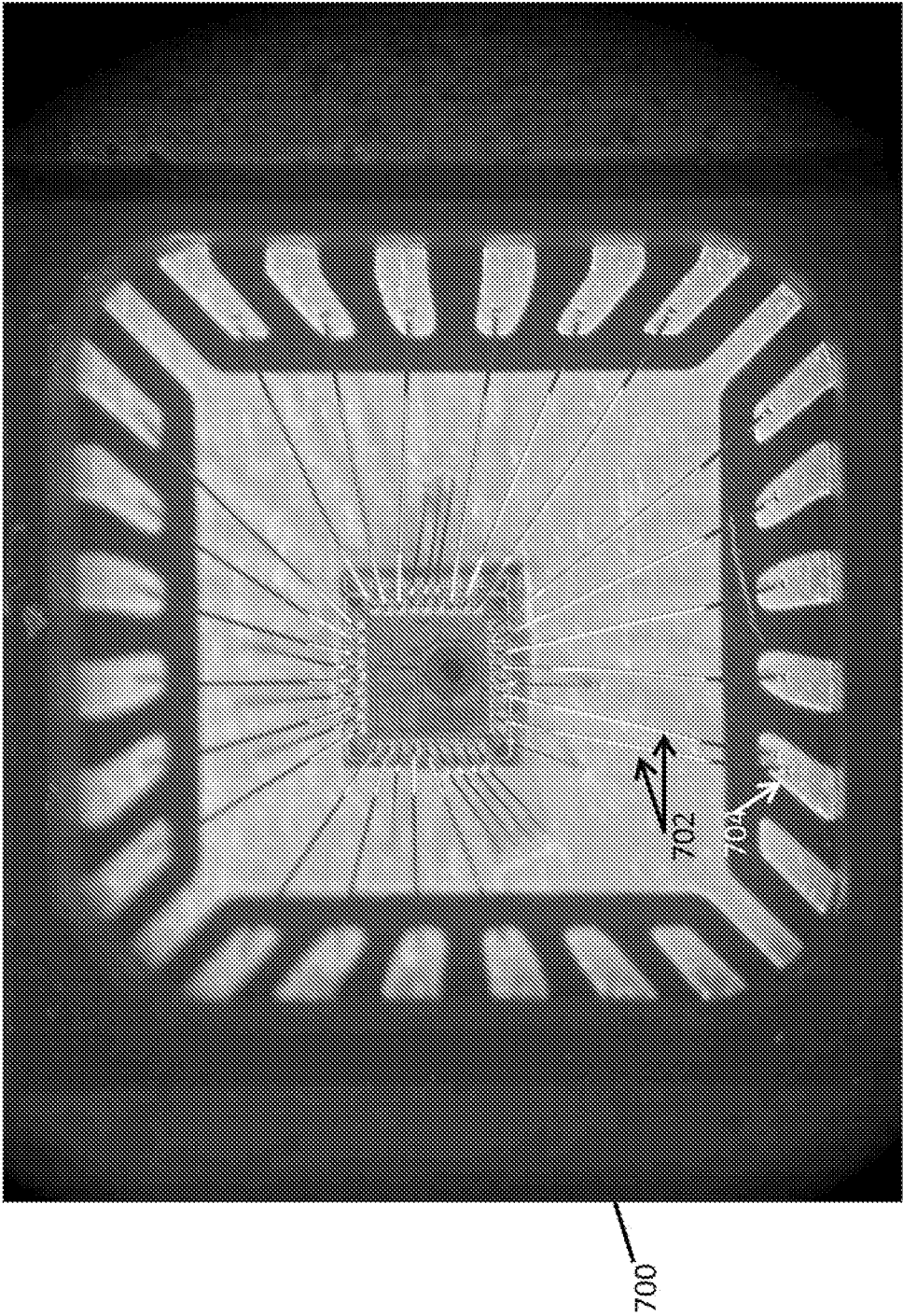


FIG. 7