(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 May 2018 (17.05.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/087264 A1

(51) International Patent Classification:
H04L 25/49 (2006.01) *H04B 10/516* (2013.01)
H04L 25/02 (2006.01)

(21) International Application Number:
PCT/EP2017/078825

(22) International Filing Date:
09 November 2017 (09.11.2017)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
16198754.0 14 November 2016 (14.11.2016) EP

(71) Applicant: **UNIVERSITEIT GENT** [BE/BE]; Sint-Pietersnieuwstraat 25, 9000 Gent (BE).

(72) Inventors: **PIERCO, Ramses**; Opvoedingstraat 28, 9000 Gent (BE). **VAERNEWYCK, Renato**; Krekelstraat 30, 9800 Deinze (BE). **DE KEULENAER, Timothy**; Ham 54, 9000 Gent (BE). **VYNCKE, Arno**; Moriaanstraat 23, 9050 Ledeberg (BE).

(74) Agent: **VAES, Peter** et al.; Leuvensesteenweg 203, 3190 Boortmeerbeek (BE).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

Published:
— *with international search report (Art. 21(3))*

(54) Title: DUO-BINARY ENCODING SYSTEM AND METHOD

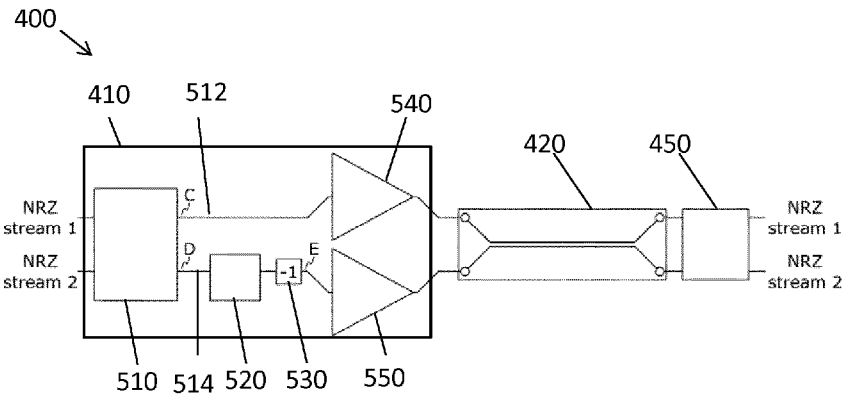

FIG. 5

(57) Abstract: A method (300) for obtaining a duo-binary signal. The method (300) comprises a first step (310) wherein a first NRZ signal and a second NRZ signal are sampled. The first NRZ signal should be synchronised with the second NRZ signal. The method (300) comprises a second step (320) for deriving a first output signal from the first NRZ signal and a second output signal from the second NRZ signal. For deriving the second output signal, the second NRZ signal is delayed over part of a bit period with regard to the first NRZ signal. The method comprises a third step (330) for differentially combining the first output signal with the second output signal such that the duo-binary signal is obtained.

WO 2018/087264 A1

Duo-binary encoding system and method.

Field of the invention

The invention relates to the field of transmission systems. More specifically it relates to the field of transmission systems using duo-binary signals.

Background of the invention

In prior art systems a high-bitrate duo-binary signal is typically generated by using a multiplexer to combine lower rate non-return-to-zero (NRZ) signals into a high-bitrate NRZ signal which is then transformed to a duo-binary signal. These duo-binary signals are in many cases used for high-speed communication across a differential electrical link (e.g. twin-axial cables in datacenters). Both the design of the multiplexer and of the encoder is troublesome at high bitrates.

Examples of such prior art communication systems are illustrated in FIG. 1 and FIG. 2. FIG. 1 schematically shows a prior art communication system 100 for transmitting a duo-binary signal across a differential electrical link 150. The system comprises a pre-coder 110 at half the bitrate, a 2:1 multiplexer 120, an NRZ to duo-binary encoder 130 and a differential driver 140 connected to a differential electrical link 150. At the opposite end of the differential electrical link a duo-binary receiver 160 is connected. The NRZ streams 1 and 2 applied at the inputs of the pre-coder 110 are reconstructed by the duo-binary receiver 160.

In FIG. 2 the prior art communication system 100 comprises a 2:1 multiplexer 120 followed by a pre-coder 110 at the full rate, an NRZ to duo-binary encoder 130 and a differential driver 140 connected to a differential electrical link 150. At the opposite end of the differential electrical link a duo-binary receiver 160 is connected. Also in this prior art communication system the NRZ streams 1 and 2 applied at the inputs of the pre-coder 110 are reconstructed by the duo-binary receiver 160.

Implementing a multiplexer and an NRZ to binary encoder for a communication system is challenging, especially at high bitrates. There is therefore room for improvement in communication systems and methods.

Summary of the invention

It is an object of embodiments of the present invention to provide methods and systems supporting the generation of duo-binary signals.

The above objective is accomplished by a method and device according to the present invention.

In a first aspect embodiments of the present invention relate to a method for obtaining a duo-binary signal on an electrical communication link comprising a first and a second input terminal. The method comprises:

- a first step wherein a first NRZ signal and a second NRZ signal are sampled and wherein the first NRZ signal is synchronised with the second NRZ signal,

- a second step (320) wherein a first output signal is derived from the first NRZ signal and a second output signal is derived from the second NRZ signal, wherein, for deriving the second output signal, the second NRZ signal is delayed over part of a bit period with regard to the first NRZ signal,

- a third step (330) wherein the first output signal is differentially combined with the second output signal such that the duo-binary signal is obtained. This is achieved by applying the first output signal to the first input terminal of the communication link and by applying the second output signal to the second input terminal of the communication link such that the duo-binary signal can be obtained at output terminals of the electrical communication link.

In embodiments of the present invention the duo-binary signal can be obtained by differentially monitoring the output terminals (a first and a second output terminal) of the communication link.

In embodiments of the present invention the communication link is a differential transmission line. In prior art systems information is transmitted over such a transmission line by applying a differential pair of input signals to the input terminals of the transmission line. This as opposed to embodiments of the present invention wherein the second NRZ signal is delayed over part of a bit period with

regard to the first NRZ signal and wherein these signals are applied to the input terminals of the transmission line. The advantage thereof is that the combination of these signals results in a duo-binary signal at the output terminals of the transmission line.

In embodiments of the present invention the communication link is a differential communication link. The communication link can for example be a twisted pair, a twinax, a differential transmission line, etc. It is an advantage of embodiments of the present invention that no multiplexer and dedicated encoder are required to generate the duo-binary signal. It is an advantage of embodiments of the present invention that these two functions can be realised by delaying the second NRZ signal over part of a bit period and by differentially combining both signals into a duo-binary signal. It is therefore an advantage of embodiments of the present invention that no high-speed multiplexer and encoder are needed.

In embodiments of the present invention the method comprises a step wherein the first or the second NRZ signal is inverted when deriving the first or second output signal.

In case the second NRZ signal is inverted this may be done before or after the delaying of the second NRZ signal.

In embodiments of the present invention during the second step the first and second NRZ signal are pre-coded for deriving the first and second output signal.

It is an advantage of embodiments of the present invention that pre-coding can be done at half the bitrate of the resulting duo-binary signal.

In embodiments of the present invention the duo-binary signal is an electrical signal.

In embodiments of the present invention the first output signal is combined with the second output signal by applying them to the inputs of a differential electrical link.

In embodiments of the present invention the first output signal is driven by a first single ended driver and the second output signal is driven by a second single ended driver before they are applied to the inputs of the differential electrical link.

In embodiments of the present invention the first output signal and the second output signal are driven by a differential driver before they are applied to the inputs of the differential electrical link.

In a second aspect embodiments of the present invention relate to a communication system. The communication system comprises a transmitter chip and an electrical communication link. The transmitter chip is adapted for receiving a first NRZ signal and a second NRZ signal, synchronous with the first NRZ signal, and for deriving a first output signal from the first NRZ signal and a second output signal from the second NRZ signal, wherein for deriving the second output signal the transmitter chip is adapted for delaying the second NRZ signal with part of a bit period with regard to the first NRZ signal, and wherein the communication system is configured such that the first output signal and the second output signal are differentially combined on the electrical communication link such that a duo-binary signal can be obtained.

In embodiments of the present invention the communication system is configured such that the first output signal is applied to the first terminal of the communication link and the second output signal is applied to the second terminal of the communication link such that the duo-binary signal can be obtained at output terminals of the communication link. In embodiments of the present invention the communication link is a differential communication link.

In embodiments of the present invention the signals on chip are only NRZ signals. No duo-binary signals are required on chip. This is possible because the NRZ signals are applied to the communication link such that the duo-binary signal is inherently created in the communication link. The fact that the signals on the transmitter chip are only NRZ signals allows a very efficient implementation of the

chip with CMOS blocks. For example inverters can be used which are more efficient and/or faster than components which have to generate a 3-level output signal. If the duo-binary signal would be made on-chip by adding a differential amplifier the power consumption would be higher than in a transmitter chip according to embodiments of the present invention.

It is an advantage of embodiments of the present invention that a duo-binary signal can be achieved by differentially combining a first output signal and a second output signal wherein the first output signal is derived from a first NRZ signal and the second output signal is derived from a second NRZ signal. For obtaining the second output signal at least one operation is performed on the second NRZ signal, i.e. delaying the second NRZ signal over part of a bit period. It is an advantage of embodiments of the present invention that no multiplexer or a dedicated encoder are required to obtain the duo-binary signal. It is moreover an advantage of embodiments of the present invention that the highest NRZ rate that needs to be processed at the transmitter chip is half this of conventional duo-binary transmitters. It is an advantage of embodiments of the present invention that by differentially combining the first NRZ signal and the second delayed NRZ signal on the communication link it is possible to obtain a duo-binary signal.

In embodiments of the present invention the transmitter chip is adapted for inverting the first or the second NRZ signal.

It is an advantage of embodiments of the present invention the desired duo-binary signal can be achieved using a transmitter chip adapted for inverting the first or the second NRZ signal in accordance with embodiments of the present invention.

In embodiments of the present invention the transmitter chip is adapted for pre-coding the first and the second NRZ-signal.

In embodiments of the present invention the communication link is an electrical link.

In embodiments of the present invention the communication system comprises a first and a second single ended driver connected between the transmitter chip and the communication link and adapted for driving the first NRZ signal and the delayed second NRZ signal.

It is an advantage of embodiments of the present invention that single-ended drivers are used for the input of the differential electrical link which makes it ideal for implementation in certain chip processes (e.g. CMOS).

Particular and preferred aspects of the invention are set out in the accompanying independent and dependent claims. Features from the dependent claims may be combined with features of the independent claims and with features of other dependent claims as appropriate and not merely as explicitly set out in the claims.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter.

Brief description of the drawings

FIG. 1 schematically shows a prior art communication system for transmitting a duo-binary signal across a differential electrical link.

FIG. 2 schematically shows a prior art communication system with a pre-coder adapted for operating at the full rate.

FIG. 3 schematically shows different steps of a method in accordance with embodiments of the present invention.

FIG. 4 is a schematic drawing of a communication system in accordance with embodiments of the present invention.

FIG. 5 is a schematic drawing of a communication system in accordance with embodiments of the present invention. This figure shows a possible implementation of a transmitter chip in accordance with embodiments of the present invention.

FIG. 6 shows exemplary signals as they may occur in a prior art communication system as illustrated in FIG. 1.

FIG. 7 shows exemplary signals as they may occur in a communication system in accordance with embodiments of the present invention

Any reference signs in the claims shall not be construed as limiting the scope. In the different drawings, the same reference signs refer to the same or analogous elements.

Detailed description of illustrative embodiments

The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes. The dimensions and the relative dimensions do not correspond to actual reductions to practice of the invention.

The terms first, second and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for describing a sequence, either temporally, spatially, in ranking or in any other manner. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein.

It is to be noticed that the term “comprising”, used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It is thus to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression “a device comprising means A and B” should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment, but may. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner, as would be apparent to one of ordinary skill in the art from this disclosure, in one or more embodiments.

Similarly it should be appreciated that in the description of exemplary embodiments of the invention, various features of the invention are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description, with each claim standing on its own as a separate embodiment of this invention.

Furthermore, while some embodiments described herein include some but not other features included in other embodiments, combinations of features of different embodiments are meant to be within the scope of the invention, and form different embodiments, as would be understood by those in the art. For example, in the following claims, any of the claimed embodiments can be used in any combination.

In the description provided herein, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known methods, structures and

techniques have not been shown in detail in order not to obscure an understanding of this description.

In a first aspect embodiments of the present invention relate to a method for obtaining a duo-binary signal, starting from a first and a second NRZ signal. The first and second NRZ signal are synchronized signals. In embodiments according to the present invention the method 300 comprises a first step 310 wherein the first NRZ signal and the second NRZ signal are sampled. In embodiments according to the present invention from these obtained NRZ signals a first and a second output signal is derived in a second step 320. The first output signal may be the same as the first NRZ signal or the first NRZ signal may be processed to obtain the first output signal. For deriving the second output signal, at least the second NRZ signal is delayed over part of a bit period with regard to the first NRZ signal. The second NRZ signal may for example be delayed over half a bit period. In embodiments of the present invention it may be delayed over a part of a bit period which is between 35% and 65% of a bit period, or even between 40% and 60% of a bit period. In embodiments according to the present invention the method comprises a third step 330 wherein the first output signal and the second output signal are differentially combined to obtain the duo-binary signal by applying the first output signal to the first terminal of the communication link and by applying the second output signal to the second terminal of the communication link such that differentially the duo-binary signal can be obtained at output terminals of the electrical communication link. An example of such a method is illustrated in FIG. 3. This figure schematically shows the first step for taking the NRZ signals, the second step for delaying one NRZ signal and the third step for differentially combining the obtained output signals to obtain the duo-binary signal.

In embodiments according to the present invention the first or the second NRZ signal additionally is inverted in the second step.

In embodiments according to the present invention the first and second output signals are connected to single ended drivers. The outputs of these single ended drivers are generating the differential signal.

In a second aspect embodiments according to the present invention relate to a communication system 400. The communication system 400 comprises a transmitter chip 410 and an electrical communication link 420. The transmitter chip 410 is adapted for receiving a first NRZ signal and a second NRZ signal. The first NRZ signal 432 should be synchronous with the second NRZ signal 434. The transmitter chip 410 is adapted for deriving a first output signal 442 from the first NRZ signal 432 and a second output signal 444 from the second NRZ signal 434. Thereby the transmitter chip 410 is adapted for at least delaying the second NRZ signal 434 over part of a bit period (e.g half a bit period) with regard to the first NRZ signal. The communication system 400 is configured such that the first output signal and the second output signal are differentially combined on the electrical communication link 420 thereby obtaining a duo-binary signal.

In embodiments according to the present invention two different NRZ signals 432, 434 are applied to the two inputs of a transmitter chip 410. One of these two NRZ signals is delayed over part of a bit period (e.g. half a bit period) with respect to the other. In embodiments of the present invention one of these two is inverted. The obtained output signals 442, 444 are differentially combined to result in a duo-binary signal. It is an advantage of embodiments of the present invention that by doing so, a three level duo-binary signal can be obtained which is the same as the three level duo-binary signal which would be attained by multiplexing both NRZ streams and convert them to a duo-binary stream by using the function $1+z^{-1}$.

In embodiments according to the present invention the obtained output signals 442, 444 are applied to the inputs of a differential electrical link 420 in such a way that the resulting differential signal is a duo-binary signal.

It is an advantage of embodiments of the present invention that the multiplexing step and the conversion step from NRZ to DB are combined. It is an advantage of embodiments of the present invention that the same differential signal can be obtained without requiring a separate multiplexing and NRZ to DB step. By eliminating the MUX, the power consumption of the transmitter chip is reduced. Moreover, by eliminating the MUX, the design of the transmitter chip is simplified. It is moreover an advantage of embodiments of the present invention that no MUX needs to be implemented which needs to operate at the highest bitrate.

In embodiments according to the present invention a first NRZ stream is directly connected to one terminal of the electrical link 420 and the other NRZ stream is delayed before it is connected to the other terminal of the electrical or optical link 420. Possibly this signal is also inverted before it is connected to the other terminal. This can be done to achieve the desired differential signal. In embodiments according to the present invention the inversion may be done in a precoding step 510.

FIG. 4 is a schematic drawing of an exemplary embodiment of the present invention. It shows a transmitter chip 410 with two input terminals for a first and second NRZ signal 432, 434 and with two output terminals for a first and second output signal 442, 444. The two output terminals of the transmitter chip are connected with the communication link 420. The other side of the communication link is connected with a duo-binary receiver 450. This duo-binary receiver is adapted for converting the three level duo-binary signal at its input to a first and second NRZ signal.

A more detailed schematic drawing of a communication system 400 in accordance with embodiments of the present invention is illustrated in FIG. 5. The transmitter chip 410 in FIG. 5 comprises a pre-coder 510 of which a first output 512 is connected to a first single ended driver 540 and of which a second output 514 is connected to a delay block 520 adapted for delaying the second NRZ signal over half a bit period with regard to the first NRZ signal. In this exemplary embodiment of the present invention the delay block 520 is connected with an inverter block 530

adapted for inverting the signal. The output of the inverter block 530 is connected to a second single ended driver 550. The outputs of the single ended drivers are connected to the inputs of the differential electrical link 420. It is thereby an advantage of embodiments of the present invention that single ended drivers are used because these can be efficiently implemented in CMOS. In embodiments of the present invention a differential driver can be replaced by two single ended drivers.

The invention is not limited to the pre-coder 510 – delay block 520 – inverter 530 sequence. The blocks may be organized in a different sequence also.

The single-ended drivers 540, 550 in FIG. 5 can be omitted if the output of the previous blocks is strong enough. In this example an inverter 530 is positioned in the chain following the second output 514 of the pre-coder 510. It, however, could have been positioned at the first output 512 of the pre-coder. In this exemplary embodiment of the present invention single ended drivers 540, 550 are used. In other embodiments a differential driver may be used instead of two single-ended drivers.

FIG. 6 shows exemplary signals as they may occur in a prior art communication system as illustrated in FIG. 1. The top two signals in FIG. 6 are the NRZ signals at the output of the pre-coder 110. The third signal in FIG. 6 is the signal after the 2:1 multiplexer 120. The bottom signal in FIG. 6 shows the differential signal input of the waveguide 150.

FIG. 7 shows exemplary signals as they may occur in a communication system 400 in accordance with embodiments of the present invention (the communication system illustrated in FIG. 5). The top two signals in FIG. 7 are the NRZ signals at the output of the pre-coder 510. These signals are the same as those shown in FIG. 6. The third signal is the signal at the output of the inverter block 550. The bottom signal shows the differential signal at the input of the waveguide 420. As can be seen from these figures the differential signals at the input of the waveguide are the same in both figures.

These examples therefore illustrate that applying two NRZ signals of which one delayed with half a bit period and one inverted leads to the same differential signal as multiplexing these two NRZ signals and encoding these to a duo-binary signal.

5

Claims

1.- A method (300) for obtaining a duo-binary signal on an electrical communication link comprising a first and a second input terminal, the method (300) comprising:

- a first step (310) sampling a first NRZ signal and a second NRZ signal wherein the first NRZ signal is synchronised with the second NRZ signal,

- a second step (320) deriving a first output signal from the first NRZ signal and a second output signal from the second NRZ signal, wherein, for deriving the second output signal, the second NRZ signal is delayed over part of a bit period with regard to the first NRZ signal,

- a third step (330) differentially combining the first output signal with the second output signal by applying the first output signal to the first input terminal of the communication link and by applying the second output signal to the second input terminal of the communication link such that differentially the duo-binary signal can be obtained at output terminals of the electrical communication link.

2.- A method (300) according to claim 1 wherein the method (300) comprises a step wherein the first or the second NRZ signal is inverted when deriving the first or second output signal.

3.- A method (300) according to any of the previous claims, wherein during the second step the first and second NRZ signal are pre-coded for deriving the first and second output signal.

4.- A method (300) according to any of the previous claims wherein the first output signal is combined with the second output signal by applying them to the inputs of a differential electrical link.

5.- A method (300) according to claim 4 wherein the first output signal is driven by a first single ended driver and the second output signal is driven by a second single ended driver before they are applied to the inputs of the differential electrical link.

6.- A method (300) according to claim 4 wherein the first output signal and the second output signal are driven by a differential driver before they are applied to the inputs of the differential electrical link.

7.- A communication system (400), the communication system (400) comprising a transmitter chip (410) and an electrical communication link (420), wherein the transmitter chip (410) is adapted for receiving a first NRZ signal and a second NRZ signal, synchronous with the first NRZ signal, and for deriving a first output signal from the first NRZ signal and a second output signal from the second NRZ signal, wherein for deriving the second output signal the transmitter chip is adapted for delaying the second NRZ signal with part of a bit period with regard to the first NRZ signal, and wherein the communication system (400) is configured such that the first output signal and the second output signal are differentially combined on the electrical communication link (420) thereby obtaining a duo-binary signal.

8.- A communication system (400) according to claim 7, wherein the transmitter chip (410) is adapted for inverting the first or the second NRZ signal.

9.- A communication system (400) according to any of the claims 7 or 8, wherein the transmitter chip (410) is adapted for pre-coding the first and the second NRZ-signal.

10.- A communication system (400) according to any of the claims 7 to 9, the communication system (400) comprising a first (540) and a second (550) single ended driver connected between the transmitter chip and the communication link and adapted for driving the first NRZ signal and the delayed second NRZ signal.

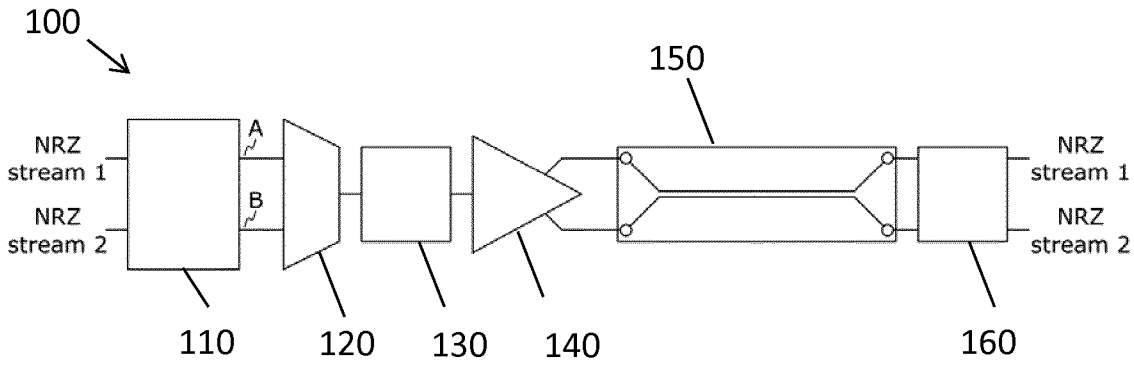

FIG. 1 (prior art)

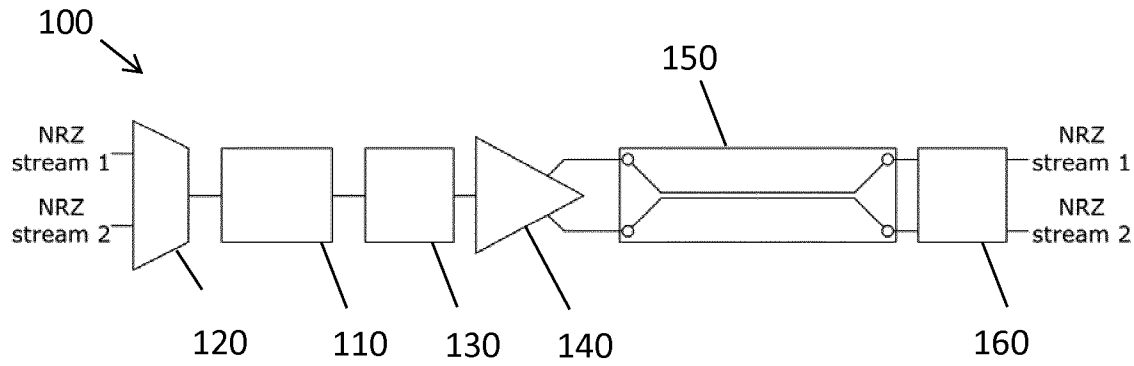

FIG. 2 (prior art)

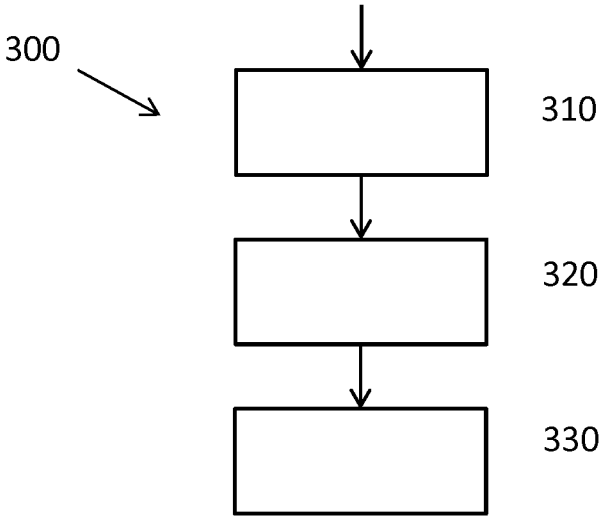

FIG. 3

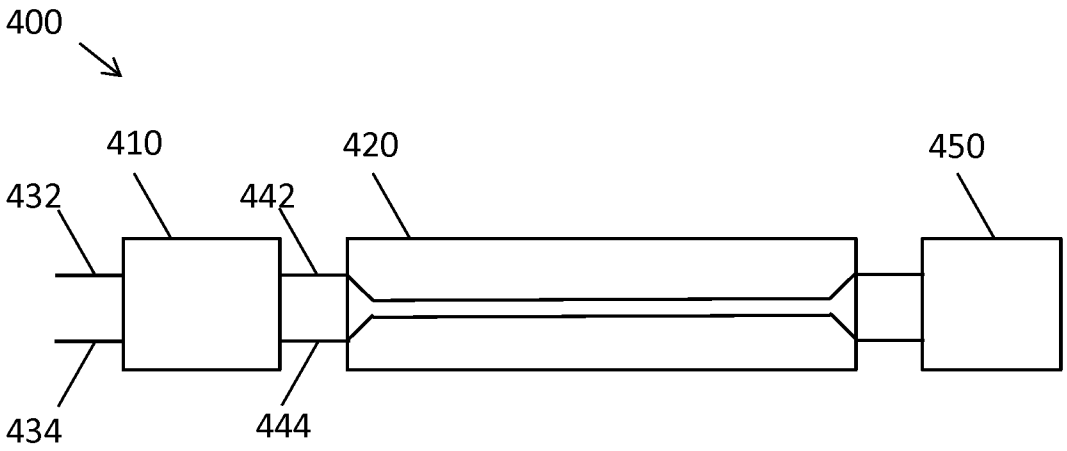

FIG. 4

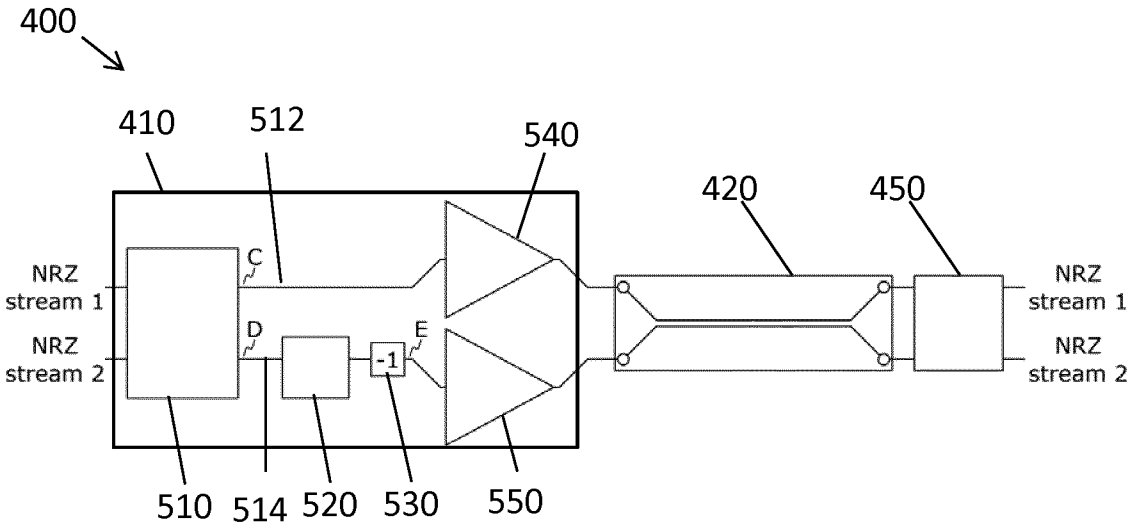

FIG. 5

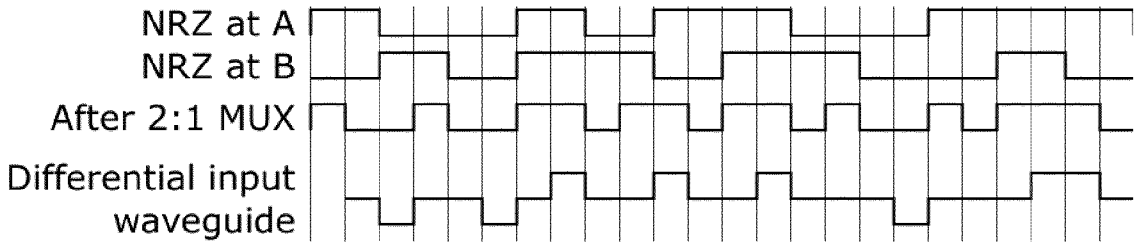

FIG. 6

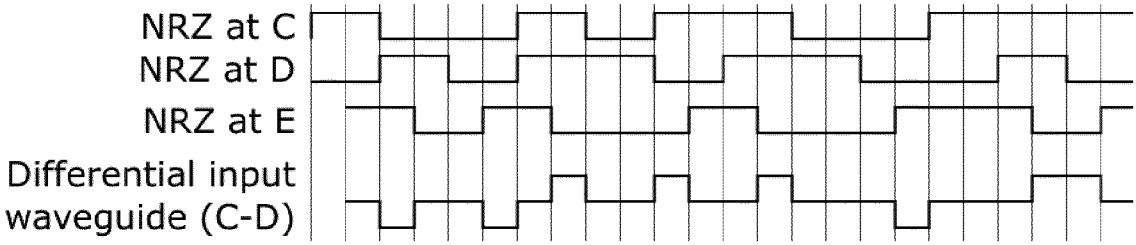

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/078825

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L25/49 H04L25/02 H04B10/516
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008/152355 A1 (NEILSON DAVID T [US]) 26 June 2008 (2008-06-26) abstract figures 2,3 paragraph [0004] paragraph [0006] paragraph [0008] paragraph [0018] paragraph [0022] - paragraph [0030] -----	1-10
A	GB 2 136 249 A (AMPEX) 12 September 1984 (1984-09-12) figure 1 page 1, line 9 - line 38 page 2, line 37 - line 51 page 2, line 64 - line 84 ----- -/--	1-10

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 January 2018	23/01/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Palacián Lisa, Marta

1

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2004/165893 A1 (WINZER PETER J [US]) 26 August 2004 (2004-08-26) abstract paragraph [0017] - paragraph [0020] paragraph [0024] - paragraph [0026] -----	1-10
A	TAWSIF HYDER: "Comparison between Duobinary Filter and Delay-And-Add Technique of Duobinary Transmission in Fiber Optic Communication System", IOSR JOURNAL OF ELECTRONICS AND COMMUNICATION ENGINEERING, vol. 9, no. 3, 1 May 2014 (2014-05-01), pages 71-81, XP055365661, ISSN: 2278-8735, DOI: 10.9790/2834-09327181 abstract I. Introduction 1.2.2 Optical Duobinary Signal from Binary Bit 1.2.3 Precoder, Duobinary Encoder and Decoder 1.2.4 Mach Zender Modulator figures 1.5, 1.9 -----	1-10

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2017/078825

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008152355 A1	26-06-2008	NONE	
GB 2136249 A	12-09-1984	DE 3404416 A1	09-08-1984
		FR 2540695 A1	10-08-1984
		GB 2136249 A	12-09-1984
		JP H0444454 B2	21-07-1992
		JP S59153357 A	01-09-1984
		US 4504872 A	12-03-1985
US 2004165893 A1	26-08-2004	NONE	