

[54] DIGITAL ELECTRONIC TIMEPIECE

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[58] Field of Search..... 58/23 R, 50 R; 235/92 T; 40/52, 130 R; 340/309.4, 309.5, 336; 307/38

[56] References Cited

UNITED STATES PATENTS

3,672,155	6/1972	Bergey et al.....	58/85.5 X
3,664,116	5/1972	Emerson et al.....	58/23 A
3,015,094	12/1961	Reynolds, Jr. et al.....	340/338
3,576,099	4/1971	Walton.....	58/23 R
3,540,209	11/1970	Zatsky et al.....	58/50 R
3,505,804	4/1970	Hofstein.....	58/23 BA
3,646,751	3/1972	Purland.....	58/152 R

OTHER PUBLICATIONS

EEE, Aug. 1968, p. 26.

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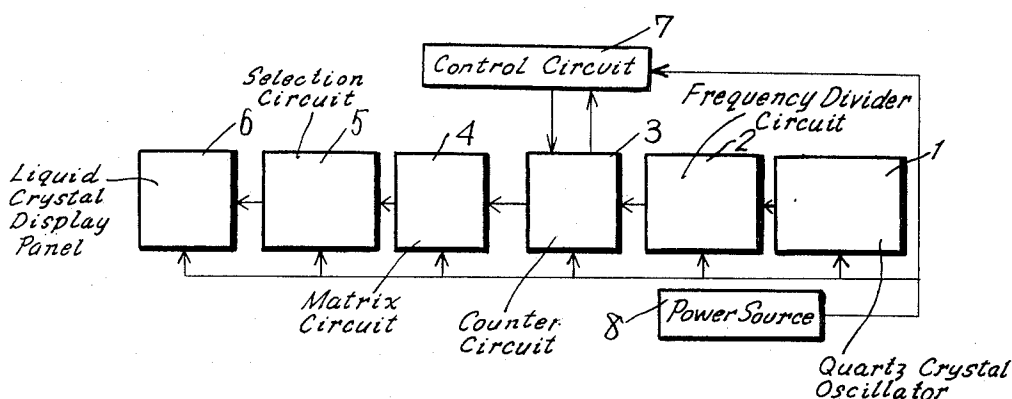
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[57]

ABSTRACT

A digital electronic timepiece wherein a fundamental frequency signal is divided into a pulse signal of 1 Hz corresponding to one second. Said pulse signal is applied to a plurality of cascade connected counters, corresponding to second, minute and hour, each of said counters being connected to a matrix circuit for converting the output binary code rows from the respective counters to binary code rows corresponding to segments of the time display device, the output of each of said matrix circuits being applied to a selection circuit for actuating selected segments of each unit of the time display device in response to the output binary code from the respective matrix circuit. The display device consists of a liquid crystal display panel having a plurality of time display units each of which is divided into a plurality of segments arranged so that respective combinations of each segments of each time display units represent all digits from 0 to 9.

8 Claims, 6 Drawing Figures



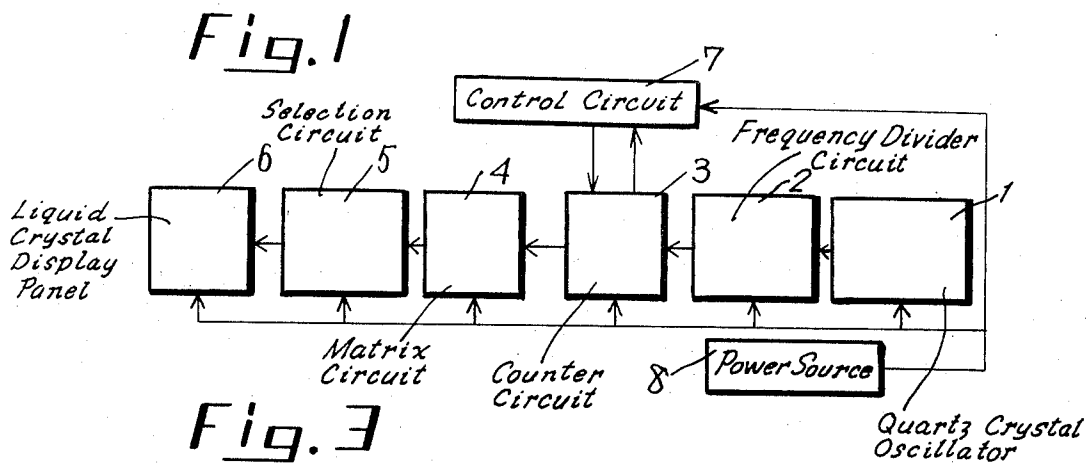


Fig. 3

Input Number of Counted Pulses	Output of the Decimal Counter				Output of the Sextuple Denotation Counter			Output of the Ternary Counter	
	D ₃₁	C ₃₁	B ₃₁	A ₃₁	C ₃₂	B ₃₂	A ₃₂	B ₃₆	A ₃₆
	D ₃₃	C ₃₃	B ₃₃	A ₃₃	C ₃₄	B ₃₄	A ₃₄		
	D ₃₅	C ₃₅	B ₃₅	A ₃₅					
0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	1	0	1
2	0	0	1	0	0	1	0	1	0
3	0	0	1	1	0	1	1		
4	0	1	0	0	1	0	0		
5	0	1	0	1	1	0	1		
6	0	1	1	0					
7	0	1	1	1					
8	1	0	0	0					
9	1	0	0						

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Fig. 2

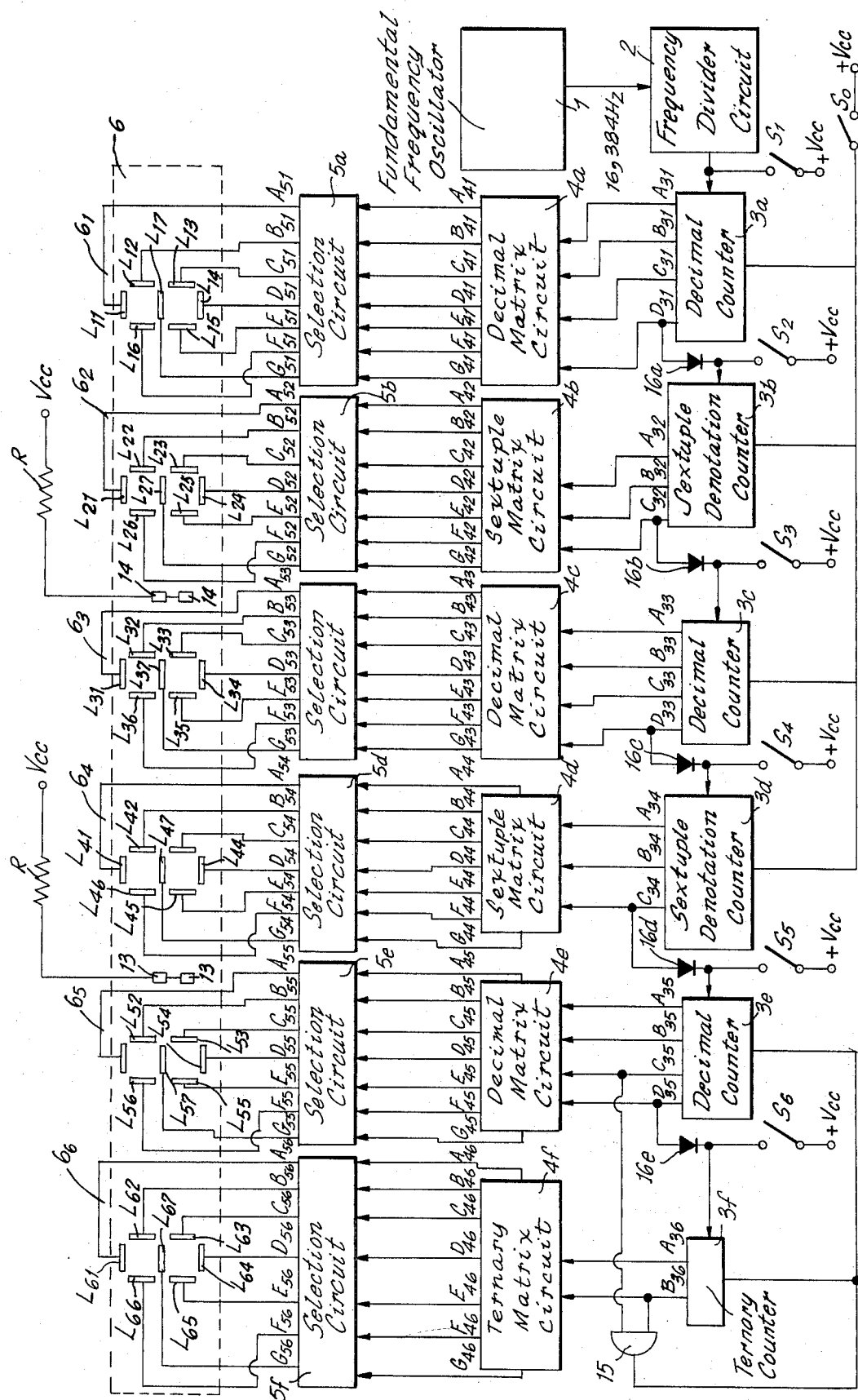


Fig. 4

NUMBER OF COUNTED PULSES	INPUT				OUTPUT OF THE DECIMAL MATRIX					OUTPUT OF THE SEXTUPLE DENOTATION MATRIX					OUTPUT OF THE TERNARY MATRIX						DISPLAY											
	D	C	B	A	G ₄₁ F ₄₁	E ₄₁ D ₄₁	C ₄₁ B ₄₁	A ₄₁	G ₄₂ F ₄₂	E ₄₂ D ₄₂	C ₄₂ B ₄₂	A ₄₂	G ₄₃ F ₄₃	E ₄₃ D ₄₃	C ₄₃ B ₄₃	A ₄₃	G ₄₄ F ₄₄	E ₄₄ D ₄₄	C ₄₄ B ₄₄	A ₄₄		G ₄₅ F ₄₅	E ₄₅ D ₄₅	C ₄₅ B ₄₅	A ₄₅	G ₄₆ F ₄₆	E ₄₆ D ₄₆	C ₄₆ B ₄₆	A ₄₆			
0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	
1	0	0	0	1	1	1	0	0	1	1	1	0	0	1	1	1	0	0	1	1	1	0	0	1	1	0	0	1	1	0	0	1
2	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0
3	0	0	1	1	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	0	0
4	0	1	0	0	0	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0
5	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0
6	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0 1 2 3 4 5 6 7 8 9

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Fig. 5

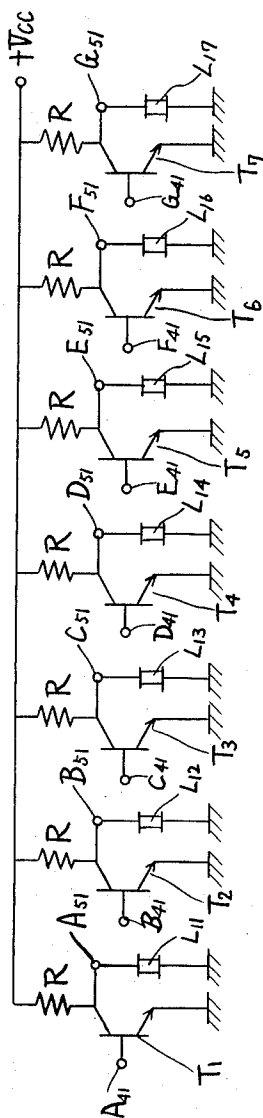
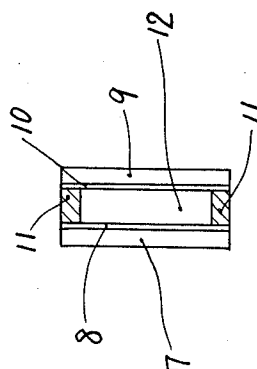


Fig. 6



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DIGITAL ELECTRONIC TIMEPIECE

BACKGROUND OF THE INVENTION

This invention relates to a digital electronic timepiece wherein time display is made in a digital system using a liquid crystal display panel.

In the prior art timepieces of this type, time display devices are used including a specific discharge tube in which digits 0 to 9 can be displayed by selectively turning on and off a red heat electrode in accordance with an input signal. But this discharge tube has drawbacks in that power consumption is generally great and the tube is not operable from an electric source of low voltage such as a battery. Since the tube is of a considerably great height and thickness, it is difficult to render it compact, so that it is not suitable for use in a wrist watch.

SUMMARY OF THE INVENTION

A digital electronic timepiece comprising a fundamental frequency oscillator for generating a predetermined fundamental frequency signal; a frequency divider for dividing the output signal from the oscillator and deriving a pulse signal of 1 Hz corresponding to one second; a plurality of counters disposed corresponding to second, minute and hour, and cascade connected, in turn, to the output terminal of the frequency divider for respectively counting the pulse signals applied from the frequency divider and simultaneously generating binary code rows varied in response to second, minute and hour, respectively; a liquid crystal display panel consisting of a plurality of time display units respectively disposed corresponding to each counter, each of said time display units being divided into a plurality of segments arranged so that respective combinations of said segments of each time display unit represents all digits from 0 to 9; a plurality of matrix circuits, one being connected to each of said counters, for receiving and converting the output binary code rows from each of said counters to the binary code rows corresponding to said segments of said time display units; and a plurality of selection circuits one being connected to each of said matrix circuits, for selectively imparting drive voltage to the segments of said time display units corresponding to the output binary codes from these respective matrix circuits.

Accordingly, an object of the invention is to provide a novel digital electronic timepiece utilizing a liquid crystal display which permits the display device to occupy a very small space and consume a very small quantity of electric power.

Still other objects and advantages of the invention will in part be obvious and will in part be apparent from the specification and drawings.

The invention accordingly comprises the features of construction, combinations of elements, and arrangement of parts which will be exemplified in the constructions hereinafter set forth, and the scope of the invention will be indicated in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a fuller understanding of the invention, reference is had to the following description taken in connection with the accompanying drawings, in which:

FIG. 1 is a general block diagram of a digital electronic timepiece illustrating an embodiment of the invention;

FIG. 2 is a full schematic and block diagram of the circuit of a digital electronic timepiece according to the invention;

FIG. 3 is a chart showing the corresponding relationship of the output binary code with respective counting numbers in the decimal counters, the sextuple denotation counters and the ternary denotation counter of FIG. 2;

FIG. 4 is a chart showing the corresponding relationship of time display digits on the respective time display units of the liquid crystal display panel of FIG. 2 with the respective input binary codes and output binary codes in the decimal matrix circuits, sextuple denotation matrix circuits and ternary denotation matrix circuit of FIG. 2;

FIG. 5 is a circuit diagram of an embodiment of any one selection circuit of FIG. 2 and associated time display unit in the liquid crystal display panel of FIG. 2; and

FIG. 6 is a cross sectional view showing an example of the respective time display units in the liquid crystal display panel according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 1, an outline of one embodiment of the digital electronic timepiece according to the invention is depicted wherein 1 indicates a fundamental frequency oscillator for generating precise fundamental frequency signals as later described using, for example, a quartz crystal oscillator. 2 indicates a frequency divider circuit for dividing fundamental frequency signals from the oscillator 1 and deriving pulse signals of 1 Hz corresponding to one second. 3 indicates a counter circuit for counting pulse signals from the frequency divider 2 to form second, minute and hour signals and simultaneously drawing out by converting these respective signals into binary code respectively varied in response to second, minute and hour. 4 indicates a matrix circuit for receiving the output binary code signals from the counter circuit and converting the same into the binary codes corresponding to the number of segments (7 segments in case of this embodiment) of the respective time display unit in the liquid crystal display panel as later described. 5 indicates a selection circuit selectively imparting drive voltage, in response to the output binary codes from the matrix circuit 4, to segments of the time display units in the liquid crystal display panel 6 which actually display time. 7 indicates a control circuit for making corrections in the time displayed, 24 reset and zero reset on the respective time display units in said liquid crystal display panel 6 as later described. 8 indicates a power source for operating each of the above-mentioned circuits.

FIG. 2 is a detailed view of the circuit construction of FIG. 1 wherein said fundamental frequency oscillator 1 has a quartz crystal vibrator having a natural frequency of, for example, 16,384 Hz. After having once converted the oscillating output signal from the quartz vibrator into a rectangular pulse through a waveform shaper (not shown), the oscillator continuously supplies the rectangular pulse of 16,384 Hz to the frequency divider circuit 2. The frequency divider circuit

consists of, for example, fourteen cascade connected flip-flop circuits and continuously generates pulse signals of $16,384/2^{14} \text{ Hz} = 1 \text{ Hz}$ corresponding to 1 second as an output signal. The output signal from the frequency divider circuit 2 is then supplied to the counter 3.

Since this timepiece provides a digital display of time consisting of two digits or places representative of each of the hour, minute and second, said counter circuit is constituted by six portions, namely, a decimal counter 3a for displaying the one second place, a sextuple denotation counter 3b for displaying the ten second place, a decimal counter 3c for the displaying 1 minute place, a sextuple denotation counter 3d for displaying the 10 minute place, a decimal counter 3e for displaying the 1 hour place and a ternary counter 3f for displaying the ten hour place. These counters 3a to 3f are so designed as to perform the counting operation by the fall off of the respective input pulses.

FIG. 3 is a view showing the corresponding relationship of output binary code with the respective number of counted pulses in said decimal counters 3a, 3c and 3e, sextuple counters 3b and 3d and ternary counter 3f. As will be apparent from FIG. 3, when the tenth pulse of 1 second has reached decimal counter 3a from said frequency divider, one pulse from the output terminal D₃₁ of the counter 3a is, at the time of the fall off of the 1 second pulse, sent to the next stage, i.e., the sextuple counter 3b. In this way, when the sixth pulse (corresponding to the sixtieth second) is added to the sextuple counter 3b, one pulse from the output terminal C₃₂ is sent to the next stage i.e., decimal counter 3c. Similarly, the output signal from the preceding counter is in turn sent to the succeeding counter and driven in the order of decimal counter 3c → sextuple counter 3d → decimal counter 3e → ternary counter 3f.

Matrix circuitry 4 consists of decimal matrix circuit 4a, sextuple matrix circuit 4b, decimal matrix circuit 4c, sextuple matrix circuit 4d, decimal matrix circuit 4e and ternary matrix circuit 4f. The respective matrix circuits 4a to 4f are each connected to the corresponding one of counters 3a to 3f. Each of the time display units 6₁, 6₂, 6₃, 6₄, 6₅, and 6₆ in the liquid crystal display panel 6 are respectively constituted by seven unit segments L₁₁–L₁₇, L₂₁–L₂₇, L₃₁–L₃₇, L₄₁–L₄₇, L₅₁–L₅₇ and L₆₁–L₆₇, the seven segments of each time display unit being combined with each other as a seven bar display defining the arabic numeral 8 as shown in FIG. 2. Accordingly, matrix circuits 4a and 4f are so constituted as to derive outputs A₄₁–A₄₆, B₄₁–B₄₆, C₄₁–C₄₆, D₄₁–D₄₆, E₄₁–E₄₆, F₄₁–F₄₆ and G₄₁–G₄₆, each group of seven outputs consisting of seven kinds of binary codes respectively corresponding to seven kinds of segments. The said seven output binary codes from each of matrix circuits 4a to 4f are applied to one of six selection circuits 5a, 5b, 5c, 5d, 5e and 5f. The seven kinds of output binary codes A₅₁–A₅₆, B₅₁–B₅₆, C₅₁–C₅₆, D₅₁–D₅₆, E₅₁–E₅₆, F₅₁–F₅₆ and G₅₁–G₅₆ from selection circuits 5a to 5f are applied to the corresponding segments L₁₁–L₆₁, L₁₂–L₆₂, L₁₃–L₆₃, L₁₄–L₆₄, L₁₅–L₆₅, L₁₆–L₆₆ and L₁₇–L₆₇ of time display units 6₁ to 6₆ in said liquid crystal display panel 6.

FIG. 4 is a chart showing the corresponding relationship of time display digit on the respective time display units 6₁ to 6₆ in liquid crystal display panel 6, with the respective input binary codes and the output binary codes in the decimal matrix circuits 3a, 3c and 3e,

sextuple matrix circuits 3b and 3d and ternary matrix circuit 3f of FIG. 2. FIG. 5 is a view showing an embodiment of the circuit of a selection circuit and time display unit of FIG. 2. In said embodiment, seven output binary codes A₄₁ to G₄₁ from matrix circuits 4a which correspond to the one second place are applied to the input terminal of the respective base of seven NPN type emitter grounded transistors T₁, T₂, T₃, T₄, T₅, T₆ and T₇ constituting selection circuit 5a. Load resistor R is respectively connected between the output terminal of the collector of these transistors and the terminal + V_{cc} of the power source. Seven respective unit segments L₁₁, L₁₂, L₁₃, L₁₄, L₁₅, L₁₆ and L₁₇ of time display unit 6₁ in said liquid crystal display panel 6 are connected between the output terminal of the collector of said transistors T₁ to T₇ and ground.

FIG. 6 is a cross sectional view showing an example of the respective time display units in said liquid crystal display panel, in which a transparent front glass panel 7 and a back glass panel 9 are positioned and spaced a fixed distance apart from each other, a transparent electrode 8 is deposited to the inner surface of the front glass panel 7 and nickel is deposited to the inner surface of the back glass panel 9. After liquid crystal 12 has been received in the space defined by the front and back glass panels 7 and 9 thus formed, the outer circumference is sealed airtight by means of spacers 11 made of suitable plastic materials. In this case, the nickel deposited on the inner surface of said back glass panel 9 is divided into seven segments positioned in said seven bar display to define arabic numeral 8, as described above. The liquid crystal display panel 6 is formed by the combination of six time display units 6₁ to 6₆ having the above mentioned construction. Lighting electrodes 13 and 14 having a square shape are preferably disposed in a portion of the display panel corresponding to the boundaries between the hour, minute and second digits as a marker for such boundaries as shown in FIG. 2. Power source V_{cc} is connected to these respective lighting electrodes 13 and 14 through respective resistors R.

The operation of the digital electronic timepiece of the present invention having the above-mentioned construction is as follows. Suppose that six pulses are supplied to the decimal counter 3a from said frequency divider 2, then the content of the output binary code A₃₁, B₃₁, C₃₁, D₃₁ is 0,1,1,0 and binary codes A₄₁, B₄₁, C₄₁, D₄₁, E₄₁, F₄₁, G₄₁ of the decimal matrix circuit 4a are 0,1,0,0,0,0 (see FIG. 4). Accordingly, inputs are applied to only transistor T₂ of the selection circuit and not applied to the other transistors, so that only transistor T₂ becomes "on." That is to say, since the collector-emitter voltage of the transistor T₂ becomes approximately zero, voltage is not applied to the segment L₁₂ of the liquid crystal display panel. Further, since input signals are not supplied to the other transistors, each transistor becomes "off" and the collector voltage of each transistor is in accord with the power source voltage, so that voltage is applied to the segments L₁₁, L₁₃, L₁₄, L₁₅, L₁₆ and L₁₇ and thus arabic numeral 6 is displayed by the electric field effect on the nematic liquid crystals 6. When decimal counter 3a counts ten pulses, one pulse is sent to a sextuple counter 3b. When the sextuple counter 3b counts six pulses, one pulse is sent to decimal counter 3c. Similarly, sextuple counter 3d, decimal counter 3e and ternary counter 3f in turn oper-

ate to produce a digital display of hour, minute and second.

An and-gate 15 is provided for displaying zero hour, zero minute and zero second after having displayed 23 hours, 59 minutes and 59 seconds. Namely, at the time of 23 hours and 59 minutes, the output C_{35} of decimal counter 3e is zero and the output B_{36} of ternary counter 3b is 1. The output C_{35} of decimal counter 3e becomes 1 by the next pulse and the output B_{36} of ternary counter 3b remains at 1. Accordingly, the output of and-gate 15 becomes 1 and decimal counter 3e and ternary counter 3b are returned to zero, so that zero hour, zero minute and zero second is displayed instead of 24 hours, zero minute and zero second.

S_0 indicates a switch for correcting the indication error of the watch and the input of each counter is connected to the power source $+V_{cc}$ through this switch. When the switch S_0 is closed at a certain correct time in response to, for example, the radio announcement of the time, voltage is applied to the reset terminal of each counter, and sextuple counter 3d, decimal counter 3c, sextuple counter 3b and decimal counter 3a are respectively reset at one time, and thus zero minute and zero second are displayed. Further, switches S_1 to S_6 are provided for the purpose of optionally correcting the display of hour, minute and second. When the switch corresponding to the optional time display unit is operated, the display on the time display unit is advanced by one increment upon each operation and thus correction can be made. Diodes 16a, 16b, 16c, 16d and 16e operate as a buffer for preventing the supply of signals to the preceding matrix circuit at the time of the operation of switches S_1 to S_6 .

The use of a liquid crystal display panel results in small power consumption while permitting digital display, and since a low voltage is used for operation of the circuit, the display can operate continuously for a long time although powered by a battery.

Accordingly, lines for the connection of a power source becomes unnecessary, so that, the device may be conveniently moved. Further, the use of the liquid crystal display panel makes the thickness of the display unit itself, and accordingly of the timepiece, very thin, so that the timepiece can be made compact. Further, the display is very visible in lighted places exposed to the direct rays of the sun. Further, since a liquid crystal display panel is used, the flexibility of design of the display panel is increased. Thus, various effects are obtained.

It will thus be seen that the objects set forth above, and those made apparent from the preceding description, are efficiently attained and, since certain changes may be made in the above construction without departing from the spirit and scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

It is also to be understood that the following claims are intended to cover all of the generic and specific features of the invention herein described, and all statements of the scope of the invention which, as a matter of language, might be said to fall therebetween.

What is claimed is:

1. A digital electronic timepiece comprising a crystal oscillator means for generating a high frequency time standard signal; frequency divider means for dividing the output signal from said oscillator means and deriv-

ing a pulse signal of 1 Hz corresponding to one second; a plurality of counter means respectively corresponding to second, minute and hour, and cascade connected, in turn, to the output of the frequency divider means for respectively counting the pulse signals applied from the frequency divider means and simultaneously generating binary code rows varied in response to second, minute and hour, respectively; a liquid crystal display panel consisting of a plurality of time display units corresponding respectively to said counter means, each of said time display units being divided into a plurality of segments arranged so that respective combinations of said segments of such time display unit represent all digits from 0 to 9; a plurality of matrix circuit means, one being connected to each of said counter means for continuously, during the operation of said divider means, receiving and converting the output binary code rows from each of said counter means to the binary code rows corresponding to said segments of said time display units; a plurality of selection circuit means, one being connected to each of said matrix circuit means for continuously, during the operation of said divider means, selectively imparting a driving voltage to the segments of said time display units corresponding to the output binary codes from the respective matrix circuit means; a power source including battery means for driving said oscillator means, divider means, counter means, matrix circuit means, selection circuit means and liquid crystal display panel said selection circuit means including a plurality of transistor means each having an emitter to collector path and a base, each of said emitter to collector paths being connected between an output terminal and ground, the binary codes from said matrix circuit means being respectively individually applied to the base of one of said transistor means, and a load resistor connected between each output terminal and said power source, each segment of each time display unit in said liquid crystal display panel being connected between the output terminal of one of said transistor means and ground.

2. A digital electronic timepiece as described in claim 1, wherein said oscillator means includes therein at least one quartz crystal oscillating element generating a predetermined frequency signal, and means for forming the output frequency signal from the oscillating element into rectangular pulses.

3. A digital electronic timepiece as described in claim 1, wherein said frequency divider means includes a plurality of mutually cascade-connected flip-flop circuits.

4. A digital electronic timepiece as described in claim 1, wherein said plurality of counter means consist of six counters for counting the one second place, ten second place, one minute place, ten minute place, one hour place and ten hour place, said counters being cascade connected one counter with another in turn.

5. A digital electronic timepiece as described in claim 1, wherein said liquid crystal display panel includes six time display units each of said time display units including a pair spaced transparent glass panels, a transparent electrode deposited on the inner surface of one of said pair of transparent glass panels, a segmented electrode deposited on the inner surface of the other glass panel and having a plurality of unit segments formed into an array adapted to selectively display the digits 0 to 9 when selected combinations of said segments are actuated, fluid crystal received between said pair of said

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glass panels, and means for air tight sealing of the outer circumference of the liquid crystal.

6. A digital electronic timepiece as described in claim 5, wherein said segmented electrode is formed of nickel.

7. A digital electronic timepiece as described in claim 5, wherein the array of said segmented electrode de-

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fines a seven-bar display defining the numeral 8.

8. A digital electronic timepiece as described in claim 1, including switch means, said counter means being provided with reset terminals through which said counter means can be optionally and selectively set to 0 by said switch means.

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