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(54) **INTEGRATION PROCESS OF TUNGSTEN ATOMIC LAYER DEPOSITION FOR METALLIZATION APPLICATION**

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(60) Provisional application No. 60/346,086, filed on Oct. 26, 2001.

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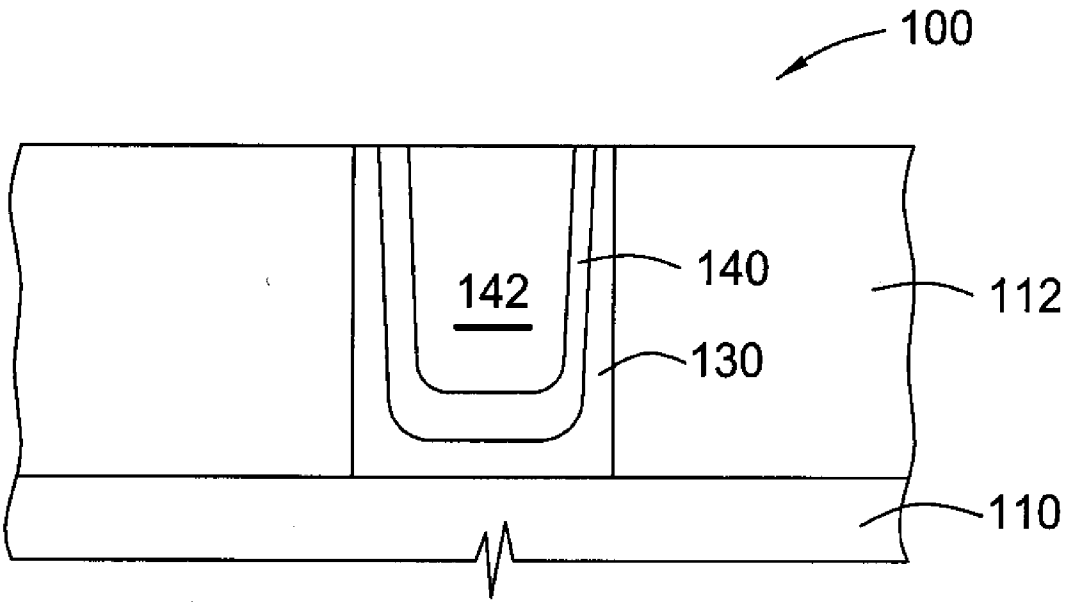
(57) **ABSTRACT**

In one embodiment, a method for forming a tungsten-containing material on a substrate is provided which includes positioning a substrate having an underlying tungsten layer within a process chamber and depositing a tungsten-containing barrier layer on the underlying tungsten layer during a cyclical layer deposition process. The tungsten-containing barrier layer contains a refractory metal nitride material. The method further provides depositing a seed layer on the tungsten-containing barrier layer during a vapor deposition process and depositing a bulk tungsten layer on the seed layer during a chemical vapor deposition process.



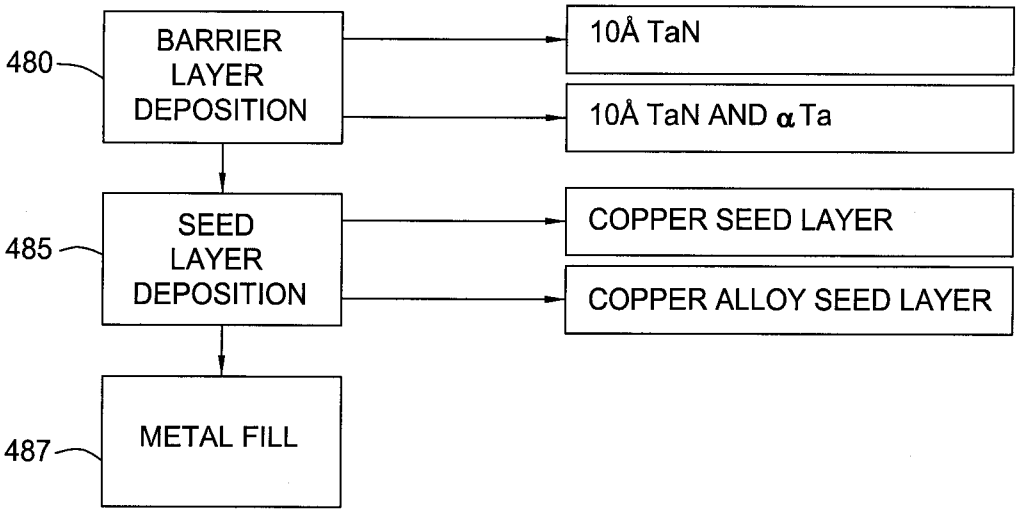

480
BARRIER LAYER DEPOSITION
10Å TaN
10Å TaN AND α Ta
485
SEED LAYER DEPOSITION
COPPER SEED LAYER
COPPER ALLOY SEED LAYER
487
METAL FILL

FIG. 1

FIG. 2A

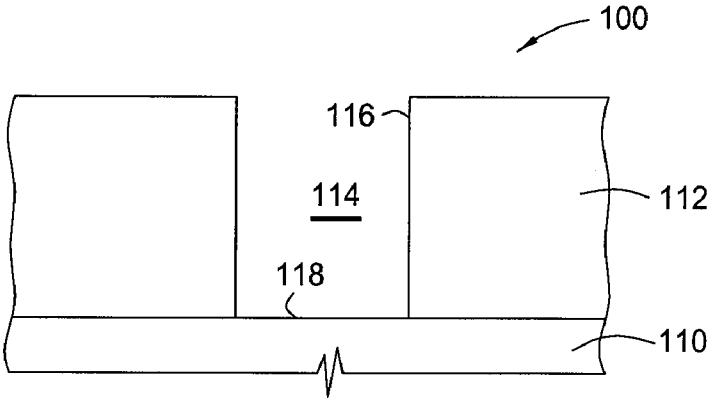


FIG. 2B

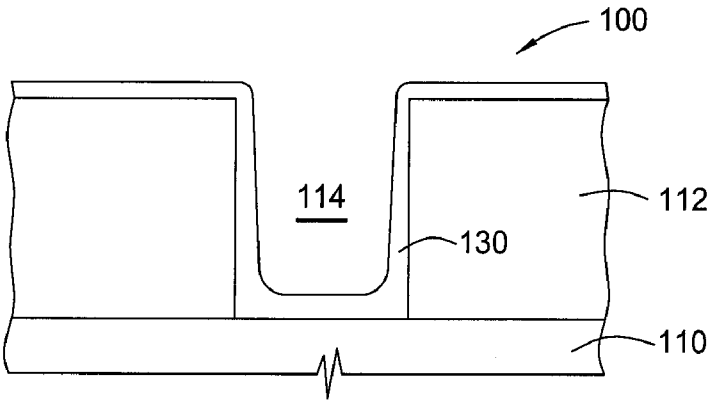


FIG. 2C

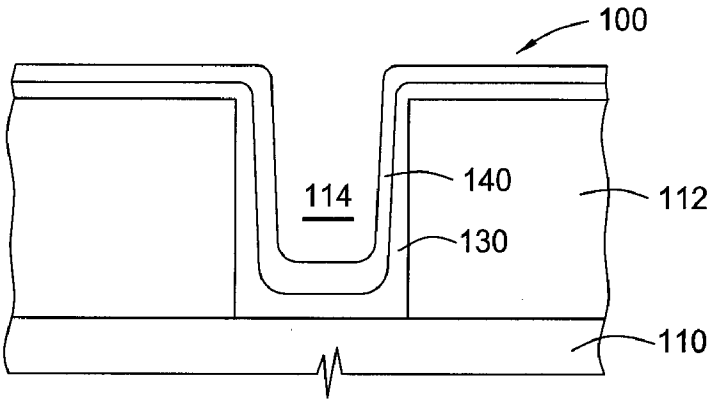
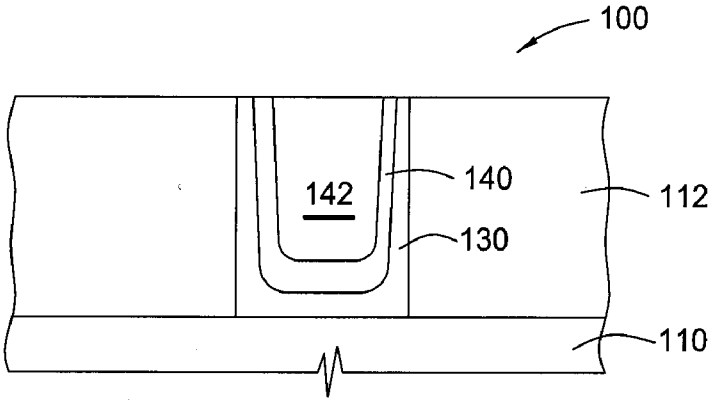


FIG. 2D



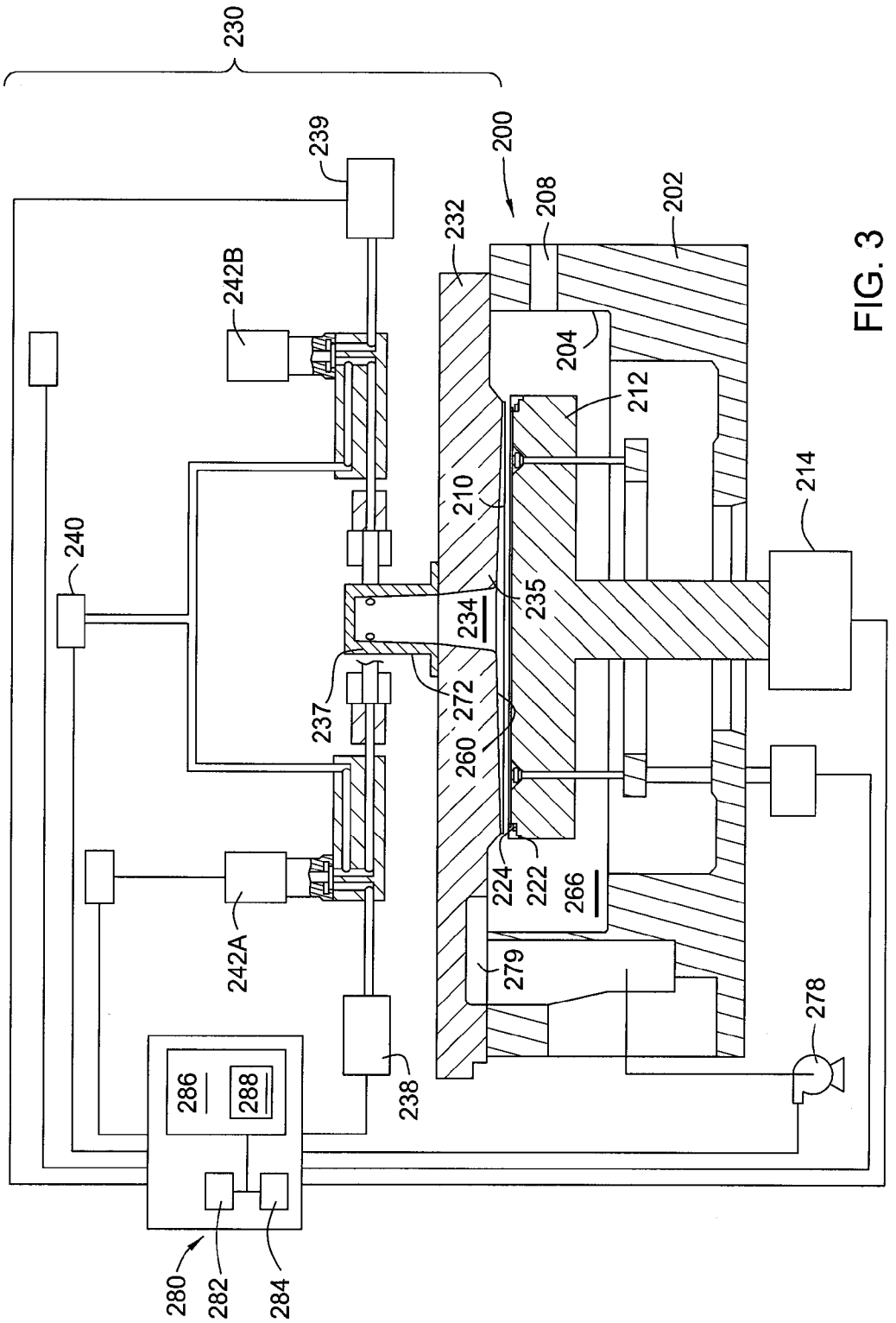

230
239
200
208
202
232
242B
204
212
214
210
240
234
235
237
272
260
224
222
266
242A
279
278
238
286
288
280
282
284

FIG. 3

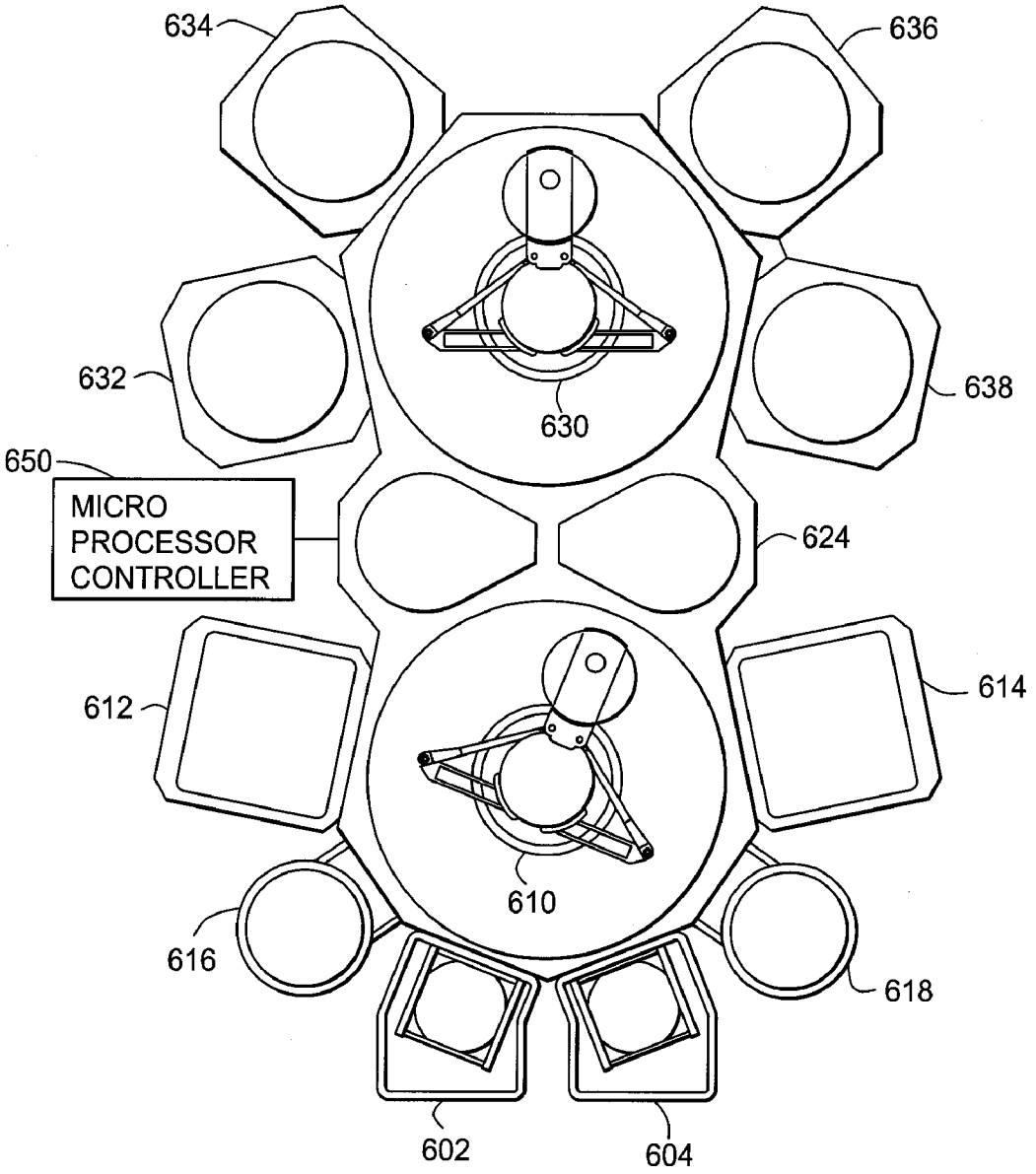

634
636
632
638
630
650
MICRO
PROCESSOR
CONTROLLER
624
612
614
610
616
618
602
604

FIG. 4

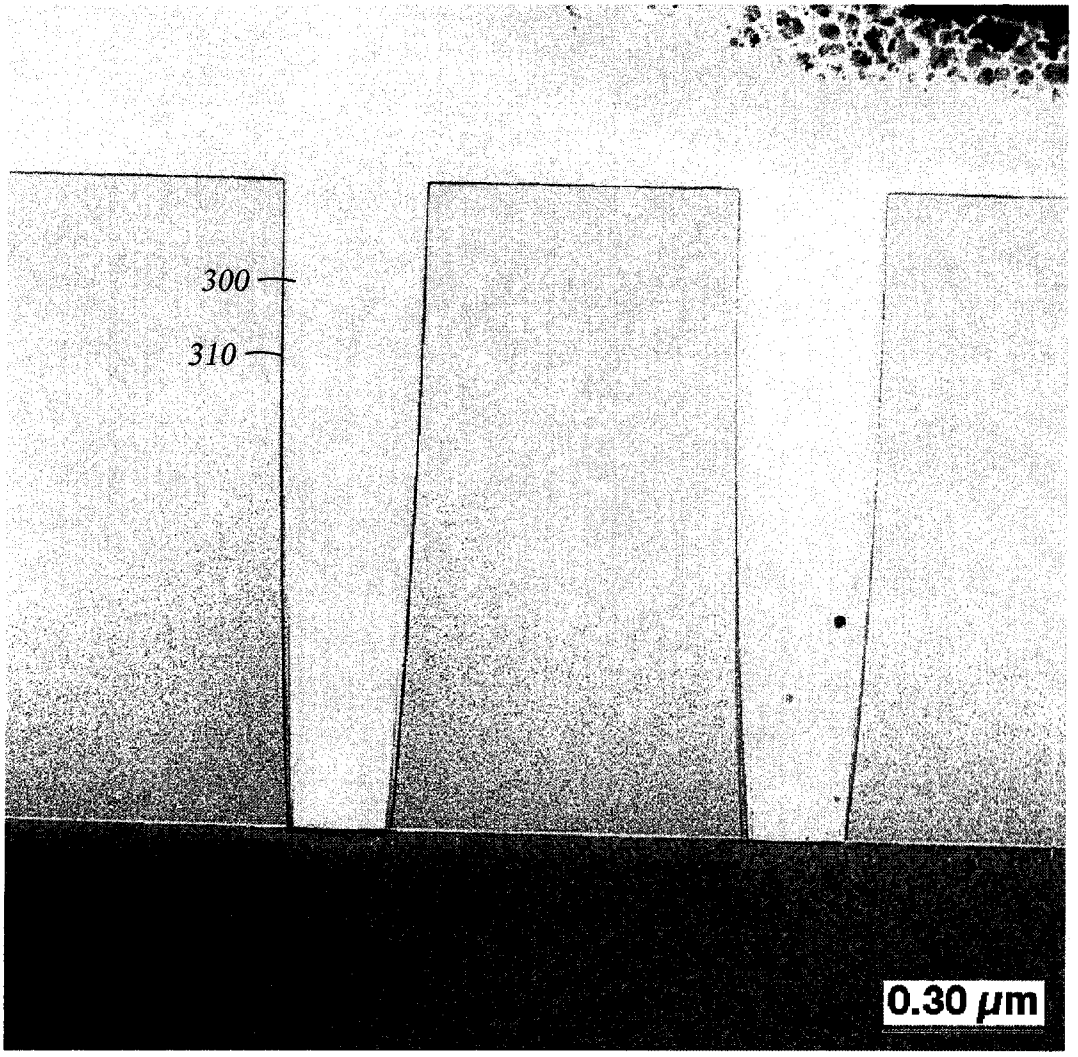


FIG. 5

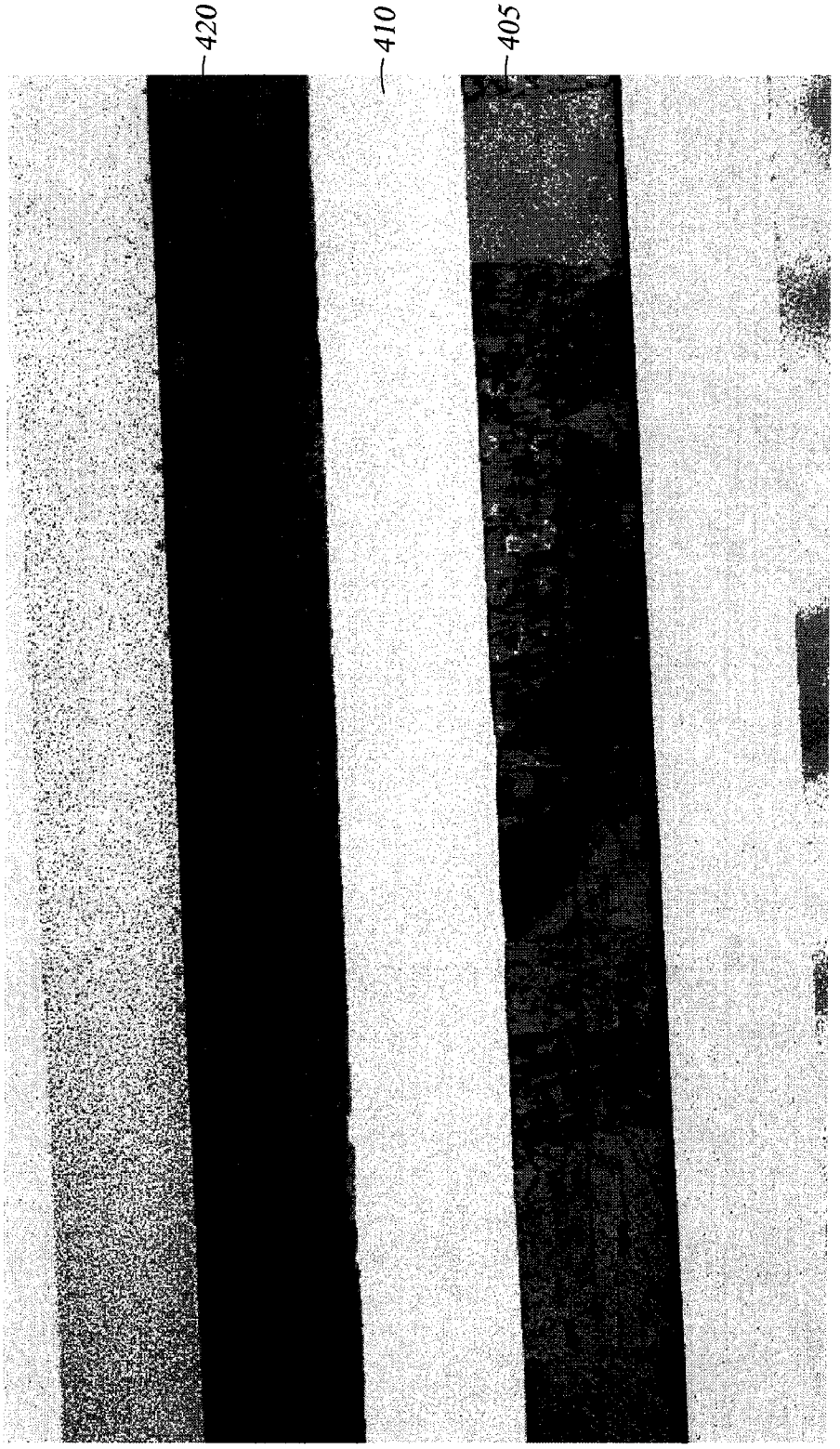


FIG. 6

INTEGRATION PROCESS OF TUNGSTEN ATOMIC LAYER DEPOSITION FOR METALLIZATION APPLICATION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of co-pending U.S. Ser. No. 10/281,386 (APPM/006303.P1), filed Oct. 25, 2002, which claims benefit of U.S. Ser. No. 60/346,086 (APPM/005192L), filed Oct. 26, 2001, which are both incorporated herein by reference in their entirety.

[0002] This application also claims benefit of U.S. Ser. No. 09/965,370 (APPM/006303), filed Sep. 26, 2001, U.S. Ser. No. 09/965,373 (APPM/006303.02), filed Sep. 26, 2001, and issued as U.S. Pat. No. 6,936,906, U.S. Ser. No. 09/965,369 (APPM/006303.03), filed Sep. 26, 2001, and now abandoned, U.S. Ser. No. 10/193,333 (APPM/006303.P2), filed Jul. 10, 2002, and U.S. Ser. No. 10/199,415 (APPM/005192.03), filed Jul. 18, 2002, and now abandoned, which are all incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

[0003] 1. Field of the Invention

[0004] Embodiments of the present invention relate to a method for manufacturing integrated circuit devices. More particularly, embodiments of the invention relate to forming metal interconnect structures using one or more cyclical deposition processes.

[0005] 2. Description of the Related Art

[0006] As the structure size of integrated circuit (IC) devices is scaled down to sub-quarter micron dimensions, electrical resistance and current densities have become an area for concern and improvement. Multilevel interconnect technology provides the conductive paths throughout an IC device, formed in high aspect ratio features, including contacts, plugs, vias, lines, wires, and other features. A typical process for forming an interconnect on a substrate includes depositing one or more layers, etching at least one of the layer(s) to form one or more features, depositing a barrier layer in the feature(s) and depositing one or more layers to fill the feature. Typically, a feature is formed within a dielectric material disposed between a lower conductive layer and an upper conductive layer. The interconnect is formed within the feature to link the upper and lower conductive layers. Reliable formation of these interconnect features is important to the production of the circuits and to continued effort to increase circuit density and quality on individual substrates and die.

[0007] Copper has recently become a choice metal for filling sub-micron high aspect ratio interconnect features because copper and its alloys have lower resistivities than aluminum. However, copper diffuses more readily into surrounding materials and can alter the electronic device characteristics of the adjacent layers and, for example, form a conductive path between layers, thereby reducing the reliability of the overall circuit and possibly resulting in device failure.

[0008] Barrier layers therefore, are deposited prior to copper metallization to prevent or impede the diffusion of copper atoms. Barrier layers typically contain a refractory metal such as tungsten, titanium, tantalum, and nitrides thereof, all of which have a greater resistivity than copper. To deposit a barrier layer within a feature, the barrier layer must be deposited on the bottom of the feature as well as the sidewalls thereof. Therefore, the additional amount of the barrier layer on the bottom of the feature not only increases the overall resistance of the feature, but also forms an obstruction between higher and lower metal interconnects of a multi-layered interconnect structure.

[0009] There is a need, therefore, for an improved method for forming metal interconnect structures which minimizes the electrical resistance of the interconnect.

SUMMARY OF THE INVENTION

[0010] A method for forming a metal interconnect on a substrate is provided. In one aspect, the method comprises depositing a refractory metal containing barrier layer having a thickness that exhibits a crystalline like structure and is sufficient to inhibit atomic migration on at least a portion of a metal layer. The interconnect is produced by alternately introducing one or more pulses of a metal-containing compound and one or more pulses of a nitrogen-containing compound, depositing a seed layer on at least a portion of the barrier layer, and depositing a second metal layer on at least a portion of the seed layer.

[0011] In another aspect, the method comprises depositing a first metal layer on a substrate surface; depositing a titanium silicon nitride layer having a thickness less than about 20 Å over at least a portion of the first metal layer by alternately introducing one or more pulses of a titanium-containing compound, one or more pulses of a silicon-containing compound, and one or more pulses of a nitrogen-containing compound; depositing a dual alloy seed layer, and depositing a second metal layer on at least a portion of the dual alloy seed layer.

[0012] In yet another aspect, the method comprises depositing a bilayer barrier having a thickness less than about 20 Å on at least a portion of a metal layer, depositing a dual alloy seed layer, and depositing a second metal layer on at least a portion of the dual alloy seed layer. The bilayer barrier comprises a first layer of tantalum nitride deposited by alternately introducing one or more pulses of a tantalum-containing compound and one or more pulses of a nitrogen-containing compound and a second layer of alpha phase tantalum.

[0013] In still yet another aspect, the method includes depositing a first metal layer on a substrate surface; depositing a tantalum nitride barrier layer having a thickness less than about 20 Å on at least a portion of the first metal layer by alternately introducing one or more pulses of a tantalum-containing compound and one or more pulses of a nitrogen-containing compound depositing a dual alloy seed layer comprising copper and a metal selected from the group consisting of aluminum, magnesium, titanium, zirconium, tin, and combinations thereof and depositing a second metal layer on at least a portion of the dual alloy seed layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] So that the manner in which the above recited features of the present invention are attained and can be

understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0015] FIG. **1** illustrates processing sequences according to various embodiments of the invention described herein.

[0016] FIGS. **2**A-**2**D are schematic cross section views of an exemplary wafer at different stages of an interconnect fabrication sequence according to embodiments described herein.

[0017] FIG. **3** illustrates a schematic, partial cross section of an exemplary processing chamber **200** for forming a thin barrier layer according to a cyclical deposition technique described herein.

[0018] FIG. **4** illustrates a schematic plan view of an exemplary integrated cluster tool adaptable to perform the interconnect fabrication sequence described herein.

[0019] FIG. **5** is a transmission electron microscope (TEM) image of a feature having a titanium nitride barrier layer deposited therein according to the deposition techniques described herein.

[0020] FIG. **6** is a TEM image showing a partial cross sectional view of a multi-level, interconnect structure.

DETAILED DESCRIPTION

[0021] A process sequence for forming one or more interconnect structures is provided. Interconnect structures formed according to embodiments described herein have an overall lower resistivity and better electrical properties than interconnects of the prior art, and are particularly useful for making memory and logic structures for use with the fabrication of integrated circuits. The formation of the interconnect structures includes the formation of a thin barrier layer at least partially deposited on an underlying metal layer, a seed layer at least partially deposited on the barrier layer, and a bulk metal layer at least partially deposited on the seed layer. The term "interconnect" as used herein refers to any conductive path formed within an integrated circuit. The term "bulk metal" as used herein refers to a greater amount of metal deposited in relation to other metals deposited to form the interconnect structure.

[0022] FIG. **1** illustrates the process sequence according to embodiments of the invention. A thin barrier layer is first deposited at least partially on an underlying substrate surface, such as a lower level metal interconnect or a metal gate, for example, as shown at step **480**. The barrier layer is deposited according to a cyclical layer deposition technique described herein. In one aspect, the barrier layer is a refractory metal-containing layer, such as tantalum, titanium, and tungsten, for example, and may include a refractory metal nitride material, such as tantalum nitride (TaN). In another aspect, the barrier layer is a thin bi-layer of TaN and alpha-phase tantalum. In yet another aspect, the barrier layer may be a ternary material formed from a refractory metal containing compound, a silicon-containing compound and a nitrogen-containing compound. The barrier layer may also act as a wetting layer, adhesion layer, or glue layer for subsequent metallization.

[0023] A "thin layer" as used herein refers to a layer of material deposited on a substrate surface having a thickness of about 20 Å or less, such as about 10 Å. The thickness of the barrier layer is so thin that electrons of the adjacent metal interconnect can tunnel through the barrier layer. Accordingly, the barrier layer significantly enhances the metal interconnect electrical performance by lowering the overall electrical resistance and providing good device reliability.

[0024] The thin barrier layer deposited according to the cyclical deposition methods described herein shows evidence of an epitaxial growth phenomenon. In other words, the barrier layer takes on the same or substantially the same crystallographic characteristics as the underlying layer. As a result, a substantially single crystal is grown such that there is no void formation at an interface between the barrier layer and the underlying layer. Likewise, subsequent metal layers deposited over the barrier layer exhibit the same or substantially the same epitaxial growth characteristics that continue the formation of the single crystal. Accordingly, no void formation is produced at this interface. The resulting structure resembling a single crystal eliminates voids formation, thereby substantially increasing device reliability. The single crystal structure also reduces the overall resistance of the interconnect feature while still providing excellent barrier properties. Furthermore, it is believed that the single crystalline growth reduces the susceptibility of electromigration and stress migration due to the conformal and uniform crystalline orientation across the interconnect material interfaces.

[0025] "Cyclical deposition" as used herein refers to the sequential introduction of two or more reactive compounds to deposit a mono layer of material on a substrate surface. The two or more reactive compounds are alternatively introduced into a reaction zone of a processing chamber. Each reactive compound is separated by a time delay to allow each compound to adhere and/or react on the substrate surface. In one aspect, a first precursor or compound A is pulsed into the reaction zone followed by a first time delay. Next, a second precursor or compound B is pulsed into the reaction zone followed by a second delay. When a ternary material is desired, such as titanium silicon nitride, for example, a third compound (C), is dosed/pulsed into the reaction zone followed by a third time delay. During each time delay an inert gas, such as argon, is introduced into the processing chamber to purge the reaction zone or otherwise remove any residual reactive compound from the reaction zone. Alternatively, the purge gas may flow continuously throughout the deposition process so that only the purge gas flows during the time delay between pulses of reactive compounds. The reactive compounds are alternatively pulsed until a desired film or film thickness is formed on the substrate surface.

[0026] A "substrate surface", as used herein, refers to any substrate surface upon which film processing is performed. For example, a substrate surface may include silicon, silicon oxide, doped silicon, germanium, gallium arsenide, glass, sapphire, and any other materials such as metals, metal nitrides, metal alloys, and other conductive materials,

depending on the application. A substrate surface may also include dielectric materials such as silicon dioxide and carbon doped silicon oxides.

[0027] A "pulse" or "dose" as used herein is intended to refer to a quantity of a particular compound that is intermittently or non-continuously introduced into a reaction zone of a processing chamber. The quantity of a particular compound within each pulse may vary over time, depending on the duration of the pulse. The duration of each pulse is variable depending upon a number of factors such as, for example, the volume capacity of the process chamber employed, the vacuum system coupled thereto, and the volatility/reactivity of the particular compound itself.

[0028] The term "compound" is intended to include one or more precursors, oxidants, reductants, reactants, and catalysts, or a combination thereof. The term "compound" is also intended to include a grouping of compounds, such as when two or more compounds are introduced in a processing system at the same time. For example, a grouping of compounds may include one or more catalysts and one or more precursors. The term "compound" is further intended to include one or more precursors, oxidants, reductants, reactants, and catalysts, or a combination thereof in an activated or otherwise energized state, such as by disassociation or ionization.

[0029] It is believed that the surface attraction used to physisorb, adsorb, absorb, or chemisorb a monolayer of reactants on a substrate surface are self-limiting in that only one monolayer may be deposited onto the substrate surface during a given pulse because the substrate surface has a finite number of sites available for the reactants. Once the finite number of sites is occupied by the reactants, further deposition of the reactants will be blocked. The cycle may be repeated to a desired thickness of the layer.

[0030] Still referring to FIG. **1**, a seed layer is at least partially deposited on the barrier layer, as shown at step **485**. The seed layer may be deposited using any conventional deposition technique, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), electroplating, or electroless plating. Preferably, the seed layer is deposited conformally on the underlying barrier layer to have a thickness between about 100 and about 500 Å. In one aspect, the seed layer is a conventional copper seed layer. In another aspect, the seed layer is a dual alloy seed layer. Exemplary dual alloy seed layers include: 1) undoped copper deposited utilizing a target containing undoped copper, 2) a copper alloy containing aluminum in a concentration of about 2.0 atomic percent deposited utilizing a copper-aluminum target comprising aluminum in a concentration of about 2.0 atomic percent, 3) a copper alloy containing tin in a concentration of about 2.0 atomic percent deposited utilizing a copper-tin target comprising tin in a concentration of about 2.0 atomic percent, and 4) a copper alloy containing zirconium in a concentration of about 2.0 atomic percent deposited utilizing a copper-zirconium target comprising zirconium in a concentration of about 2.0 atomic percent.

[0031] The bulk metal layer is at least partially deposited on the seed layer, as shown at step **487**. The metal layer may also be deposited using any conventional deposition technique, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), electroplating, or electroless plating. The metal layer preferably includes any conductive material such as aluminum, copper, tungsten, or combinations thereof, for example.

[0032] FIGS. **2**A-**2**D are schematic representations of an exemplary interconnect structure at different stages of fabrication. FIG. **2**A shows an underlying metal layer **110** having a dielectric layer **112** formed thereon. FIG. **2**B shows a barrier layer **130** at least partially deposited on the underlying metal layer **110**. The underlying metal layer **110** may contain any conductive metal such as aluminum, copper, tungsten, or combinations thereof, for example, and may form part of an interconnect feature such as a plug, via, contact, line, wire, and may also be part of a metal gate electrode. FIG. **2**C shows a seed layer **140** at least partially deposited on the barrier layer **130**, and FIG. **2**D shows a bulk metal layer **142** at least partially deposited on the seed layer **140**.

[0033] Referring to FIG. **2**A, the dielectric layer **112** may be any dielectric material including a low k dielectric material (k<4.0), whether presently known or yet to be discovered. For example, the dielectric layer **112** may be a silicon oxide or a carbon doped silicon oxide, for example. The dielectric layer **112** has been etched to form a feature **114** therein using conventional and well-known techniques. The feature **114** may be a plug, via, contact, line, wire, or any other interconnect component. Typically, the feature **114** has vertical sidewalls **116** and a floor **118**, having an aspect ratio of about 4:1 or greater, such as about 6:1. The floor **118** exposes at least a portion of the lower level metal interconnect **110**.

[0034] Referring to FIG. **2**B, the barrier layer **130** is conformally deposited on the floor **118** as well as the side walls **116** of the feature **114**. Preferably, the barrier layer contains tantalum nitride deposited to a thickness of about 20 Å or less, preferably about 10 Å, by providing one or more pulses of a tantalum-containing compound at a flow rate between about 100 sccm and about 1,000 sccm for a time period of about 1.0 second or less and one or more pulses of a nitrogen-containing compound at a flow rate between about 100 sccm and about 1,000 sccm for a time period of about 1.0 second or less to a reaction zone having a substrate disposed therein. Exemplary tantalum-containing compounds include t-butylimino tris(diethylamino) tantalum (TBTDET), pentakis (ethylmethylamino), tantalum (PEMAT), pentakis (dimethylamino) tantalum (PDMAT), pentakis (diethylamino) tantalum (PDEAT), t-butylimino tris(diethyl methylamino) tantalum (TBTMET), t-butylimino tris(dimethyl amino) tantalum (TBTDMT), bis(cyclopentadienyl) tantalum trihydride ($(Cp)_2TaH_3$), bis(methylcyclopentadienyl) tantalum trihydride ($(CpMe)_2TaH_3$), derivatives thereof, and combinations thereof. Exemplary nitrogen-containing compounds include ammonia, hydrazine, methylhydrazine, dimethylhydrazine, t-butylhydrazine, phenylhydrazine, azotertbutane, ethylazide, derivatives thereof, and combinations thereof.

[0035] It is to be understood that these compounds or any other compound not listed above may be a solid, liquid, or gas at room temperature. For example, PDMAT is a solid at room temperature and TBTDET is a liquid at room temperature. Accordingly, the non-gas phase precursors are subjected to a sublimation or vaporization step, which are both well known in the art, prior to introduction into the

processing chamber. A carrier gas, such as argon, helium, nitrogen, hydrogen, or a mixture thereof, may also be used to help deliver the compound into the processing chamber, as is commonly known in the art.

[0036] Each pulse is performed sequentially, and is accompanied by a separate flow of non-reactive gas at a rate between about 200 sccm and about 1,000 sccm. The separate flow of non-reactive gas may be pulsed between each pulse of the reactive compounds or the separate flow of non-reactive gas may be introduced continuously throughout the deposition process. The separate flow of non-reactive gas, whether pulsed or continuous, serves to remove any excess reactants from the reaction zone to prevent unwanted gas phase reactions of the reactive compounds, and also serves to remove any reaction by-products from the processing chamber, similar to a purge gas. In addition to these services, the continuous separate flow of non-reactive gas helps deliver the pulses of reactive compounds to the substrate surface similar to a carrier gas. The term "non-reactive gas" as used herein refers to a single gas or a mixture of gases that does not participate in the metal layer formation. Exemplary non-reactive gases include argon, helium, nitrogen, hydrogen, and combinations thereof.

[0037] A "reaction zone" is intended to include any volume that is in fluid communication with a substrate surface being processed. The reaction zone may include any volume within a processing chamber that is between a gas source and the substrate surface. For example, the reaction zone includes any volume downstream of a dosing valve in which a substrate is disposed.

[0038] The durations for each pulse/dose are variable and may be adjusted to accommodate, for example, the volume capacity of the processing chamber as well as the capabilities of a vacuum system coupled thereto. Additionally, the dose time of a compound may vary according to the flow rate of the compound, the pressure of the compound, the temperature of the compound, the type of dosing valve, the type of control system employed, as well as the ability of the compound to adsorb onto the substrate surface. Dose times may also vary based upon the type of layer being formed and the geometry of the device being formed.

[0039] Typically, the duration for each pulse or "dose time" is typically about 1.0 second or less. However, a dose time can range from microseconds to milliseconds to seconds, and even to minutes. In general, a dose time should be long enough to provide a volume of compound sufficient to adsorb/chemisorb onto the entire surface of the substrate and form a layer of the compound thereon.

[0040] FIG. **3** illustrates a schematic, partial cross section of an exemplary processing chamber **200** capable of forming a barrier layer using cyclical layer deposition, atomic layer deposition, digital chemical vapor deposition, and rapid chemical vapor deposition techniques. The terms "cyclical layer deposition", "atomic layer deposition", "digital chemical vapor deposition", and "rapid chemical vapor deposition" are used interchangeably herein and refer to gas phase deposition techniques whereby two or more compounds are sequentially introduced into a reaction zone of a processing chamber to deposit a thin layer of material on a substrate surface. Such a processing chamber **200** is available from Applied Materials, Inc. located in Santa Clara, Calif., and a brief description thereof follows. A more detailed description may be found in commonly assigned U.S. Ser. No. 10/032,284, filed Dec. 21, 2001, and issued as U.S. Pat. No. 6,916,398, which is incorporated herein by reference.

[0041] The processing chamber **200** may be integrated into an integrated processing platform, such as an ENDURAE platform also available from Applied Materials, Inc., located in Santa Clara, Calif. Details of the ENDURA® platform are described in commonly assigned U.S. Ser. No. 09/451,628, entitled "Integrated Modular Processing Platform," filed Nov. 30, 1999, which is incorporated by reference herein.

[0042] Referring to FIG. **3**, the chamber **200** includes a chamber body **202** having a slit valve **208** formed in a sidewall **204** thereof and a substrate support **212** disposed therein. The substrate support **212** is mounted to a lift motor **214** to raise and lower the substrate support **212** and a substrate **210** disposed thereon. The substrate support **212** may also include a vacuum chuck, an electrostatic chuck, or a clamp ring for securing the substrate **212** to the substrate support **212** during processing. Further, the substrate support **212** may be heated using an embedded heating element, such as a resistive heater, or may be heated using radiant heat, such as heating lamps disposed above the substrate support **212**. A purge ring **222** may be disposed on the substrate support **212** to define a purge channel **224** that provides a purge gas to prevent deposition on a peripheral portion of the substrate **210**.

[0043] A gas delivery apparatus **230** is disposed at an upper portion of the chamber body **202** to provide a gas, such as a process gas and/or a purge gas, to the chamber **200**. A vacuum system **278** is in communication with a pumping channel **279** to evacuate gases from the chamber **200** and to help maintain a desired pressure or a desired pressure range inside a pumping zone **266** of the chamber **200**.

[0044] The gas delivery apparatus **230** includes a chamber lid **232** having an expanding channel **234** formed within a central portion thereof. The chamber lid **232** also includes a bottom surface **260** extending from the expanding channel **234** to a peripheral portion of the chamber lid **232**. The bottom surface **260** is sized and shaped to substantially cover the substrate **210** disposed on the substrate support **212**. The expanding channel **234** has an inner diameter that gradually increases from an upper portion **237** to a lower portion **235** adjacent the bottom surface **260** of the chamber lid **232**. The velocity of a gas flowing therethrough decreases as the gas flows through the expanding channel **234** due to the expansion of the gas. The decreased gas velocity reduces the likelihood of blowing off reactants adsorbed on the surface of the substrate **210**.

[0045] The gas delivery apparatus **230** also includes at least two high speed actuating valves **242** having one or more ports. At least one valve **242** is dedicated to each reactive compound. For example, a first valve is dedicated to a refractory metal-containing compound, such as tantalum and titanium, and a second valve is dedicated to a nitrogen-containing compound. When a ternary material is desired, a third valve is dedicated to an additional compound. For example, if a silicide is desired, the additional compound may be a silicon-containing compound.

[0046] The valves **242** may be any valve capable of precisely and repeatedly delivering short pulses of com-

pounds into the chamber body **202**. In some cases, the on/off cycles or pulses of the valves **242** may be as fast as about 100 milliseconds or less. The valves **242** can be directly controlled by a system computer, such as a mainframe for example, or controlled by a chamber/application specific controller, such as a programmable logic computer (PLC) which is described in more detail in commonly assigned U.S. Ser. No. 09/800,881, filed Mar. 7, 2001, and issued as U.S. Pat. No. 6,734,020, which is incorporated by reference herein. For example, the valves **242** may be electronically controlled (EC) valves, which are commercially available from Fujikin of Japan as part number FR-21-6.35 UGF-APD.

[**0047**] To facilitate the control and automation of the overall system, the integrated processing system may include a controller **280** comprising a central processing unit (CPU) **282**, memory **286**, and support circuits **284**. The CPU **282** may be one of any form of computer processors that are used in industrial settings for controlling various drives and pressures. The memory **286** is connected to the CPU **282**, and may be one or more of a readily available memory such as random access memory (RAM), read only memory (ROM), floppy disk, hard disk, or any other form of digital storage, local or remote. Software instructions **288** and data can be coded and stored within the memory **286** for instructing the CPU **282**. The support circuits **284** are also connected to the CPU **282** for supporting the processor in a conventional manner. The support circuits **284** may include cache, power supplies, clock circuits, input/output circuitry, subsystems, and the like.

[**0048**] In a particular embodiment, a TaN barrier layer is formed by cyclically introducing PDMAT and ammonia to the substrate surface. To initiate the cyclical deposition of the TaN layer, a carrier/inert gas such as argon is introduced into the processing chamber **200** to stabilize the pressure and temperature therein. The carrier gas is allowed to flow continuously during the deposition process such that only the argon flows between pulses of each compound. A first pulse of PDMAT is provided from the gas source **238** at a flow rate between about between about 100 sccm and about 400 sccm, with a pulse time of about 0.6 seconds or less after the chamber temperature and pressure have been stabilized at about 200° C. to about 300° C. and about 1 Torr to about 5 Torr. A pulse of ammonia is then provided from the gas source **239** at a flow rate between about 200 sccm and about 600 sccm, with a pulse time of about 0.6 seconds or less.

[**0049**] A pause between pulses of PDMAT and ammonia is about 1.0 second or less, preferably about 0.5 seconds or less, more preferably about 0.1 seconds or less. In various aspects, a reduction in time between pulses at least provides higher throughput. As a result, a pause after the pulse of ammonia is also about 1.0 second or less, about 0.5 seconds or less, or about 0.1 seconds or less. Argon gas flowing between about 100 sccm and about 1,000 sccm, such as between about 100 sccm and about 400 sccm, is continuously provided from the gas source **240** through each valve **242**. In one aspect, a pulse of PDMAT may still be in the chamber when a pulse of ammonia enters. In general, the duration of the carrier gas and/or pump evacuation should be long enough to prevent the pulses of PDMAT and ammonia from mixing together in the reaction zone.

[**0050**] The heater temperature is maintained between about 100° C. and about 300° C. at a chamber pressure between about 1.0 and about 5.0 Torr. Preferably, the deposition temperature is between about 200° C. and about 250° C. Each cycle consisting of a pulse of PDMAT, pause, pulse of ammonia, and pause provides a tantalum nitride layer having a thickness between about 0.3 Å and about 1.0 Å per cycle. The alternating sequence may be repeated until the desired thickness is achieved, which is less than about 20 Å, such as about 10 Å. Accordingly, the deposition method requires between 10 cycles and 70 cycles, more typically between 20 cycles and 30 cycles.

[**0051**] In another aspect, a ternary barrier layer having a thickness less than about 20 Å, such as 10 Å, is deposited by providing one or more pulses of a refractory metal-containing compound, one or more pulses of a nitrogen-containing compound, and one or more pulses of a silicon-containing compound. Each pulse is adjusted to provide a desirable composition, silicon incorporation level, thickness, density, and step coverage of the refractory metal silicon nitride layer. A "ternary barrier layer" as used herein refers to a material having a composition comprising three major elements, such as titanium, nitrogen and silicon. An exemplary "ternary barrier layer" may also include tantalum, nitrogen and silicon.

[**0052**] Each pulse is performed sequentially, and is accompanied by a separate flow of carrier/inert gas at the same process conditions described above. The separate flow of carrier/inert gas may be pulsed between each pulse of reactive compound or the separate flow of carrier/inert gas may be introduced continuously throughout the deposition process.

[**0053**] Preferably, the ternary barrier layer contains titanium silicon nitride. In this embodiment, each cycle consists of a pulse of a titanium-containing compound, a pause, a pulse of a silicon-containing compound, a pause, a pulse of a nitrogen-containing compound, and a pause. Exemplary titanium-containing compound include tetrakis (dimethylamino) titanium (TDMAT), tetrakis (ethylmethylamino) titanium (TEMAT), tetrakis (diethylamino) titanium (TDEAT), titanium tetrachloride ($TiCl_4$), titanium iodide (TiI_4), titanium bromide ($TiBr_4$), and other titanium halides. Exemplary silicon-containing compounds include silane, disilane, methylsilane, dimethylsilane, chlorosilane (SiH_3Cl), dichlorosilane (SiH_2Cl_2), and trichlorosilane ($SiHCl_3$). Exemplary nitrogen-containing compounds include ammonia, hydrazine, methylhydrazine, dimethylhydrazine, t-butylhydrazine, phenylhydrazine, azotertbutane, ethylazide, derivatives thereof, and combinations thereof.

[**0054**] To initiate the cyclical deposition of a Ti_xSi_yN layer, argon is introduced into the processing chamber **200** to stabilize the pressure and temperature therein. This separate flow of argon flows continuously during the deposition process such that only the argon flows between pulses of each compound. The separate flow of argon flows between about 100 sccm and about 1,000 sccm, such as between about 100 sccm and about 400 sccm. In one aspect, a pulse of TDMAT is provided at a flow rate between about between about 10 sccm and about 1,000 sccm, with a pulse time of about 0.6 seconds or less after the chamber pressure and temperature have been stabilized at about 250° C. and 2 Torr. A pulse of silane is then provided at a flow rate between about 5 sccm and about 500 sccm, with a pulse time of 1 second or less. A pulse of ammonia is then provided at a flow

rate between about 100 sccm and about 5,000 sccm, with a pulse time of about 0.6 seconds or less.

[0055] A pause between pulses of TDMAT and silane is about 1.0 second or less, preferably about 0.5 seconds or less, more preferably about 0.1 seconds or less. A pause between pulses of silane and ammonia is about 1.0 second or less, about 0.5 seconds or less, or about 0.1 seconds or less. A pause after the pulse of ammonia is also about 1.0 second or less, about 0.5 seconds or less, or about 0.1 seconds or less. In one aspect, a pulse of TDMAT may still be in the chamber when a pulse of silane enters, and a pulse of silane may still be in the chamber when a pulse of ammonia enters.

[0056] The heater temperature is maintained between about 100° C. and about 300° C. at a chamber pressure between about 1.0 Torr and about 5.0 Torr. Each cycle consisting of a pulse of TDMAT, pause, pulse of silane, pause, pulse of ammonia, and pause provides a titanium silicon nitride layer having a thickness between about 0.3 Å and about 1.0 Å per cycle. The alternating sequence may be repeated until the desired thickness is achieved, which is less than about 20 Å, such as about 10 Å. Accordingly, the deposition method requires between 10 cycles and 70 cycles.

[0057] In yet another aspect, an alpha phase tantalum (α-Ta) layer having a thickness of about 20 Å or less, such as about 10 Å, may be deposited over at least a portion of the previously deposited binary (TaN) or ternary (TiSiN) layers. The α-Ta layer may be deposited using conventional techniques, such as PVD and CVD for example, to form a bilayer stack. For example, the bilayer stack may include a TaN portion deposited by cyclical layer deposition described above and an α-Ta portion deposited by high density plasma physical vapor deposition (HDP-PVD). An alpha phase tantalum is preferred due to its lower resistance compared to a beta phase tantalum.

[0058] To further illustrate, the α-Ta portion of the stack may be deposited using an ionized metal plasma (IMP) chamber, such as a VECTRA IMP SOURCE® chamber, available from Applied Materials, Inc. of Santa Clara, Calif. The IMP chamber includes a target, coil, and biased substrate support member, and may also be integrated into an ENDURA® platform, also available from Applied Materials, Inc. A power between about 0.5 kW and about 5 kW is applied to the target, and a power between about 0.5 kW and 3 kW is applied to the coil. A power between about 200 watts and about 500 watts at a frequency of about 13.56 MHz is also applied to the substrate support member to bias the substrate. Argon is flowed into the chamber at a rate of about 35 sccm to about 85 sccm, and nitrogen may be added to the chamber at a rate of about 5 sccm to about 100 sccm. The pressure of the chamber is typically between about 5 milliTorr to about 100 milliTorr, while the temperature of the chamber is between about 20° C. and about 300° C.

[0059] The barrier layer films described above may benefit from a post deposition treatment process, such as a plasma treatment process or a chemical treatment process, for example. A plasma treatment process can decrease resistance and improve yield. A typical plasma treatment may include an argon plasma, a nitrogen plasma, or a nitrogen and hydrogen plasma. The plasma treatment may be performed in the same deposition chamber in which the barrier layer deposition occurs or in a different chamber. If the plasma treatment occurs in the same chamber, the plasma can be an in situ plasma or a plasma delivered from a remote plasma source, such as a remote inductively coupled source or a microwave source.

[0060] While not wishing to be bound by theory, it is believed that a plasma treatment of a tantalum nitride film, for example, reduces the nitrogen content of one or more sublayers by sputtering off nitrogen, which in turn reduces resistivity. For example, a plasma treatment is believed to make a tantalum-nitride layer more tantalum-rich as compared to a non-plasma treated tantalum-nitride layer. In other words, a 1:1 Ta:N film may be converted to a 2:1 Ta:N film using a plasma treatment process. Tantalum nitride films having a sheet resistance of approximately equal to or less than 1,200 μΩ-cm for 0.004 μm (40 Å) films may be achieved.

[0061] Additionally, other non-chemically reactive gases may be used for physically displacing nitrogen from the barrier layer, such as neon (Ne), xenon (Xe), helium (He), and hydrogen (H_2), for example. Generally, it is more desirable to have a plasma-gas atom or molecule with an atomic-mass closer to N than to Ta in order to have preferential sputtering of the N. However, a chemically reactive process may be used where a particular gas preferentially reacts for removal of N while leaving Ta.

[0062] A chemical treatment process can also decrease resistance and improve yield. A typical chemical treatment may include exposure to aluminum compounds or silicon compounds. These compounds can include, but are not limited to, DMAH, TMA, silane, dimethylsilane, trimethylsilane and other organosilane compounds. A chemical treatment is typically operated at a pressure between about 1 Torr and about 10 Torr at a temperature between about 200° C. and about 400° C. Following a chemical treatment, it has been observed that a tantalum nitride film deposited according to the methods described above shows an improvement in dewetting compared with no chemical treatment.

[0063] The post deposition treatment processes may be performed after the formation of the barrier layer. Alternatively, the treatments may be performed between deposition of each monolayer or between deposition of each cycle. For example, a treatment process may take place after approximately every 0.003 μm to 0.005 μm (30 Å to 50 Å) of layer or after approximately every 7 cycles to 10 cycles.

[0064] Furthermore, the patterned or etched substrate dielectric layer **112** may be cleaned to remove native oxides or other contaminants from the surface thereof prior to depositing the barrier layer **130**. For example, reactive gases are excited into a plasma within a remote plasma source chamber such as a Reactive Pre-clean chamber available from Applied Materials, Inc., located in Santa Clara, Calif. Pre-cleaning may also be done within a metal CVD or PVD chamber by connecting the remote plasma source thereto. Alternatively, metal deposition chambers having gas delivery systems could be modified to deliver the pre-cleaning gas plasma through existing gas inlets such as a gas distribution showerhead positioned above the substrate.

[0065] In one aspect, the reactive pre-clean process forms radicals from a plasma of one or more reactive gases such as argon, helium, hydrogen, nitrogen, fluorine-containing com-

pounds, and combinations thereof. For example, a reactive gas may include a mixture of tetrafluorocarbon (CF_4) and oxygen (O_2), or a mixture of helium (He) and nitrogen trifluoride (NF_3). More preferably, the reactive gas is a mixture of helium and nitrogen trifluoride.

[0066] Following the argon plasma, the chamber pressure is increased to about 140 milliTorr, and a processing gas consisting essentially of hydrogen and helium is introduced into the processing region. Preferably, the processing gas comprises about 5% hydrogen and about 95% helium. The hydrogen plasma is generated by applying between about 50 watts and about 500 watts power. The hydrogen plasma is maintained for about 10 seconds to about 300 seconds.

[0067] Referring again to FIG. **2**C, the seed layer **140** may be deposited using high density plasma physical vapor deposition (HDP-PVD) to enable good conformal coverage. One example of a HDP-PVD chamber is the Self-Ionized Plasma SIP™ chamber, available from Applied Materials, Inc. of Santa Clara, Calif., which may be integrated into an ENDURA® platform, available from Applied Materials, Inc. Of course, other techniques, such as physical vapor deposition, chemical vapor deposition, electroless plating, and electroplating, may be used.

[0068] A typical SIP™ chamber includes a target, coil, and biased substrate support member. To form the copper seed layer, a power between about 0.5 kW and about 5 kW is applied to the target, and a power between about 0.5 kW and 3 kW is applied to the coil. A power between about 200 watts and about 500 watts at a frequency of about 13.56 MHz is applied to bias the substrate. Argon is flowed into the chamber at a rate of about 35 sccm to about 85 sccm, and nitrogen may be added to the chamber at a rate of about 5 sccm to about 100 sccm. The pressure of the chamber is typically between about 5 milliTorr to about 100 milliTorr.

[0069] Alternatively, a seed layer **140** containing a copper alloy may be deposited by any suitable technique such as physical vapor deposition, chemical vapor deposition, electroless deposition, or a combination of techniques. Preferably, the copper alloy seed layer **140** contains aluminum and is deposited using a PVD technique described above. During deposition, the process chamber is maintained at a pressure between about 0.1 milliTorr and about 10 milliTorr. The target includes copper and between about 2 and about 10 atomic weight percent of aluminum. The target may be DC-biased at a power between about 5 kW and about 100 kW. The pedestal may be RF-biased at a power between about 10 watts and about 1,000 watts. The copper alloy seed layer **140** is deposited to a thickness of at least about 5 Å, and between about 5 Å and about 500 |.

[0070] Referring to FIG. **2**D, the metal layer **142** may be formed, using chemical vapor deposition (CVD), physical vapor deposition (PVD), electroplating, or a combination thereof. For example, an aluminum (Al) layer may be deposited from a reaction of a gas mixture containing dimethyl aluminum hydride (DMAH) and hydrogen (H_2) or argon (Ar) or other DMAH containing mixtures, a CVD copper layer may be deposited from a gas mixture containing $Cu^{+2}(hfac)_2$ (copper hexafluoro acetylacetonate), $Cu^{+2}(fod)_2$ (copper heptafluoro dimethyl octanediene), Cu^{+1}hfac TMVS (copper hexafluoro acetylacetonate trimethylvinylsilane), or combinations thereof, and a CVD tungsten layer may be deposited from a gas mixture containing tungsten hexafluoride (WF_6) and a reducing gas. A PVD layer can be deposited from a copper target, an aluminum target, or a tungsten target.

[0071] Moreover, the metal layer **142** may be a refractory metal compound including but not limited to titanium (Ti), tungsten (W), tantalum (Ta), zirconium (Zr), hafnium (Hf), molybdenum (Mo), niobium (Nb), vanadium (V), and chromium (Cr), among others. Conventionally, a refractory metal is combined with reactive species, such as for example chlorine (Cl) or fluorine (F), and is provided with another gas to form a refractory metal compound. For example, titanium tetrachloride ($TiCl_4$), tungsten hexafluoride (WF_6), tantalum pentachloride ($TaCl_5$), zirconium tetrachloride ($ZrCl_4$), hafnium tetrachloride ($HfCl_4$), molybdenum pentachloride ($MOCl_5$), niobium pentachloride ($NbCl_5$), vanadium pentachloride (VCl_5), or chromium tetrachloride ($CrCl_4$) may be used as a refractory metal-containing compound gas.

[0072] Preferably, the metal layer **142** is copper and is formed within an electroplating cell, such as the ELECTRA Cue ECP system, available from Applied Materials, Inc., of Santa Clara, Calif. The ELECTRA Cu® ECP system may also be integrated into an ENDURA® platform also available from Applied Materials, Inc.

[0073] A copper electrolyte solution and copper electroplating technique is described in commonly assigned U.S. Pat. No. 6,113,771, which is incorporated by reference herein. Typically, the electroplating bath has a copper concentration greater than about 0.7 M, a copper sulfate concentration of about 0.85 M, and a pH of about 1.75. The electroplating bath may also contain various additives as is well known in the art. The temperature of the bath is between about 15° C. and about 25° C. The bias is between about −15 volts to about 15 volts. In one aspect, the positive bias ranges from about 0.1 volts to about 10 volts and the negatives bias ranges from about −0.1 volts to about −10 volts.

[0074] Optionally, a thermal anneal process may be performed following the metal layer **142** deposition whereby the wafer is subjected to a temperature between about 100° C. and about 400° C. for about 10 minutes to about 1 hour, preferably about 30 minutes. A carrier/purge gas such as helium, hydrogen, nitrogen, or a mixture thereof is introduced at a rate of about 100 sccm to about 10,000 sccm. The chamber pressure is maintained between about 2 Torr and about 10 Torr. The RF power is about 200 watts to about 1,000 watts at a frequency of about 13.56 MHz, and the preferable substrate spacing is between about 300 mils and about 800 mils.

[0075] Following deposition, the top portion of the resulting structure may be planarized. A chemical mechanical polishing (CMP) apparatus may be used, such as the MIRRA® System available from Applied Materials, Santa Clara, Calif., for example. Optionally, the intermediate surfaces of the structure may be planarized between the deposition of the subsequent layers described above.

[0076] FIG. **4** is a schematic top-view diagram of an exemplary multi-chamber processing system **600** that may be adapted to perform the deposition sequence disclosed above. Such a processing system **600** may be an ENDURA® system, commercially available from Applied Materials,

Inc., of Santa Clara, Calif. A similar multi-chamber processing system is disclosed in U.S. Pat. No. 5,186,718, which is incorporated by reference herein.

[0077] The system **600** generally includes load lock chambers **602**, **604** for the transfer of substrates into and out from the system **600**. Typically, since the system **600** is under vacuum, the load lock chambers **602**, **604** may "pump down" the substrates introduced into the system **600**. A first robot **610** may transfer the substrates between the load lock chambers **602**, **604**, and a first set of one or more substrate processing chambers **612**, **614**, **616**, **618** (four are shown). Each processing chamber **612**, **614**, **616**, **618**, can be outfitted to perform a number of substrate processing operations such as cyclical layer deposition, chemical vapor deposition (CVD), physical vapor deposition (PVD), etch, pre-clean, degas, orientation and other substrate processes. The first robot **610** also transfers substrates to/from one or more transfer chambers **622**, **624**.

[0078] The transfer chambers **622**, **624**, are used to maintain ultrahigh vacuum conditions while allowing substrates to be transferred within the system **600**. A second robot **630** may transfer the substrates between the transfer chambers **622** and **624** and a second set of one or more processing chambers **632**, **634**, **636**, and **638**. Similar to processing chambers **612**, **614**, **616**, and **618**, the processing chambers **632**, **634**, **636**, and **638** can be outfitted to perform a variety of substrate processing operations, such as cyclical layer deposition, chemical vapor deposition (CVD), physical vapor deposition (PVD), etch, pre-clean, degas, and orientation, for example. Any of the substrate processing chambers **612**, **614**, **616**, **618**, **632**, **634**, **636**, and **638** may be removed from the system **600** if not necessary for a particular process to be performed by the system **600**.

[0079] In one arrangement, each processing chamber **632** and **638** may be a physical vapor deposition chamber, a chemical vapor deposition chamber, or a cyclical deposition chamber adapted to deposit a seed layer; each processing chamber **634** and **636** may be a cyclical deposition chamber, a chemical vapor deposition chamber, or a physical vapor deposition chamber adapted to deposit a barrier layer; each processing chamber **612** and **614** may be a physical vapor deposition chamber, a chemical vapor deposition chamber, or a cyclical deposition chamber adapted to deposit a dielectric layer; and each processing chamber **616** and **618** may be an etch chamber outfitted to etch apertures or openings for interconnect features. This one particular arrangement of the system **600** is provided to illustrate the invention and should not be used to limit the scope of the invention.

[0080] It is believed that a refractory metal nitride layer having a thickness greater than about 20 Å will terminate the growth pattern of the lower level metal interconnect. A refractory metal nitride layer having a thickness of about 20 Å or more will establish a distinct growth pattern of its own, which would be initially adopted by the higher interconnect until the higher interconnect reaches a particular thickness and establishes its own pattern, thereby forming a different crystal structure. This phenomenon occurs because a growth pattern of a subsequently deposited layer typically resembles a growth pattern of an underlying layer during its initial stages of deposition, but the subsequent layer then takes on its own, inherent pattern once the subsequent layer reaches a particular thickness.

[0081] Tantalum nitride, for example, has a natural inclination to form an amorphous structure at about 20 Å or more. Below about 20 Å, TaN resembles the growth pattern of its underlying layer. Therefore, a subsequent copper interconnect layer was surprisingly grown across a barrier layer deposited according to the methods of the present invention exhibiting a similar growth pattern as the underlying copper interconnect. In other words, a 20 Å or less TaN barrier layer enables good grain growth of copper such that copper grains can extend growth across the TaN barrier layer, or simply stated, copper exhibits epitaxial growth on the tantalum nitride barrier layer.

[0082] FIG. **5** is a transmission electron microscope (TEM) image of a feature **300** having a titanium nitride barrier layer **310** deposited therein according to the deposition techniques described above. The feature **300** had an aspect ratio of 5:1 and was formed on a 200 mm wafer. The barrier layer **310** consisted of tantalum nitride and was deposited at 250° C. and 2 Torr. Each cycle lasted about 2 seconds and 30 cycles were performed. The tantalum nitride barrier layer **310** had a thickness of about 15 Å. As shown, the barrier layer **310** is conformal and shows good step coverage throughout the entire feature **300**.

[0083] FIG. **6** is a TEM image showing a partial cross sectional view of a multi-level, interconnect structure **400**. The multi-level, interconnect structure **400** included a lower level copper interconnect **405**, a tantalum nitride barrier layer **410**, and an upper level copper interconnect **420**. The copper grain growth of the lower level copper interconnect **405** extended across the barrier layer **410** into the upper level copper interconnect **420**, showing epitaxial growth of the tantalum nitride barrier layer **410**. The barrier layer **410** consisted of tantalum nitride and was deposited at 250° C. and 2 Torr. Each cycle lasted about 2 seconds and 30 cycles were performed. The barrier layer **410** had a thickness of about 10 Å, which was sufficient to inhibit copper migration into the dielectric material.

[0084] The barrier layers **310**, **410** shown and described with reference to FIGS. **3** and **4** were measured using a TEM instrument. It can be appreciated that a margin of error is present with this kind of measurement technique as well as any other measurement technique for determining a thickness of a deposited layer. Therefore, the thicknesses provided herein are approximate and quantified according to the best available known techniques and are not intended to limit the scope of the present invention.

[0085] The following example is intended to provide a non-limiting illustration of one embodiment of the present invention.

EXAMPLE

[0086] A TaN layer was deposited over a lower level copper layer using cyclical deposition to a thickness of about 20 Å. A copper alloy seed layer was deposited over the TaN layer by physical vapor deposition to a thickness of about 100 Å. The copper alloy seed layer contained aluminum in a concentration of about 2.0 atomic percent, and was deposited by PVD using a copper-aluminum target consisting of aluminum in a concentration of about 2.0 atomic percent. A bulk copper layer was then deposited using ECP to fill the feature. The substrate was then thermally annealed at a

temperature of about 380° C. for about 15 minutes in a nitrogen (N_2) and hydrogen (H_2) ambient.

[0087] The overall feature resistance was significantly reduced and the upper level copper layer surprisingly exhibited a grain growth similar to that of the lower level copper layer. The barrier performance of the TaN layer exhibited longer time to failure (TTF) compared with 50 Å PVD Ta. Further, the TaN layer showed low contact resistance and a tight spread distribution. The TaN layer also exhibited excellent topography including a smooth morphology and pinhole free surface.

[0088] Additionally, the TaN film deposited according to the PDMAT and ammonia process described herein demonstrated exceptional film uniformity. The film thickness was linearly proportional to the number of deposition cycles, allowing accurate thickness control. Thickness uniformity was found to be 1.8 percent for a 10 Å film and 2.1 percent for a 100 Å film on a 200 mm substrate. The deposited films exhibited exceptionally conformal coverage, approaching 100 percent in at least some results.

[0089] Finally, the copper alloy seed layer showed excellent adhesion/wetting to the TaN layer. The (PVD) copper seed layer exhibited a preferred {111} orientation on the deposited barrier layer. The crystal orientation of {111} is preferred because this orientation provides large grain sizes and exhibits good electromigration resistance as a result of the larger grain sizes.

[0090] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

1. A method for forming a tungsten-containing material on a substrate, comprising:

positioning a substrate comprising an underlying tungsten layer within a process chamber;

depositing a tungsten-containing barrier layer on the underlying tungsten layer during a cyclical layer deposition process, wherein the tungsten-containing barrier layer comprises a refractory metal nitride material;

depositing a seed layer on the tungsten-containing barrier layer during a vapor deposition process; and

depositing a bulk tungsten layer on the seed layer during a chemical vapor deposition process.

2. The method of claim 1, wherein the refractory metal nitride material comprises tungsten.

3. The method of claim 1, wherein the tungsten-containing barrier layer has a thickness of about 20 Å or less.

4. The method of claim 3, wherein the thickness is about 10 Å or less.

5. The method of claim 1, wherein the bulk tungsten layer is deposited during the chemical vapor deposition process by exposing the substrate to a gas mixture comprising tungsten hexafluoride and a reducing gas.

6. The method of claim 1, wherein the seed is deposited by a physical vapor deposition process.

7. The method of claim 6, wherein the seed layer comprises tungsten.

8. The method of claim 1, wherein the underlying tungsten layer is part of an interconnect feature.

9. The method of claim 8, wherein the interconnect feature comprises a member selected from the group consisting of plug, via, contact, line, and wire.

10. A method for forming a tungsten-containing material on a substrate, comprising:

positioning a substrate comprising interconnect features within a process chamber, wherein the interconnect features comprise vertical walls, a floor, and an underlying tungsten layer on the floor;

depositing a tungsten-containing barrier layer on the underlying tungsten layer during a cyclical layer deposition process;

depositing a seed layer on the tungsten-containing barrier layer during a vapor deposition process; and

filling the interconnect features by depositing a bulk tungsten layer on the substrate during a chemical vapor deposition process.

11. The method of claim 10, wherein the tungsten-containing barrier layer comprises a nitride material.

12. The method of claim 10, wherein the tungsten-containing barrier layer has a thickness of about 20 Å or less.

13. The method of claim 12, wherein the thickness is about 10 Å or less.

14. The method of claim 10, wherein the bulk tungsten layer is deposited during the chemical vapor deposition process by exposing the substrate to a gas mixture comprising tungsten hexafluoride and a reducing gas.

15. The method of claim 10, wherein the seed is deposited by a physical vapor deposition process.

16. The method of claim 15, wherein the seed layer comprises tungsten.

17. The method of claim 10, wherein the interconnect features are a member selected from the group consisting of plug, via, contact, line, and wire.

18. A method for forming a tungsten-containing material on a substrate, comprising:

positioning a substrate comprising interconnect features within a process chamber, wherein each of the interconnect features comprises vertical walls and a floor;

depositing a tungsten-containing barrier layer on the substrate during a cyclical layer deposition process, wherein the tungsten-containing barrier layer comprises a refractory metal material and a refractory metal nitride material;

depositing a seed layer on the tungsten-containing barrier layer during a vapor deposition process; and

filling the interconnect features by depositing a bulk tungsten layer on the substrate during a chemical vapor deposition process.

19. The method of claim 18, wherein the refractory metal nitride material comprises tungsten.

20. The method of claim 19, wherein the refractory metal material comprises tungsten.

21. The method of claim 20, wherein the tungsten-containing barrier layer has a thickness of about 20 Å or less.

22. The method of claim 21, wherein the thickness is about 10 Å or less.

23. The method of claim 18, wherein the bulk tungsten layer is deposited during the chemical vapor deposition

process by exposing the substrate to a gas mixture comprising tungsten hexafluoride and a reducing gas.

24. The method of claim 18, wherein the seed is deposited by a physical vapor deposition process.

25. The method of claim 23, wherein the seed layer comprises tungsten.

26. The method of claim 18, wherein the interconnect features are a member selected from the group consisting of plug, via, contact, line, and wire.

27. A method for forming a tungsten-containing material on a substrate, comprising:

positioning a substrate comprising interconnect features within a process chamber, wherein the interconnect features comprise vertical walls and a floor;

depositing a tantalum-containing barrier material on the substrate and within the interconnect features, wherein the tantalum-containing barrier material comprises a metallic tantalum layer deposited by a physical vapor deposition process and a tantalum nitride layer deposited by an atomic layer deposition process;

exposing the tantalum-containing barrier material to a silicon-containing compound during chemical treatment process;

depositing a seed layer on the tantalum-containing barrier material during a vapor deposition process; and

filling the interconnect feature by depositing a bulk tungsten layer on the substrate during a chemical vapor deposition process.

28. The method of claim 27, wherein the silicon-containing compound is silane or disilane.

* * * * *