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(71) Applicant *(for all designated States except US)*: **MEMORIGHT MEMORITECH (SHENZHEN) CO., LTD** [CN/CN]; 3/F, Building W2A, High-Tech Industrial Park, Nanshan District, Shenzhen, Guangdong 518057 (CN).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **HUANG, He** [CN/CN]; 3/F, Building W2A, High-Tech Industrial Park, Nanshan District, Shenzhen, Guangdong 518057 (CN).

(74) Agent: **SHENZHEN TRUER IP**; Suite 2201, Block B, Jia Zhao Ye Center, Shangbu Road, Futian District, Shenzhen, Guangdong 518031 (CN).

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(54) Title: FLASH MEMORY DATA READ/WRITE PROCESSING METHOD

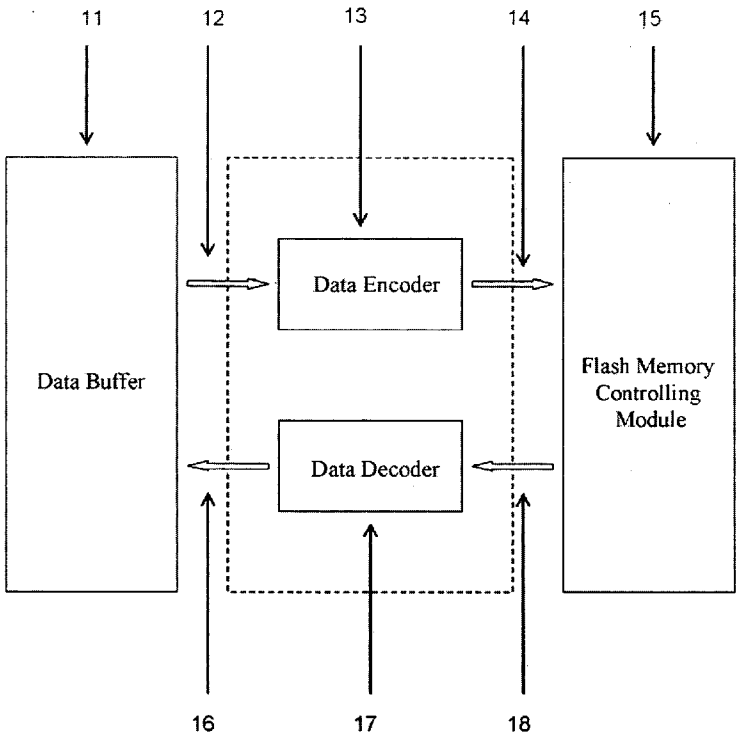

FIG. 1

(57) Abstract: A flash memory data read/write processing method is provided. The method includes the following steps. In Step 1, during storing the flash memory data, an encoding process is performed on the data to be stored so that the number of specific values in the processed data is reduced compared with that before the encoding, and the encoded data is written into a flash memory cell. In Step 2, during reading the flash memory data, first, the encoded data in the flash memory cell is read out, then a decoding process corresponding to the encoding process described in Step 1 is performed on the read data, and finally, the decoded original data is output. This method may reduce the consumption of a flash memory chip due to writing and erasing operations, thereby prolonging the operating life span of the flash memory chip. This method may also increase the efficiency of writing and erasing operations, reduce the operating time, as well as reduce the power consumption of flash memory operations.

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FLASH MEMORY DATA READ/WRITE PROCESSING METHOD

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates to a flash memory data read/write processing method, and more particularly to a method of optimizing flash memory operations by performing an encoding/decoding process on data.

Related Art

Flash memory is a commonly used storage device. Flash memory is widely used in the fields of personal computers, various digital electronic devices, and other various digital storage devices more and more because it may perform data reading/writing and erasing many times and also has the characteristics of high density, large capacity, low time consumption in reading/writing operations as well as non-volatility and low power consumption. In recent years, the increasing improvements in technology, gradually reduced cell cost prices, and increasing improvement in back-end application technology have all greatly stimulated the development of the flash memory market and made flash memory gradually have equal market share with the hard disk in the storage field. However, the flash memory has had some unavoidable defects since it came into being due to some problems in its own manufacturing process. These defects have limited the further application of the flash memory. On one hand, a general flash memory chip has an operating life span, which is determined by a flash cell's own storage principle. The flash cell usually operates as follows. First, a suspended gate of the memory cell is discharged (i.e., commonly described as 'erasing') to reach a general state. Then, during the writing of the data, the suspended gate is charged (i.e., commonly described as 'programming') to reach a state needed for storing the data. As the number of erasing and programming times gradually increases, some tunneling electrons will be gradually accumulate in the suspended gate under such tunneling effect, thereby requiring a larger forward voltage for programming the memory cell again. At the same time, during erasing, the insulator medium is aging under the repeated tunneling effect

and finally fails to function as a barrier (i.e., commonly described as 'barrier punctured'). Both cases will result in the memory cell's inability to operate normally (i.e., the commonly-said ending its operating period). The most commonly used NAND-type flash memory is used as an example for illustration below. The number of erasing or re-programming times of the NAND-type flash memory is generally around 100,000. On the other hand, the writing and erasing operations of the flash memory chip are special in that the flash memory chip performs the writing operation in a unit of a page and performs the erasing operation in the unit of a block. The process time for the writing and erasing operations of the flash memory is generally long. The process time for writing the data of each page on the inside the flash memory chip is 200 μs-700 μs, and the time for the erasing operation of a block is 2 ms. At the same time, the operating time is closely related to the technology of the flash memory chip. The erasing operation of the flash memory configures all memory cells within the block to a state 1. During writing of the data, if the data required to be written is 1, a flash memory cell bit corresponding to the data does not need to be re-programmed. If the data required to be written is 0, the re-programming is required, i.e., the suspended gate must be charged. At the same time, before writing data to this page for the next time, the erasing operation must be performed once again first, and those memory cells written as 0 will be discharged again. Therefore, during one operation, the larger the number of 0s in the page data, the more the memory cells required to be consumed in the page. Thirdly, according to the manufacturing process of the flash memory cell, the time for the writing operation of the flash memory is related to the written data values in that the larger the number of 0s written to the page during each operation, the longer the time required by the operation. At the same time, the conclusion is the same for the erasing operation. Fourthly, the power consumption of the flash memory chip is related to the written content. When the flash cell performs the writing operation, if the data to be written is 1, the suspended gate does not need to be charged since the data bit after the erasing operation is 1. On the contrary, if the data to be written is 0, the suspended gate must be charged. Therefore, the smaller the number of written 0s in the page data, the less the memory cells needed to be charged, and the lower the power consumption.

The existing method for addressing the problem of limited operating life span of the flash memory mainly lies in distributing the writing and erasing operations to each block as equally as possible so that each block is uniformly consumed during the use of the flash memory chip. This method is currently widely used by flash memory manufacturers. However, this method only distributes the operating consumption of the flash memory equally in each block of the flash memory chip without reducing the consumption of the flash memory chip.

SUMMARY OF THE INVENTION

The present invention is directed to provide a flash memory data read/write processing method, which is applicable for reducing the number of times of operations causing consumption on a flash memory cell, increasing the life span and storage efficiency of the flash memory, and reducing the power consumption during the operation of the flash memory.

The present invention provides a flash memory data read/write processing method, which includes the following steps.

Step 1: during writing the flash memory data, first, an encoding process is performed on the data to be stored so that the number of specific values in the processed data is reduced compared with that before the encoding, and the encoded data are written into a flash memory cell.

Step 2: during reading the flash memory data, first the encoded data in the flash memory cell is read out, a decoding process corresponding to the encoding process in Step 1 is performed on the read data, and the decoded original data is output.

Preferably, when the data is binary data, the specific values are 0 or 1.

Preferably, Step 1 includes performing the encoding process on the data to be stored at either the system host side, the flash memory controller side, or the flash memory chip side.

Preferably, Step 2 includes performing the decoding process on the read data at either the system host side, the flash memory controller side, or the flash memory chip side.

Preferably, the method further includes storing the encoded/decoded information within the flash memory chip.

Preferably, the number of the specific values in each set of binary data after the encoding process in Step 1 is no more than the number of the specific values in the corresponding set of binary data before the encoding, and Step 2 employs the decoding process corresponding thereto.

Preferably, the method further includes creating a mapping relationship between the data and the encoding so that the number of the specific values in the encoding is smaller than that in the data. Step 1 includes completing the encoding process of the data by querying the mapping relationship, and Step 2 includes completing the decoding process of the data by querying the mapping relationship.

Preferably, the encoding process of Step 1 includes performing an inverse on the data whose number of the specific values is larger than that of another code value, and the decoding process in Step 2 includes performing the inverse on the inversed data in the encoding process to obtain the original data information.

Preferably, in a set period, the total number of the specific values in all sets of binary data after the encoding process in Step 1 is smaller than the total number of the specific values in all sets of binary data before the encoding, and Step 2 employs the decoding process corresponding thereto.

Preferably, for an NAND-type flash memory, Step 1 includes performing the encoding process on the binary data to be stored so that the number of 0s in the processed binary data is smaller than that before the encoding, and writing the encoded binary data into a flash memory cell.

The flash memory data read/write processing method of the present invention mainly reduces the number of specific values in the data by way of encoding/decoding, thereby reducing the consumption of the flash memory chip by writing and erasing operations, and prolonging the operating life span of the flash memory chip. Secondly, the algorithm reduces the number of written data with specific values in the flash memory chip, increases the efficiency of writing and erasing operations, and reduces the operating time. Thirdly, the

encoding/decoding operating method reduces the power consumption of flash memory operations.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description given herein below for illustration only, and thus are not limitative of the present invention, and wherein:

FIG. 1 is a schematic view illustrating the principles of an embodiment of the present invention performing an encoding/decoding process on the flash memory controller side;

FIG. 2 is a schematic view of a writing operation of the embodiment of the present invention performing the encoding/decoding process on the flash memory controller side;

FIG. 3 is a schematic view of a reading operation of the embodiment of the present invention performing the encoding/decoding process on the flash memory controller side;

FIG. 4 is an operating schematic view of a flash memory chip's page data processed by the embodiment method of the present invention;

FIG. 5 is an operating schematic view of the flash memory chip's page data without being processed by the embodiment method of the present invention;

FIG. 6 is a schematic view of combinations of 4-bit data in a mapping encoding/decoding embodiment of the present invention;

FIG. 7 is a schematic view of combinations of data increased by 2 bits in width in the mapping encoding/decoding embodiment of the present invention;

FIG. 8 is a schematic view of a mapping relationship between the 4-bit original data and the data with increased width in the mapping encoding/decoding embodiment of the present invention;

FIG. 9 is a schematic view of the uncompressed original data in a compression encoding/decoding embodiment of the present invention;

FIG. 10 is a schematic view of a correspondence between the original data and the

compression encoding in the compression encoding/decoding embodiment of the present invention; and

FIG. 11 is a schematic view of the compression-encoded data in the compression encoding/decoding embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention will be illustrated in detail below by an NAND-type flash memory as an embodiment in combination with the accompanying drawings.

According to the operating characteristics of a memory cell within a flash memory block, the main reason affecting the life span of the flash memory cell lies in the consumption of the memory cell caused by an operation from 1 to 0 during writing and an operation from 0 to 1 during erasing. Therefore, after the erasing operation of the block, the smaller the number of 0s written to a page during each operation, the smaller the number of memory cells consumed during erasing and the larger the number of times of using the block. According to a statistical method, the entire life span of a flash memory chip will be prolonged as well. At the same time, the operating time may be reduced and the efficiency of writing and erasing operations may be increased by a method of controlling the written data value. Meanwhile, the power consumption of flash memory operations may be reduced by controlling the written data value. The present invention achieves the purposes of prolonging the life span of the flash memory, optimizing flash memory operations, and reducing the flash memory power consumption by a method of optimizing the written data through encoding/decoding.

The encoding manner employed by the present invention may include many types. Codes may be generated directly by using an algorithm so that the number of 0s after the encoding is smaller than the number of 0s in the original data before the encoding. Besides, the amount of data written to the memory cell, and more importantly, the number of 0s in the data may be reduced by a data compression method. The encoding/decoding algorithm of the present invention may include many types, of whose main purposes lie in that the written data is encoded during the writing operation so that the generated codes contain as few 0s as

possible to reduce the consumption of the memory cell by writing and erasing operations, and at the same time the original data may be restored by a corresponding decoding method during the reading operation.

The flash memory read/write encoding/decoding algorithm provided by the present invention can be realized widely and may be implemented by the following description methods. Method 1 is implemented by software. When a host is sending data to a flash memory device, an encoding operation is directly performed on the data, and then the encoded data is sent to an interface of the flash memory device. When the host is reading the flash memory device, a decoding operation is directly performed on the flash memory data read from the interface, and then the data is transmitted to other storage devices. Method 2 is implemented by hardware. An encoding/decoding module may be added in a controller module in the flash memory device. During the writing operation, after the encoder receives the data sent from the interface of the device, it performs the encoding operation on the data and then sends the encoded result to the flash memory chip for storage. During the reading operation, the controller module reads out the encoded data in the flash memory chip, performs the decoding operation, and finally transmits the decoded data to the host through the interface. Method 3 includes adding an encoding/decoding module within the flash memory chip. When the flash memory chip receives the data sent from an external controller module, it directly performs the encoding operation on the data, and then writes the encoded result into a memory cell within the corresponding address. When the controller module performs the reading operation on the flash memory chip, the encoding/decoding module within the flash memory chip first performs the decoding operation on the encoded result read from the memory cell with the corresponding address, and then sends the result to the controller module. The encoder and decoder can be respectively and separately set at different device sides, including a system host side, a flash memory controller side, or a flash memory chip side.

FIG. 1 is a schematic view illustrating principles of an embodiment of the present invention performing an encoding/decoding process at a flash memory controller side. In

the figure, 11 indicates the device data buffer for buffering the data during operation. 12 indicates writing data from the data buffer module to a data encoder during the writing operation of the device. 13 indicates the encoder in the encoding/decoding module, which mainly functions to perform an encoding operation on the data written in the buffer and write the corresponding encoded information into a redundant area or information area in the flash memory chip. 14 indicates the writing of the data after the processing of the encoder in the encoder/decoder into a flash memory controlling module. 15 indicates the flash memory controlling module for controlling flash memory operations and at the same time transmitting the encoded result to the flash memory chip. 18 indicates the flash memory controller transmitting the read data stored within the flash memory chip to the decoder during a reading operation. 17 indicates the decoder in the encoder/decoder, which mainly functions to perform a corresponding decoding operation on data in the data area according to the encoded information recorded in the data flash memory chip, and then transmit the decoded result to the data buffer as indicated by 16 in the figure.

FIG. 2 shows an encoding operation during a writing operation of a certain page by an embodiment algorithm of the present invention. As shown in the figure, a size of the page for data operating is set to be 8 bytes and a redundant area is set to be 1 byte, i.e., each flash memory writing operation has a unit of 9 bytes. Assume an arbitrarily selected page whose data values are shown in a block in the left of the figure as "01100000 10000100 01000100 10101001 01001001 00101000 00000100 00100001", where the redundant area is "xxxxxxx1". The first 7 bits of the redundant area record other data information and the 8^{th} bit is the designated encoded information. According to statistics of the encoder, the number of 0s is 46 and the number of 1 is 18. According to the judgment, the encoding operation needs to be performed on the data. The data shown in a block in the right of the figure as "11001111 01111011 10111011 01010110 10110110 11010111 11111011 11011110" is obtained through the embodiment algorithm of the present invention, and the encoded information is written into the redundant area "xxxxxxx0" (here it is defined that the encoded information bit of 0 represents that an inverse operation has been performed; and the encoded

information bit of 1 represents that the inverse operation has not been performed). According to statistics of the encoder on the data area, the number of 0s is 18 and the number of 1s is 46. The encoded result is written into the flash memory chip, and at the same time a corresponding mark is written in the designated bit within the redundant area to record that the inverse operation has been performed on the page data.

FIG. 3 shows a decoding operation during a reading operation of data recorded by a certain page by the embodiment algorithm of the present invention. As shown in the figure, a decoder performs the decoding operation on the encoded result and reads out the data originally written to the device according to the marking bit information in the redundant area written during the writing operation.

FIG. 4 shows the changes of memory cell bits in the data area within the flash memory chip after the writing operation and final erasing operation of a certain page in the embodiment of the present invention. First, an erasing operation is required to be performed on the flash memory page with the address to be operated before writing data. After the erasing operation, as shown in the left block in the figure, all the memory cells are changed to 1. Then, the data is written. During writing, if the value at this position is 1, the memory cell at this position does not need to be charged. If the value at this position is 0, the charging operation is required and the memory cell is correspondingly written as 0, as shown in the middle block in the figure. Finally, the erasing operation is performed on the written data, i.e. all the bits are discharged. If the bit is 1, it is not consumed during the current writing and erasing operations. If the bit is 0, it is consumed once during the current writing and erasing operations.

Statistics are performed on this embodiment. The flash memory cell in the data area would be consumed 46 times without being processed by the encoding/decoding operation of the embodiment of the present invention as shown in FIG. 5, and is consumed 18 times after being processed by the embodiment algorithm of the present invention, so the number of times of consuming the memory cells of this page is greatly reduced. Similarly, the operating life span can be effectively prolonged for both the entire flash memory chip and the

flash memory device. At the same time, according to characteristics of writing and erasing operations of the flash memory, the smaller the number of 0s in the data written or erased during each operation, the shorter the operating time, and the higher the efficiency. At the same time, the smaller the number of 0s, the less the energy consumption required by the operation.

The present invention is illustratively described in the above example with an inverse operation, which is the most simple and handy algorithm as an example. In addition, algorithms and implementation methods involved in the present invention may include many types and may be implemented not only by software but also by hardware. The ultimate purpose thereof is to reduce operations consuming the flash memory cell as much as possible, and to reduce the consumption of the flash memory chip by the data written into the flash memory chip as much as possible, thereby achieving optimizing purposes of prolonging the operating life span of the flash memory chip and the flash memory device, shortening the operating time, increasing the operating rate of the flash memory, as well as reducing the power consumption of flash memory operations.

A mapping encoding/decoding process manner is introduced below. As shown in FIG. 6, this embodiment uses 4-bit data as an example. The figure shows all the collections of the 4-bit data, one of which has zero 0s, four have one 0, six have two 0s, four have three 0s, and one has four 0s.

FIG. 7 shows all the combinations of the data after a 2-bit redundant area is added, one of which contains zero 0s, six contain one 0, fifteen contain two 0s, twenty contain three 0s, fifteen contain four 0s, six contain five 0s, and one contains six 0s.

As shown in FIG. 8, a new mapping relationship is created between the 4-bit data combinations and the 6-bit data combinations containing the redundant areas. After performing the encoding operation on the data during writing the data according to this mapping relationship, the number of 0s in the data may be greatly reduced. In the mapped 6-bit data in the figure, one has zero 0s, six have one 0, and nine have two 0s.

Statistics are performed on the above results. Since the data is randomly generated, each value in the combination has the same probability of being recorded and written into the flash memory chip. Assume each value in the combination is written n times, the number of times of writing 0 is 4n+12n+12n+4n=32n, and the actual number of times of writing 0 after the encoding operation is 6n+18n=24n. According to the statistics, a total of 8n times of writing 0 is reduced, and the 4-bit writing operation is performed for 16n times. Therefore, a consumption saving of 12.5% may be achieved for each bit after the writing operation of this embodiment.

During reading the data, the code values after the data encoding are read from the flash memory cell and the decoding operation is performed according to the mapping relationship, where the decoding is an inverse operation of the encoding to obtain the corresponding original data.

According to the above mapping principle, each flash memory page includes a data area of 2048B and a redundant area of 64B. An encoding operation may be created. The host data is encoded and written into the flash memory cells. Due to the existence of the redundant area, the number of bits of the encoded data is larger than the number of bits of the original host data. Such encoding operation creates a new mapping relationship by combining the host data and the data with increased number of bits, so that the number of 0s in the data after the encoding operation is smaller than the number of 0s in the original host data, thereby achieving purposes of reducing the consumption of the flash memory chip, and prolonging the life span of the flash memory device.

A compression-encoding process is employed by an embodiment of the present invention is illustrated in detail below. The present invention employs an encoding as an embodiment with a simple implementation. Statistics are performed on occurrence frequencies of hexadecimal data in a data segment. The encoded number of bits is determined according to the occurrence frequencies. The code value having the highest occurrence frequency is 0, followed by 10, 110, 1110 ... in turn according to the frequencies. One bit is added each time and one 1 is added in the highest bit. In case of the same frequency, the encoded value

is determined by a hexadecimal value corresponding to the data. The smaller the value, the smaller the number of bits of the encoded value, and vice versa.

FIG. 9 shows the original 128-bit data without being processed by a compression operation. The compression operation is performed in an operational unit of 4 bits. According to statistics, all the number of combinations of 4-bit data unit in the data is shown in FIG. 10. A compression encoding is designed according to data writing frequencies of the statistical result, in which a correspondence between the data and the compression encoding is shown in FIG. 10. According to the statistics, the number of 0s in the original data without being processed by the compression operation is 72 and the number of 1s is 56.

A result shown in FIG. 11 may be obtained by performing the compression encoding operation on the original 128-bit data. The data after the compression operation has 125 bits, wherein the number of 0s is 32 and the number of 1s is 93. Compared with the data before the compression, it is found that the number of 0s is reduced by 40 and the total number of data bits is reduced by 3. Therefore, the number of 0s in the data may be effectively reduced, and at the same time the number of written data bits may be reduced by such compression encoding operation.

During the reading operation of the data, first, the written encoding is read from the flash cell, and the decoding is performed according to the correspondence between the compressed codes and the data in the compression operation, where the decoding operation is an inverse operation of the encoding to obtain the corresponding original data.

According to the above compression encoding/decoding algorithm, it has many implementations, and merely one is provided here as an example. The main purpose thereof is to reduce the number of bits of the written data, especially the number of 0s in the data by the compression algorithm, thereby achieving purposes of reducing the consumption of the flash memory, prolonging the life span of the device, as well as optimizing the writing speed, and reducing its power consumption.

Although only a few embodiments are introduced in the present invention for illustration,

it has many available algorithms, all of which are follow the guiding principle of the present invention and is apparent to those skilled in the art. In addition, the memory chip provided in the present invention includes not only NAND, NOR etc., other semiconductor memory chips having similar writing consumption all fall in the guiding principle and applying scope of the present invention, and changes apparent to those skilled in the art are within the scope of the present invention.

CLAIMS

What is claimed is:

1. A flash memory data read/write processing method, comprising:

Step 1: during writing the flash memory data, first performing an encoding process on data to be stored so that number of specific values in the processed data is reduced compared with that before the encoding, and writing the encoded data into a flash memory cell;

Step 2: during reading the flash memory data, first reading out the encoded data in the flash memory cell, then performing a decoding process corresponding to the encoding process in Step 1 on the read data, and outputting the decoded original data.

2. The flash memory data read/write processing method as claimed in claim 1, wherein when the data is binary data, the specific values are 0 or 1.

3. The flash memory data read/write processing method as claimed in claim 1, wherein Step 1 comprises performing the encoding process on the data to be stored at any of a system host side, a flash memory controller side, and a flash memory chip side.

4. The flash memory data read/write processing method as claimed in claim 1, wherein Step 2 comprises performing the decoding process on the read data at any of the system host side, the flash memory controller side, and the flash memory chip side.

5. The flash memory data read/write processing method as claimed in claim 1, further comprising storing the encoded/decoded information within the flash memory chip.

6. The flash memory data read/write processing method as claimed in any of the claims 1, 2, 3 and 4, wherein the number of the specific values in each set of binary data after the encoding process in Step 1 is no more than the number of the specific values in the corresponding set of binary data before the encoding, and Step 2 employs the decoding process corresponding thereto.

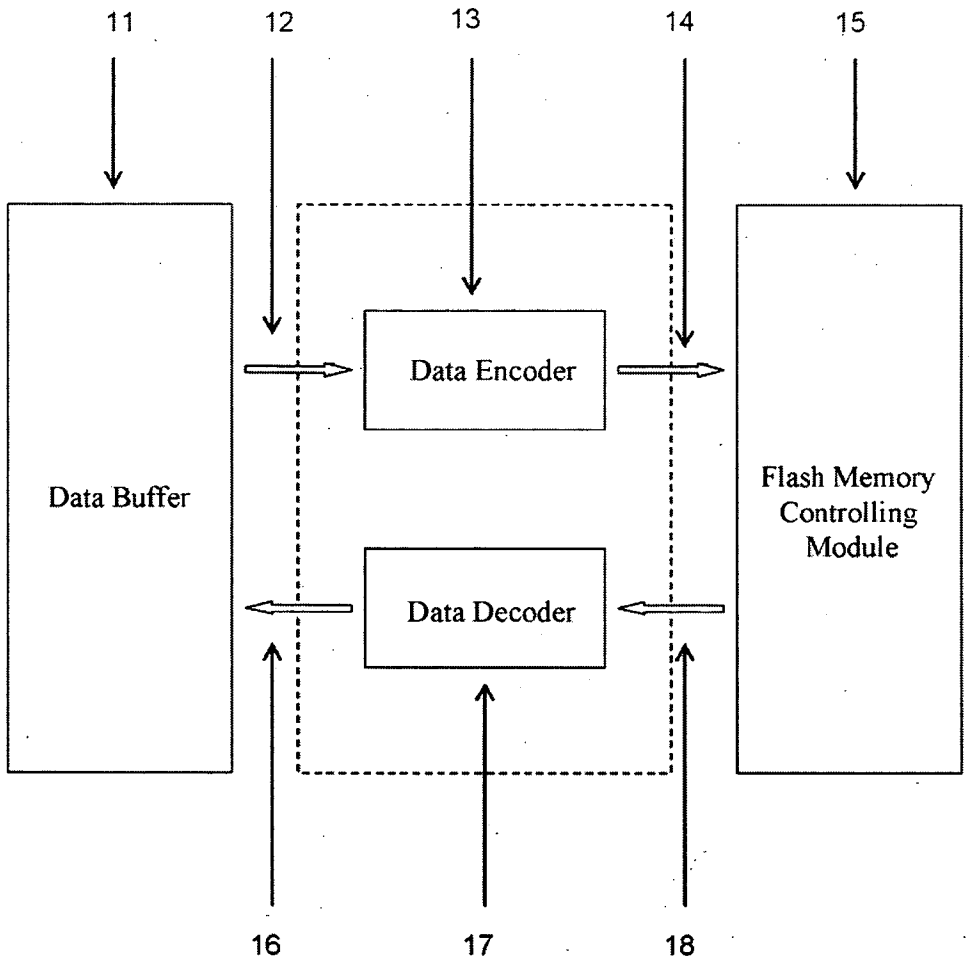
7. The flash memory data read/write processing method as claimed in claim 6, further comprising creating a mapping relationship between the data and the encoding, so that the

number of the specific values in the encoding is smaller than that in the data, wherein Step 1 comprises completing the encoding process of the data by querying the mapping relationship, and Step 2 comprises completing the decoding process of the data by querying the mapping relationship.

8. The flash memory data read/write processing method as claimed in claim 6, wherein the encoding process of Step 1 comprises performing an inverse on the data whose number of the specific values is larger than that of another code value, and the decoding process in Step 2 comprises performing the inverse on the inversed data in the encoding process to obtain the original data information.

9. The flash memory data read/write processing method as claimed in any of the claims 1, 2, 3 and 4, wherein in a set period, the total number of the specific values in all sets of binary data after the encoding process in Step 1 is smaller than the total number of the specific values in all sets of binary data before the encoding, and Step 2 employs the decoding process corresponding thereto.

10. The flash memory data read/write processing method as claimed in claim 1 or 2, wherein for an NAND-type flash memory, Step 1 comprises performing the encoding process on the binary data to be stored so that the number of 0s in the processed binary data is smaller than that before the encoding, and writing the encoded binary data into a flash memory cell.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Data Buffer
Data Encoder
Data Decoder
Flash Memory Controlling Module
16
17
18

FIG. 1

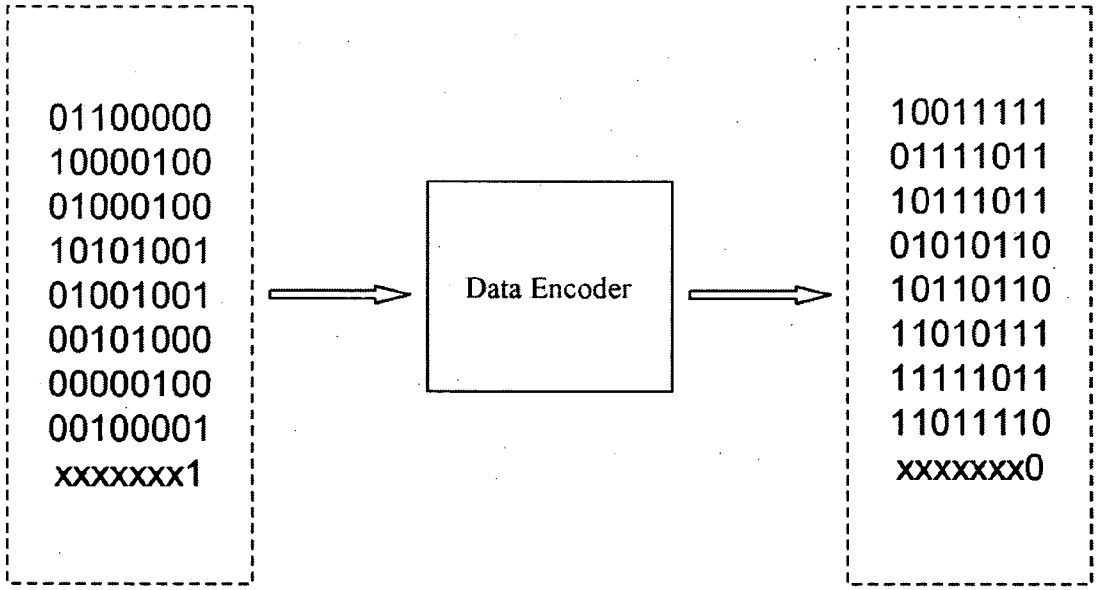
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FIG. 2

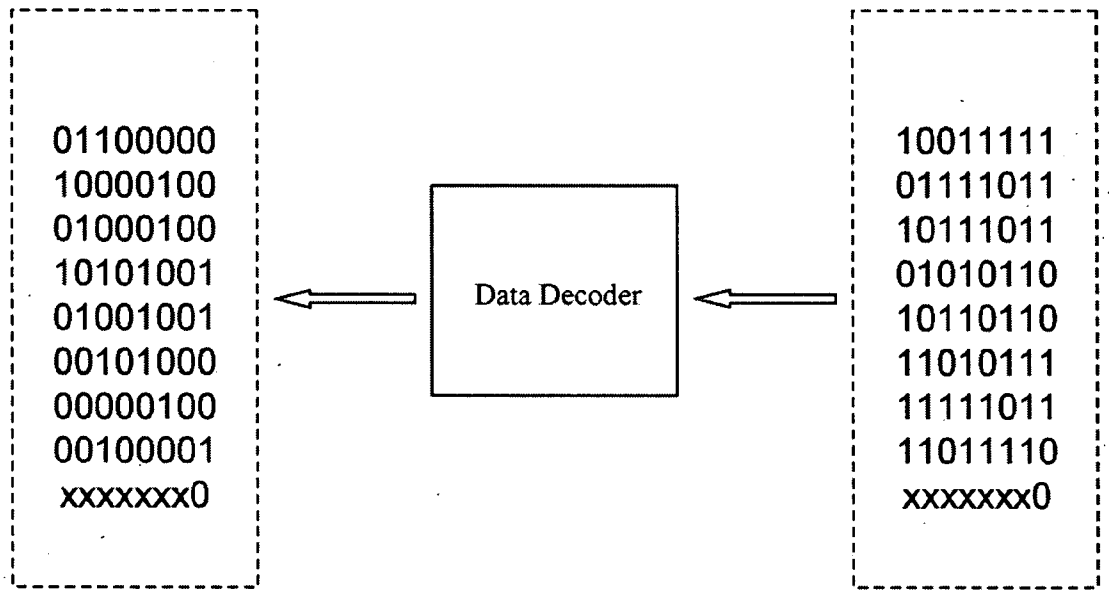
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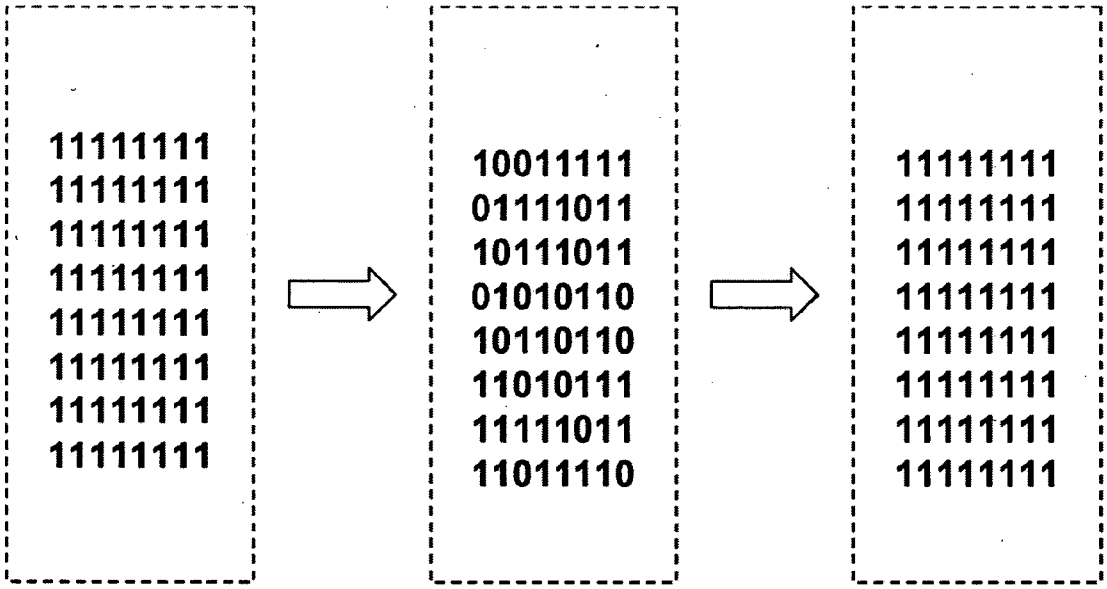
FIG. 3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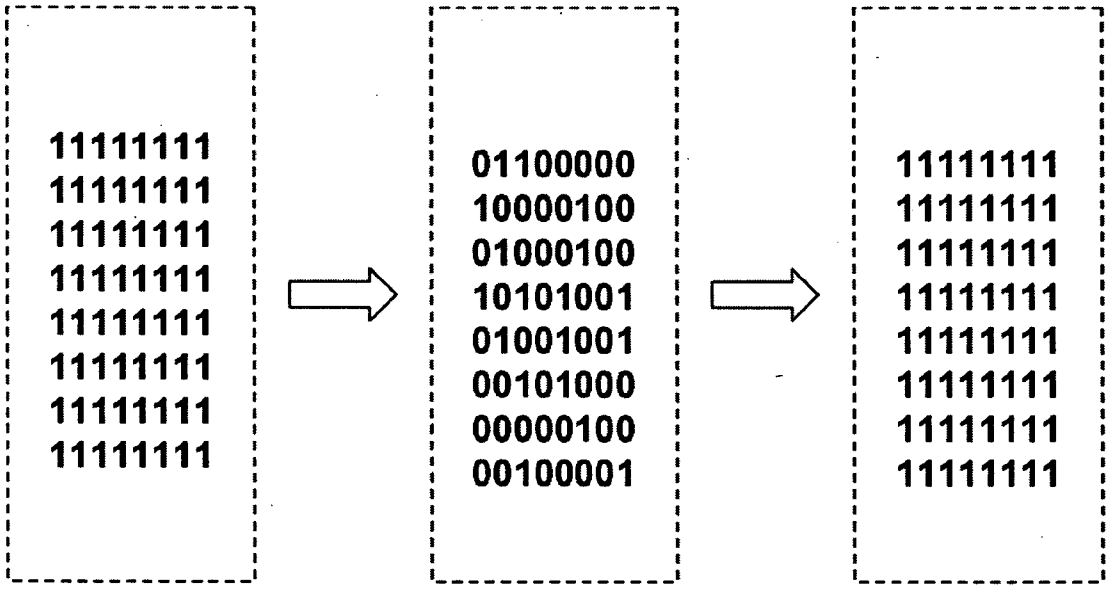
11111111
11111111
11111111
10011111
01111011
10111011
01010110
10110110
11010111
11111011
11011110
11111111
11111111
11111111
11111111
11111111
11111111
11111111
11111111

FIG. 4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11111111
11111111
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11111111
11111111
11111111
11111111
01100000
10000100
01000100
10101001
01001001
00101000
00000100
00100001
11111111
11111111
11111111
11111111
11111111
11111111
11111111
11111111

FIG. 5

0000	1001
0001	1010
0010	0101
0100	0111
1000	1011
0011	1101
0110	1110
1100	1111

FIG. 6

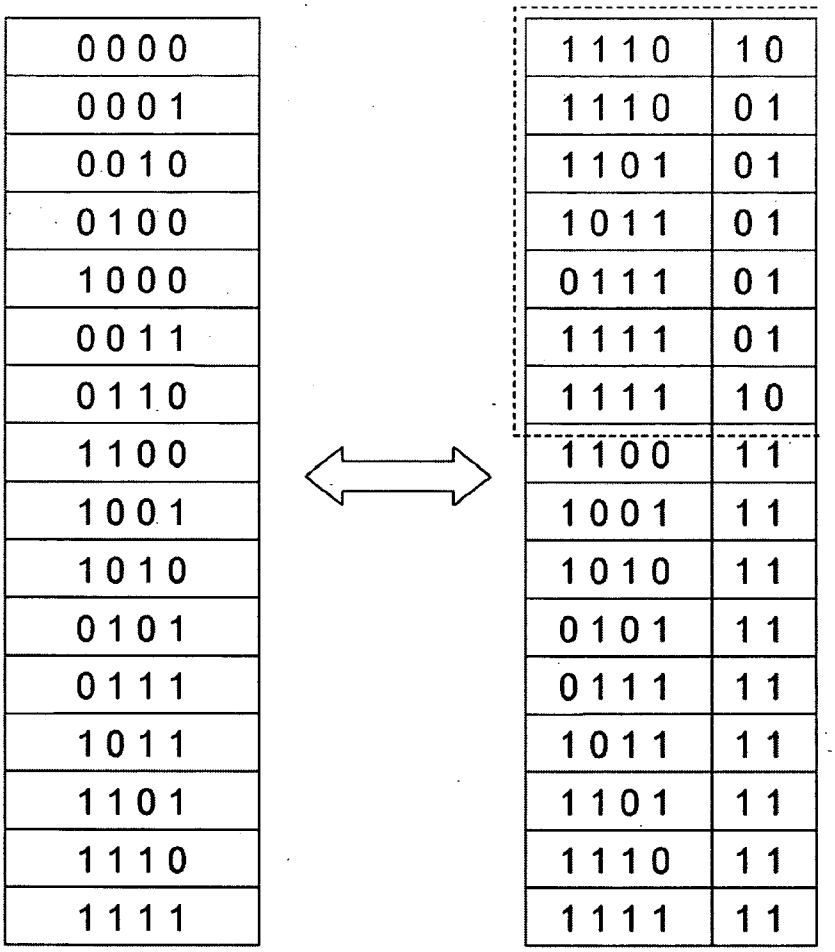
0000	11	1001	11
0001	11	1010	11
0010	11	0101	11
0100	11	0111	11
1000	11	1011	11
0011	11	1101	11
0110	11	1110	11
1100	11	1111	11

0000	01	1001	01
0001	01	1010	01
0010	01	0101	01
0100	01	0111	01
1000	01	1011	01
0011	01	1101	01
0110	01	1110	01
1100	01	1111	01

0000	10	1001	10
0001	10	1010	10
0010	10	0101	10
0100	10	0111	10
1000	10	1011	10
0011	10	1101	10
0110	10	1110	10
1100	10	1111	10

0000	00	1001	00
0001	00	1010	00
0010	00	0101	00
0100	00	0111	00
1000	00	1011	00
0011	00	1101	00
0110	00	1110	00
1100	00	1111	00

FIG. 7



0000	1110	10
0001	1110	01
0010	1101	01
0100	1011	01
1000	0111	01
0011	1111	01
0110	1111	10
1100	1100	11
1001	1001	11
1010	1010	11
0101	0101	11
0111	0111	11
1011	1011	11
1101	1101	11
1110	1110	11
1111	1111	11

FIG. 8

0011 0100 0101 0110
0001 1010 1010 1010
0010 1010 0100 0110
0100 1011 1010 0001
1000 0011 0100 0110
0011 1010 0011 0101
0110 1001 0100 1010
1100 1010 1001 0101

FIG. 9

1010		0	8
0100		10	5
0011		110	4
0110		1110	4
0101		11110	3
0001		111110	2
1001		1111110	2
0010	⟺	11111110	1
1000		111111110	1
1011		1111111110	1
1100		11111111110	1
0000		111111111110	0
0111		1111111111110	0
1101		11111111111110	0
1110		111111111111110	0
1111		1111111111111110	0

FIG. 10

1101	0111	1011	1011
1110	0001	1111	1100
1011	1010	1111	1111
1001	1111	0111	1111
1011	0101	1101	1001
1011	1101	1101	1111
1010	0111	1111	1110
0111	1110	1111	0

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2008/071142

A. CLASSIFICATION OF SUBJECT MATTER

see the extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G11C16/, G06F13/; EC: G11C16/10E, G06F13/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI;EPODOC;PAJ;CPRS;CNKI flash, memory, zero, binary, encod+, decod+, read+, writ+, stor+, eras+, speed, compress, ,reverse, inverse, map+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant
	CN1480953A (HONGFUJIN PRECISION IND SHENZHEN CO LTD) 10 Mar. 2004 (10.03.2004)	
Y	Description Page 4 Line 7- Page 5 Line 19, Figure 3	1-5
A	The whole document	6-10
	CN1249084A (TELEFONAKTIEBOLAGET ERICSSON LM) 29 Mar. 2000 (29.03.2000)	
Y	Description Page 1 Line 18- Page 2 Line 11, Claim1	1-5
A	The whole document	6-10
A	JP2000231793A (NEC CORP) 22 Aug. 2000 (22.08.2000) The whole document	1-10
PX	CN101083138A (YIZHENG STORAGE TECHNOLOGY CO LTD) 05 Dec. 2007 (05.12.2007) The whole document	1-10

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 Aug. 2008 (19.08.2008)	**04 Sep. 2008 (04.09.2008)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer WANG, Tao Telephone No. (86-10)62411627

Form PCT/ISA/210 (second sheet) (April 2007)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2008/071142

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN1480953A	10.03.2004	NONE	
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		HK1027228A1	06.02.2004

INTERNATIONAL SEARCH REPORT
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International application No.
PCT/CN2008/071142

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
		KR100375278B	10.03.2003
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JP2000231793A	22.08.2000	NONE	
CN101083138A	05.12.2007	NONE	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2008/071142

Continuation of: A. CLASSIFICATION OF SUBJECT MATTER

G11C16/10（2006.01）i

G06F13/00（2006.01）i