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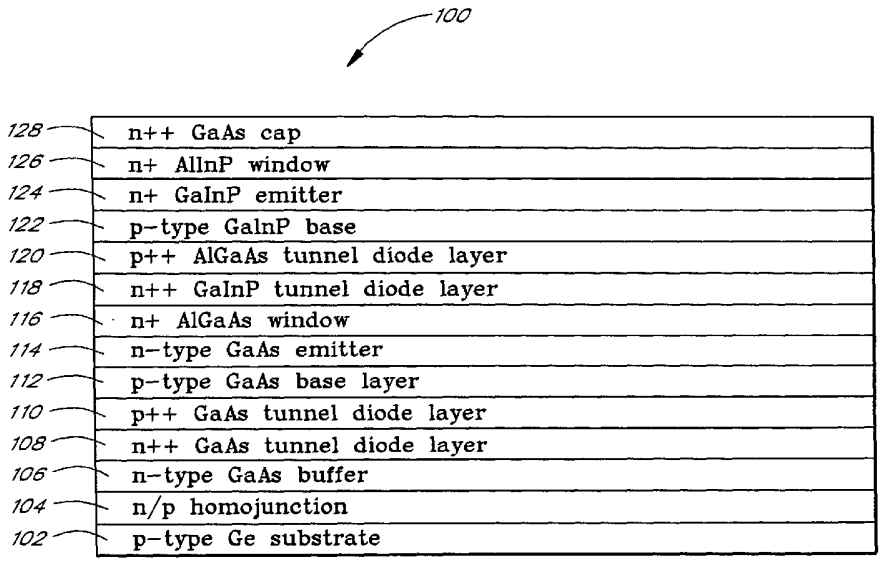
(54) **Title:** METHOD AND APPARATUS OF SOLAR CELL HAVING A BYPASS DIODE FOR REVERSE BIAS PROTECTION



(57) **Abstract:** Reverse bias protection for a solar cell is provided with a diode on the solar cell. In one embodiment, the Schottky diode is formed at the interface between a metallic diode contact and a semiconductor substrate on which the solar cell is grown. The solar cell includes a Ge substrate, which may further include a photoactive junction. In one embodiment, the Schottky diode is provided in a trough or recess extending through the solar cell layers to the front surface of the substrate. In this embodiment, the Schottky diode is electrically connected across some or all of the cells of the solar cell structure with a jumper bar or other suitable interconnect. In another embodiment, the Schottky diode is provided on a back surface of the substrate, with a C-clamp interconnecting at least one solar cell contact to the diode contact.

WO 03/012880 A2

METHOD AND APPARATUS OF SOLAR CELL HAVING A BYPASS DIODE FOR REVERSE BIAS PROTECTION

PRIORITY

Pursuant to 35 U.S.C. 119(e) and 37 C.F.R. 1.78, the present application claims priority to the provisional application entitled "Solar Cell Having A Schottky Diode For Reverse Bias Protection" Application Number 60/308,503, filed on July 27, 2001, the inventor of which is Chaw-Long Chu.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to semiconductor devices. More specifically, the present invention relates to methods and apparatuses of solar cells.

Description in the Related Art

Photovoltaic cells, commonly called solar cells, are well-known devices which convert solar energy into electrical energy. Solar cells have long been used to generate electrical power in both terrestrial and space applications. Solar cells offer several advantages over more conventional power sources. For example, solar cells offer a clean method for generating electricity. Furthermore, solar cells do not have to be replenished with fossil fuels. Instead, solar cells are powered by the virtually limitless energy of the sun. The solar cell is a particularly attractive device for generating energy in space, where low-cost conventional power sources are unavailable.

Solar cells are typically assembled into arrays of solar cells connected together in series, or in parallel, or in a series-parallel combination. The desired output voltage and current, at least in part, determine the number of cells in an array, as well as the array topology.

When all cells in an array are illuminated, each cell will be forward biased. However, if one or more of the cells is shadowed (i.e., not illuminated), by a satellite antenna or the like, the shadowed cell or cells may become reversed biased because of the voltage generated by the unshadowed cells. Reverse biasing of a cell can cause permanent degradation in cell performance or even complete cell failure. To guard against such damage, it is customary to provide protective bypass diodes. One bypass diode may be connected across several cells, or for enhanced reliability, each cell may have its own bypass diode. Multijunction solar cells are particularly susceptible to damage when subjected to reverse bias condition. Thus, multijunction cells in particular benefit from having the bypass diode protection.

Conventionally, a bypass diode is connected in an anti-parallel configuration, with the anode and the cathode of the bypass diode respectively connected to the cathode and the anode of the solar cell, so that the bypass diode will be reversed biased when the cells are illuminated. When a cell is shadowed, current through the shadowed cell becomes limited and the shadowed cell becomes reverse biased. The bypass diode connected across the shadowed cell in turn becomes forward biased. Most of the current will flow through the bypass diode rather than through the shadowed cell, thereby allowing current to continue flowing through the array. In addition, the bypass diode limits the reverse bias voltage across the shadowed cell, thereby protecting the shadowed cell.

Several different conventional methods have been used to provide solar cells with bypass diode protection. Each conventional method has its drawbacks. For example, in an attempt to provide increased bypass protection, one method involves locating a bypass diode between adjacent cells, with the anode of the bypass diode connected to one cell and the cathode of the diode connected to an adjoining cell. However, this technique typically requires that the cells be assembled into an array before the bypass diode protection can be added. This assembly method is difficult and inefficient. Furthermore,

this technique requires the bypass diodes to be added by the array assembler, rather than the cell manufacturer. In addition, this technique requires the cells to be spaced far enough apart so as to accommodate the bypass diode. This spacing results in the array having a lower packing factor, and thus, the array is less efficient on the area basis.

Another conventional technique providing a bypass diode for each cell requires that a recess be formed on the back of the cell in which a bypass diode is placed. Each cell is provided with a first polarity contact on a front surface of the cell and a second polarity contact is provided on a back surface of each cell. An "S" shaped interconnect must then be welded from a back surface contact of a first cell to a front surface contact of an adjoining cell. Thus, this technique disadvantageously requires the cells to be spaced far enough apart to accommodate the interconnect which must pass between the adjoining cells. Additional disadvantages of this method include the possibility of microcracks generated during formation of the recess. In addition, this technique requires a thick bondline of adhesive, thereby adding stress-risers, increasing stresses generated during temperature cycling. Furthermore, the conventional technique requires the connection of the interconnect to the adjoining cell to be performed by the array assembler as opposed to the cell manufacturer.

Thus, what is needed is a more efficient mechanism for providing reverse bias protection to a solar cell.

SUMMARY OF THE INVENTION

A method and an apparatus of solar cells having diodes for reverse bias protection. In one embodiment, a Schottky diode is formed at the interface between a metallic diode contact and a semiconductor substrate on which the solar cell is grown. In this embodiment, the solar cell circuit comprises a substrate having a front surface and a back surface, the substrate selected to have at least a portion thereof forming part of a Schottky diode. A multijunction solar cell structure includes at least a first photovoltaic cell having a first photoactive junction therein and a second photovoltaic cell having a second photoactive junction therein overlaying at least a portion of the first photovoltaic cell. A Schottky diode is electrically connected across the at least first and second photovoltaic cells to protect the at least first and said second photovoltaic cells against reverse biasing. The Schottky diode is formed at least in part from the substrate and a diode contact formed over the substrate.

In another aspect of the present invention, a solar cell structure having protection against reverse biasing comprises a substrate having a front surface and a back surface and at least one photovoltaic cell over the front surface of the substrate. A front contact is applied over the at least one photovoltaic cell, and a back contact is applied over the back surface of the substrate. A trough extends through the at least one photovoltaic cell to expose at least a portion of the front surface of the substrate. A diode is formed over the exposed portion of the front surface of the substrate in the trough. The diode contact and the substrate together form a Schottky diode in the trough, which is electrically connected across the at least one photovoltaic cell.

Additional features and benefits of the present invention will become apparent from the detailed description, figures and claims set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the invention, which, however, should not be taken to limit the invention to the specific embodiments, but are for explanation and understanding only.

Figure 1 illustrates the layers of a multijunction solar cell structure formed over a substrate in accordance with one embodiment of the present invention;

Figure 2 illustrate a first processing step for forming a solar cell with protection against reverse biasing, showing a photoresist layer formed over the multijunction solar cell structure of Figure 1;

Figure 3 illustrates a second processing step for forming a solar cell with protection against reverse biasing, showing a trough formed through the multijunction solar cell structure of Figure 2 extending to the front surface of the substrate;

Figure 4 illustrates a third processing step for forming a solar cell with protection against reverse biasing, showing the photoresist layer of Figure 3 removed and a n-type doped island isolated within the trough;

Figure 5 illustrates a fourth processing step for forming a solar cell with protection against reverse biasing, showing contacts formed on the structure;

Figure 6 illustrates a fifth processing step for forming a solar cell with protection against reverse biasing, showing a back cell contact formed on the back surface of the substrate;

Figure 7 illustrates a sixth processing step for forming a solar cell with protection against reverse biasing, showing a jumper bar connecting a front cell contact and a diode contact, and a second interconnect connecting the island with a p-type portion of the substrate;

Figure 8 illustrates an alternative embodiment of a solar cell with protection against reverse biasing, showing the metallic interconnects formed over insulator layers;

Figure 9 illustrates an alternative embodiment of a solar cell with protection against reverse biasing, showing a Schottky diode formed in a recess on the back surface of the solar cell structure;

Figure 10 illustrates a series of interconnected solar cell structures having Schottky diode protection when solar cells are exposed to light; and

Figure 11 illustrates a series of interconnected solar cell structures having Schottky diode protection when the cells are shadowed.

DETAILED DESCRIPTION

A method and an apparatus of solar cells having diodes for reverse bias protection.

For purposes of explanation, various specific details are set forth to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that these specific details may not be required to practice the present invention. In other instances, well-known devices are shown in block diagram form to avoid obscuring the present invention.

It should be understood that the present invention may contain circuits that can be manufacturable using well-known CMOS ("complementary metal-oxide semiconductor) technology, or other semiconductor manufacturing processes. In addition, the present invention may be implemented with other manufacturing processes for making digital devices.

In one embodiment, a multijunction solar cell circuit uses Schottky diodes as bypass diodes for providing reverse bias protection. A Schottky diode is formed at the interface between a metallic diode contact and a semiconductor substrate on which the solar cell is grown. In another embodiment, the solar cell is a multijunction cell formed from at least group III, IV, or V materials. The solar cell includes a Ge substrate, which may further include a photoactive junction. In this embodiment, a Schottky diode is provided in a trough or recess extending through the solar cell layers to a doped region on the front surface of the substrate. The Schottky diode is electrically connected across some or all of the cells of the solar cell structure with a jumper bar or other suitable interconnect. In yet another embodiment, the Schottky diode is provided on a back surface of the substrate, with a C-clamp interconnecting at least one solar cell contact to the diode contact.

In another embodiment, a solar cell structure comprises a substrate having a front surface and a back surface, the substrate selected to have a least a portion thereof forming

part of a Schottky diode. A multijunction solar cell structure includes at least a first photovoltaic cell having a first photoactive junction therein and a second photovoltaic cell having a second photoactive junction therein overlaying at least a portion of the first photovoltaic cell. A Schottky diode is electrically connected across the at least first and second photovoltaic cells to protect the at least first and said second photovoltaic cells against reverse biasing. The Schottky diode is formed at least in part from the substrate and a diode contact formed over the substrate.

In yet another embodiment, a solar cell structure having protection against reverse biasing comprises a substrate having a front surface and a back surface and at least one photovoltaic cell over the front surface of the substrate. A front contact is applied over the at least one photovoltaic cell, and a back contact is applied over the back surface of the substrate. A trough extends through the at least one photovoltaic cell to expose at least a portion of the front surface of the substrate. A diode is formed over the exposed portion of the front surface of the substrate in the trough. The diode contact and the substrate together form a Schottky diode in the trough, which is electrically connected across the at least one photovoltaic cell.

In another embodiment, the solar cell structure comprises a substrate having a front surface and a back surface and at least one photovoltaic cell over the front surface of the substrate. A front contact is applied over the at least on photovoltaic cell, and a back contact is applied over the back surface of the substrate. A recess extends through the back contact to expose the back surface of the substrate. A diode contact is applied over the back surface of the substrate in the recess. The diode contact and the back surface of the substrate together form a Schottky diode in the recess which is electrically connected across the at lest one photovoltaic cell. In one embodiment, this electrical connection is formed with a C-clamp that connects the diode contact to the front contact.

In another aspect of the present invention, a method of manufacturing a protected multijunction solar cell circuit is provided. A substrate is selected having a front surface and a back surface, the substrate having at least a portion thereof capable of forming a Schottky diode. A multijunction solar cell structure is formed over at least a portion of the front surface of the substrate. The multijunction solar cell structure includes at least a first photovoltaic cell having a first photovoltaic junction therein and a second photovoltaic cell having a second photoactive junction therein overlaying at least a portion of the first photovoltaic cell. A diode contact is formed over the substrate to form a Schottky diode at the interface between the diode contact and the substrate. The Schottky diode is electrically connected across the at least first and second photovoltaic cells to protect the at least first and said second photovoltaic cells against reverse biasing.

As discussed above, the solar cell may be a single junction or multijunction solar cell. In one embodiment, a bypass diode is provided on a multijunction solar cell structure, which may be a Schottky diode formed at the connection of a metallic contact and a semiconductor substrate. The solar cell/bypass diode device may be interconnected with other solar cells to form series and/or parallel strings of solar cells. The strings may be further connected to form a reliable and robust solar cell array. The solar cell array in one embodiment may be mounted to a space vehicle, thereby providing power to the space vehicle.

Figure 1 shows a sequence of III-V layers 104-128 which are grown sequentially on a Ge substrate 102 in one embodiment of the present invention to form a multijunction solar cell structure 100. The Ge substrate 102 may further include a photoactive junction. In one embodiment, the layers are epitaxially grown, meaning that they replicate the single crystalline structure of material. The growth parameters (deposition temperature, growth rate, compound alloy composition, and impurity dopant concentrations) are selected to provide layers with the desired electrical qualities and thickness, to thereby

obtain the desired overall cell performance. The epitaxial techniques which may be used to grow the cell layers include, by way o example, MOCVD (metal-organic chemical vapor deposition) epitaxy, sometimes called OMVPE (organic-metal vapor phase epitaxy), MBE (molecular beam epitaxy), and MOMBE (metal-organic molecular beam epitaxy).

In the illustrated embodiment, a GaAs buffer layer 106 is grown over at least a portion of the substrate 102. At the interface between layer 102 and layer 106 a photoactive junction is formed, constituting the lower cell of the solar cell structure. In the embodiment shown, when a p-type Ge substrate 102 is used, the diffusion of As form the n-type layer 106 forms an n/p homojunction 104 in the substrate 102. In another embodiment, when a n-type Ge substrate is used, the photoactive junction is an n+GaAs/n+Ge heterodiode.

As illustrated in Figure 1, a highly n doped GaAs layer 108 and a highly p doped GaAs layer 110 are grown over at least a portion of the GaAs buffer layer 106. The combined layers 108 and 110 function as a tunnel diode. A p-type GaAs layer 112 is grown on the tunnel diode layer 110, and an n-type GaAs emitter layer 114 is formed over the base layer 112. The base layer 112 and the n type emitter layer 114 together form a middle cell stage. A highly n doped A1GaAs window layer 116 overlays the emitter layer 114. A tunnel diode, including very highly doped n-type GaInP and p-type A1GaAs layers 118, 120, is grown over the window layer 116. An upper cell stage, including a p doped base layer 122 is a highly n doped emitter layer 124, is formed over the tunnel diode. The upper cell base layer and emitter layer are formed of GaInP.

In one embodiment, the last two layers grown for the solar cell are respectively a highly n doped A1InP window layer 126 and a highly n-doped GaAs cap layer 128. The window layer 126 is a thin layer of wide band gap material that passivates (reduces carrier recombination) the surface onto which the front surface ohmic contacts are deposited. In

one embodiment, the contacts are in grid-finger form, to balance low electrical resistance and high optical transparency. However, other contact patterns may be used as well. Formation of these contacts is described below.

It will be understood by one of ordinary skill in the art, that the three cells, three-junction, solar cell structure 100, illustrated in Figure 1, is only one of may possible cell embodiments which can be used. In another embodiment, a complementary structure, with the polarities of one or more layers switched (i.e., n doped layers are, instead, p doped, and p doped layers are, instead, n doped) may be used. For example, the cell and diode configurations illustrated in the figures and discussed below, can be changed from n/p to p/n. Also, the doping concentrations or layer thicknesses may be varied. Furthermore, in other embodiments, the solar cell structure 100 may include four or more photovoltaic cells, or only one or two cells. Similarly, the solar cell structure may alternatively include only one junction or two or more junctions. By way of example, in one embodiment, the cell structure 100 may include four junctions. It will also be appreciated that the term "formed over" as used herein does not limit a layer to being formed directly on top of another layer, and thus, a structure having a layer "formed over" another layer can include one or more additional layers formed between the two layers.

Furthermore, the solar cell structure 100 may include cells made from other materials, including but not limited to AlGaAs or InP. In other embodiments, the substrate 102 may be formed using a variety of different materials. For example, the solar cell 100 may use other semiconductors, including but not limited to GaAs, Si, or InP for the substrate, rather than the Ge substrate 102 illustrated in Figure 1. Alternatively, insulating substrates, such as sapphire, may be used. In one embodiment, the substrate 102 is a single crystal. If the solar cell structure 100 is intended for space use, such as on a space vehicle or satellite, then the cell materials are space-qualified for the appropriate

space environment. For example, the solar cell structure 100 may be space qualified to operate in an AM0 radiation environment.

Solar cell structures incorporating bypass diode protection, and their associated methods of fabrication, will now be described. Figure 2-9 illustrate the formation of solar cell structures having a Schottky diode formed at the junction of the Ge substrate and a metallic contact formed on the Ge substrate. More particularly, Figures 7 and 8 describe embodiments in which the Schottky diode is formed in a trough or recess extending through the solar cell structure down to the upper surface of the substrate (i.e., the surface on which the solar cell is grown). Figure 9 describes an embodiment in which the Schottky diode is formed on the back surface of the substrate.

In one embodiment, the solar cell structure having bypass diode protection is formed by first epitaxially growing the layers shown in Figure 1 by conventional MOCVD and/or MBE technologies. As shown in Figure 2, portions of the front surface of the layers are then protected with a photoresist layer 130, which is exposed through a photomask (not shown) patterned to create open areas in the front surface of the structure. As shown in Figure 3, etching occurs through these open areas to form a trough 132 through the layers of the solar cell structure.

The etching process creates a trough 132 that extends down to the front surface of the n/p homojunction 104 in the germanium substrate 102, such that the exposed surface of the Ge substrate is in an arsenic doped region. In one embodiment, a etchant to remove layers 106-128 is HC1 and a mixed acid comprising H_2SO_4, H_2O_2, and H_20 at a volume basis of (1:8:5). Also, an HBr etchant with a Br percentage greater than about 48% can be used to etch the epi-grown layers.

In the illustrated embodiment, portions of the n/p homojunction 104 formed in the Ge substrate 102 are next removed within the trough 132 with a photoresist layer (not shown) and by using a second etchant, a solution of $HF/H_2O_2/H_2O$ prepared at various

ratios. For example, the ratio can vary from (1:1:2) to (1:1:10) on a volume basis. The etching temperature can vary from about 20°C to about 35°C. As shown in Figure 4, this etching step leaves an island 152 in the trough 132, the island 152 being part of the Ge substrate 102. The front surface of the island 152 is n-type Ge, more As-doped germanium. A recess 154 surrounds the island 152, exposing portion a p-type 156 of the Ge substrate.

After masking to form the regions described above, the photoresist layers are removed using acetone to leave the structure solar cell structure shown in Figure 4. Microstripping techniques may be used to remove any residual photoresist left remaining after the acetone removal process. One the photoresist layer is removed, the contact fabrication process, including corresponding photoresist coating, baking, exposing, developing, metal evaporation, and lift off operations, can take place.

To form contacts on the structure, photoresist layers (not shown) are coated over the whole front surface of the structure, including in the trough 132. The photoresist layers are then baked and exposed with a photomask which leaves opened areas where contacts are to be deposited to the front surface of the Ge substrate 102 on the island 152, to a small region of the exposed n-doped GaAs layer cap layer 128, and to the p-type Ge substrate surface 156. Metals are evaporated into the exposed areas and over the remaining photoresist layer. As shown in Figure 5, a front cell contact 134 is thereby formed on the cap layer 128, and contacts 136 and 158 are formed on the front surface of the island 152 in the trough 132. A fourth contact 160 is provided on the exposed surface 156 of the p-type Ge substrate. The contact 136 is made of a titanium material or other types of materials such as, for example Ti/Pd/Ag, to facilitate the formation of a Schottky diode as described below. The contact 134 may similarly be made of titanium or other suitable material. The contact 158 is made of gold or other suitable material, and the contact 160 is made of gold, titanium or other suitable material.

In addition to these contacts, the photoresist also provides open slots to provide gridlines and bars/pad contacts to the cell. Next, a lift-off process is performed. The solar cell structure 100 is immersed in acetone, causing the photoresist to swell, and thereby breaks the metal film everywhere except on the regions designated to retain contacts, including contacts 134, 136, 158 and 160.

As shown in Figure 6, a back metal contact 138 is formed by evaporating a metallic material such as, for example Ag, over the back surface of the Ge substrate 102. The contacts 134, 136, 158, 160 and 138 are then heat-treated or sintered at about 400°C for about 5 minutes. Ohmic contacts are thereby formed between layer 134 and cap layer 128, and layer 138 and substrate 102. Ohmic contacts are also formed between the contact 158 and the n-type island 152, and the contact 160 and the p-type substrate 102. It will be appreciated that the contact 160 need not be provided on the front surface of the substrate, and therefore, could be provided at a p-type portion of the substrate on the back as well. A Schottky diode 142, described below, is formed between the As-doped Ge 152 and contact 136. A further processing step (not shown) may also include using the front contact metal 134 as an etch-mask, and etching the GaAs cap layer 128 off a major part of the exposed front surface. The cap layer 128 remains under the metallized areas, forming part of a low resistance contact mechanism. Using a resist mask to protect the front metallic area, on the rest of the surface an anti-reflecting layer may be deposited.

As shown in Figure 7, the solar cell structure 100 is completed by forming a first interconnect 162 between the contact 158 and the germanium substrate contact 160. It will be appreciated that the contact 158, the interconnect 162 and the contact 160 could be made from on piece of material. In one embodiment, the interconnects may be jumper bars made of a material such as silver, although other suitable materials, such as silver coated invar, covar or other alloys and metals may be used as well.

The interface of the metallic diode contact 136 and the As-doped semiconductor substrate 152 forms a Schottky diode 142. In one embodiment, the contacts are sintered at a temperature of about 400°C for about 5 minutes, although sintering temperatures in the range of about 350°C to 450°C can also be used. In another embodiment, sintering takes place at a temperature less than about 450°C in order to avoid formation of a high ohmic resistance contact between the contact 136 and the As-doped island 152. In one embodiment, after the metallic contacts are sintered, a second sintering step can be used to make the contacts stronger without damaging the diode characteristics. This second sintering takes place at 300°C for about 5 minutes. The Schottky diode provides protection against reverse biasing for the top, middle and bottom cells of the solar cell structure across which it is connected by the interconnects 140 and 162. It will be appreciated that the Schottky diode can also be formed to protect a fewer or greater number of cells. By proper interconnection, the Schottky diode can be used to protect both p/n and n/p solar cells.

It will be appreciated that, for one embodiment, the formation of the Schottky diode is facilitated by the selection of a highly As doped germanium substrate such as, for example, on the order of about 5×10^{16} cm^{-3} or higher. This doping can occur during n-type Ge ingot growth or by As diffusion during GaAs growth (for both n-type Ge and p-Type Ge). In the embodiment described above, the Ge substrate 102 is doped with Ga to make it p-type, and the following MOCVD process will diffuse high concentration As into the Ge substrate at layer 152. This layer of As-doped Ge 152 can generate a Schottky diode with the Ti alloy 136 used as a metal contact. For an n-type Ge substrate, if As is used as the n-type dopant, a Schottky diode can be formed by Ti alloy deposition without additional As diffusion. In one embodiment, the diode contacts are formed of a titanium material such as, for example, a Ti/Pd/Ag alloy. However, other metals or alloys,

including but not limited to Ti/Au/Ag and Ti/Ge/Ni/Ag, can also form a Ge-Schottky diode.

Figure 8 illustrates another embodiment of a solar cell structure 100 similar to the embodiment of Figure 7. However, instead of using a jumper bar, the front cell contact 134 and the diode contact 136 are electrically connected with an interconnect 140 running along the walls of the trough 132. An insulating material 144, which may be a polyimide material, separates the metallic interconnect from the walls of the trough. Other materials, such Al_2O_3, TiOx, and other inorganic materials can also function as the insulator. For the connection 162 between the contact 158 and the p-type Ge contact 160, a second insulating material 146 can be used to separate the interconnect 162 from the walls of the island 152.

Figure 9 illustrates another embodiment of a solar cell structure having bypass diode protection. In this embodiment, a Schottky diode 142 is positioned on the back surface of the Ge substrate 102. To form this structure, the layers as shown in Figure 1 are first deposited. In one embodiment, the Ge substrate is doped with As at the back surface, with doping occurring during ingot growth from residual GaAs inside the MOCVD chamber, or by a specific As diffusion step by turning the Ge wafer upside down. This forms as As-doped region 164 at the bottom surface of the substrate. Then, the front contact 134 is formed as described above. The back contact 138 is formed, with a mask protecting an area of the back surface of the Ge substrate 102 in order to form a recess 148.

To form the diode contact 136 in the recess 148, a photoresist layer is coated over the entire back surface, and is baked an exposed with a photomask to leave opened areas where the contact is to be deposited to the back surface of the substrate. In one embodiment, the metallic diode contact, which may be a titanium material or a Ti/Pd/Ag alloy, is evaporated into the exposed area and over the remaining photoresist layer. A lift-

off process is used to remove the photoresist, by immersing the solar cell structure in acetone, causing the photoresist to swell, and thereby breaks the metal film everywhere except on the regions designated to retain the diode contact 136.

The interface of the metallic diode contact 136 and the Ge substrate 102 at As-doped region 164 forms a Schottky diode in the recess 148. In one embodiment, the back side metal contact 138 is Au/Ge/Ni/Ag, which will not form a Schottky diode with the Ge substrate. The Schottky diode 142 is electrically connected with the front contact using a C-clamp 150, which is made of Ag or other suitable material. Thus, the C-clamp electrically connects the diode across all of the photovoltaic cells.

A second contact 162 is provided on the back surface of the Ge substrate 102 to connect the n-type Ge substrate with the surrounding p-type Ge substrate. Thus, a contact 164 is formed on a p-type portion of the back surface, and an interconnect 170 is used to adjoin the contacts 166 and 168. As described above, the second contact on the As-doped portion of the germanium substrate, and the contact 168 may be made of titanium, gold or other suitable materials to form an ohmic contact with the p-type portion of the substrate.

A variety of other interconnect techniques may be used to connect the solar cell structure to the Schottky diodes discussed above. The final choice may depend on the additional complexity and the effect on cell yields and costs which results from the use of these alternative approaches.

Using at least some of the techniques described above, a solar cell incorporating a Schottky diode with cascaded cells has achieved efficiencies of well over 25%, and even over 27.0%. These efficiencies are comparable to conventional cascade cells lacking the Schottky diode. In one embodiment, a Schottky diode made with a Ge substrate has a forward bias voltage drop of approximately 0.3 to 0.6 volts when conducting 400 mA of forward current. Thus, compared to the forward voltage of an integrally formed GaAs bypass diode (1.6 V at 1 Isc and 2.1 V at 6 Isc), such as described in copending U.S.

Patent Application Serial No. 09/314,597, filed May 19, 1999, the Ge diode generates less heat during operation. The leakage current of the Schottky diode, tested at –2.5V, is about –0.2 to –1.1 mA. This falls well within a standard required specification of –0.6 mA.

Figure 10 illustrates a device 1000 with a series of interconnected solar cell structures having bypass diodes protection in accordance to one embodiment of the present invention. In one embodiment, the solar cell structures 1002-1006 are multijunction solar cell structures as shown in Figure 7. The solar cell structures 1002-1006 further contain bypass diodes 1010-1014 and the bypass diodes 1010-1014 are deposited on the solar cell structures 1002-1006 for providing reverse bias protection. The device 1000 further includes cell interconnections 1020-1024 as coupling mechanism between individual solar cells. In one embodiment, the bypass diodes 1010-1014 are Schottky diodes wherein one terminal of the Schottky diode is connected to the substrate of the solar cell while the other terminal of the Schottky diode is connected to the front cell contacts via interconnecting wires 1030. It should be apparent to one skill in the art that other arrangements between the solar cells or solar cell structures are possible.

When the solar cell structures 1002-1006 are exposed to light, each illuminated cell, in one embodiment, becomes forward biased and generates power and/or electrical current. As discussed earlier, when the solar cell structure is in forward bias mode, the bypass diode, such as for example a Schottky diode, comes reverse biased. In operation, the solar cell structure 1002 generates electrical current and passes the current from the solar cell structure 1002 to the solar cell structure 1004 through the cell interconnection 1020. Similarly, the solar cell structure 1004 transports the electrical current to the solar cell structure 1006 via the cell connection 1022. It should be apparent to one skilled in the art that other arrangements of the solar cell structures are possible within the framework of the present invention.

Figure 11 illustrates a solar cell structure 1100 having bypass diode for reverse bias protection when the solar cell structure 1100 is under the shadow. The solar cell structure 1100 is connected with a first cell connection 1110 for receiving electrical current and a second cell connection 1112 for sending the electrical current. The solar cell structure 1100 further includes a bypass diode 1104 for providing reverse bias protection. In one embodiment, the bypass diode 1104 is a Schottky diode.

In operation, when the solar cell structure 1102 is shadowed or not exposed to the light, the shadowed solar cell structure 1102, in one embodiment, comes the reverse biased while the bypass diode, such as a Schottky diode, comes forward biased. As illustrated in Figure 11, the bypass diode passes electrical current received from the cell connection 1110 to the stage, which is not shown in Figure 11, via the cell connection 1112. In other words, when the solar cell structure 1102 is shadowed, current through the shadowed structure 1102 becomes limited and the shadowed structure becomes reverse biased. The bypass diode connected across the shadowed structure in turn becomes forward biased. Most of the current will flow through the bypass diode 1104 rather than through the shadowed structure 1102, thereby allowing current to continue flowing through the shadowed structure 1102. In addition, the bypass diode 1104 limits the reverse bias voltage across the shadowed structure 1102, thereby protecting the shadowed structure 1102. It should be apparent to one skilled in the art that this concept can be applied to various related solar cell structure arrangements.

In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense.

WHAT IS CLAIMED IS:

1. A multijunction solar cell circuit comprising:

a substrate having a front surface and a back surface, said substrate selected to have a portion thereof forming part of a Schottky diode;

a multijunction solar cell structure overlaying at least a portion of said front surface of said substrate, said multijunction solar cell structure including at least a first photovolatic cell having a first photoactive junction therein and a second photovoltaic cell having a second photoactive junction therein overlaying at least a portion of said first photovoltaic cell; and

a Schottky diode electrically connected across said at least first and second photovoltaic cells to protect said at least first and said second photovoltaic cells against reverse biasing, said Schottky diode being formed at least in part from said substrate and a diode contact formed over said substrate.

2. The circuit of Claim 1, wherein the substrate is germanium.

3. The circuit of Claim 1, wherein the substrate is p-type germanium and the substrate is n-doped to form a bottom cell homojunction therein.

4. The circuit of Claim 1, wherein the substrate is p-type germanium.

5. The circuit of Claim 4, wherein at least a portion of the substrate is doped with arsenic.

6. The circuit of Claim 5, wherein the Schottky diode is formed at least in part from the portion of the substrate doped with arsenic.

7. The circuit of Claim 6, further comprising an interconnect between the portion of the substrate doped with arsenic and a p-type portion of the substrate.

8. The circuit of Claim 6, wherein the substrate is doped with arsenic on the front surface of the substrate.

9. The circuit of Claim 6, wherein the substrate is doped with arsenic on the front surface of the substrate.

10. The circuit of Claim 1, wherein the first photovolatic cell is made of GaAs.

11. The circuit of Claim 1, wherein the second photovoltaic cell is made of GaInP.

12. The circuit of Claim 1, wherein the multijunction solar cell structure includes a third photovoltaic cell provided below the first photovolatic cell.

13. The circuit of Claim 12, wherein the third photovoltaic cell is a homojunction.

14. The circuit of Claim 1, wherein the multijunction solar cell structure includes a trough that exposes said front surface of said substrate.

15. The circuit of Claim 14, wherein the Schottky diode is formed in said trough.

16. The circuit of Claim 15, wherein said Schottky diode is electrically connected across said at least first and second photovoltaic cells with a jumper bar.

17. The circuit of Claim 1, wherein said Schottky diode is provided on said back surface of said substrate.

18. The circuit of Claim 17, wherein said Schottky diode is electrically connected across said at least first and second photovoltaic cells with a C-shaped clamp.

19. The circuit of Claim 1, wherein said diode contact comprises titanium.

20. The circuit of Claim 19, wherein said diode contact is made of Ti/Pd/Ag.

21. The circuit of Claim 1, wherein the Schottky diode has a forward voltage drop of about 0.3 to 0.6 volts when conducting 400 mA of forward current.

22. The circuit of Claim 1, comprising at least two said multijunction solar cell structures, each of said structures having a Schottky diode electrically connected across said at least first and second photovoltaic cells of said structures, wherein each of said structures are interconnected to one another.

23. A solar cell having protection against reverse biasing, comprising:

a substrate having a front surface and a back surface;

at least one photovoltaic cell over said front surface of said substrate;

a front contact over said at least one photovoltaic cell;

a trough through said at least one photovolatic cell to expose at least a portion of said front surface of said substrate;

a Schottky diode formed in said trough electrically connected across said at least one photovoltaic cell; and

a back contact over said back surface of said substrate.

24. The solar cell structure of Claim 23, wherein the substrate is germanium.

25. The solar cell structure of Claim 24, wherein the substrate is p-type germanium, and a portion of the germanium substrate is doped with arsenic.

26. The solar cell structure of Claim 25, wherein the diode contact is positioned over the arsenic-doped portion of the germanium substrate.

27. The solar cell structure of Claim 26, further comprising an interconnect between the arsenic-doped portion of the germanium substrate and a exposed p-type portion of the germanium substrate.

28. The solar cell structure of Claim 23, comprising a plurality of photovoltaic cells over said front surface of said substrate.

29. The solar cell structure of Claim 23, wherein the diode contact comprises titanium.

30. The solar cell structure of Claim 29, wherein the diode contact is made of Ti/Pd/Ag.

31. The solar cell structure of claim 23, further comprising an interconnect between said front contact and said diode contact.

32. The solar cell structure of Claim 31, wherein the interconnect is a jumper bar.

33. A solar cell structure having protection against reverse biasing, comprising:

a substrate having a front surface and a back surface;

at least one photovoltaic cell over said front surface of said substrate;

a front contact over said at least one photovoltaic cell;

a back contact over said back surface of said substrate;

a recess extending through said back contact to expose said back surface of said substrate;

a diode contact over said back surface of said substrate in said recess; and

a Schottky diode formed in said recess electrically connected across said at least one photovoltaic cell.

34. The solar cell structure of Claim 33, wherein said Schottky diode is electrically connected across said at least one photovoltaic cell with a C-shaped clamp.

35. The solar cell structure of Claim 33, wherein the substrate is germanium.

36. The solar cell structure of Claim 33, wherein the substrate is p-type germanium, and the diode contact is formed over an arsenic-doped portion of the germanium substrate.

37. The solar cell structure of Claim 36, further comprising an interconnect between the arsenic-doped portion of the germanium substrate and an exposed p-type portion of the germanium substrate.

38. The solar cell structure of Claim 33, comprising a plurality of photovoltaic cells over said front surface of said substrate.

39. The solar cell structure of Claim 33, wherein the diode contact comprises titanium.

40. The solar cell structure of Claim 39, wherein the diode contact is made of Ti/Pd/Ag.

41. A solar cell structure having protection against reverse biasing, comprising;

an p-type germanium substrate having a front surface and a back surface;

at least one photovoltaic cell over said front surface of said substrate;

a front contact over said at least one photovoltaic cell;

a trough through said at least one photovoltaic cell to expose an arsenic-doped surface on said front surface of said substrate;

a recess surrounding said exposed portion of said front surface of said substrate to expose a p-type surface of the germanium substrate;

a diode contact comprising titanium on said arsenic-doped surface on said front surface of said substrate in said trough, wherein said diode contact and said arsenic-doped surface form a Schottky diode;

a first metallic interconnect between said front contact and said diode contact; and

a second metallic interconnect between said arsenic-doped surface on said front surface of said substrate and said exposed p-type surface of said germanium substrate.

42. The solar cell structure of Claim 41, wherein said arsenic-doped surface has an arsenic concentration of about 5×10^{16} cm^{-3} or higher.

43. A method of manufacturing a protected multijunction solar cell circuit, comprising:

selecting a substrate having a front surface and a back surface, said substrate having at least a portion thereof capable of forming a Schottky diode;

forming a multijunction solar cell structure over at least a portion of said front surface of said substrate, said multijunction solar cell structure including at least a first photovoltaic cell having a first photoactive junction therein and a second photovoltaic cell having a second photoactive junction therein overlaying at least a portion of said first photovoltaic cell;

forming a diode contact over said substrate at said portion of capable of forming a Schottky diode; and

electrically connecting a Schottky diode formed at the interface between the diode contact and the substrate across said at least first and second photovoltaic cells to protect said at least first and said second photovoltaic cells against reverse biasing.

44. The method of Claim 43, further comprising interconnecting said multijunction solar cell structure to another multijunction solar cell structure.

45. The method of Claim 43, wherein the substrate is germanium.

46. The method of Claim 45, wherein the substrate is p-type germanium.

47. The method of Claim 46, wherein the substrate is n-doped to form a bottom cell homojunction therein.

48. The method of Claim 43, wherein the portion capable of forming a Schottky diode is doped with arsenic.

49. The method of Claim 43, wherein the first photovoltaic cell is made of GaAs.

50. The method of Claim 43, wherein the second photovoltaic cell is made of GaInP.

51. The method of Claim 43, wherein forming the multijunction solar cell structure further comprises forming a third photovoltaic cell before forming the first photovoltaic cell.

52. The method of Claim 51, wherein the third photovoltaic cell is a homojunction.

53. The method of Claim 43, further comprising forming a trough in the multijunction solar cell structure that exposes said front surface of said substrate.

54. The method of Claim 53, comprising forming said diode contact in said trough.

55. The method of Claim 54, wherein said Schottky diode is electrically connected across said at least first and second photovoltaic cells with a jumper bar.

56. The method of Claim 43, comprising forming said diode contact on said back surface of said substrate.

57. The method of Claim 56, wherein said Schottky diode is electrically connected across said at least first and second photovoltaic cells with a C-shaped clamp.

58. The method of Claim 43, wherein said diode contact comprises titanium.

59. The method of Claim 58, wherein said diode contact is made of Ti/Pd/Ag.

60. A semiconductor device comprising:

a substrate having first side and second side;

a multijunction having at least a top layer and a bottom layer deposited on a portion of the first side of the substrate, wherein the bottom layer of the multijunction is in contact with the first side of the substrate;

a contact deposited on the top side of the multijunction;

a bypass diode, having first and second terminals, deposited on another portion of the first side of the substrate;

a first connection wire coupled between the contact and the first terminal of the bypass diode; and

a second connection wire coupled between the second terminal of the bypass diode and the first side of the substrate.

61. The semiconductor device of claim 60 further comprising a back metal contact coupled to the second side of the substrate.

62. The semiconductor device of claim 61, wherein the substrate is germanium.

63. The semiconductor device of claim 60, wherein the substrate is p-type germanium and the substrate is n-doped to form a bottom cell homojunction therein.

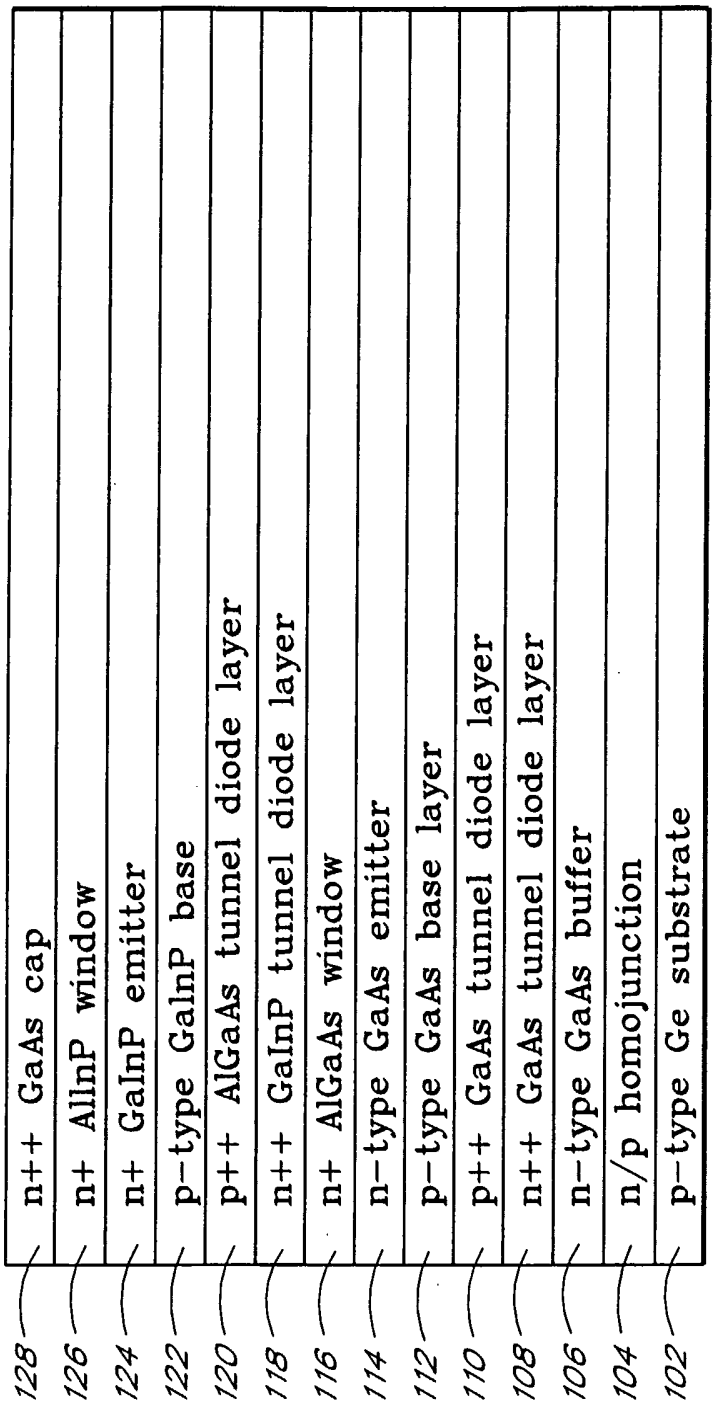
64. The semiconductor device of claim 60, wherein the bypass diode is a Schottky diode.

65. The semiconductor device of claim 64, wherein at least a portion of the substrate is doped with arsenic.

66. The semiconductor device of claim 65, wherein the Schottky diode is formed at least in part from the portion of the substrate doped with arsenic.

67. The semiconductor device of claim 66, wherein the multijunction includes at least two solar cells.

68. The semiconductor device of claim 66, wherein the multijunction has one solar cell.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n++ GaAs cap
n+ AlInP window
n+ GaInP emitter
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p++ AlGaAs tunnel diode layer
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n+ AlGaAs window
n-type GaAs emitter
p-type GaAs base layer
p++ GaAs tunnel diode layer
n++ GaAs tunnel diode layer
n-type GaAs buffer
n/p homojunction
p-type Ge substrate
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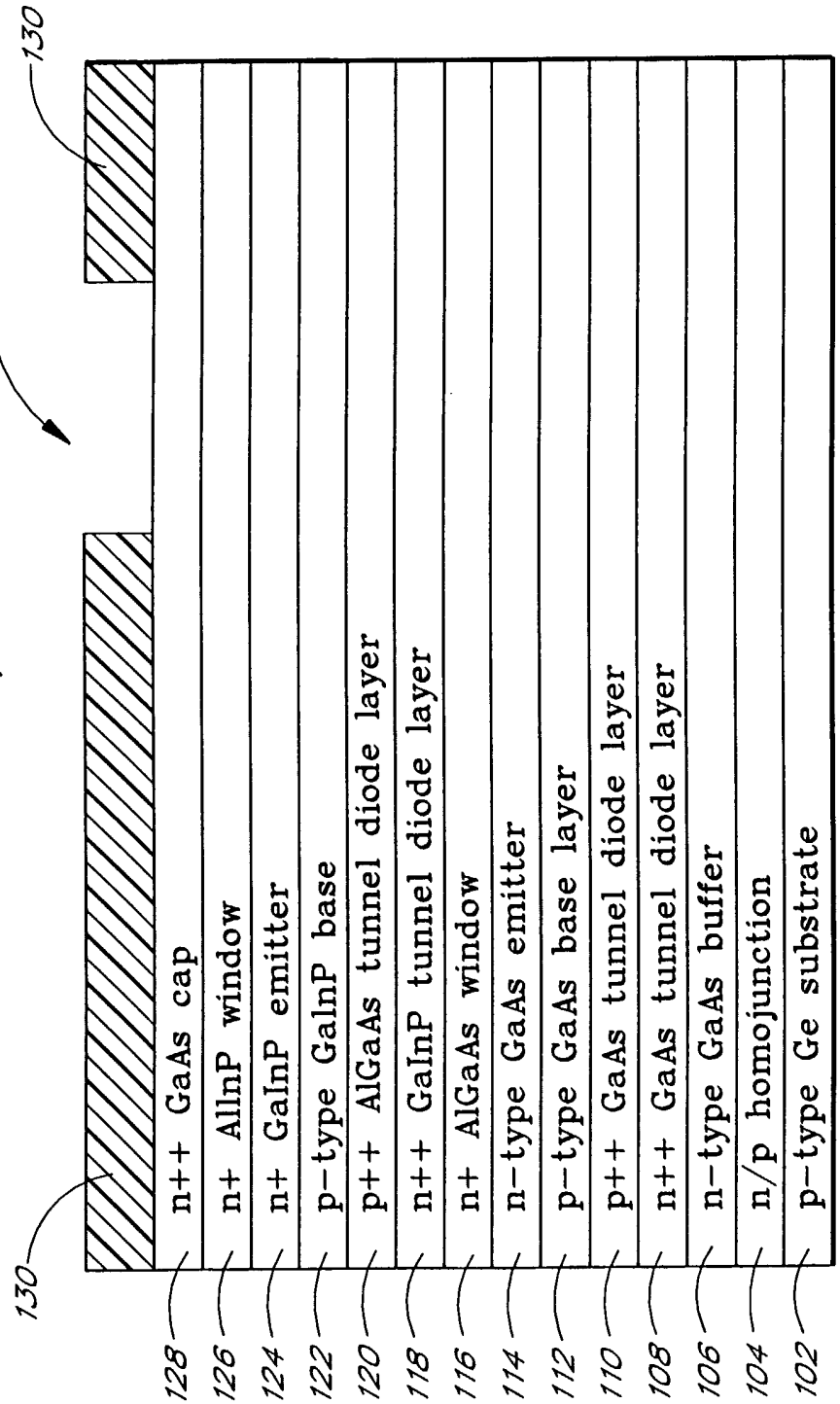
FIG. 1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128 n++ GaAs cap
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124 n+ GaInP emitter
122 p-type GaInP base
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116 n+ AlGaAs window
114 n-type GaAs emitter
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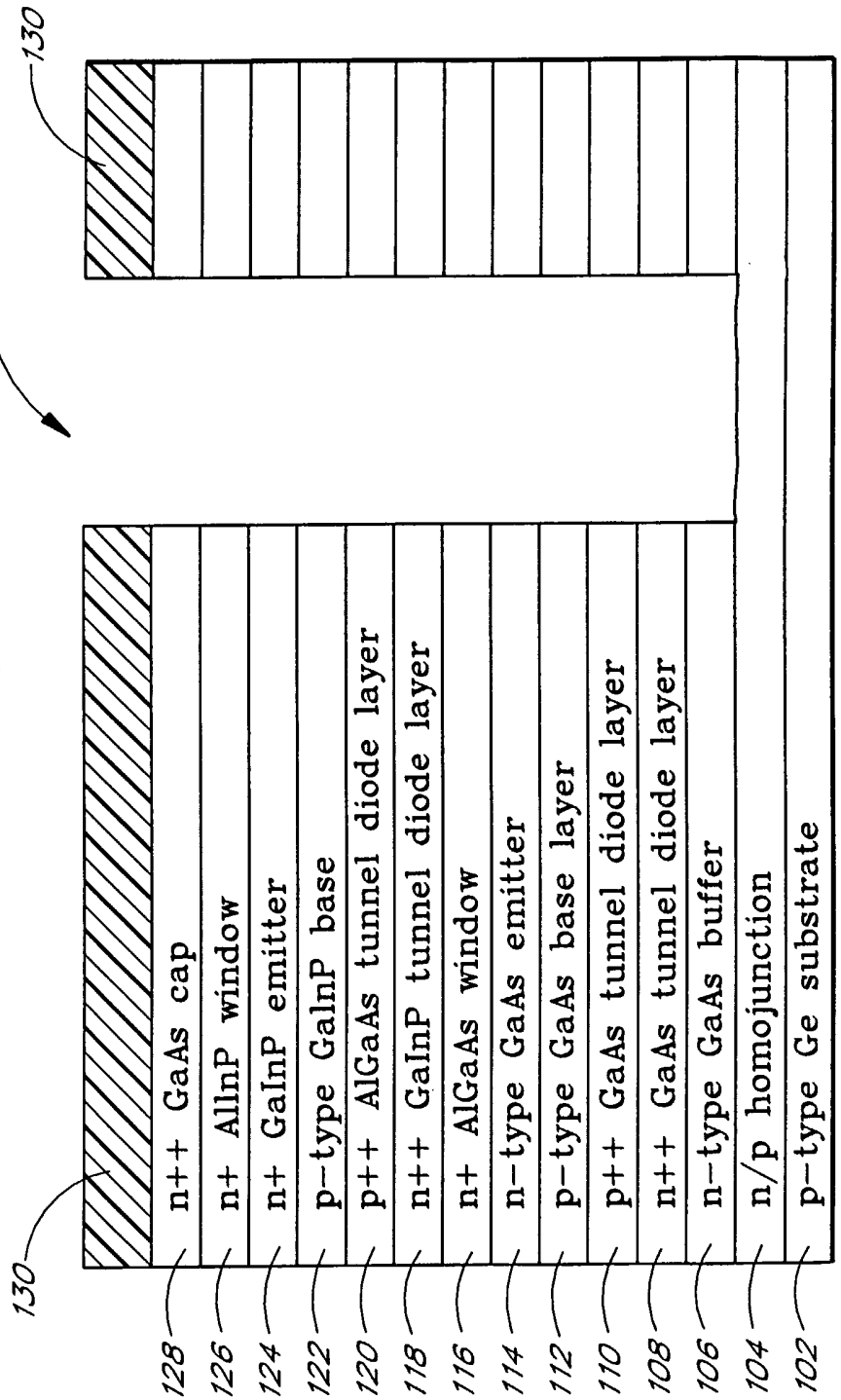
108 n++ GaAs tunnel diode layer
106 n-type GaAs buffer
104 n/p homojunction
102 p-type Ge substrate

FIG. 2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n++ GaAs cap
n+ AlInP window
n+ GaInP emitter
p-type GaInP base
p++ AlGaAs tunnel diode layer
n++ GaInP tunnel diode layer
n+ AlGaAs window
n-type GaAs emitter
p-type GaAs base layer
p++ GaAs tunnel diode layer
n++ GaAs tunnel diode layer
n-type GaAs buffer
n/p homojunction
p-type Ge substrate
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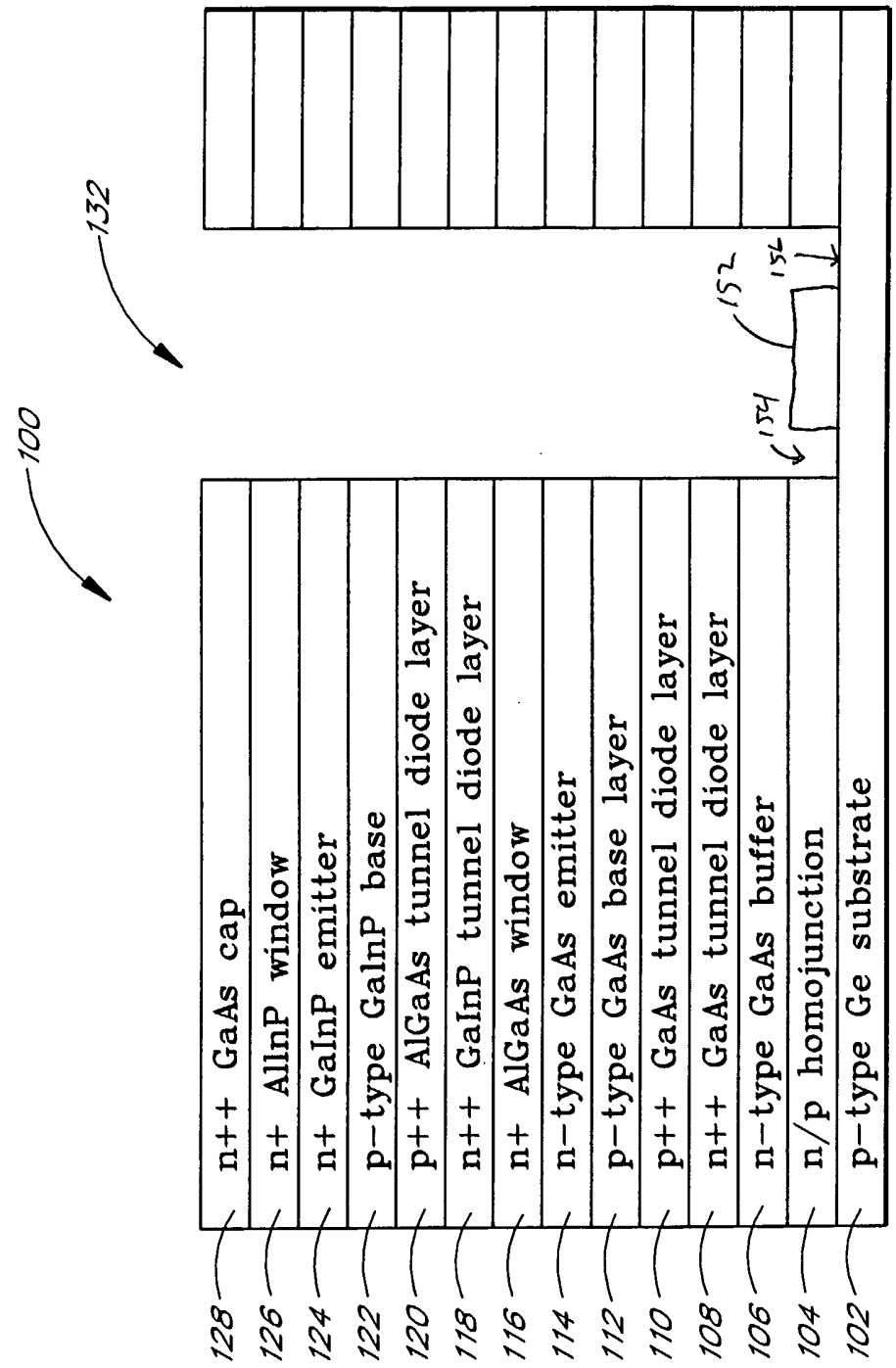
FIG. 3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n+ GaInP emitter
p-type GaInP base
p++ AlGaAs tunnel diode layer
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n+ AlGaAs window
n-type GaAs emitter
p-type GaAs base layer
p++ GaAs tunnel diode layer
n++ GaAs tunnel diode layer
n-type GaAs buffer
n/p homojunction
p-type Ge substrate
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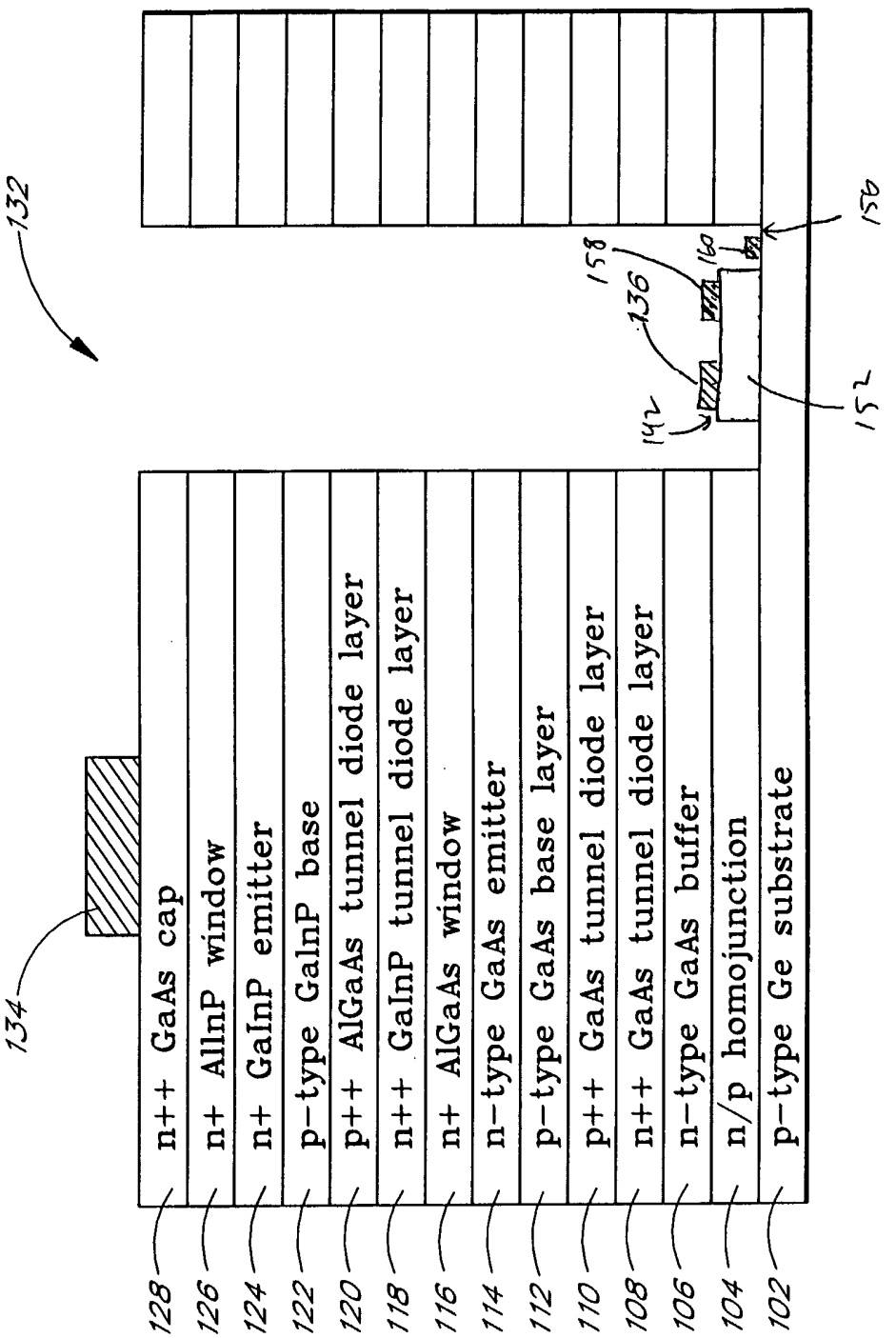
FIG. 4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p++ AlGaAs tunnel diode layer
n++ GaInP tunnel diode layer
n+ AlGaAs window
n-type GaAs emitter
p-type GaAs base layer
p++ GaAs tunnel diode layer
n++ GaAs tunnel diode layer
n-type GaAs buffer
n/p homojunction
p-type Ge substrate
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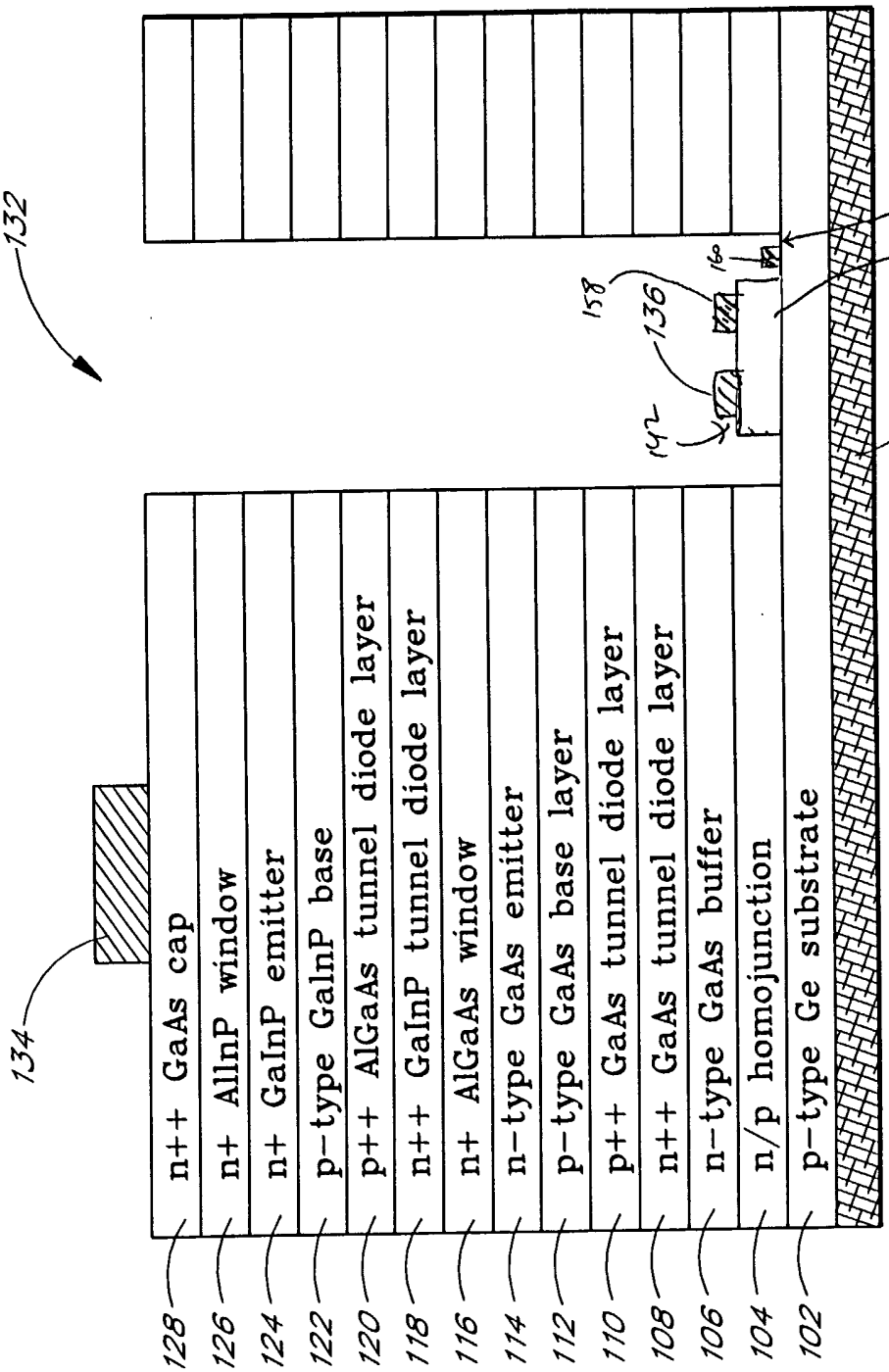
FIG. 5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n+ AlGaAs window
n-type GaAs emitter
p-type GaAs base layer
p++ GaAs tunnel diode layer
n++ GaAs tunnel diode layer
n-type GaAs buffer
n/p homojunction
p-type Ge substrate
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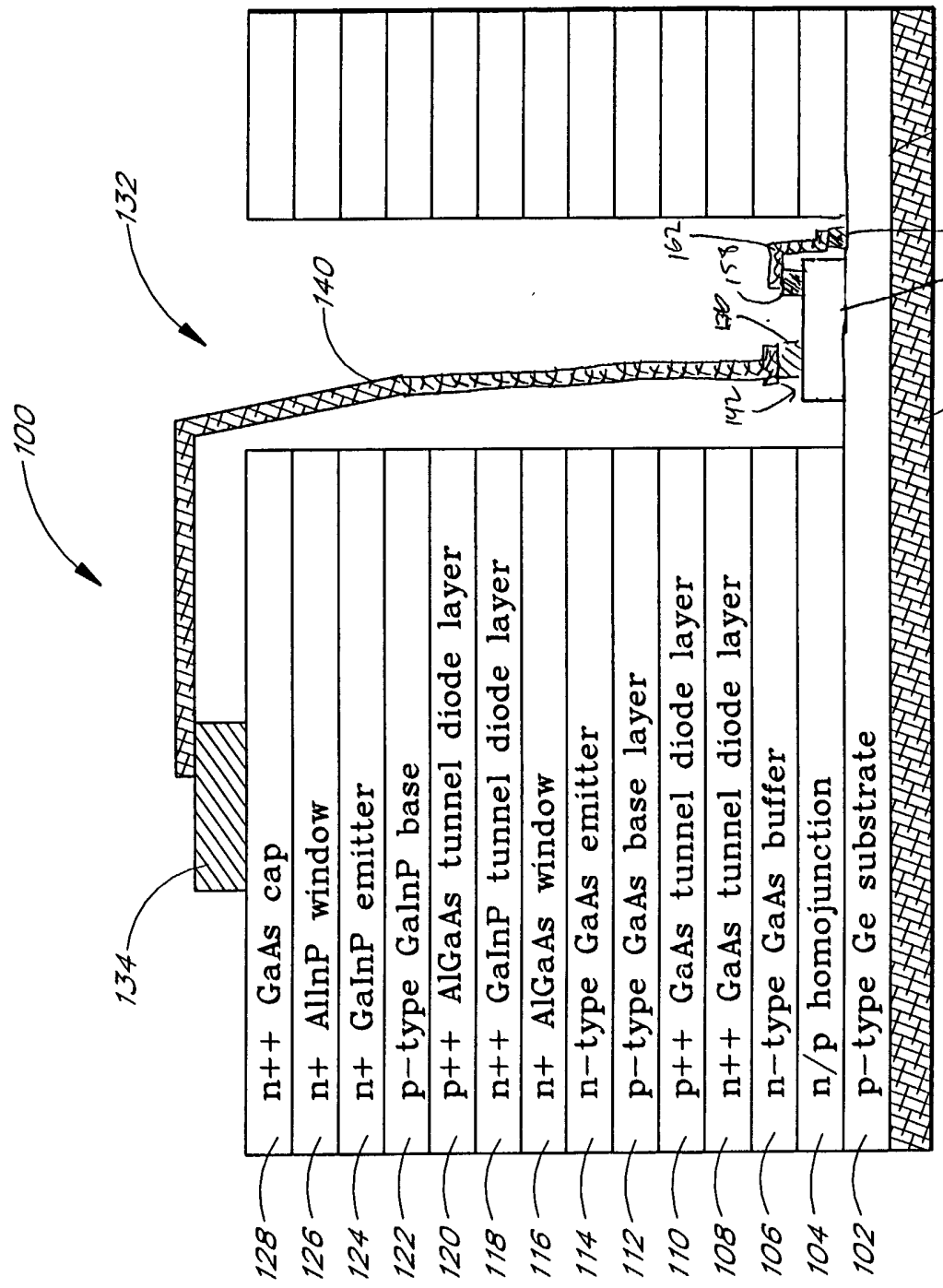
FIG. 6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n++ GaInP tunnel diode layer
n+ AlGaAs window
n-type GaAs emitter
p-type GaAs base layer
p++ GaAs tunnel diode layer
n++ GaAs tunnel diode layer
n-type GaAs buffer
n/p homojunction
p-type Ge substrate
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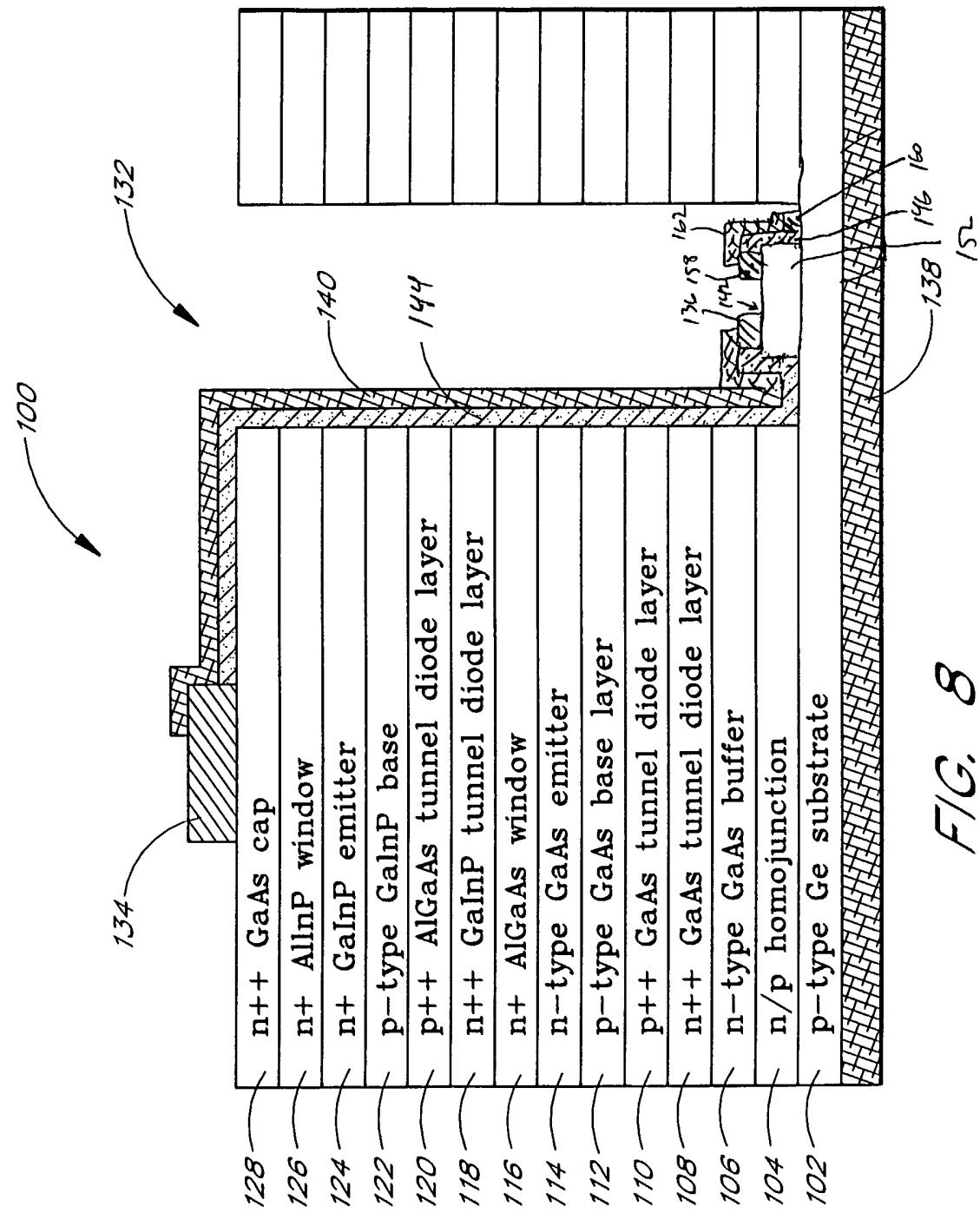
FIG. 7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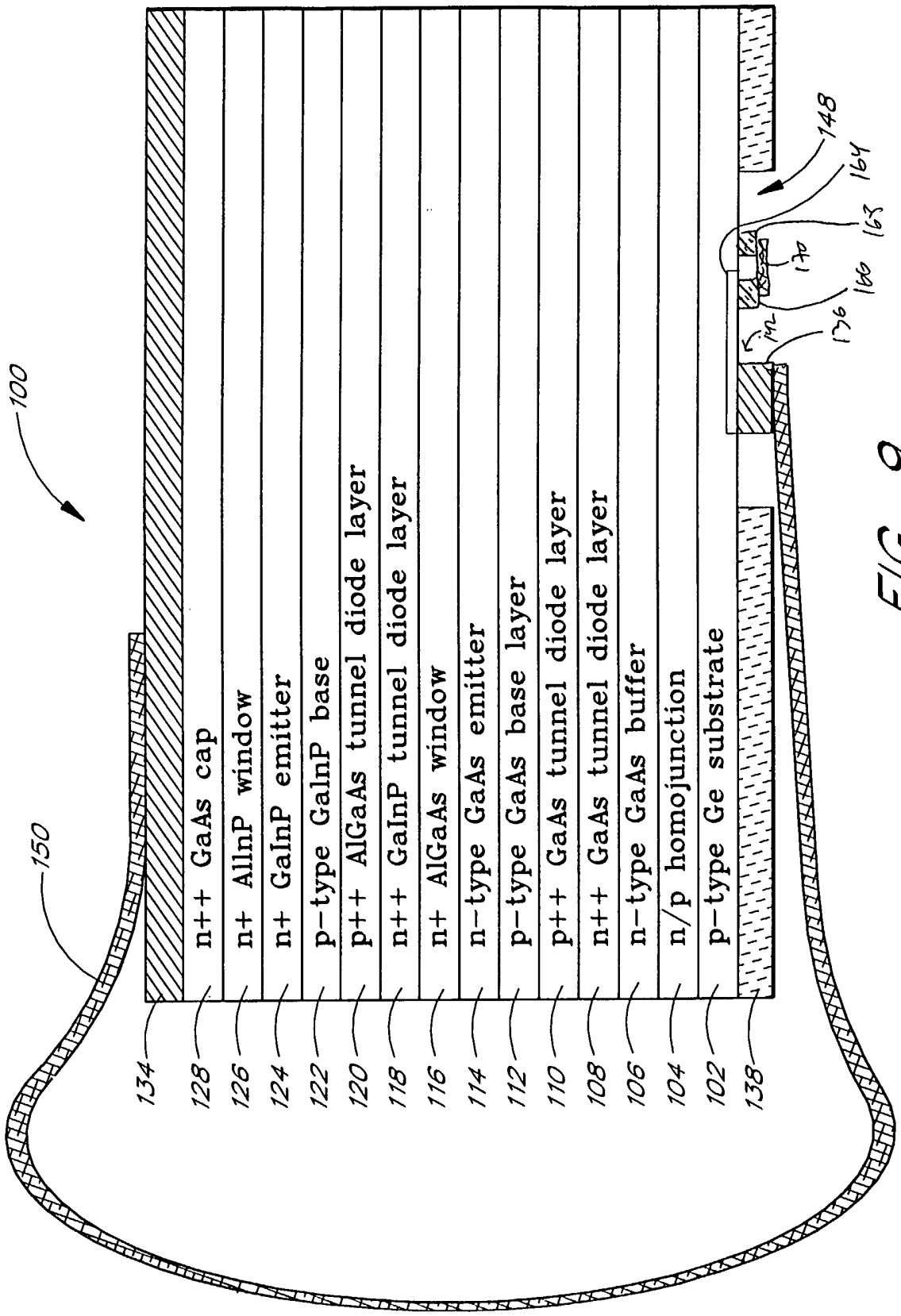
124 n+ GaInP emitter
122 p-type GaInP base
120 p++ AlGaAs tunnel diode layer
118 n++ GaInP tunnel diode layer
116 n+ AlGaAs window
114 n-type GaAs emitter
112 p-type GaAs base layer
110 p++ GaAs tunnel diode layer
108 n++ GaAs tunnel diode layer
106 n-type GaAs buffer
104 n/p homojunction
102 p-type Ge substrate

FIG. 8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p++ AlGaAs tunnel diode layer
n++ GaInP tunnel diode layer
n+ AlGaAs window
n-type GaAs emitter
p-type GaAs base layer
p++ GaAs tunnel diode layer
n++ GaAs tunnel diode layer
n-type GaAs buffer
n/p homojunction
p-type Ge substrate
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FIG. 9

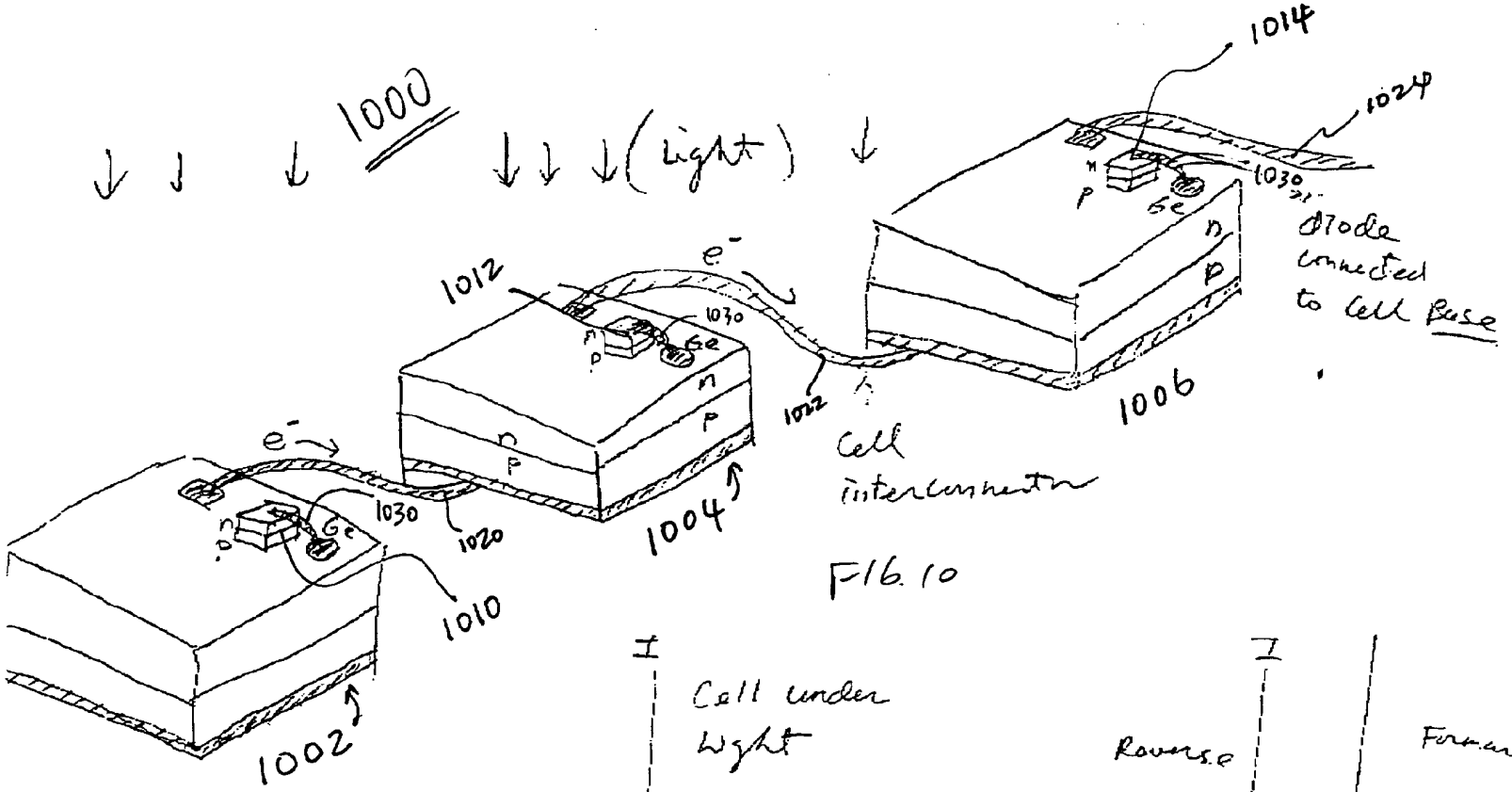
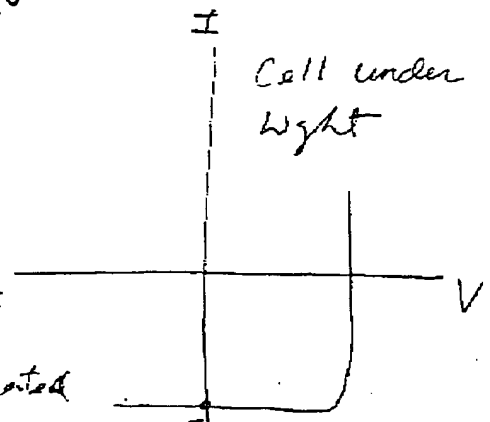
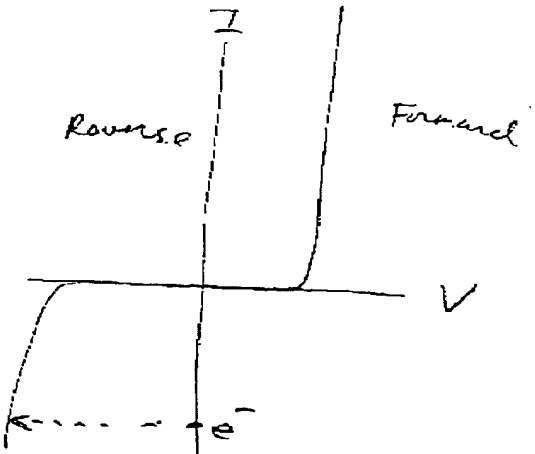


FIG. 10

Case 1:

As cell under light illumination: cell generated power, e^- flows and diode off.



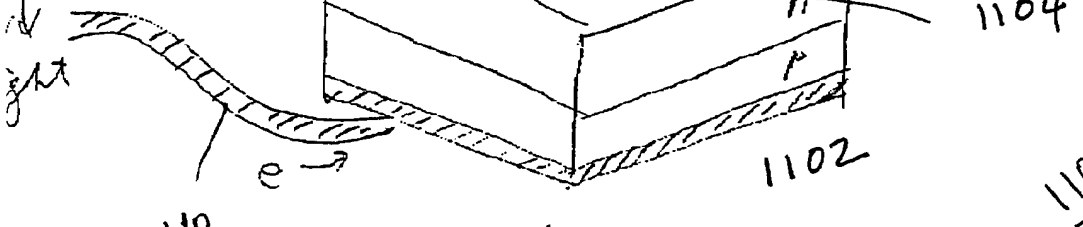


Diode at reverse mode, diode is off. No e^- flows through.

Case II

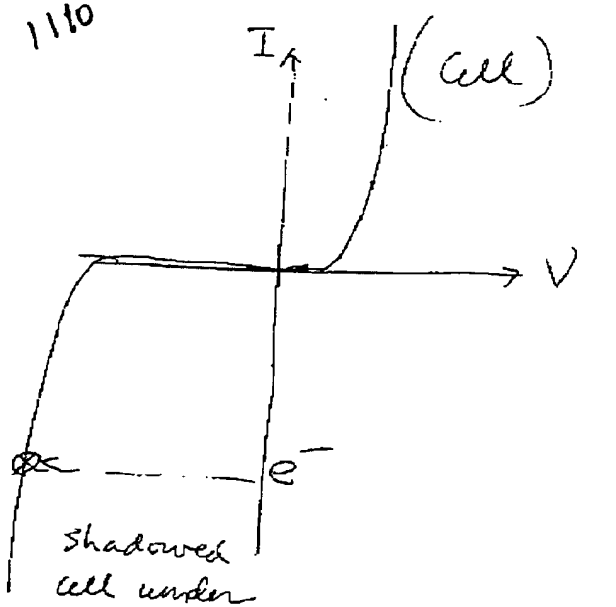
But

Other cells are still generating e^- to flow through the shaded cell



Cell under shadow, No light shine on cell

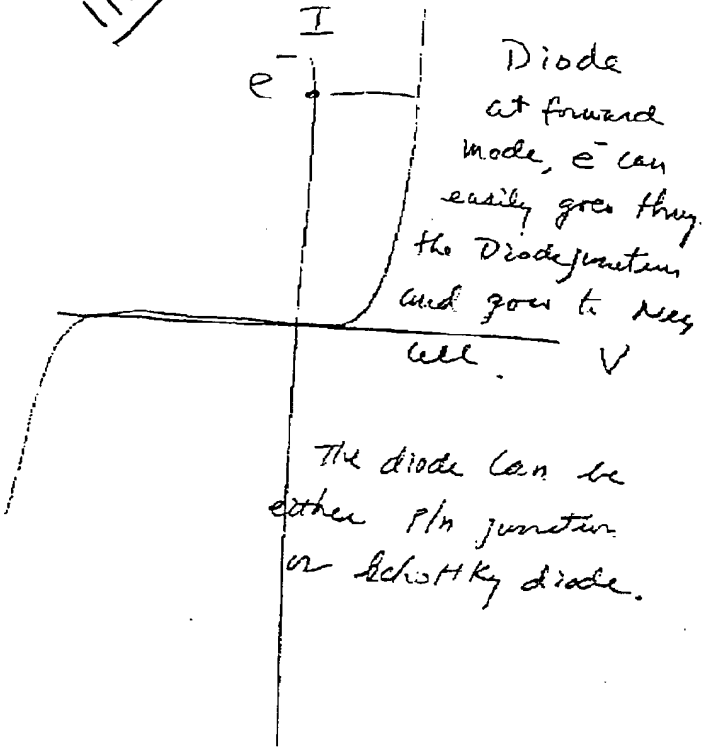
light



Shadowed cell under reverse mode, the e^- can't flow through the cell junction.

FIG. 11

1100



Diode at forward mode, e^- can easily goes thru the Diode junction and goes to neg cell.

The diode can be either P/n junction or Schottky diode.