(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 July 2019 (11.07.2019)

WIPO | PCT

(10) International Publication Number
WO 2019/135154 A1

(51) International Patent Classification:
H01L 29/41 (2006.01)

(21) International Application Number:
PCT/IB2018/060735

(22) International Filing Date:
31 December 2018 (31.12.2018)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15/862,930 05 January 2018 (05.01.2018) US

(71) Applicant: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, New York 10504 (US).

(71) Applicants *(for MG only)*: **IBM UNITED KINGDOM LIMITED** [GB/GB]; PO Box 41, North Harbour, Portsmouth Hampshire PO6 3AU (GB). **IBM (CHINA) INVESTMENT COMPANY LIMITED** [CN/CN]; 25/F, Pangu Plaza, No. 27, Central North 4th Ring Road, Chaoyang District, Beijing 100101 (CN).

(72) Inventors: **LEE, Choonghyun**; IBM Corporation, 257 Fuller Road, Albany, New York 12203 (US). **YEUNG, Chun Wing**; IBM Corporation, 257 Fuller Road, Albany, New York 12203 (US). **BAO, Ruqiang**; IBM Corporation, 257 Fuller Road, Albany, New York 12203 (US). **JAGANNATHAN, Hemanth**; IBM Corporation, 257 Fuller Road, Albany, New York 12203 (US).

(74) Agent: **WILLIAMS, Julian**; IBM United Kingdom Limited, Intellectual Property Law, Hursley Park, Winchester Hampshire SO21 2JN (GB).

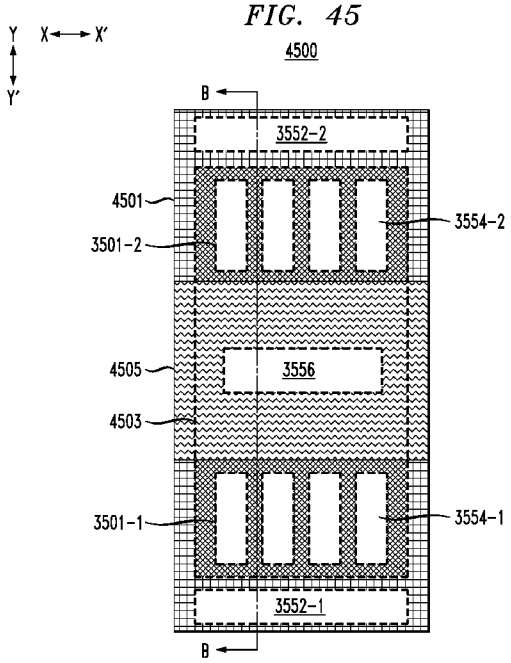
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,

(54) Title: REPLACEMENT METAL GATE PROCESSES FOR VERTICAL TRANSPORT FIELD-EFFECT TRANSISTOR

(57) Abstract: A method of forming a semiconductor structure comprises forming a plurality of fins disposed over a top surface of a substrate and forming one or more vertical transport field-effect transistors (VTFETs) from the plurality of fins using a replacement metal gate (RMG) process. A gate surrounding at least one fin of a given one of the VTFETs comprises a gate self-aligned contact (SAC) capping layer disposed over a gate contact metal layer, the gate contact metal layer being disposed adjacent an end of the at least one fin.

FIG. 45



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MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

REPLACEMENT METAL GATE PROCESSES FOR VERTICAL TRANSPORT FIELD-EFFECT TRANSISTOR

BACKGROUND

[0001] The present invention relates to semiconductors, and more specifically, to techniques for forming semiconductor structures. Semiconductors and integrated circuit chips have become ubiquitous within many products, particularly as they continue to decrease in cost and size. There is a continued desire to reduce the size of structural features and/or to provide a greater amount of structural features for a given chip size. Miniaturization, in general, allows for increased performance at lower power levels and lower cost. Present technology is at or approaching atomic level scaling of certain micro-devices such as logic gates, field-effect transistors (FETs), and capacitors.

SUMMARY

[0002] Embodiments of the invention provide techniques for replacement metal gate (RMG) processes for vertical transport field-effect transistors (VTFETs).

[0003] In one embodiment of the invention, a method of forming a semiconductor structure comprises forming a plurality of fins disposed of the invention over a top surface of a substrate and forming one or more VTFETs from the plurality of fins using a RMG process. A gate surrounding at least one fin of a given one of the VTFETs comprises a gate self-aligned contact (SAC) capping layer disposed over a gate contact metal layer, the gate contact metal layer being disposed adjacent an end of the at least one fin.

[0004] In another embodiment of the invention, a semiconductor structure comprises a substrate and a plurality of fins disposed over a top surface of the substrate, the plurality of fins comprising channels for one or more VTFETs formed with a RMG process. A given one of the VTFETs comprises a gate surrounding at least one of the plurality of fins, the gate of the given VTFET comprising a gate SAC capping layer disposed over a gate contact metal layer, the gate contact metal layer being disposed adjacent an end of the at least one fin.

[0005] In another embodiment of the invention, an integrated circuit comprises one or more VTFETs comprising a substrate and a plurality of fins disposed over a top surface of the substrate, the plurality of fins comprising channels for the one or more VTFETs formed with a RMG process. A given one of the VTFETs comprises a gate surrounding at least one of the plurality of fins, the gate of the given VTFET comprising a gate SAC capping layer disposed over a gate contact metal layer, the gate contact metal layer being disposed adjacent an end of the at least one fin.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 depicts a side cross-sectional view of a semiconductor structure with a plurality of fins disposed over a substrate, according to an embodiment of the invention.

[0007] FIG. 2 depicts a side cross-sectional view of the semiconductor structure of FIG. 1 following formation of bottom source/drain regions and bottom spacers, according to an embodiment of the invention.

[0008] FIG. 3 depicts a side cross-sectional view of the semiconductor structure of FIG. 2 following dummy gate formation, according to an embodiment of the invention.

[0009] FIG. 4 depicts a side cross-sectional view of the semiconductor structure of FIG. 3 following recess of the dummy gate, according to an embodiment of the invention.

[0010] FIG. 5 depicts a side cross-sectional view of the semiconductor structure of FIG. 4 following formation of top spacers, according to an embodiment of the invention.

[0011] FIG. 6 depicts a side cross-sectional view of the semiconductor structure of FIG. 5 following formation and activation of top junctions, according to an embodiment of the invention.

[0012] FIG. 7 depicts a side cross-sectional view of the semiconductor structure of FIG. 6 following fill with an isolation layer, according to an embodiment of the invention.

[0013] FIG. 8 depicts a side cross-sectional view of the semiconductor structure of FIG. 7 following formation of an additional spacer and interlevel dielectric, according to an embodiment of the invention.

[0014] FIG. 9 depicts a side cross-sectional view of the semiconductor structure of FIG. 8 following opening to expose the tops of the junctions for formation of top source/drain contacts, according to an embodiment of the invention.

[0015] FIG. 10 depicts a side cross-sectional view of the semiconductor structure of FIG. 9 following top source/drain formation, according to an embodiment of the invention.

[0016] FIG. 11 depicts a side cross-sectional view of the semiconductor structure of FIG. 10 following fill with a metal layer over the top source/drain regions, according to an embodiment of the invention.

[0017] FIG. 12 depicts a side cross-sectional view of the semiconductor structure of FIG. 11 following recess of

the metal layer and formation of a top source/drain self-aligned contact capping layers, according to an embodiment of the invention.

[0018] FIG. 13 depicts another side cross-sectional view of the semiconductor structure of FIG. 11 after formation of the top source/drain self-aligned contact capping layers, according to an embodiment of the invention.

[0019] FIG. 14 depicts a side cross-sectional view of the semiconductor structure of FIGS. 12 and 13 following masking to open the dummy gate, according to an embodiment of the invention.

[0020] FIG. 15 depicts a side cross-sectional view of the semiconductor structure of FIG. 14 following formation of a liner on sidewalls of the gate opening, according to an embodiment of the invention.

[0021] FIG. 16 depicts a side cross-sectional view of the semiconductor structure of FIG. 15 following removal of the dummy gate, according to an embodiment of the invention.

[0022] FIG. 17 depicts a side cross-sectional view of the semiconductor structure of FIG. 16 following a replacement metal gate process, according to an embodiment of the invention.

[0023] FIG. 18 depicts a side cross-sectional view of the semiconductor structure of FIG. 17 following fill of a metal in the gate opening, according to an embodiment of the invention.

[0024] FIG. 19 depicts a side cross-sectional view of the semiconductor structure of FIG. 18 following recess of the metal in the gate opening and formation of a gate self-aligned contact capping layer, according to an embodiment of the invention.

[0025] FIG. 20 depicts a side cross-sectional view of the semiconductor structure of FIG. 19 following masking to open the bottom source/drain regions, according to an embodiment of the invention.

[0026] FIG. 21 depicts a side cross-sectional view of the semiconductor structure of FIG. 20 following filling of the opening to the bottom source/drain regions with a metal and formation of a bottom source/drain self-aligned contact capping layer, according to an embodiment of the invention.

[0027] FIG. 22 depicts a side cross-sectional view of the semiconductor structure of FIG. 21 following formation of a liner and an interlevel dielectric, according to an embodiment of the invention.

[0028] FIG. 23 depicts a side cross-sectional view of the semiconductor structure of FIG. 22 following formation of vias to access contacts, according to an embodiment of the invention.

[0029] FIG. 24 depicts a top-down view of the semiconductor structure of FIG. 23, according to an embodiment of the invention.

[0030] FIG. 25 depicts a side cross-sectional view of a semiconductor structure comprising fins in long and short channel regions, according to an embodiment of the invention.

[0031] FIG. 26 depicts a side cross-sectional view of the semiconductor structure of FIG. 25 following dummy gate patterning, according to an embodiment of the invention.

[0032] FIG. 27 depicts a side cross-sectional view of the semiconductor structure of FIG. 26 following formation of a liner, according to an embodiment of the invention.

[0033] FIG. 28 depicts a side cross-sectional view of the semiconductor structure of FIG. 27 following recess of the dummy gate, according to an embodiment of the invention.

[0034] FIG. 29 depicts a side cross-sectional view of the semiconductor structure of FIG. 28 following formation of top spacers, according to an embodiment of the invention.

[0035] FIG. 30 depicts a side cross-sectional view of the semiconductor structure of FIG. 29 following formation of top junctions, according to an embodiment of the invention.

[0036] FIG. 31 depicts a side cross-sectional view of the semiconductor structure of FIG. 30 following fill with an isolation layer and formation of an additional spacer and interlevel dielectric, according to an embodiment of the invention.

[0037] FIG. 32 depicts a side cross-sectional view of the semiconductor structure of FIG. 31 following opening to expose the tops of the junctions for formation of top source/drain contacts, according to an embodiment of the invention.

[0038] FIG. 33 depicts a side cross-sectional view of the semiconductor structure of FIG. 32 following formation of top source/drain regions and fill with a metal layer, according to an embodiment of the invention.

[0039] FIG. 34 depicts a side cross-sectional view of the semiconductor structure of FIG. 33 following recess of the metal layer and forming of top source/drain region self-aligned contact capping layers, according to an embodiment of the invention.

[0040] FIG. 35 depicts a side cross-sectional view of a semiconductor structure with a shared dummy gate,

according to an embodiment of the invention.

[0041] FIG. 36 depicts a side cross-sectional view of the semiconductor structure of FIG. 35 following opening of the shared dummy gate, according to an embodiment of the invention.

[0042] FIG. 37 depicts a side cross-sectional view of the semiconductor structure of FIG. 36 following formation of a liner, according to an embodiment of the invention.

[0043] FIG. 38 depicts a side cross-sectional view of the semiconductor structure of FIG. 37 following removal of the shared dummy gate, according to an embodiment of the invention.

[0044] FIG. 39 depicts a side cross-sectional view of the semiconductor structure of FIG. 38 following formation of a work function metal for a p-type field-effect transistor, according to an embodiment of the invention.

[0045] FIG. 40 depicts a side cross-sectional view of the semiconductor structure of FIG. 39 following patterning of the p-type work function metal, according to an embodiment of the invention.

[0046] FIG. 41 depicts a side cross-sectional view of the semiconductor structure of FIG. 40 following formation of a work function metal for an n-type field-effect transistor, according to an embodiment of the invention.

[0047] FIG. 42 depicts a side cross-sectional view of the semiconductor structure of FIG. 41 following fill with a metal, according to an embodiment of the invention.

[0048] FIG. 43 depicts a side cross-sectional view of the semiconductor structure of FIG. 42 following recess of the metal and formation of a gate self-aligned contact capping layer, according to an embodiment of the invention.

[0049] FIG. 44 depicts a side cross-sectional view of the semiconductor structure of FIG. 43 following formation of vias to access contacts, according to an embodiment of the invention.

[0050] FIG. 45 depicts a top-down view of the semiconductor structure of FIG. 44, according to an embodiment of the invention.

DETAILED DESCRIPTION

[0051] Illustrative embodiments of the invention may be described herein in the context of illustrative methods for replacement metal gate processes for vertical transport field-effect transistors, along with illustrative apparatus, systems and devices formed using such methods. However, it is to be understood that embodiments of the

invention are not limited to the illustrative methods, apparatus, systems and devices but instead are more broadly applicable to other suitable methods, apparatus, systems and devices.

[0052] A field-effect transistor (FET) is a transistor having a source, a gate, and a drain, and having action that depends on the flow of carriers (electrons or holes) along a channel that runs between the source and drain. Current through the channel between the source and drain may be controlled by a transverse electric field under the gate.

[0053] FETs are widely used for switching, amplification, filtering, and other tasks. FETs include metal-oxide-semiconductor (MOS) FETs (MOSFETs). Complementary MOS (CMOS) devices are widely used, where both n-type and p-type transistors (NFET and PFET) are used to fabricate logic and other circuitry. Source and drain regions of a FET are typically formed by adding dopants to target regions of a semiconductor body on either side of a channel, with the gate being formed above the channel. The gate includes a gate dielectric over the channel and a gate conductor over the gate dielectric. The gate dielectric is an insulator material that prevents large leakage current from flowing into the channel when voltage is applied to the gate conductor while allowing applied gate voltage to produce a transverse electric field in the channel.

[0054] Increasing demand for high density and performance in integrated circuit devices requires development of new structural and design features, including shrinking gate lengths and other reductions in size or scaling of devices. Continued scaling, however, is reaching limits of conventional fabrication techniques.

[0055] Vertical FET process flows have strict constraints on thermal budgets for downstream processing steps, such as top source/drain epitaxial growth and dopant activation anneal processes, because the high-k metal gate (HKMG) module is formed earlier in processing. Channel length (Lgate) is highly dependent on metal gate recess processing, which causes large chip variation in Lgate. High temperature processes (e.g., greater than 550 degrees Celsius (°C)) for top source/drain module causes threshold voltage (Vt) shift, increase in inversion thickness (Tinv), and leakage current metric (Toxgl) degradation due to oxygen and metal diffusion into the channel. Thus, replacement metal gate (RMG) process flows for vertical transport FETs (VTFETs) are needed.

[0056] Embodiments of the invention provide techniques for forming VTFET devices with a RMG process, removing the limitation of thermal budgets for gate stacks. RMG processes disclosed herein provide an accurate Lgate definition as well as self-aligned top junctions. In addition to providing techniques for forming VTFETs with a RMG process, embodiments also allow for formation of VTFETs with multiple channel lengths, self-aligned gate cap formation to avoid gate-to-source/drain region shorts, and CMOS patterning with negligible n/p boundary shift.

[0057] Illustrative processes for forming VTFETs using RMG processes, including VTFETs with multiple channel lengths and CMOS VTFET devices, will now be described with respect to FIGS. 1-45.

[0058] FIG. 1 depicts a side cross-sectional view 100 of a semiconductor structure, comprising a substrate 102 with a plurality of fins 101 formed therein. As shown, each of the fins 101 is topped by a hard mask 104. The fins 101 may be formed using sidewall image transfer (SIT) or other suitable techniques such as lithography and etching including reactive-ion etching (RIE), etc. Each of the fins 101 may have a width or horizontal thickness (in direction X-X') in the range of 5 nanometers (nm) to 10nm, although other widths above or below this range may be used as desired for a particular application. Each of the fins 101 may have a height or vertical thickness (in direction Y-Y') ranging from 30nm to 150nm, although other heights above or below this range may be used as desired for a particular application. A spacing between adjacent ones of the fins 101 may be in the range of 20nm to 100nm, although other spacing may be used as desired for a particular application.

[0059] In some embodiments of the invention, the substrate 102 comprises a semiconductor substrate formed of silicon (Si), although other suitable materials may be used. For example, the substrate 102 can include any suitable substrate structure, e.g., a bulk semiconductor. The substrate 102 can include a silicon-containing material. Illustrative examples of Si-containing materials suitable for the substrate 102 can include, but are not limited to, Si, silicon germanium (SiGe), silicon germanium carbide (SiGeC), silicon carbide (SiC) and multi-layers thereof. Although silicon is the predominantly used semiconductor material in wafer fabrication, alternative semiconductor materials can be employed as additional layers, such as, but not limited to, germanium (Ge), gallium arsenide (GaAs), gallium nitride (GaN), SiGe, cadmium telluride (CdTe), zinc selenide (ZnSe), etc. The fins 101 are formed by patterning the substrate 102 as discussed above, and thus may be formed of the same material as the substrate 102.

[0060] The substrate 102 may have a width or horizontal thickness (X-X') selected as desired based on a number of fins 101 or other features to be formed thereon. The substrate 102 may have a height or vertical thickness (in direction Y-Y') in the range of 20nm to 500nm, although other heights above or below this range may be used as desired for a particular application.

[0061] The hard mask 104 may be initially formed over a top surface of the entire substrate, followed by patterning using SIT or other suitable techniques, with the fins 101 being formed by etching portions of the substrate exposed by the patterned hard mask 104. The hard mask 104 may be formed of silicon nitride (SiN), although other suitable materials such as silicon oxide (SiOX), silicon dioxide (SiO2) and silicon oxynitride (SiON) may be used. The hard mask 104 may have a height or vertical thickness (in direction Y-Y') in the range of 20nm to 100nm, although other heights above or below this range may be used as desired for a particular application.

[0062] FIG. 2 depicts a side cross-sectional view 200 of the semiconductor structure of FIG. 1 following formation of bottom source/drain regions 106 over a top surface of the substrate 102 surrounding the fins 101, and formation of bottom spacers 108 over the bottom source/drain regions 106 surrounding the fins 101.

[0063] The bottom source/drain regions 106 may be suitably doped, such as using ion implantation, gas phase doping, plasma doping, plasma immersion ion implantation, cluster doping, infusion doping, liquid phase doping, solid phase doping, etc. N-type dopants may be selected from a group of phosphorus (P), arsenic (As) and antimony (Sb), and p-type dopants may be selected from a group of boron (B), boron fluoride (BF2), gallium (Ga), indium (In), and thallium (Tl). The bottom source/drain regions 106 may be formed by an epitaxial growth process. In some embodiments, the epitaxy process comprises in-situ doping (dopants are incorporated in epitaxy material during epitaxy). Epitaxial materials may be grown from gaseous or liquid precursors. Epitaxial materials may be grown using vapor-phase epitaxy (VPE), molecular-beam epitaxy (MBE), liquid-phase epitaxy (LPE), rapid thermal chemical vapor deposition (RTCVD), metal organic chemical vapor deposition (MOCVD), ultra-high vacuum chemical vapor deposition (UHVCVD), low-pressure chemical vapor deposition (LPCVD), limited reaction processing CVD (LRPCVD), or other suitable processes. Epitaxial silicon, silicon germanium (SiGe), germanium (Ge), and/or carbon doped silicon (Si:C) silicon can be doped during deposition (in-situ doped) by adding dopants, such as n-type dopants (e.g., phosphorus or arsenic) or p-type dopants (e.g., boron or gallium), depending on the type of transistor. The dopant concentration in the source/drain can range from 1x1019 cm-3 to 3x1021 cm-3, or preferably between 2x1020 cm-3 to 3x1021 cm-3.

[0064] The bottom source/drain regions 106 may have a height or vertical thickness (in direction Y-Y') in the range of 10nm to 50nm, although other heights above or below this range may be used as desired for a particular application.

[0065] The bottom spacers 108 are formed over the bottom source/drain regions 106 using non-conformal deposition and etch-back processing (e.g., physical vapor deposition (PVD), high density plasma (HDP) deposition, etc.). The bottom spacers 108 may be formed of SiO2, SiN, silicon carbide oxide (SiCO), silicon boron carbide nitride (SiBCN), etc., although other suitable materials may be used. The bottom spacers 108 may have a height or vertical thickness (in direction Y-Y') in the range of 3nm to 10nm, although other heights above or below this range may be used as desired for a particular application.

[0066] FIG. 3 depicts a side cross-sectional view 300 of the semiconductor structure of FIG. 2 following dummy gate formation. Dummy gate formation includes formation of an oxide 110 over top surfaces of the bottom spacers 108 and on sidewalls of the fins 101 and hard mask 104. The oxide 110 may be formed by a conformal deposition process, such as atomic layer deposition (ALD) or chemical vapor deposition (CVD). The oxide 110 may be formed of SiO2, SiON, etc., although other suitable materials may be used. The oxide 110 may have a uniform thickness in the range of 2nm to 6nm, although other thicknesses above or below this range may be used as desired for a particular application.

[0067] Dummy gate 112 is formed over the oxide 110, using processing such as CVD or ALD. The dummy gate 112 may be formed of amorphous silicon (a-Si), amorphous silicon germanium (a-SiGe), SiO2, titanium oxide

(TiO2) or another suitable material.

[0068] FIG. 4 depicts a side cross-sectional view 400 of the semiconductor structure of FIG. 3 following recess of the dummy gate 112 and removal of exposed portions of the oxide 110 on sidewalls of the fins 101 and hard masks 104 disposed over the fins 101. The dummy gate 112 and oxide 110 may be recessed using processing such as a wet etch, RIE, etc. The dummy gate 112 and oxide 110 may be recessed a depth (in direction Y-Y') in the range of 5nm to 20nm, although other depths may be used, so long as at least a portion of the sidewalls of the fins 101 below the hard mask 104 is exposed.

[0069] FIG. 5 depicts a side cross-sectional view 500 of the semiconductor structure of FIG. 4 following removal of the hard masks 104 and formation of top spacers 114. The hard masks 104 may be removed using selective dry or wet etch processing. The top spacers 114 may be formed using a conformal deposition such as ALD or CVD processing. The top spacers 114 may be formed of SiN, SiO2 or another suitable material such as SiON, SiOC, SiBCN, etc. The top spacers 114 may have a uniform thickness in the range of 3nm to 10nm, although other thicknesses above or below this range may be used as desired for a particular application.

[0070] FIG. 6 depicts a side cross-sectional view 600 of the semiconductor structure of FIG. 5 following formation and activation of top junctions 116. Ion implantation, plasma doping or another suitable process is used to form top junctions 116 (e.g., heavily doped regions) at the tops of the fins 101. The top junctions 116 may use dopants including n-type dopants selected from a group of phosphorus (P), arsenic (As) and antimony (Sb) and p-type dopants selected from a group of boron (B), boron fluoride (BF2), gallium (Ga), indium (In) and thallium (Tl). The height of the top junctions 116 extends in a region of the fins below a bottom surface of the top spacers 114. The top junctions 116 may have a height or vertical thickness (in direction Y-Y') in the range of 5nm to 20nm, although other heights above or below this range may be used as desired for a particular application.

[0071] FIG. 7 depicts a side cross-sectional view 700 of the semiconductor structure of FIG. 6 following fill with an isolation or interlevel dielectric (ILD) layer 118. The isolation layer 118 may be formed of SiO2 or another suitable material such as SiOC, SiON, etc. The isolation layer 118 may be formed by fill with the isolation material followed by planarization using chemical mechanical polishing or planarization (CMP) to a top surface of the top spacers 114.

[0072] FIG. 8 depicts a side cross-sectional view 800 of the semiconductor structure of FIG. 7 following formation of a spacer 120 and an ILD layer 122. The spacer 120 may be formed of SiN, although other suitable materials such as SiO2, SiON, SiBCN, SiCO, etc. may be used. The spacer 120 may have a height or vertical thickness (in direction Y-Y') in the range of 5nm to 15nm, although other heights above or below this range may be used as desired for a particular application. The spacer 120 may be formed using conformal deposition processing such as ALD or CVD.

[0073] The ILD 122 may be formed of SiO2, although other suitable materials such as SiON, SiCO, etc. may be used. The ILD 122 may be formed using CVD or ALD processing. The ILD 122 may have a height or vertical thickness (in direction Y-Y') in the range of 30nm to 150nm, although other heights above or below this range may be used as desired for a particular application.

[0074] FIG. 9 depicts a side cross-sectional view 900 of the semiconductor structure of FIG. 8 following opening to expose the tops of the junctions 116 for formation of top source/drain contacts. A mask layer 124 is patterned over a top surface of the ILD 122, using lithography and etching or other suitable techniques. The mask layer 124 may be formed of a suitable combination of organic materials, SiO2, titanium oxide (TiOx), although other suitable materials may be used. The mask layer 124 may have a height or vertical thickness (in direction Y-Y') in the range of 30nm to 150nm, although other heights above or below this range may be used as desired for a particular application.

[0075] The mask layer 124 is patterned so to provide openings above the tops of the fins 101. The tops of the openings above the fins 101 are wider than the fins 101, such as having a width 901 in the range of 20nm to 80nm, which narrow to a width substantially matching the widths of the fins 101 as distance from a top surface of the fins 101 decreases. The openings in ILD 122 may be formed by directional RIE or other suitable processing.

[0076] FIG. 10 depicts a side cross-sectional view 1000 of the semiconductor structure of FIG. 9 following top source/drain formation. The mask layer 124 is removed, using processing such as plasma ashing/removal. To assist with epitaxial growth, a lateral etch of material of the spacers 114 and 120 may optionally be performed. Following the optional lateral etch, top source/drain regions 126 are epitaxially grown over the junctions 116 (and in the regions exposed by the optional lateral etch of spacers 114 and 120). The top source/drain regions 126 may have a height or vertical thickness (in direction Y-Y') in the range of 10nm to 50nm, although other heights above or below this range may be used as desired for a particular application. The top source/drain regions 126 may be formed of similar materials as the bottom source/drain regions 106.

[0077] FIG. 11 depicts a side cross-sectional view 1100 of the semiconductor structure of FIG. 10 following fill with metal to form a metal layer 128 over the top source/drain regions 126. The metal layer 128, also referred to as top source/drain contact metal layers, may be formed of tungsten (W), although other suitable materials such as titanium (Ti), cobalt (Co), etc. may be used. The metal layer 108 may be formed by fill with the metal material followed by planarizing using CMP or another suitable technique such that a top surface of the metal layer 128 is substantially coplanar with a top surface of ILD 122.

[0078] FIG. 12 depicts a side cross-sectional view 1200 of the semiconductor structure of FIG. 11 following recess of the metal layer 128 and formation of a self-aligned contact (SAC) capping layer 130, also referred to as top source/drain SAC capping layers, over top surfaces of the metal layer 128. The metal layer 128 may be

recessed using a wet or dry etch process. The SAC capping layer 130 may be formed using ALD or CVD processing. The metal layer 128 may be recessed to a depth in the range of 5nm to 20nm, although other depths outside this range may be used as desired for a particular application. The SAC capping layer 130 may have a height or thickness (in direction Y-Y') that matches the depth to which the metal layer 128 is recessed, such that the SAC capping layer 130 has a top surface matching the top surface of ILD 122.

[0079] FIG. 13 depicts another side cross-sectional view 1300 of the semiconductor structure of FIG. 11 following formation of the SAC capping layer 130. While the side cross-sectional view 1200 of FIG. 12 (as well as the side cross-sectional views of FIGS. 1-11) is taken perpendicular to the fins 101, the side cross-sectional view 1300 is taken parallel to the fins 101. One of the fins 101 is shown in dashed outline in the side cross-sectional view 1300, indicating that it is "behind" the dummy gate 112 in this view. The side cross-sectional view 1300 further shows shallow trench isolation (STI) regions 103 formed as shown. The STI regions 103 may be formed of similar materials as the isolation layer 118 and ILD 122.

[0080] FIG. 14 depicts a side cross-sectional view 1400 of the semiconductor structure of FIGS. 12 and 13, following masking to open the dummy gate 112. The side cross-sectional view 1400, similar to the side cross-sectional view 1300, is taken parallel to the fins 101. A mask layer 132 is patterned over the top surface of the ILD 122 and SAC capping layer 130. The mask layer 132 may be formed with similar materials and sizing as that of the mask layer 124. The SAC capping layer 130 ensures that there will be no short between the top source/drain regions 126 and the gate. The mask layer 132 may be patterned as shown to open the dummy gate 112, as the SAC capping layer 130 over the top source/drain regions 126 is not merged due to the confined epitaxial layers. The opening to expose the dummy gate 112 may have a width 1401 of 75nm or more generally in the range of 30nm to 100nm, although other widths outside this range may be used as desired for a particular application.

[0081] FIG. 15 depicts a side cross-sectional view 1500 of the semiconductor structure of FIG. 14 following deposition of a liner 134 on sidewalls of the gate opening, and following a directional etch to expose the top surface of the dummy gate 112 in the gate opening. The liner 134 may be formed of a material similar to that of the bottom spacers 108 and top spacers 114 (e.g., SiN), although other suitable materials may be used. The liner 134 may have a thickness in the range of 3nm to 10nm, although other thicknesses outside this range may be used as desired for a particular application. The directional etch to expose the top surface of the dummy gate 112 may be a directional RIE.

[0082] FIG. 16 depicts a side cross-sectional view 1600 of the semiconductor structure of FIG. 15 following removal of the dummy gate 112. The mask layer 132 is removed prior to removal of the dummy gate 112. The dummy gate 112 may be removed using gas phase etch, wet etch or other suitable processing to selectively remove the dummy gate 112 on the oxide layer 110, which protects the fin 101 during the removal of the dummy gate 112. The oxide layer 110 covering the fin 101 is removed, such as using a diluted HF etch prior to the

replacement metal gate (RMG) process described in further detail below. Following removal of the dummy gate 112 and oxide layer 110 covering the fin 101, the fin 101 behind the dummy gate 112 is seen as illustrated.

[0083] FIG. 17 depicts a side cross-sectional view 1700 of the semiconductor structure of FIG. 16 following a RMG process, where a gate dielectric (not shown) is formed surrounding the fin 101 followed by formation of a gate conductor 136.

[0084] The gate dielectric may be formed of a high-k dielectric material, although other suitable materials may be used. Examples of high-k materials include but are not limited to metal oxides such as hafnium oxide (HfO2), hafnium silicon oxide (Hf-Si-O), hafnium silicon oxynitride (HfSiON), lanthanum oxide (La2O3), lanthanum aluminum oxide (LaAlO3), zirconium oxide (ZrO2), zirconium silicon oxide, zirconium silicon oxynitride, tantalum oxide (Ta2O5), titanium oxide (TiO2), barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide (Y2O3), aluminum oxide (Al2O3), lead scandium tantalum oxide, and lead zinc niobate. The high-k material may further include dopants such as lanthanum (La), aluminum (Al), and magnesium (Mg). The gate dielectric may have a uniform thickness in the range of 2nm to 5nm, although other thicknesses above or below this range may be used as desired for a particular application.

[0085] The gate conductor 136 may be formed of any suitable conducting material, including but not limited to, a metal (e.g., tungsten (W), titanium (Ti), tantalum (Ta), ruthenium (Ru), zirconium (Zr), cobalt (Co), copper (Cu), aluminum (Al), lead (Pb), platinum (Pt), tin (Sn), silver (Ag), gold (Au), etc.), a conducting metallic compound material (e.g., tantalum nitride (TaN), titanium nitride (TiN), tantalum carbide (TaCX), titanium carbide (TiC), titanium aluminum carbide, tungsten silicide (WSi2), tungsten nitride (WN), ruthenium oxide (RuO2), cobalt silicide, nickel silicide, etc.), or any suitable combination of these and other suitable materials. The conductive material may further comprise dopants that are incorporated during or after deposition. In some embodiments, the gate conductor includes a work function metal (WFM) layer to set the threshold voltage of the vertical transistor to a desired value. The WFM may be: a nitride, including but not limited to titanium nitride (TiN), titanium aluminum nitride (TiAlN), hafnium nitride (HfN), hafnium silicon nitride (HfSiN), tantalum nitride (TaN), tantalum silicon nitride (TaSiN), tungsten nitride (WN), molybdenum nitride (MoN), niobium nitride (NbN); a carbide, including but not limited to titanium carbide (TiC) titanium aluminum carbide (TiAlC), tantalum carbide (TaC), hafnium carbide (HfC); and combinations thereof.

[0086] The gate conductor 136 fills the regions around the fin 101 as shown, and has a thickness on sidewalls of the spacers and surrounding the gate opening in the range of 3nm to 10nm, although other thicknesses outside this range may be used as desired for a particular application.

[0087] The gate dielectric and gate conductor 136, as mentioned above, are formed using a RMG process. The gate dielectric film and the gate conductor 136 can be formed by suitable deposition processes such as CVD,

plasma enhanced chemical vapor deposition (PECVD), ALD, evaporation, PVD, chemical solution deposition, or other like processes. The thickness of the gate dielectric and the gate conductor 136 can vary depending on the deposition process as well as the composition and number of gate dielectric materials used.

[0088] FIG. 18 depicts a side cross-sectional view 1800 of the semiconductor structure of FIG. 17 following fill with a metal layer 138, also referred to as a gate contact metal layer, in the gate opening as illustrated. The metal layer 138 may be planarized using CMP or other suitable processing to have a surface substantially coplanar with a top surface of ILD 122. The metal layer 138 may be formed of materials similar to that of metal layer 128.

[0089] FIG. 19 depicts a side cross-sectional view 1900 of the semiconductor structure of FIG. 18 following recess of the metal layer 138 and formation of SAC capping layer 140, also referred to as a gate SAC capping layer. The SAC capping layer 140 may be formed of similar materials as that of the SAC capping layer 130, and with similar thickness. The metal layer 138 may be recessed using processing similar to that used for recess of metal layer 128.

[0090] FIG. 20 depicts a side cross-sectional view 2000 of the semiconductor structure of FIG. 19 following patterning of a mask layer 142 and forming an opening to the bottom source/drain regions 106. The mask layer 142 may be formed with similar materials and sizing as that described above with respect to mask layer 124. The opening to the bottom source/drain regions 106 may be formed by directional RIE or other suitable processing.

[0091] FIG. 21 depicts a side cross-sectional view 2100 of the semiconductor structure of FIG. 20 following fill of a metal layer 144, also referred to as bottom source/drain contact metal layer, in the opening to the bottom source/drain regions 106. FIG. 21 also depicts recess of the metal layer 144 and formation of a SAC capping layer 146, also referred to as a bottom source/drain capping layer. The metal layer 144 may be formed of similar materials and with similar processing as metal layers 128 and 138. The SAC capping layer 146 may be formed of similar materials and similar sizing using processing similar to that described with respect to formation of SAC capping layers 130 and 140.

[0092] FIG. 22 depicts a side cross-sectional view 2200 of the semiconductor structure of FIG. 21 following formation of a liner 148 and an ILD 150. The liner 148 may be formed of similar materials as the top spacers 114 and SAC capping layers 130, 140 and 146. The liner 148 may have a height or vertical thickness (in direction Y-Y') in the range of 5nm to 20nm, although other thickness outside this range may be used as desired for a particular application. The ILD 150 may be formed of similar materials as the ILD 122. The ILD 150 have a height or vertical thickness (in direction Y-Y') in the range of 30nm to 150nm, although other thickness outside this range may be used as desired for a particular application.

[0093] FIG. 23 depicts a side cross-sectional view 2300 of the semiconductor structure of FIG. 22 following

formation of vias 152, 154 and 156 providing access to contacts for the bottom source/drain regions 106, the top source/drain regions 126, and to the gate conductor 136, respectively (via metal layers 128, 138 and 144, respectively). The vias 152, 154 and 156 may be formed using conformal deposition processing such as CVD or ALD, and may each have a width or horizontal thickness (in direction X-X') at top surfaces thereof in the range of 20nm to 100nm, although other widths outside this range may be used as desired for a particular application. It is also to be appreciated that the vias 152, 154 and 156 may have different widths.

[0094] FIG. 24 depicts a top-down view 2400 of the semiconductor structure of FIG. 23. It should be noted that the top-down view 2400 is presented to illustrate locations of the vias 152, 154 and 156 relative to fins 101, and as such omits various details of underlying layers for clarity of illustration. The bottom source/drain contact via 152 may have a thickness (in direction Y-Y') of 30nm, or more generally in the range of 20nm to 100nm, although other suitable thicknesses may be used as desired for a particular application. Each of the fins 101 may have a length (in direction Y-Y') of 45nm, or more generally in the range of 10nm to 200nm, although other suitable lengths may be used as desired for a particular application. The top source/drain contacts 154 may have lengths that match that of the fins 101 as illustrated, though this is not a requirement. The gate contact via 156 may have a thickness (in direction Y-Y') of 20nm, or more generally in the range of 15nm to 100nm, although other suitable thicknesses may be used as desired for a particular application.

[0095] The top-down view 2400 shows mask regions 2401, 2403 and 2405 of the semiconductor structure. The mask region 2401 illustrates where the bottom source/drain 106 is formed. The mask region 2403 illustrates where the gate is formed. The mask region 2405 illustrates where the opening to expose the dummy gate 112 is formed.

[0096] RMG schemes for a vertical transistor requires the removal of the dummy gate and deposition of gate dielectrics and gate conductor through the gate contact opening 156. Since there is a high risk of gate to source/drain region shorts due to the process variation of lithography and etch, the gate contact opening should be placed away from the top source/drain region. The distance between the fin 101 and the gate contact opening 156 is generally in the range of 20nm to 100nm, which makes it difficult to remove the dummy gate and deposit the gate dielectrics and gate conductor. However, the SAC capping layers formed on the tops of the openings to the top and bottom source/drain regions in illustrative embodiments advantageously enables the RMG process without dimensional limitations and gate to top source/drain shorts.

[0097] As mentioned above, the side cross-sectional views of FIGS. 1-12 are taken perpendicular to a length of the fins 101, such as along line A-A in the top-down view 2400 of FIG. 24. The side cross-sectional views of FIGS. 13-23 are taken parallel to a length of the fins 101, such as along line B-B in the top-down view 2400 of FIG. 24.

[0098] In some embodiments, RMG processes may be used to form multiple different channel lengths for VTFETs formed on a common substrate. FIGS. 25-34 illustrate an example of such processing for forming multiple

different channel lengths.

[0099] FIG. 25 depicts a side cross-sectional view 2500 of a semiconductor structure similar to the semiconductor structure shown in FIG. 3, with similarly labeled elements being formed of similar materials, with similar size and with similar processing. In the semiconductor structure shown in FIG. 25, however, the fins are arranged in different regions 2501-1 and 2501-2, with a STI region 2503 (formed of similar materials as STI region 103) formed between the fins in the different regions 2501-1 and 2501-2. The STI region 2503 may be formed after formation of bottom source/drain regions 106. In the example process described below with respect to FIGS. 25-34, the fins in region 2501-1 are used to form "long" channel devices with the fins in region 2501-2 being used to form "short" channel devices.

[00100] FIG. 26 depicts a side cross-sectional view 2600 of the semiconductor structure of FIG. 25 following patterning of a mask layer 2505 over a top surface thereof, and etching to pattern or remove the portions of the dummy gate 112 exposed by the mask layer 2505. The mask layer 2505 may be formed of similar materials and with similar sizing as that described above with respect to mask layer 124. The opening 2601 may have a width in the range of 20nm to 150nm, although other suitable widths above or below this range may be used so long as a sufficient portion of the dummy gate 112 material remains surrounding the fins nearest to the opening 2601 in the regions 2501-1 and 2501-2. The dummy gate 112 exposed by the mask layer 2505 may be removed using directional RIE or other suitable processing.

[00101] FIG. 27 depicts a side cross-sectional view 2700 of the semiconductor structure of FIG. 26 following formation of liner 2507. The liner 2507 may be formed of materials similar to that bottom spacers 108 (e.g., SiN). The liner 2507 may have a width or thickness (in direction X-X') in the range of 5nm to 20nm, although other suitable widths above or below this range may be used as desired for a particular application. The liner 2508 may be formed by any suitable deposition followed by RIE.

[00102] FIG. 28 depicts a side cross-sectional view 2800 of the semiconductor structure of FIG. 27 following recess of the dummy gate 112. The recess of the dummy gate 112 may use processing similar to that described above with respect to FIG. 4, though in the FIG. 28 example the dummy gate 112 in the long channel region (e.g., 2501-1) is recessed a first depth 2801 while the dummy gate 112 in the short channel region (e.g., 2501-2) is recessed a second depth 2803, with the second depth 2803 being greater than the first depth 2801. In some embodiments, the first depth 2801 may be in the range of 15nm to 100nm, while the second depth 2803 is in the range of 25nm to 110nm, although other depths outside these ranges may be used to form different channel lengths as desired. It is to be appreciated that while FIGS. 25-34 illustrate an example wherein two different channel lengths are formed, embodiments are not so limited. Instead, any number of different channel lengths may be formed as desired using techniques similar to those described with respect to FIGS. 25-34.

[00103] The recess of dummy gate 112 to the different depths 2801 and 2803 may involve first recessing the dummy gate 112 in both the long and short channel regions to the depth 2801, followed by masking or protecting the dummy gate 112 in the long channel region followed by additional recess of the dummy gate 112 in the short channel region. Alternately, the recess of the dummy gate 112 in the long channel region may be performed while the dummy gate 112 in the short channel region is protected, followed by recess of the dummy gate 112 in the short channel region while the dummy gate 112 in the long channel region is protected (or vice versa).

[00104] FIG. 29 depicts a side cross-sectional view 2900 of the semiconductor structure of FIG. 28 following formation of top spacers 2514, which may be formed with similar materials, similar sizing and with similar processing as top spacers 114. Prior to formation of the top spacers 2514, the hard mask 104 over each fin is removed, and the oxide 110 is recessed to have a top surface substantially coplanar with the surrounding dummy gate 112. The liner 2507 is also removed prior to formation of top spacers 2514.

[00105] FIG. 30 depicts a side cross-sectional view 3000 of the semiconductor structure of FIG. 29 following formation of top junctions 2516. The formation of top junctions 2516 may use processing similar to that described above with respect to formation of top junctions 116. As shown in FIG. 30, the top junctions 2516 in the short channel region are “longer” or have greater vertical thickness relative to the top junctions 2516 in the long channel region. The top junctions 2516 in both the long and short channel regions extend below a surface of the surrounding dummy gate 112 to a depth in the range of 2nm to 10nm, although other suitable depths outside this range may be used as desired for a particular application. The top junctions 2516, however, should be overlapped with the gate conductor, otherwise transistor performance may be degraded due to the undoped region.

[00106] FIG. 31 depicts a side cross-sectional view 3100 of the semiconductor structure of FIG. 30 following formation of isolation layer 2518, spacer 2520 and ILD 2522. The isolation layer 2518, spacer 2520 and ILD 2522 may be formed of similar materials, with similar sizing and using similar processing as that described above with respect to isolation layer 118, spacer 120 and ILD 122, respectively.

[00107] FIG. 32 depicts a side cross-sectional view 3200 of the semiconductor structure of FIG. 31 following opening to expose the top junctions 2516, by using a patterned mask layer 2524. The mask layer 2524 may be patterned in a manner similar to that described above with respect to mask layer 124. The openings to expose the top junctions 2516 may be formed using processing similar to that described above with respect to FIG. 9.

[00108] FIG. 33 depicts a side cross-sectional view 3300 of the semiconductor structure of FIG. 32 following formation of top source/drain regions 2526 and formation of metal layer 2528 over the top source/drain regions 2526. The top source/drain regions 2526 may be formed of similar materials, with similar sizing and using similar processing as that described above with respect to top source/drain regions 126. FIG. 33, however, illustrates an embodiment where the optional lateral etch of FIG. 10 is not performed. In other embodiments, however, the

optional lateral etch described above with respect to FIG. 10 may also be used for formation of top source/drain regions 2526. The metal layer 2528 may be formed of similar materials, with similar sizing and using similar processing as that described above with respect to metal layer 128.

[00109] FIG. 34 depicts a side cross-sectional view 3400 of the semiconductor structure of FIG. 33 following recess of the metal layer 2528 and formation of SAC capping layer 2530, also referred to herein as top source/drain SAC capping layer. The recess of metal layer 2528 and formation of SAC capping layer 2530 may use processing similar to that described above with respect to FIG. 12. The SAC capping layer 2530 may be formed of similar materials and with similar sizing as SAC capping layer 130.

[00110] FIGS. 25-34, similar to FIGS. 1-12, are cross-sectional views taken perpendicular to the fins (e.g., along the line A-A in the top-down view 2400 of FIG. 24). The semiconductor structure of FIG. 34 may be subject to further processing for RMG similar to that described above with respect to FIGS. 13-23.

[00111] The RMG techniques described herein may also be used in the formation of CMOS devices or for CMOS patterning. RMG processes for CMOS patterning will now be described with respect to FIGS. 35-45.

[00112] FIG. 35 depicts a side cross-sectional view 3500 of a semiconductor structure with a shared dummy gate 3512. The semiconductor structure of FIG. 35 includes a substrate 3502, STI region 3503, bottom source/drain regions 3506-1 and 3506-2 (collectively, bottom source/drain regions 3506), bottom spacer 3508, top spacer 3510, ILD 3522, top source/drain regions 3526-1 and 3526-2 (collectively, top source/drain regions 3526), metal layer 3528 and SAC capping layer 3530, which may be formed of similar materials, with similar sizing and using similar processing as that described above with respect to substrate 102, STI region 103, bottom source/drain regions 106, bottom spacer 108, top spacer 110, ILD 122, top source/drain regions 126, metal layer 128 and SAC capping layer 130, respectively. FIG. 35, however, illustrates a CMOS arrangement, with a first fin 3501-1 that forms an NFET and a second fin 3502-2 that forms a PFET. The fins 3501-1 and 3501-2 (collectively, fins 3501) are shown in dashed outline as they are "behind" the shared dummy gate 3512 in the side cross-sectional view 3500.

[00113] The bottom source/drain region 3506-1 and top source/drain region 3526-1 for the NFET may be doped with an n-type dopant, with the bottom source/drain region 3506-2 and top source/drain region 3526-2 being doped with a p-type dopant. A distance 3505 between the fins 3501-1 and 3501-2 may be 75nm, or more generally in the range of 30nm to 100nm, although other distances outside this range may be used as desired, so long as there is sufficient space for formation of a shared gate contact using the processing described below.

[00114] FIG. 36 depicts a side cross-sectional view 3600 of the semiconductor structure of FIG. 35 following opening of the shared dummy gate 3512 using a patterned mask layer 3532. The opening to the shared dummy gate 3512 may be formed using processing similar to that described above with respect to FIG. 14. The mask layer

3532 may be formed with similar materials and with similar sizing as the mask layer 132.

[00115] FIG. 37 depicts a side cross-sectional view 3700 of the semiconductor structure of FIG. 36 following formation of a liner 3534 using processing similar to that described above with respect to FIG. 15. The liner 3534 may be formed with similar materials and with similar sizing as the liner 134.

[00116] FIG. 38 depicts a side cross-sectional view 3800 of the semiconductor structure of FIG. 37 following removal of the shared dummy gate 3512. The shared dummy gate 3512 may be removed using processing similar to that described above with respect to removal of dummy gate 112.

[00117] FIG. 39 depicts a side cross-sectional view 3900 of the semiconductor structure of FIG. 38 following deposition of a gate dielectric (not shown) and a PFET WFM 3536-2 (more generally, a PFET gate conductor 3536-2). Initially, the PFET WFM 3536-2 is formed surrounding the fin 3501-1 for the NFET device as shown, but is removed during later processing described below. The PFET WFM 3536-2 may be formed of a nitride such as titanium nitride (TiN), titanium aluminum nitride (TiAlN), tantalum nitride (TaN), tantalum silicon nitride (TaSiN), or a carbide including but not limited to titanium carbide (TiC), titanium aluminum carbide (TiAlC), tantalum carbide (TaC), although other suitable materials may be used. The PFET WFM 3536-2 may be formed using conformal deposition processing such as ALD or CVD.

[00118] FIG. 40 depicts a side cross-sectional view 4000 of the semiconductor structure of FIG. 39 following patterning of the PFET WFM 3536-2. The PFET WFM 3536-2 is patterned by blocking the PFET region (e.g., the PFET WFM 3536-2 surrounding the fin 3501-2) while the PFET WFM 3536-2 in the NFET region (e.g., portions of the PFET WFM 3536-2 surrounding the fin 3501-1) is removed using a wet chemical etch (e.g., SC1) or other suitable processing. The PFET WFM 3536-2 may be blocked in the PFET region using an organic polymer layer (OPL) 3537. When the PFET WFM 3536-2 is removed in the NFET region, the gate dielectric 3534 surrounding the fin 3501-1 is visible (the gate dielectric 3534 similarly surrounds the fin 3501-2, but it is not visible in the side cross-sectional view 4000). Although the PFET region is blocked by OPL 3537 during removal of the PFET WFM 3536-2 from the NFET region, there is some lateral undercut 4001 removal of the PFET WFM 3536-2 in the PFET region as illustrated. The lateral undercut 4001, however, is small, which advantageously corresponds to very small n-to-p boundary shift during patterning of the gate metal.

[00119] FIG. 41 depicts a side cross-sectional view 4100 of the semiconductor structure of FIG. 40 following formation of an NFET WFM 3536-1 (more generally, an NFET gate conductor 3536-1). The NFET WFM 3536-1 may be formed using conformal deposition processing such as ALD or CVD. The NFET WFM 3536-1 may be formed of a nitride such as titanium nitride (TiN), titanium aluminum nitride (TiAlN), tantalum nitride (TaN), tantalum silicon nitride (TaSiN), a carbide including but not limited to titanium carbide (TiC), titanium aluminum carbide (TiAlC), tantalum carbide (TaC), and combinations thereof, although other suitable materials may be used. It is to

be appreciated that while FIGS. 39-41 illustrate formation of the PFET WFM 3536-2 followed by formation of the NFET WFM 3536-1, in other embodiments the NFET WFM 3536-1 may be formed before formation of the PFET WFM 3536-2 using similar processing (e.g., forming the NFET WFM 3536-1 first followed by blocking the NFET region while the NFET WFM 3536-1 is removed from the PFET region).

[00120] FIG. 42 depicts a side cross-sectional view 4200 of the semiconductor structure of FIG. 41 following fill with metal layer 3538, which may be formed using similar materials and with similar processing as metal layer 138.

[00121] FIG. 43 depicts a side cross-sectional view 4300 of the semiconductor structure of FIG. 42 following recess of the metal layer 3538 (as well as recess of the NFET WFM 3536-1 and PFET WFM 3536-2) and formation of SAC capping layer 3540, also referred to as a gate SAC capping layer or shared gate SAC capping layer. The recess of metal layer 3538 (as well as recess of the NFET WFM 3536-1 and the PFET WFM 3536-2) and formation of SAC capping layer 3540 may use processing similar to that described above with respect to recess of metal layer 138 and formation of SAC capping layer 140. The SAC capping layer 3540 may be formed with similar materials and similar sizing as the SAC capping layer 140.

[00122] FIG. 44 depicts a side cross-sectional view 4400 of the semiconductor structure of FIG. 43 following formation of vias 3554-1 and 3554-2 to access contacts for the top source/drain regions 3526-1 and 3526-2, respectively, as well as formation of via 3556 to access the shared gate contact. The vias 3554-1 and 3554-2 (collectively, vias 3554) and via 3556 may be formed of similar materials, with similar sizing and using similar processing as that described above with respect to formation of vias 154 and 156. Although not shown in FIG. 44, vias 3552-1 and 3552-2 to the bottom source/drain regions 3506-1 and 3506-2 are also formed (as illustrated in FIG. 45, with similar processing as that described with respect to formation of via 152).

[00123] FIG. 45 depicts a top-down view 4500 of the semiconductor structure of FIG. 44. It should be noted that the top-down view 4500 is presented to illustrate locations of the vias 3552-1, 3552-2, 3554-1, 3554-2 and 3556 relative to fins 3501-1 and 3501-2, and as such omits various details of underlying layers for clarity of illustration. The bottom source/drain contacts via 3552-1 and 3552-2 may have sizing similar to that of bottom source/drain contacts 152. Each of the fins 3501 may have a length (in direction Y-Y') similar to that of fins 101. The top source/drain contacts 3554-1 and 3554-2 may have lengths that match that of the fins 3501 as illustrated, though this is not a requirement. The gate contact via 3556 may have a thickness similar to that of gate contact 156.

[00124] The top-down view 4500 shows mask regions 4501, 4503 and 4505 similar to the mask regions 2401, 2403 and 2405. The side cross-sectional views of FIGS. 35-44 are taken parallel to a pair of fins 3501-1 and 3501-2, e.g., along the line B-B in the top-down view 4500 of FIG. 45.

[00125] In some embodiments of the invention, a method of forming a semiconductor structure comprises forming

a plurality of fins disposed over a top surface of a substrate and forming one or more VTFETs from the plurality of fins using a RMG process. A gate surrounding at least one fin of a given one of the VTFETs comprises a gate SAC capping layer disposed over a gate contact metal layer, the gate contact metal layer being disposed adjacent an end of the at least one fin.

[00126] Forming the one or more VTFETs may comprise forming bottom source/drain regions disposed over the top surface of the substrate surrounding the plurality of fins and forming bottom spacers disposed over the bottom source/drain regions.

[00127] Forming the one or more VTFETs may further comprise forming an oxide layer disposed over the bottom spacers and sidewalls of the plurality of fins, forming a dummy gate disposed over the oxide layer, recessing the dummy gate below top surfaces of the plurality of fins, removing exposed portions of the oxide layer, and forming top spacers disposed over the dummy gate and the plurality of fins.

[00128] Forming the one or more VTFETs may further comprise forming top junctions in upper portions of the plurality of fins, forming an oxide layer disposed over the top spacers, forming a liner disposed over the oxide layer, and forming an interlevel dielectric layer disposed over the liner.

[00129] Forming the one or more VTFETs may further comprise forming top source/drain openings in the interlevel dielectric layer to expose top surfaces of the top junctions of each of the plurality of fins, forming top source/drain regions disposed over the top junctions, forming top source/drain contact metal layers disposed over the top source/drain regions, recessing the top source/drain contact metal layers below a top surface of the interlevel dielectric, and forming top source/drain SAC capping layers disposed over the recessed top source/drain contact metal layers.

[00130] Forming the one or more VTFETs may further comprise forming a gate opening in the interlevel dielectric layer to expose a portion of the top spacer disposed over the dummy gate, depositing a liner on sidewalls of the opening of the interlevel dielectric layer, etching the exposed portion of the top spacer to expose a portion of the dummy gate, removing the dummy gate, performing the replacement metal gate process to form a gate dielectric surrounding the one or more fins and to form a metal gate conductor surrounding the gate dielectric, filling the gate contact metal layer in remaining portions of the gate opening in the interlevel dielectric layer, recessing the gate contact metal layer below the top surface of the interlevel dielectric layer, and forming the gate SAC capping layer disposed over the recessed gate contact metal layer.

[00131] Forming the one or more VTFETs may further comprise forming a bottom source/drain opening in the interlevel dielectric layer to expose a portion of the top surface of the bottom source/drain regions, filling a bottom source/drain contact metal layer in the bottom source/drain opening disposed over the exposed portion of the top

surface of the bottom source/drain regions, recessing the bottom source/drain contact metal layer below a top surface of the interlevel dielectric layer, and forming a bottom source/drain SAC capping layer disposed over the recessed bottom source/drain contact layer.

[00132] Forming the one or more VTFETs may further comprise forming an additional liner disposed over the interlevel dielectric, the top source/drain SAC capping layers, the gate SAC capping layer and the bottom source/drain SAC capping layer, forming an additional interlevel dielectric disposed over the additional liner, forming vias in the additional liner, the additional interlevel dielectric, the top source/drain SAC capping layers, the gate SAC capping layer and the bottom source/drain SAC capping layer to expose portions of the top surfaces of the top source/drain contact metal layers, the gate contact metal layer and the bottom source/drain contact metal layer, and forming top source/drain contacts, a gate contact and a bottom source/drain contact in the vias.

[00133] Forming the one or more VTFETs may further comprise forming at least one shallow trench isolation region in the substrate and the bottom source/drain region between a first subset of the plurality of fins and at least a second subset of the plurality of fins, wherein recessing the dummy gate comprises recessing a first portion of the dummy gate surrounding the first subset of the plurality of fins to a first depth and recessing a second portion of the dummy gate surrounding the second subset of the plurality of fins to a second depth greater than the first depth. The first subset of the plurality of fins form VTFETs having a first channel length and the second subset of the plurality of fins form VTFETs having a second channel length smaller than the first channel length.

[00134] Recessing the first portion of the dummy gate and recessing the second portion of the dummy gate may comprise patterning a mask layer over the dummy gate to expose a top surface of the dummy gate disposed over the at least one shallow trench isolation region, removing the exposed portion of the dummy gate to expose a portion of the bottom spacer disposed over the at least one shallow trench isolation region, and forming a liner on exposed sidewalls of the dummy gate.

[00135] The dummy gate may comprise a shared dummy gate surrounding pairs of the plurality of fins, each pair of the plurality of fins comprising a first fin forming a channel for one of a PFET of a given CMOS device and an NFET of the given CMOS device, and a second fin forming a channel for the other one of the PFET and the NFET of the given CMOS device.

[00136] Forming the one or more VTFETs may further comprise patterning a gate opening in an interlevel dielectric layer disposed over a top spacer disposed over the shared dummy gate, removing portions of the interlevel dielectric layer to expose a portion of the top surface of the top spacer, forming a liner on exposed sidewalls of the interlevel dielectric layer in the gate opening, and removing the shared dummy gate.

[00137] Forming the one or more VTFETs may further comprise forming a gate dielectric surrounding the first fin

and the second fin, forming a first gate conductor layer surrounding the gate dielectric, the top surface of the substrate, and the liner disposed on the exposed sidewalls of the interlevel dielectric layer, blocking a first portion of the gate opening and the first gate conductor layer surrounding the first fin with an organic polymer layer, removing the first gate conductor layer surrounding the second fin exposed by the organic polymer layer, removing the organic polymer layer, and forming a second gate conductor layer surrounding the gate dielectric surrounding second fin.

[00138] The method may further comprise filling the gate contact metal layer in the gate opening contacting the first gate conductor layer and the second gate conductor layer, recessing the gate contact metal layer below a top surface of the interlevel dielectric, and forming the gate SAC capping layer disposed over the recessed gate contact metal layer.

[00139] In some embodiments of the invention, a semiconductor structure comprises a substrate and a plurality of fins disposed over a top surface of the substrate, the plurality of fins comprising channels for one or more VTFETs formed with a RMG process. A given one of the VTFETs comprises a gate surrounding at least one of the plurality of fins, the gate of the given VTFET comprising a gate SAC capping layer disposed over a gate contact metal layer, the gate contact metal layer being disposed adjacent an end of the at least one fin.

[00140] The semiconductor structure may further comprise a bottom source/drain region disposed over the top surface of the substrate surrounding the plurality of fins, a bottom spacer disposed over the bottom source/drain region, the gate surrounding the plurality of fins, a top spacer disposed over the gate, top source/drain regions disposed over a portion of the top spacer disposed over each of the plurality of fins, top source/drain contact metal layers disposed over the top source/drain regions, top source/drain SAC capping layers disposed over the top source/drain metal contact layers, a bottom source/drain contact metal layer disposed over a portion of the bottom source/drain region, and a bottom source/drain SAC capping layer disposed over the bottom source/drain metal contact layer.

[00141] In some embodiments, at least two of the plurality fins have different heights.

[00142] In some embodiments, the gate of the given VTFET comprises a shared gate surrounding pairs of the plurality of fins, each pair of the plurality of fins comprising a first fin forming a channel for one of a PFET of a given CMOS device and an NFET of the given CMOS device and a second fin forming a channel for the other one of the PFET and the NFET of the given CMOS device.

[00143] In some embodiments of the invention, the shared gate comprises a first gate conductor surrounding the first fin and a second gate conductor surrounding the second fin, the gate contact metal layer contacting the first gate conductor and the second gate conductor.

[00144] In some embodiments of the invention, an integrated circuit comprises one or more VTFETs comprising a substrate and a plurality of fins disposed over a top surface of the substrate, the plurality of fins comprising channels for the one or more VTFETs formed with a RMG process. A given one of the VTFETs comprises a gate surrounding at least one of the plurality of fins, the gate of the given VTFET comprising a gate SAC capping layer disposed over a gate contact metal layer, the gate contact metal layer being disposed adjacent an end of the at least one fin.

[00145] It is to be appreciated that the various materials, processing methods (e.g., etch types, deposition types, etc.) and dimensions provided in the discussion above are presented by way of example only. Various other suitable materials, processing methods, and dimensions may be used as desired.

[00146] Semiconductor devices and methods for forming same in accordance with the above-described techniques can be employed in various applications, hardware, and/or electronic systems. Suitable hardware and systems for implementing embodiments of the invention may include, but are not limited to, sensors an sensing devices, personal computers, communication networks, electronic commerce systems, portable communications devices (e.g., cell and smart phones), solid-state media storage devices, functional circuitry, etc. Systems and hardware incorporating the semiconductor devices are contemplated embodiments of the invention. Given the teachings provided herein, one of ordinary skill in the art will be able to contemplate other implementations and applications of embodiments of the invention.

[00147] Various structures described above may be implemented in integrated circuits. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

[00148] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope the invention. The terminology used herein was chosen to best explain the principles of the embodiments of the invention, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments of the invention disclosed herein.

CLAIMS

1. A method of forming a semiconductor structure, comprising:

forming a plurality of fins disposed over a top surface of a substrate; and

forming one or more vertical transport field-effect transistors (VTFETs) from the plurality of fins using a replacement metal gate (RMG) process;

wherein a gate surrounding at least one fin of a given one of the VTFETs comprises a gate self-aligned contact (SAC) capping layer disposed over a gate contact metal layer, the gate contact metal layer being disposed adjacent an end of the at least one fin.

2. The method of claim 1, wherein forming the one or more VTFETs comprises:

forming bottom source/drain regions disposed over the top surface of the substrate surrounding the plurality of fins; and

forming bottom spacers disposed over the bottom source/drain regions.

3. The method of claim 2, wherein forming the one or more VTFETs further comprises:

forming an oxide layer disposed over the bottom spacers and sidewalls of the plurality of fins;

forming a dummy gate disposed over the oxide layer;

recessing the dummy gate below top surfaces of the plurality of fins;

removing exposed portions of the oxide layer; and

forming top spacers disposed over the dummy gate and the plurality of fins.

4. The method of claim 3, wherein forming the one or more VTFETs further comprises:

forming top junctions in upper portions of the plurality of fins;

forming an oxide layer disposed over the top spacers;

forming a liner disposed over the oxide layer; and

forming an interlevel dielectric layer disposed over the liner.

5. The method of claim 4, wherein forming the one or more VTFETs comprises:

forming top source/drain openings in the interlevel dielectric layer to expose top surfaces of the top junctions of each of the plurality of fins;

forming top source/drain regions disposed over the top junctions;

forming top source/drain contact metal layers disposed over the top source/drain regions;

recessing the top source/drain contact metal layers below a top surface of the interlevel dielectric; and

forming top source/drain SAC capping layers disposed over the recessed top source/drain contact metal layers.

6. The method of claim 5, wherein forming the one or more VTFETs further comprises:

forming a gate opening in the interlevel dielectric layer to expose a portion of the top spacer disposed over the dummy gate;

depositing a liner on sidewalls of the opening of the interlevel dielectric layer;

etching the exposed portion of the top spacer to expose a portion of the dummy gate;

removing the dummy gate;

performing the replacement metal gate process to form a gate dielectric surrounding the one or more fins and to form a metal gate conductor surrounding the gate dielectric;

filling the gate contact metal layer in remaining portions of the gate opening in the interlevel dielectric layer;

recessing the gate contact metal layer below the top surface of the interlevel dielectric layer; and

forming the gate SAC capping layer disposed over the recessed gate contact metal layer.

7. The method of claim 6, wherein forming the one or more VTFETs further comprises:

forming a bottom source/drain opening in the interlevel dielectric layer to expose a portion of the top surface of the bottom source/drain regions;

filling a bottom source/drain contact metal layer in the bottom source/drain opening disposed over the exposed portion of the top surface of the bottom source/drain regions;

recessing the bottom source/drain contact metal layer below a top surface of the interlevel dielectric layer; and

forming a bottom source/drain SAC capping layer disposed over the recessed bottom source/drain contact layer.

8. The method of claim 7, wherein forming the one or more VTFETs further comprises:

forming an additional liner disposed over the interlevel dielectric, the top source/drain SAC capping layers, the gate SAC capping layer and the bottom source/drain SAC capping layer;

forming an additional interlevel dielectric disposed over the additional liner;

forming vias in the additional liner, the additional interlevel dielectric, the top source/drain SAC capping layers, the gate SAC capping layer and the bottom source/drain SAC capping layer to expose portions of the top surfaces of the top source/drain contact metal layers, the gate contact metal layer and the bottom source/drain contact metal layer; and

forming top source/drain contacts, a gate contact and a bottom source/drain contact in the vias.

9. The method of claim 3, wherein forming the one or more VTFETs further comprises forming at least one shallow trench isolation region in the substrate and the bottom source/drain region between a first subset of the plurality of fins and at least a second subset of the plurality of fins, wherein recessing the dummy gate comprises:

recessing a first portion of the dummy gate surrounding the first subset of the plurality of fins to a first depth; and

recessing a second portion of the dummy gate surrounding the second subset of the plurality of fins to a second depth greater than the first depth;

wherein the first subset of the plurality of fins form VTFETs having a first channel length; and

wherein the second subset of the plurality of fins form VTFETs having a second channel length smaller than the first channel length.

10. The method of claim 9, wherein recessing the first portion of the dummy gate and recessing the second portion of the dummy gate comprises:

patterning a mask layer over the dummy gate to expose a top surface of the dummy gate disposed over the at least one shallow trench isolation region;

removing the exposed portion of the dummy gate to expose a portion of the bottom spacer disposed over the at least one shallow trench isolation region; and

forming a liner on exposed sidewalls of the dummy gate.

11. The method of claim 3, wherein the dummy gate comprises a shared dummy gate surrounding pairs of the plurality of fins, each pair of the plurality of fins comprising:

a first fin forming a channel for one of a p-type field-effect transistor (PFET) of a given complementary metal-oxide-semiconductor (CMOS) device and an n-type field-effect transistor (NFET) of the given CMOS device; and

a second fin forming a channel for the other one of the PFET and the NFET of the given CMOS device.

12. The method of claim 11, wherein forming the one or more VTFETs further comprises:

patterning a gate opening in an interlevel dielectric layer disposed over a top spacer disposed over the shared dummy gate;

removing portions of the interlevel dielectric layer to expose a portion of the top surface of the top spacer;

forming a liner on exposed sidewalls of the interlevel dielectric layer in the gate opening; and

removing the shared dummy gate.

13. The method of claim 12, wherein forming the one or more VTFETs further comprises:

forming a gate dielectric surrounding the first fin and the second fin;

forming a first gate conductor layer surrounding the gate dielectric, the top surface of the substrate, and the liner disposed on the exposed sidewalls of the interlevel dielectric layer;

blocking a first portion of the gate opening and the first gate conductor layer surrounding the first fin with an organic polymer layer;

removing the first gate conductor layer surrounding the second fin exposed by the organic polymer layer;

removing the organic polymer layer; and

forming a second gate conductor layer surrounding the gate dielectric surrounding second fin.

14. The method of claim 13, further comprising:

filling the gate contact metal layer in the gate opening contacting the first gate conductor layer and the second gate conductor layer;

recessing the gate contact metal layer below a top surface of the interlevel dielectric; and

forming the gate SAC capping layer disposed over the recessed gate contact metal layer.

15. A semiconductor structure, comprising:

a substrate; and

a plurality of fins disposed over a top surface of the substrate, the plurality of fins comprising channels for one or more vertical transport field-effect transistors (VTFETs) formed with a replacement metal gate (RMG) process;

wherein a given one of the VTFETs comprises a gate surrounding at least one of the plurality of fins, the gate of the given VTFET comprising a gate self-aligned contact (SAC) capping layer disposed over a gate contact metal layer, the gate contact metal layer being disposed adjacent an end of the at least one fin.

16. The semiconductor structure of claim 15, further comprising:

a bottom source/drain region disposed over the top surface of the substrate surrounding the plurality of fins;

a bottom spacer disposed over the bottom source/drain region;

the gate surrounding the plurality of fins;

a top spacer disposed over the gate;

top source/drain regions disposed over a portion of the top spacer disposed over each of the plurality of fins;

top source/drain contact metal layers disposed over the top source/drain regions;

top source/drain SAC capping layers disposed over the top source/drain metal contact layers;

a bottom source/drain contact metal layer disposed over a portion of the bottom source/drain region; and

a bottom source/drain SAC capping layer disposed over the bottom source/drain metal contact layer.

17. The semiconductor structure of claim 16, wherein at least two of the plurality fins have different heights.

18. The semiconductor structure of claim 16, wherein the gate of the given VTFET comprises a shared gate surrounding pairs of the plurality of fins, each pair of the plurality of fins comprising:

a first fin forming a channel for one of a p-type field-effect transistor (PFET) of a given complementary metal-oxide-semiconductor (CMOS) device and an n-type field-effect transistor (NFET) of the given CMOS device; and

a second fin forming a channel for the other one of the PFET and the NFET of the given CMOS device.

19. The semiconductor structure of claim 18, wherein the shared gate comprises a first gate conductor surrounding the first fin and a second gate conductor surrounding the second fin, the gate contact metal layer contacting the first gate conductor and the second gate conductor.

20. An integrated circuit comprising a semiconductor structure as claimed in any of claims 15 to 19.

FIG. 1

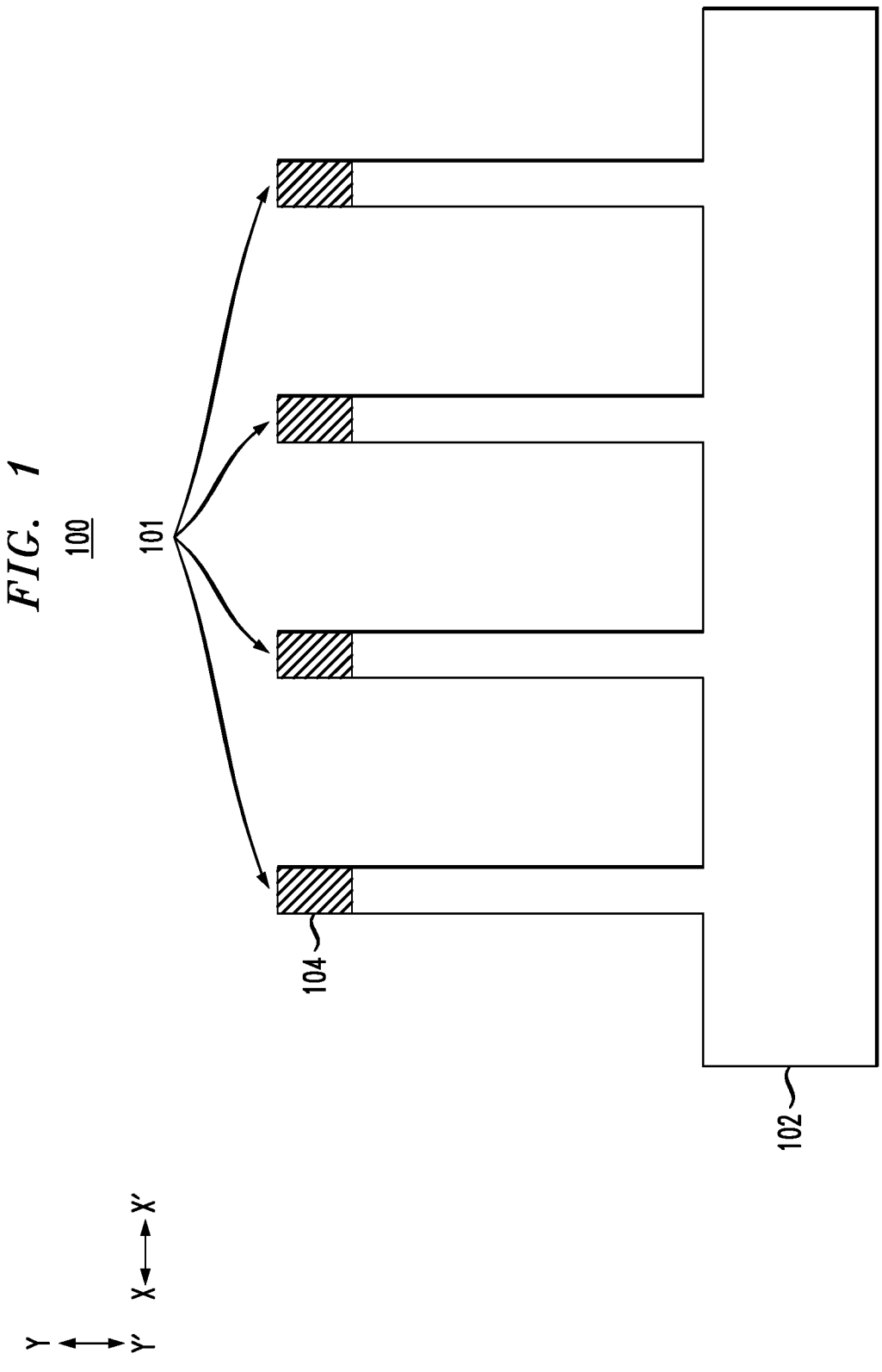


FIG. 2

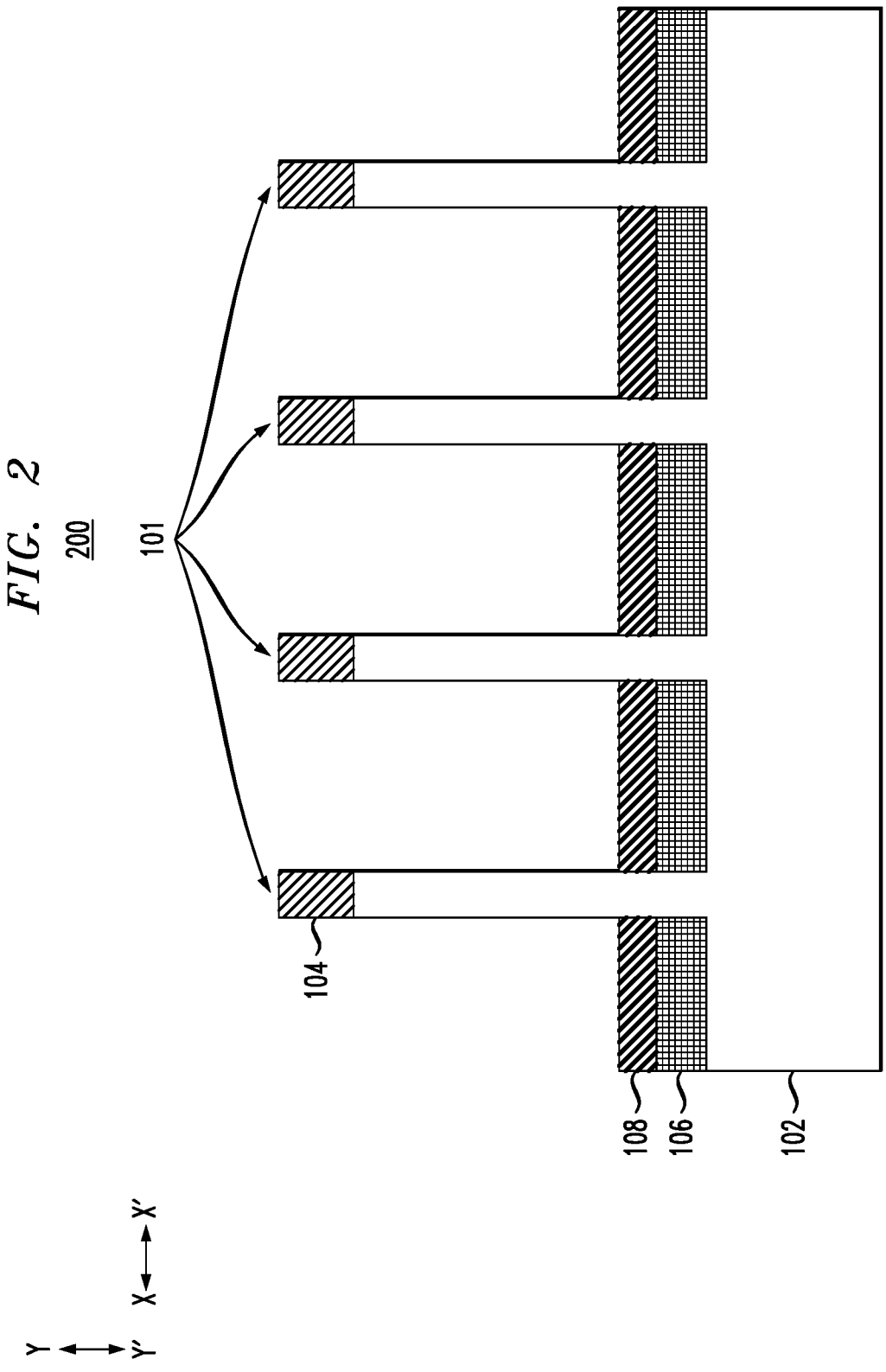


FIG. 3

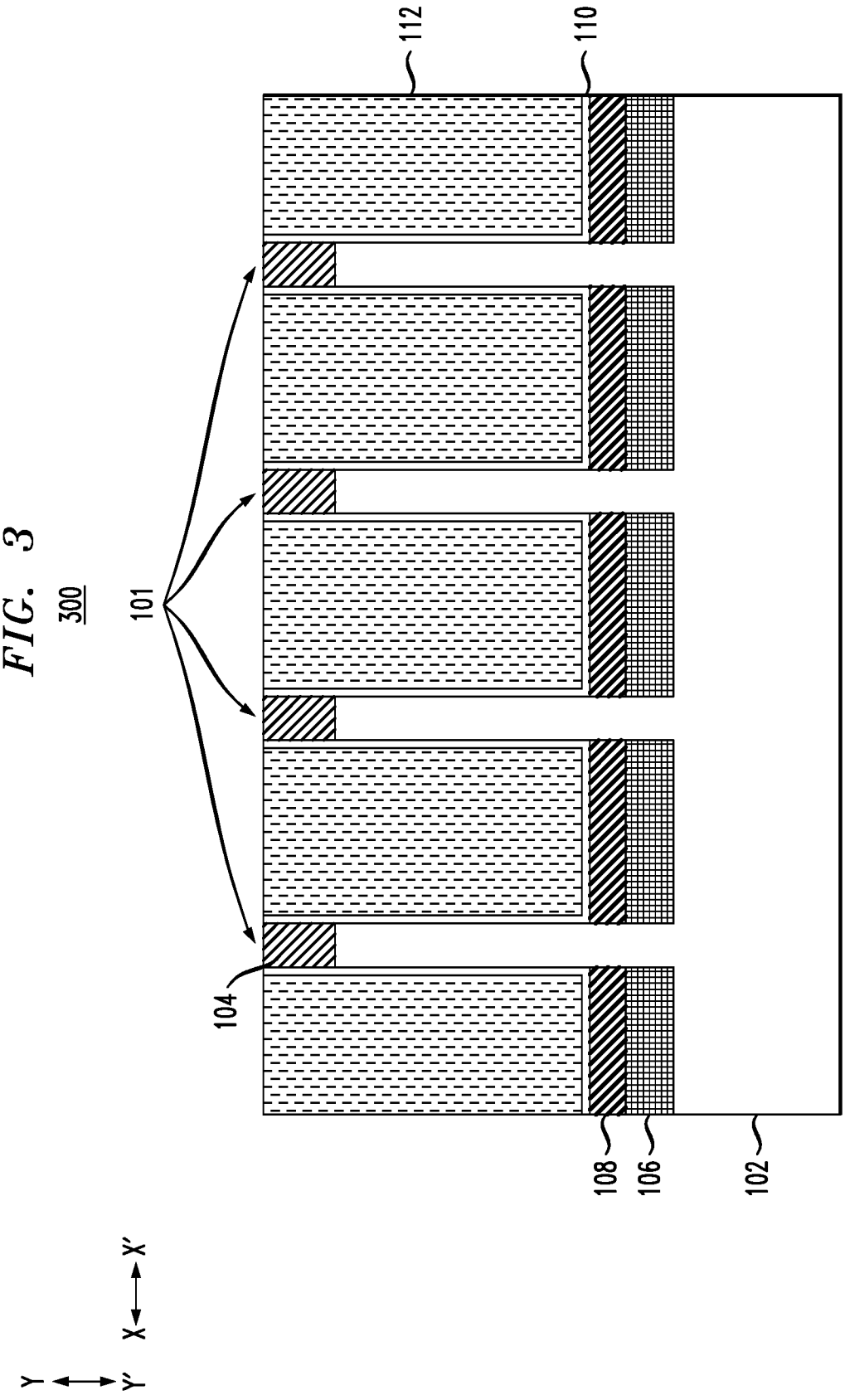


FIG. 4

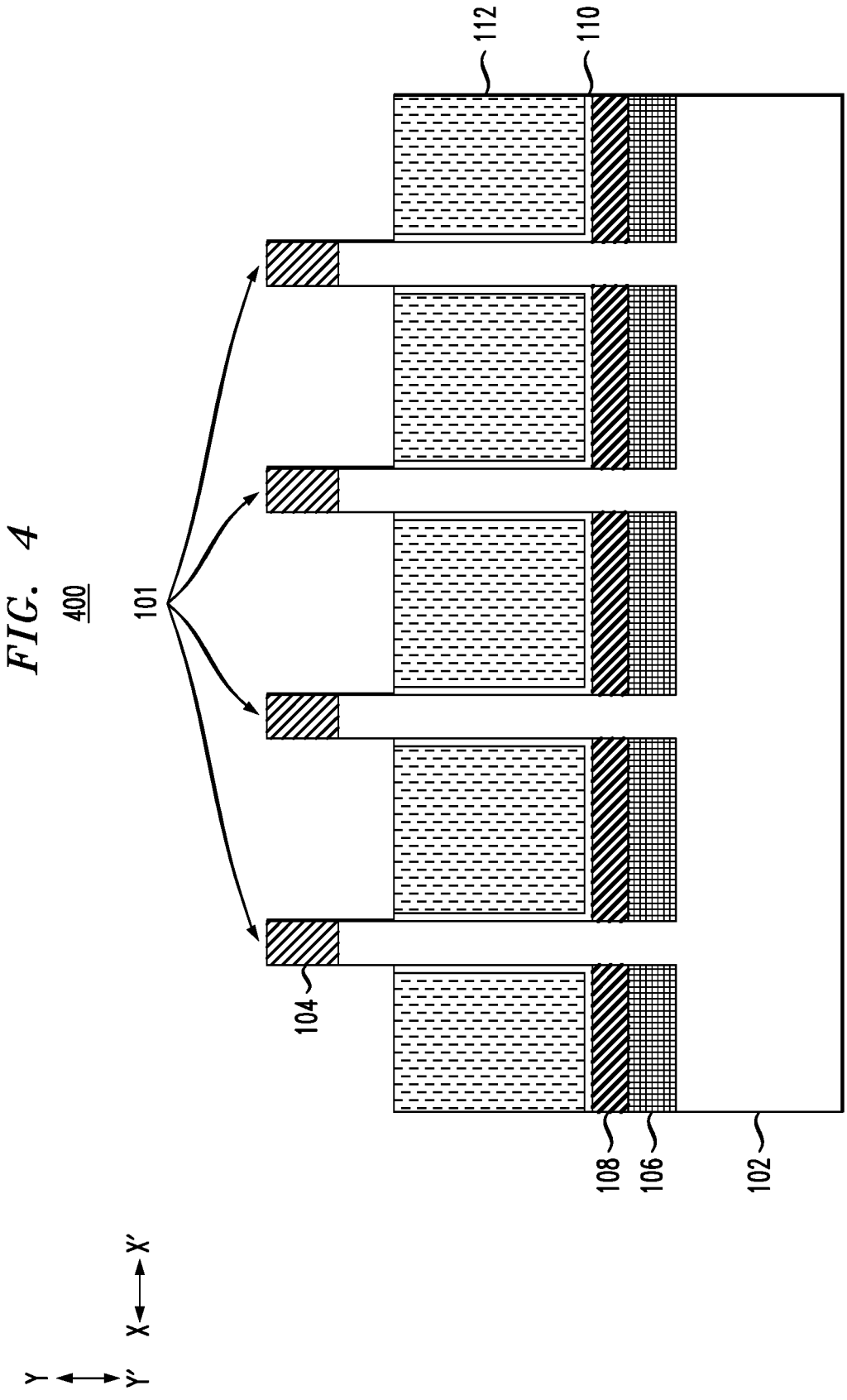


FIG. 5

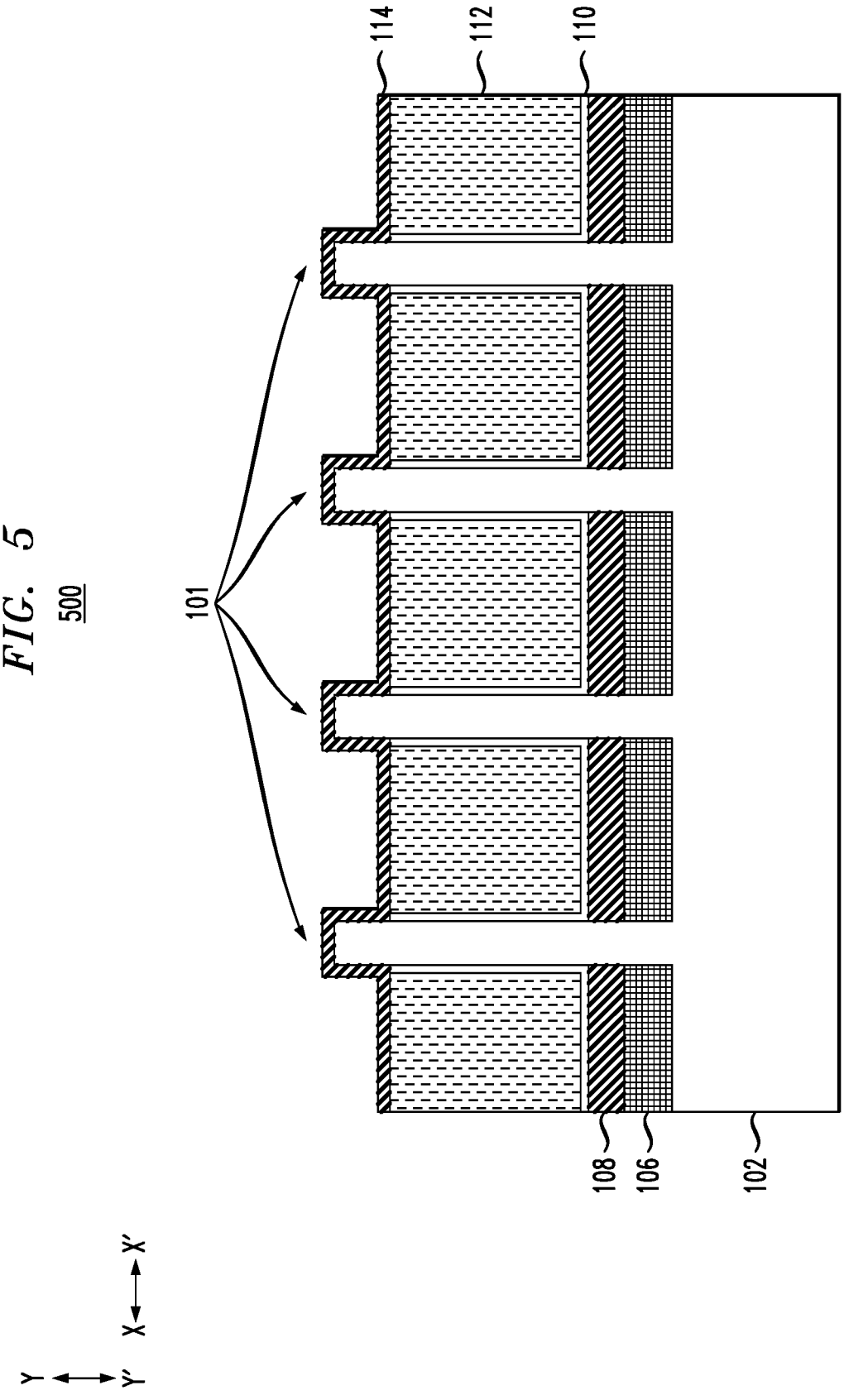


FIG. 6

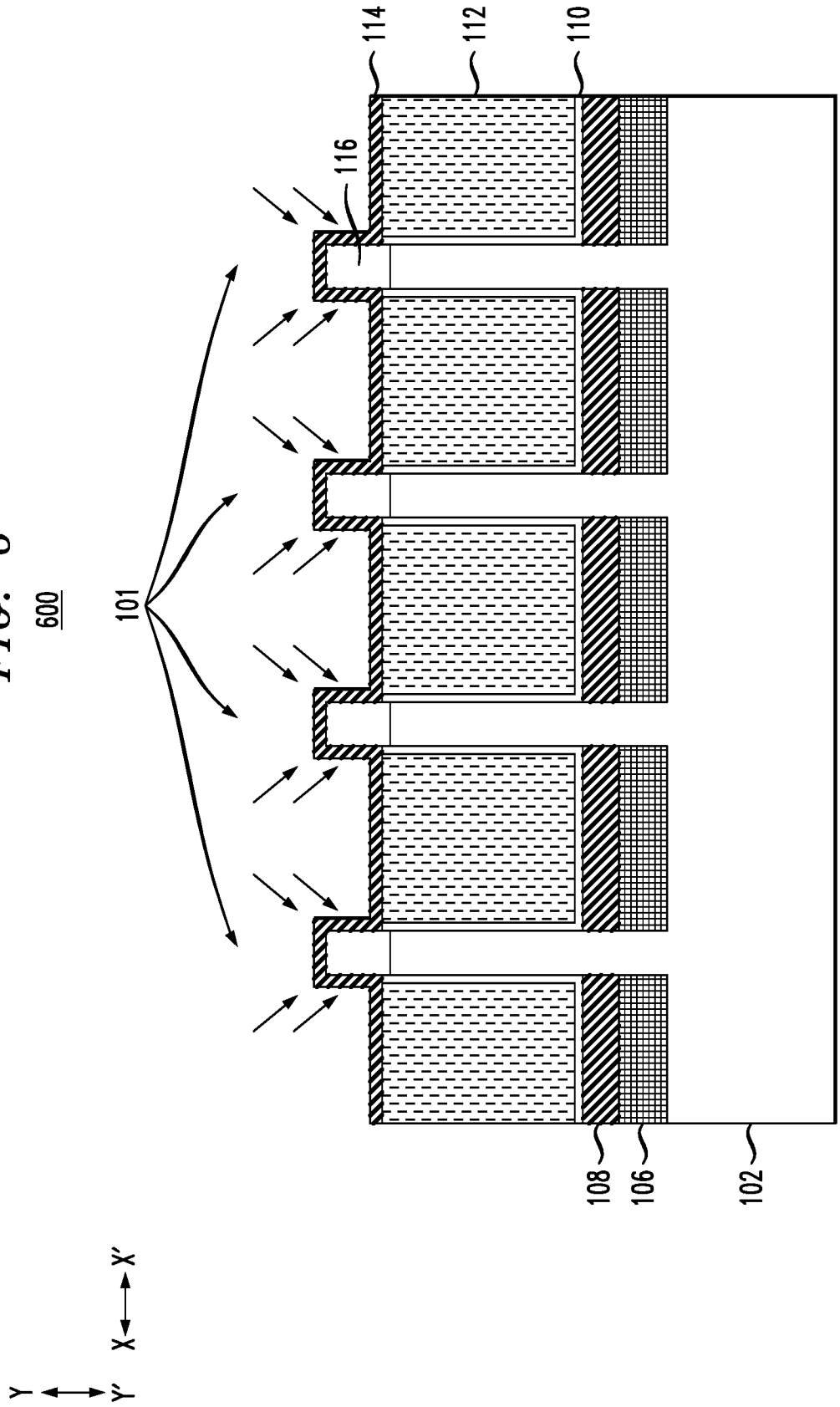


FIG. 7

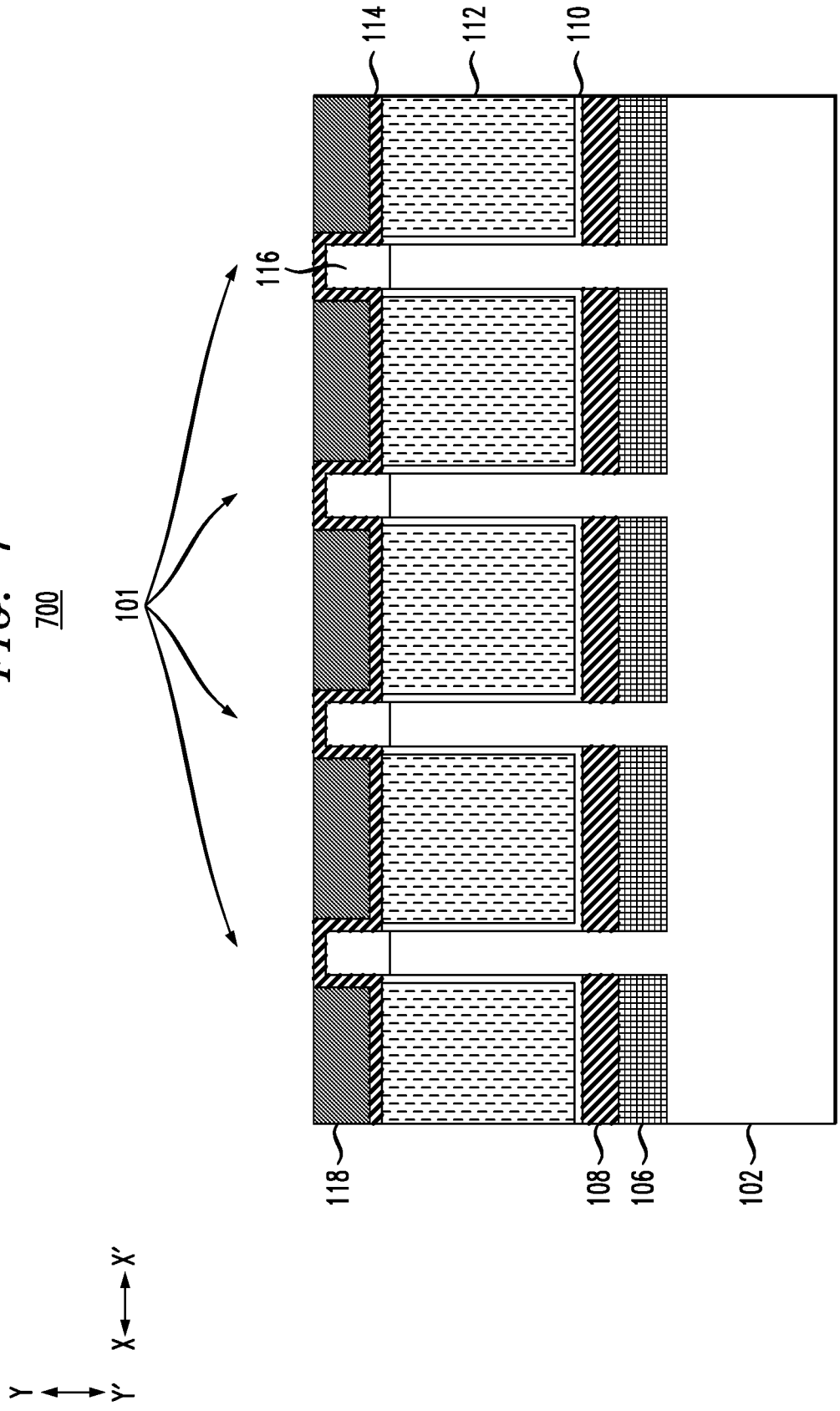


FIG. 8

800

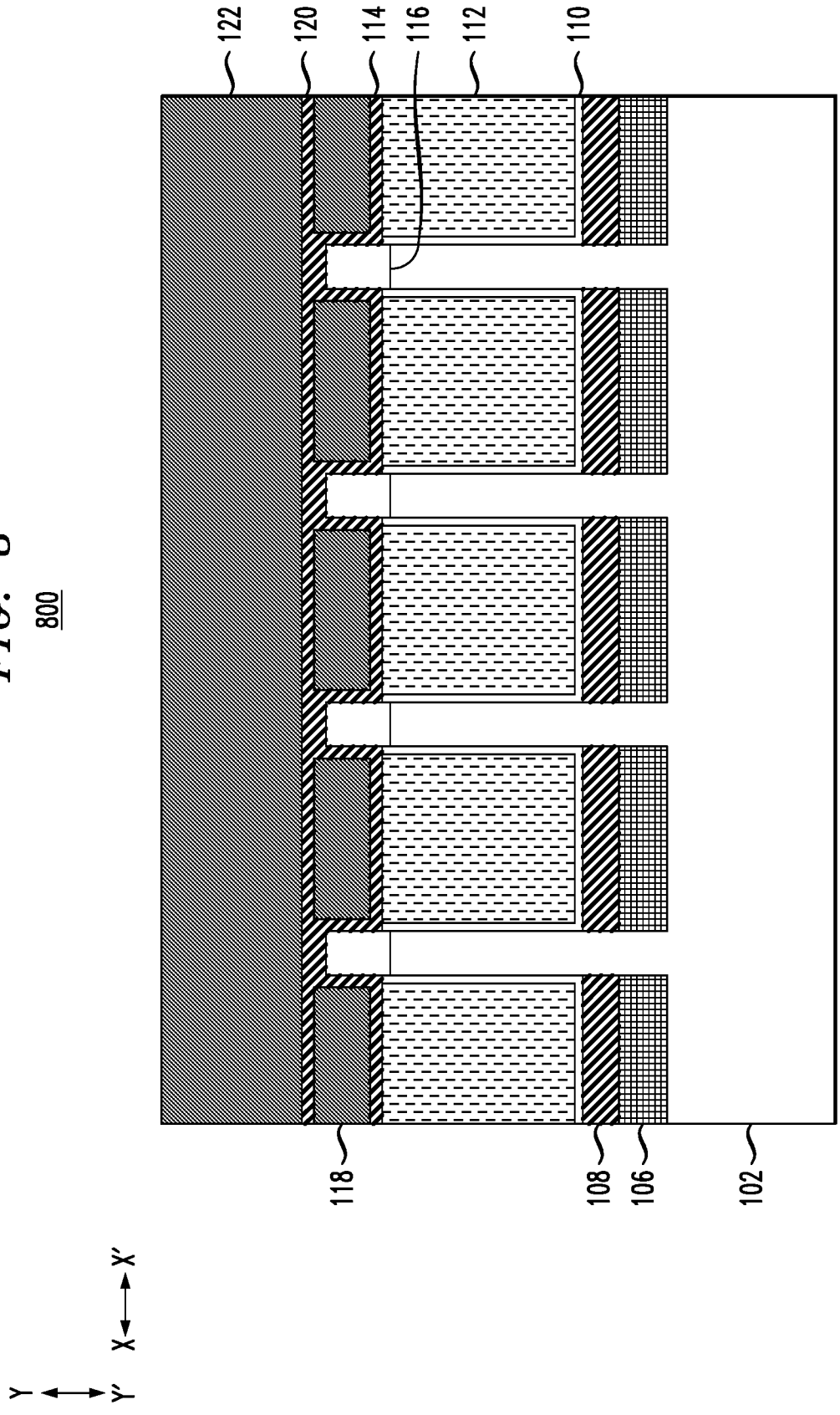


FIG. 9

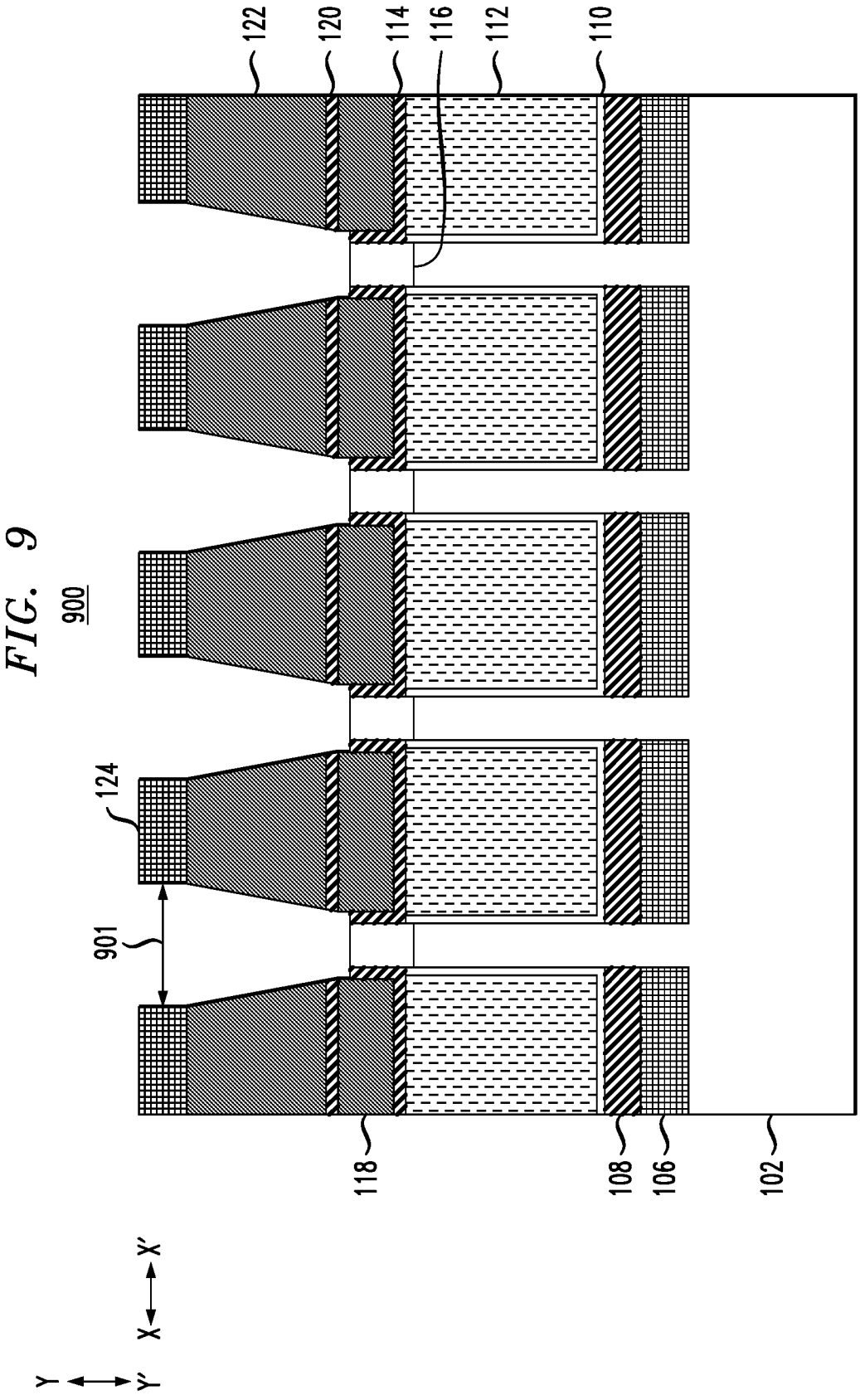


FIG. 10

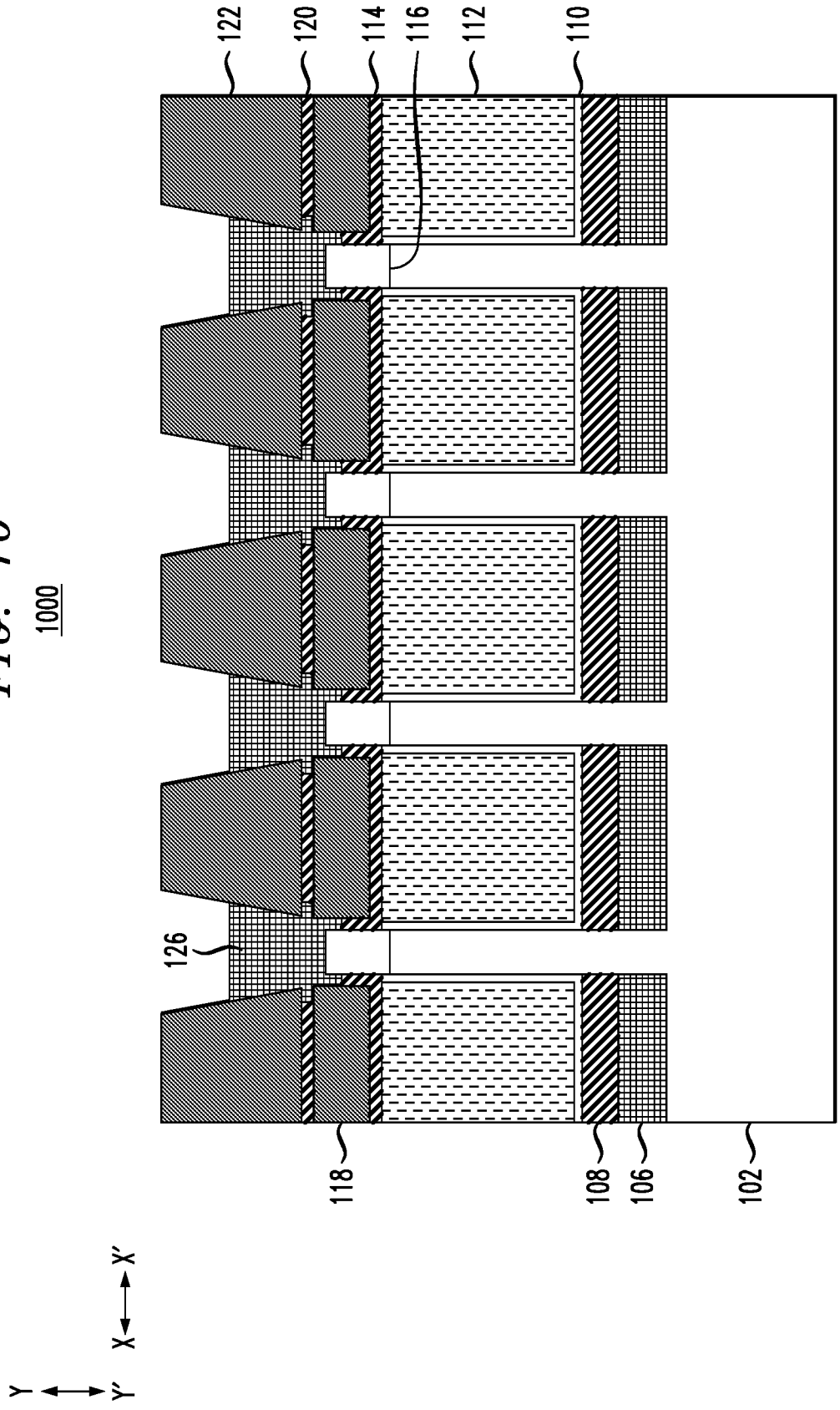


FIG. 11

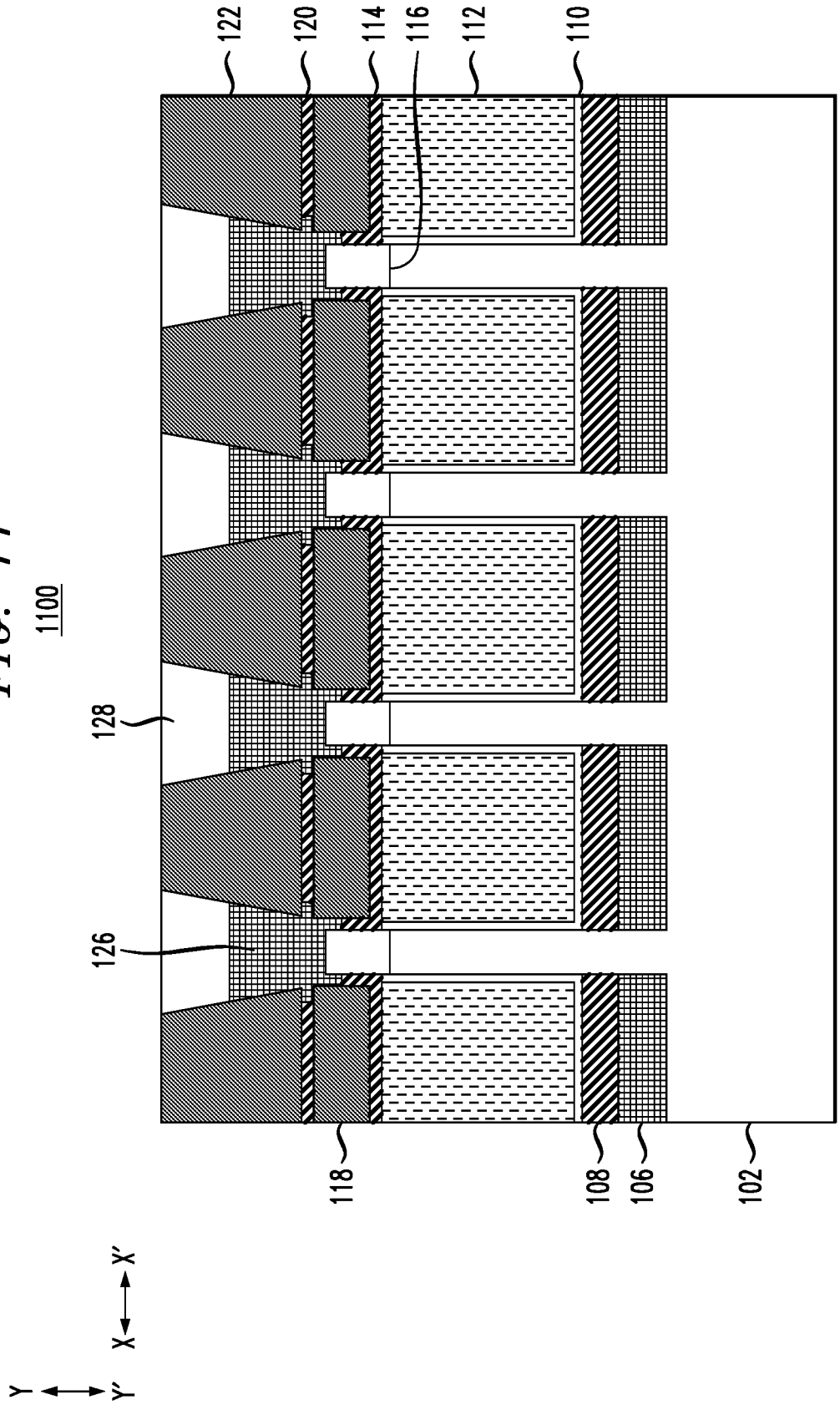


FIG. 12

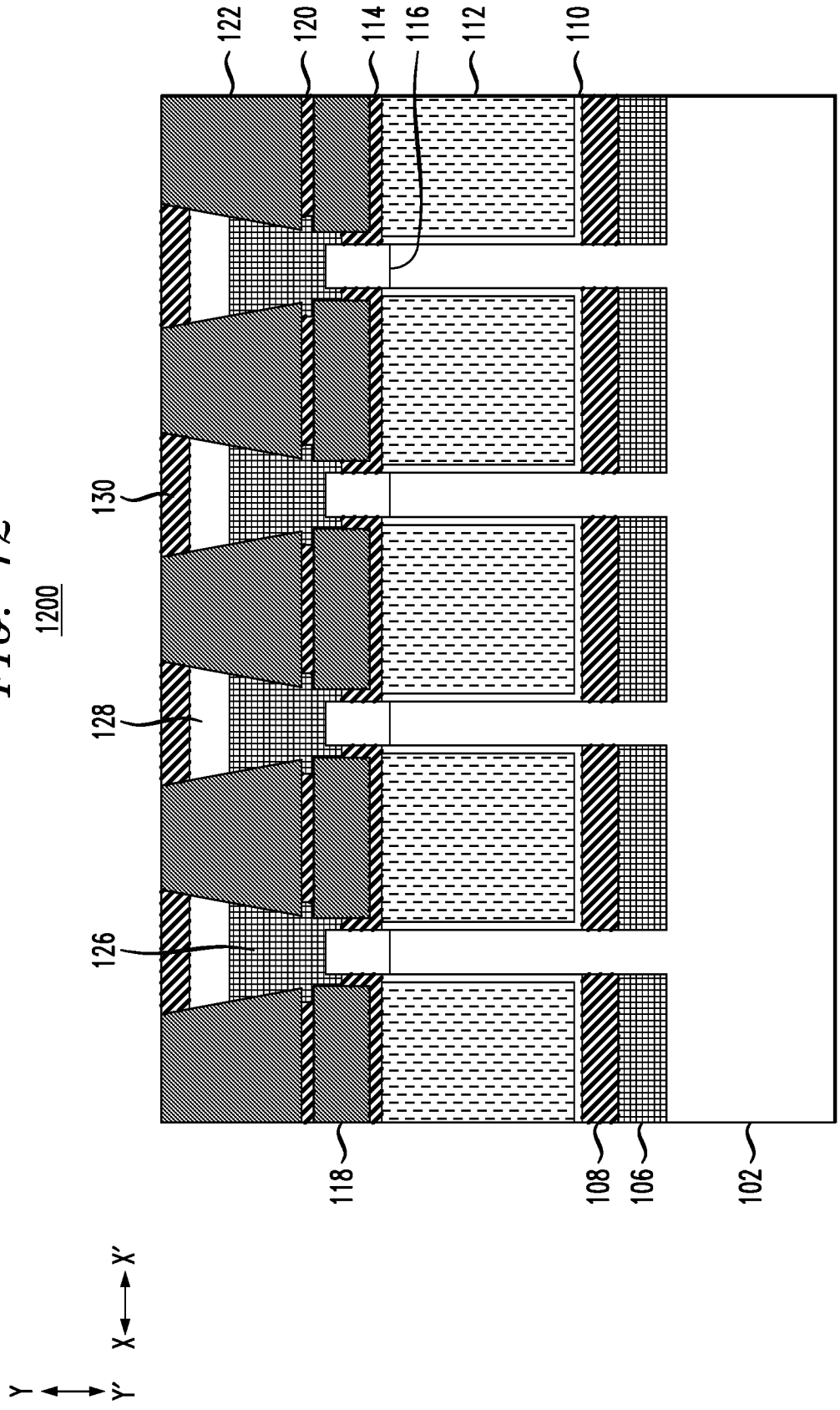


FIG. 13

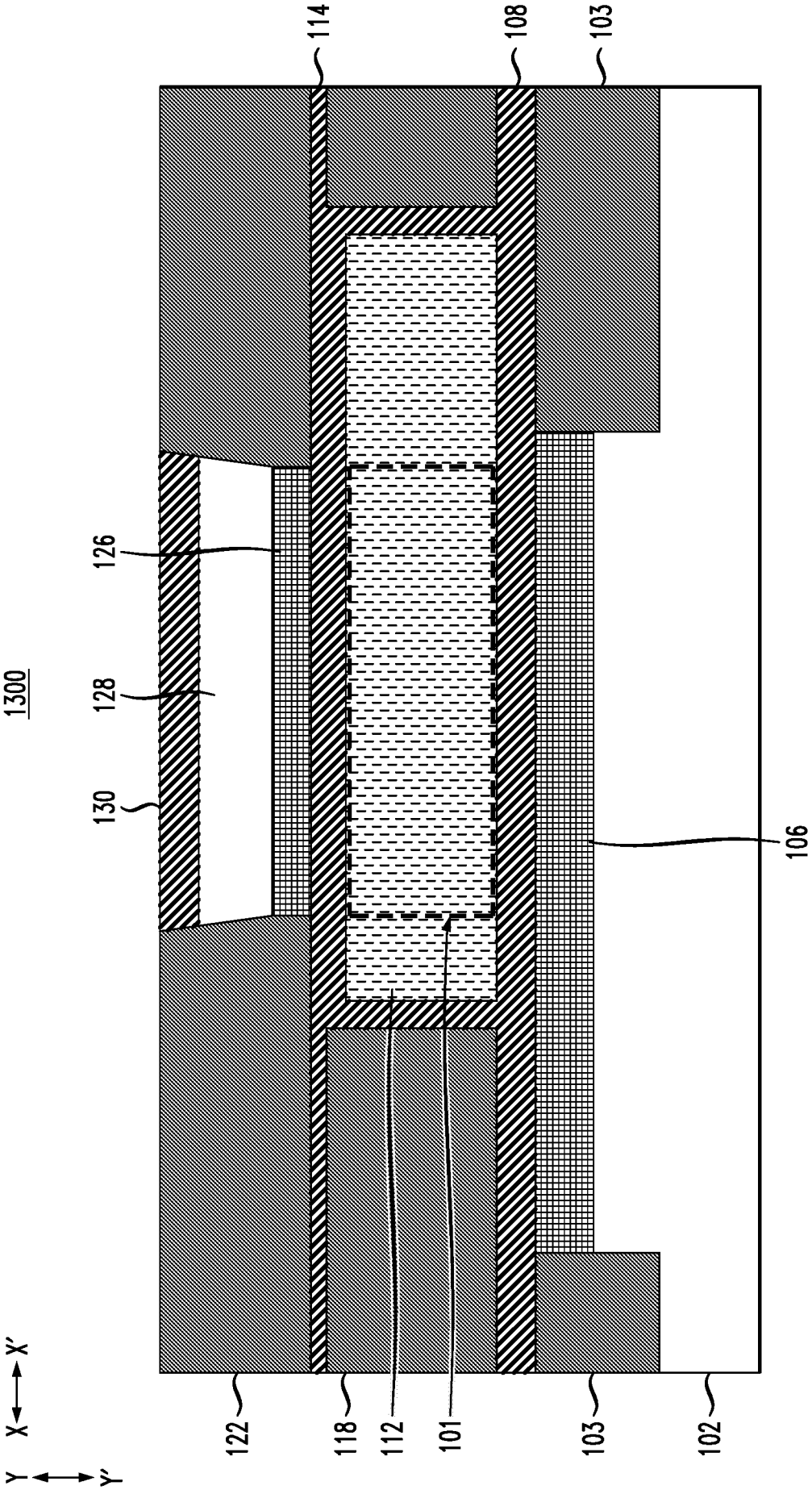
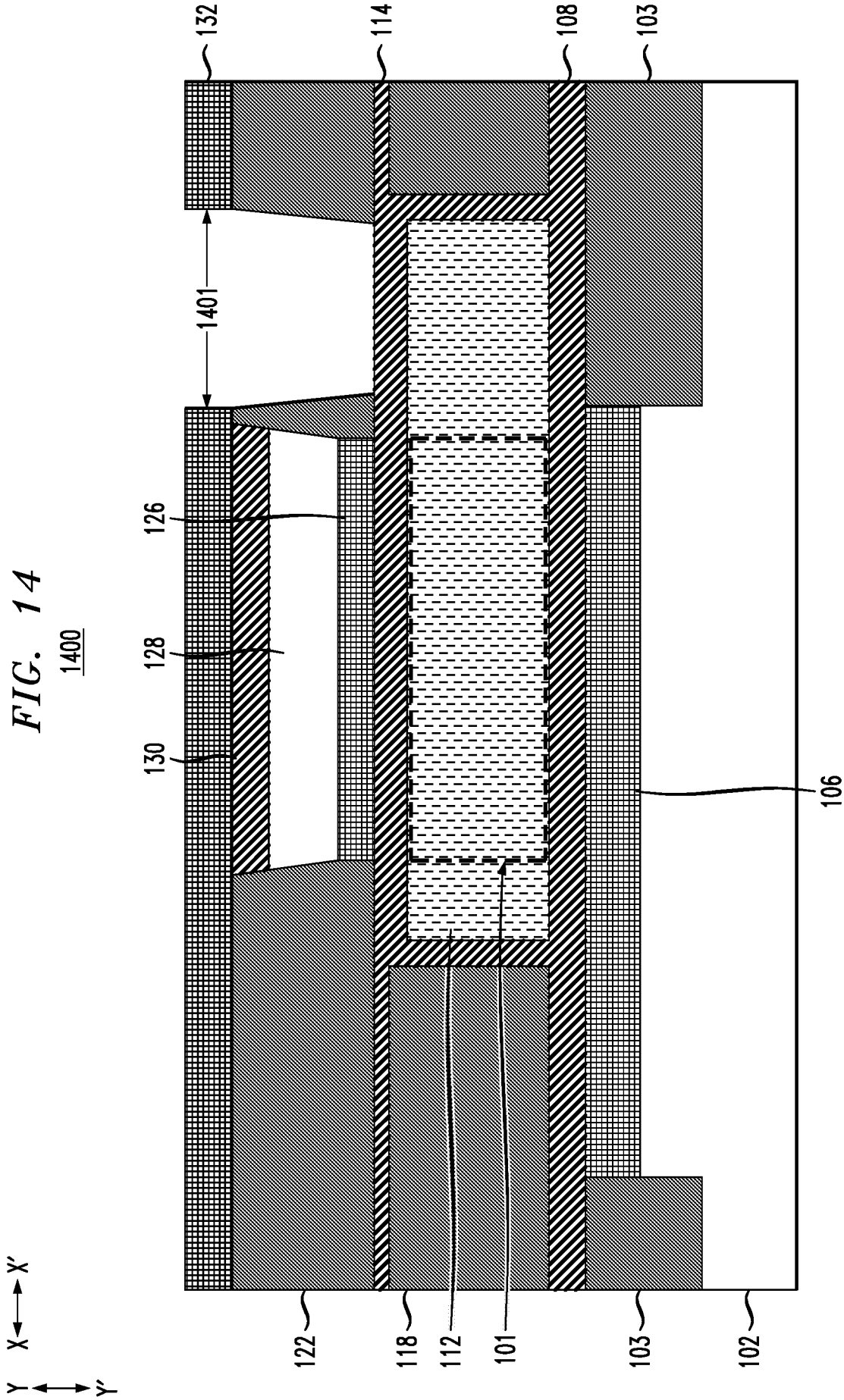


FIG. 14

1400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118
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X
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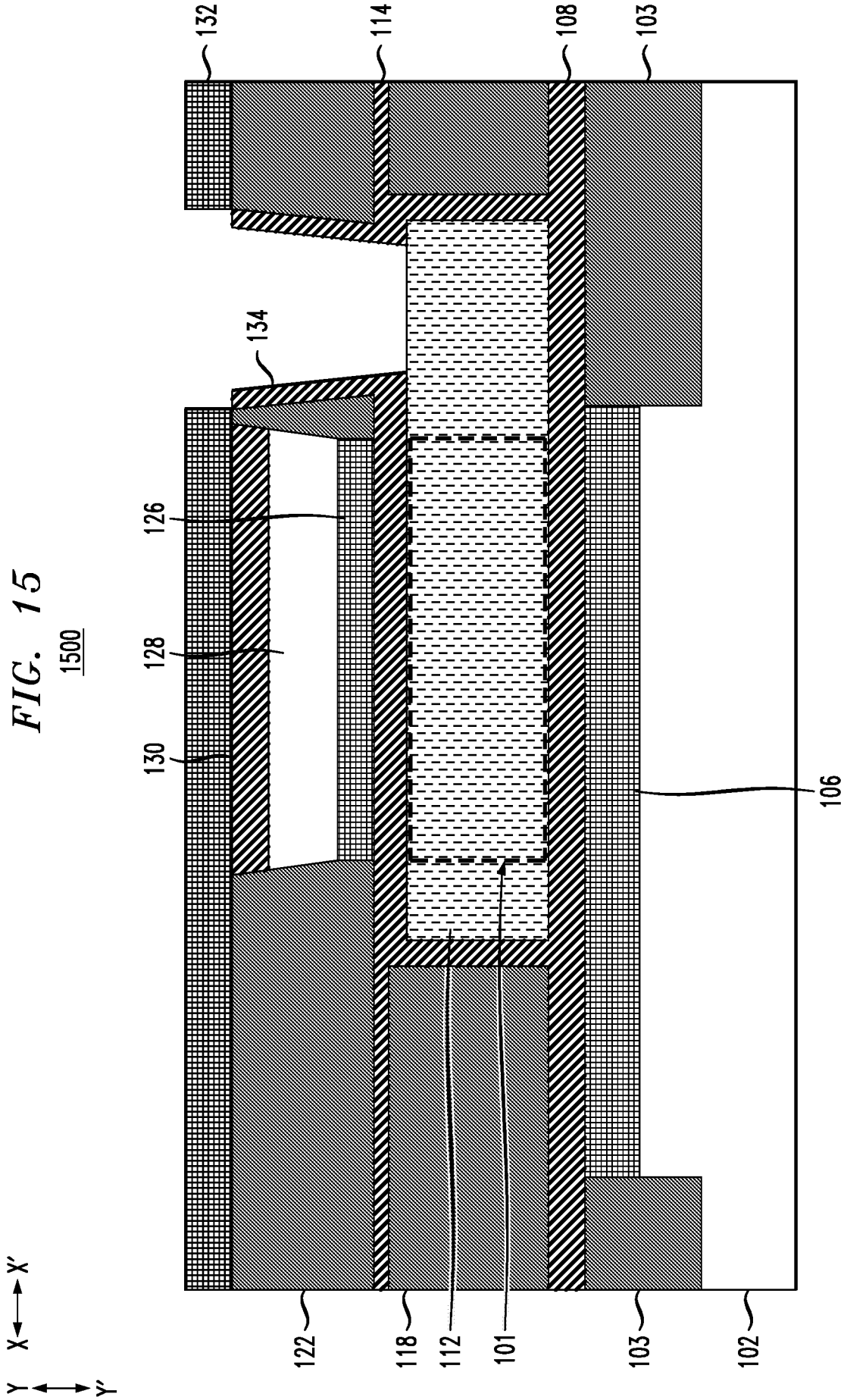
FIG. 15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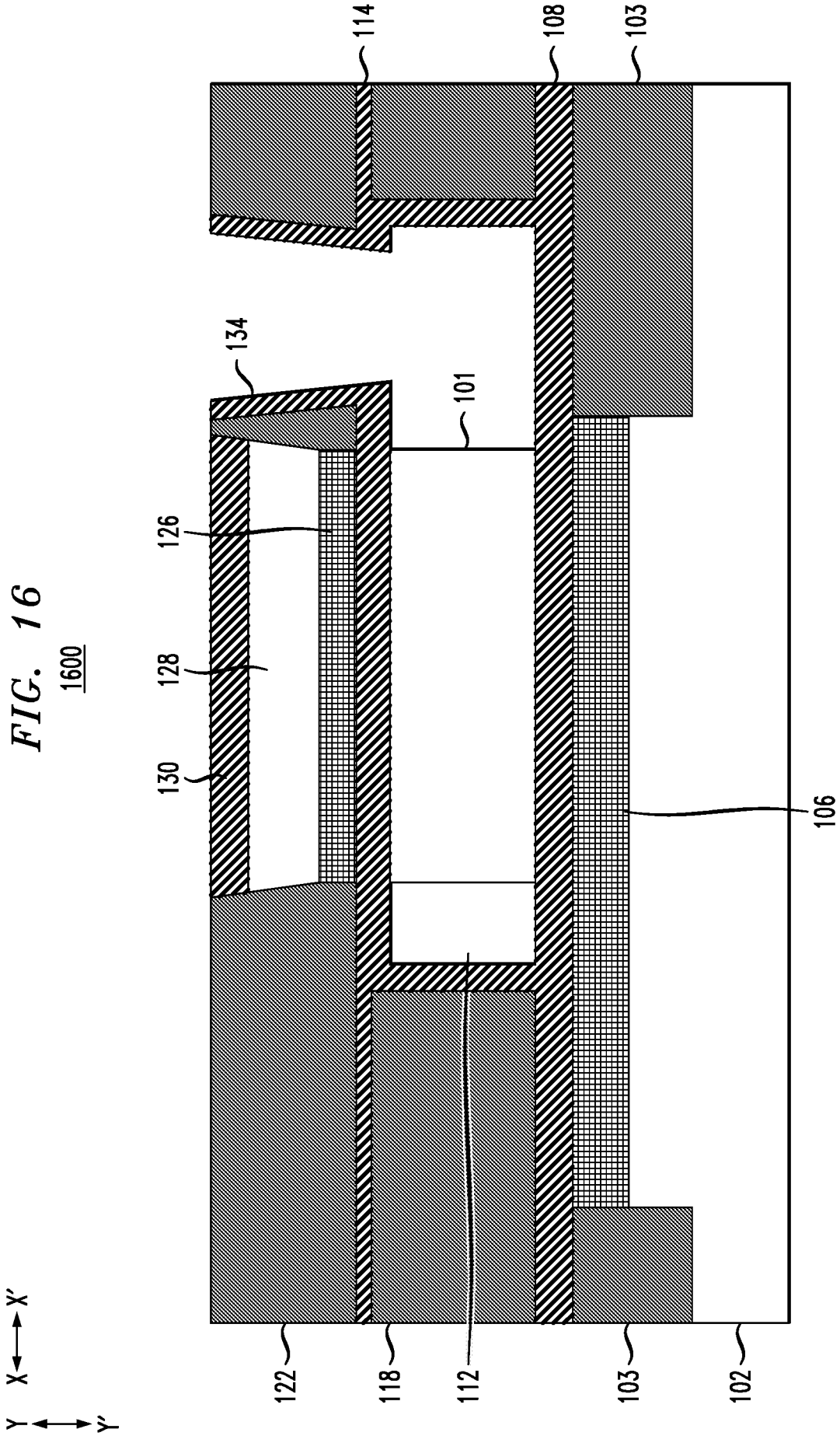
Y'

FIG. 16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Y
Y'

FIG. 17
1700

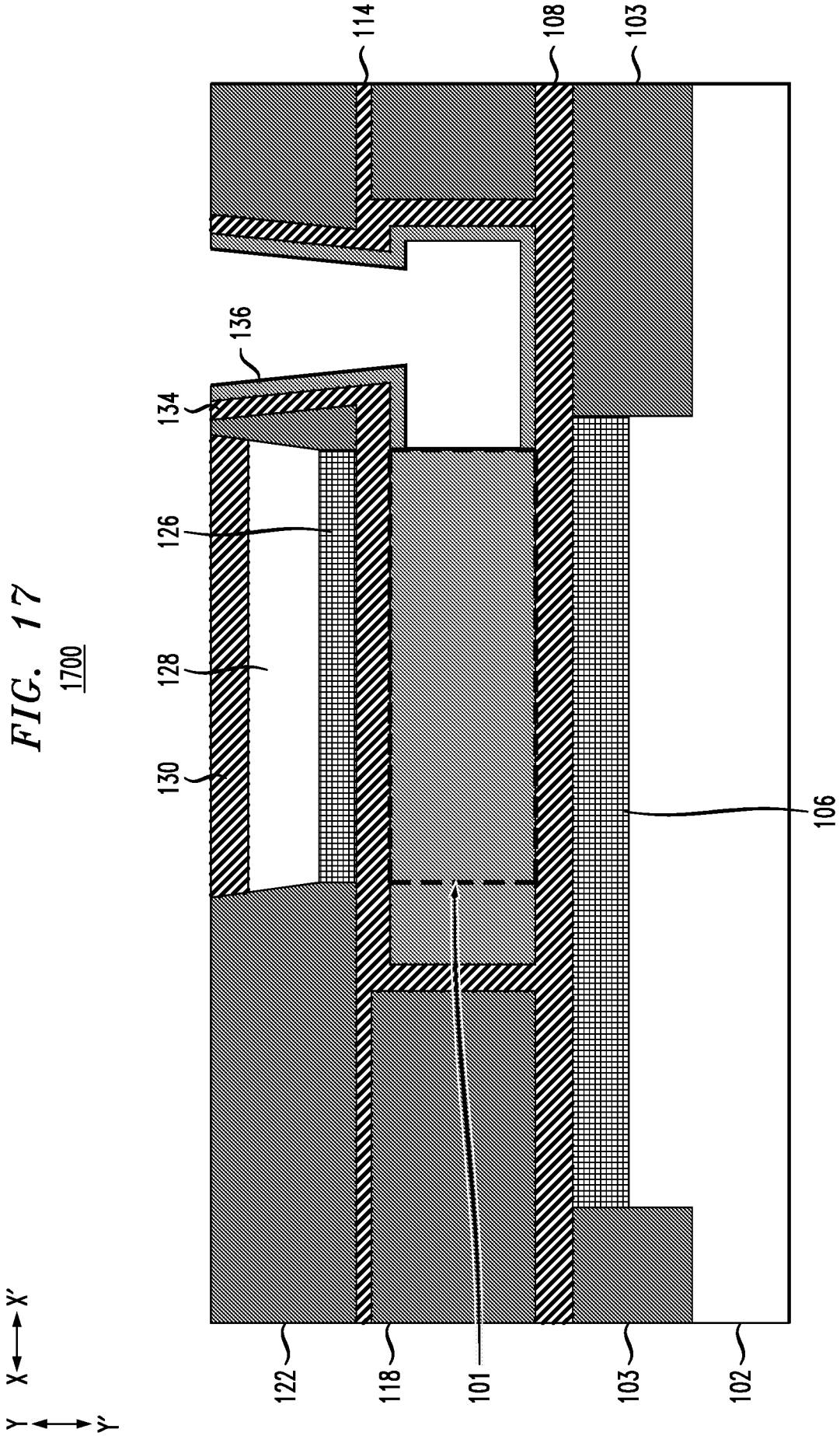

FIG. 18

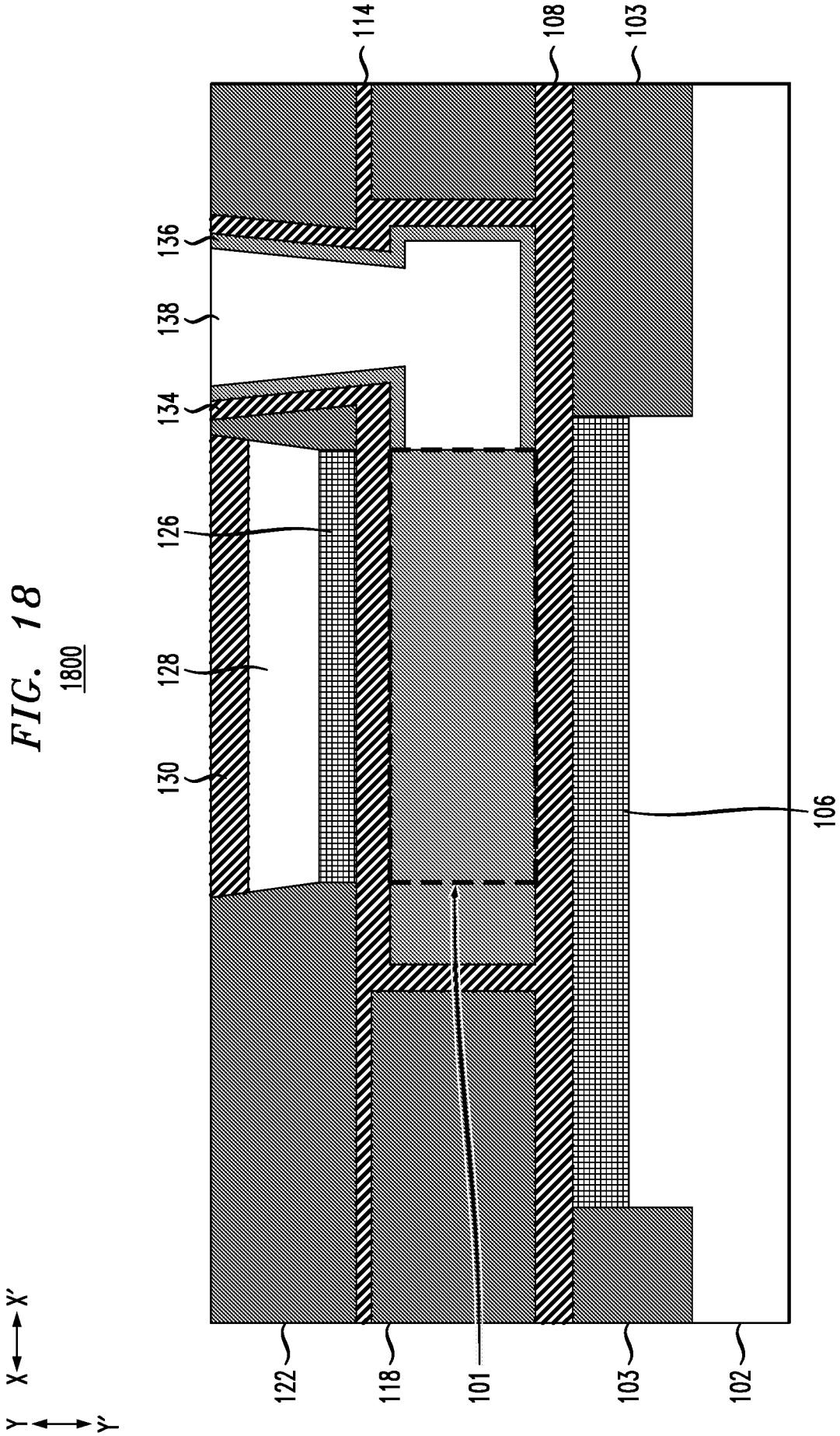
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FIG. 19

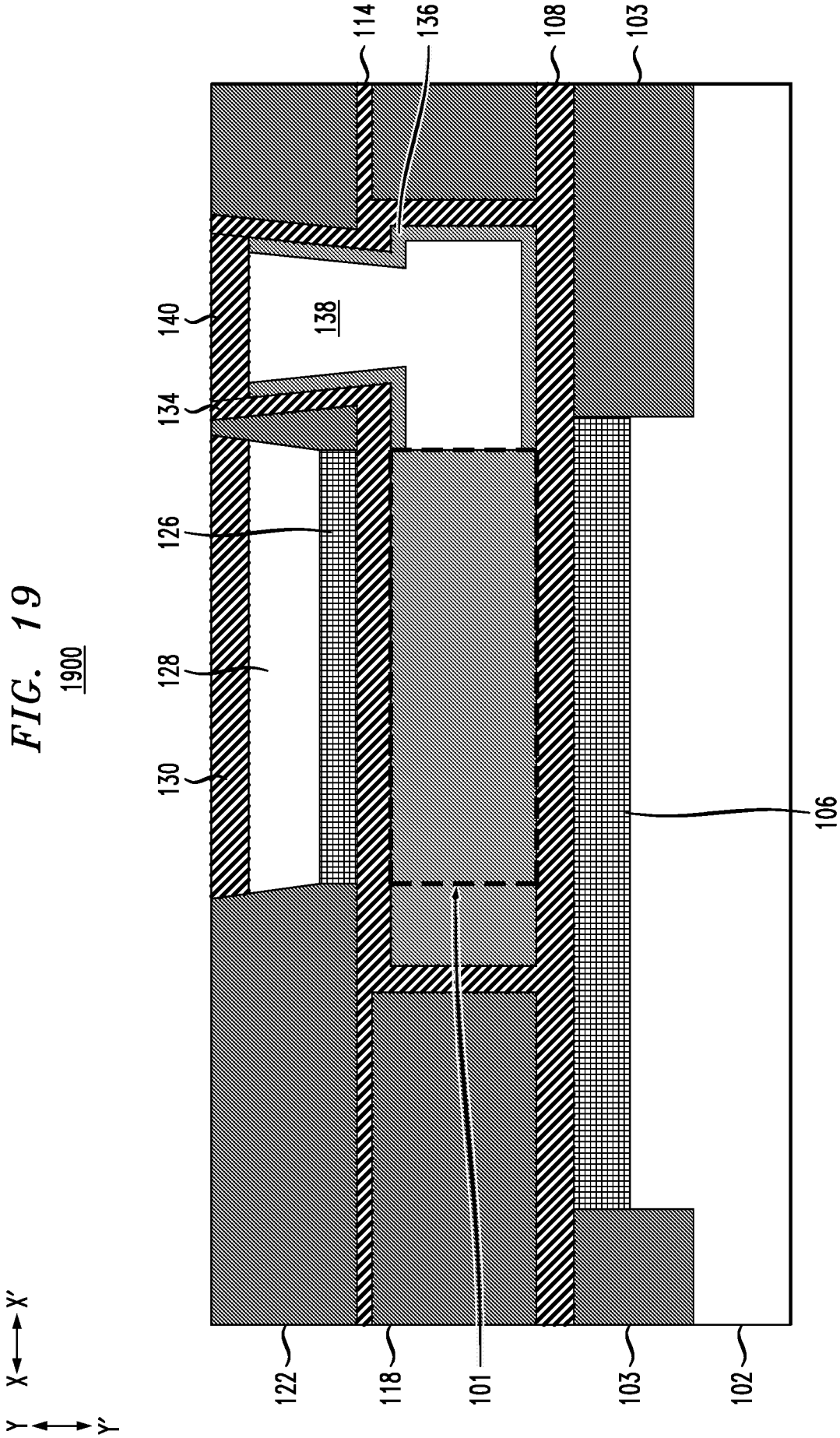
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FIG. 20

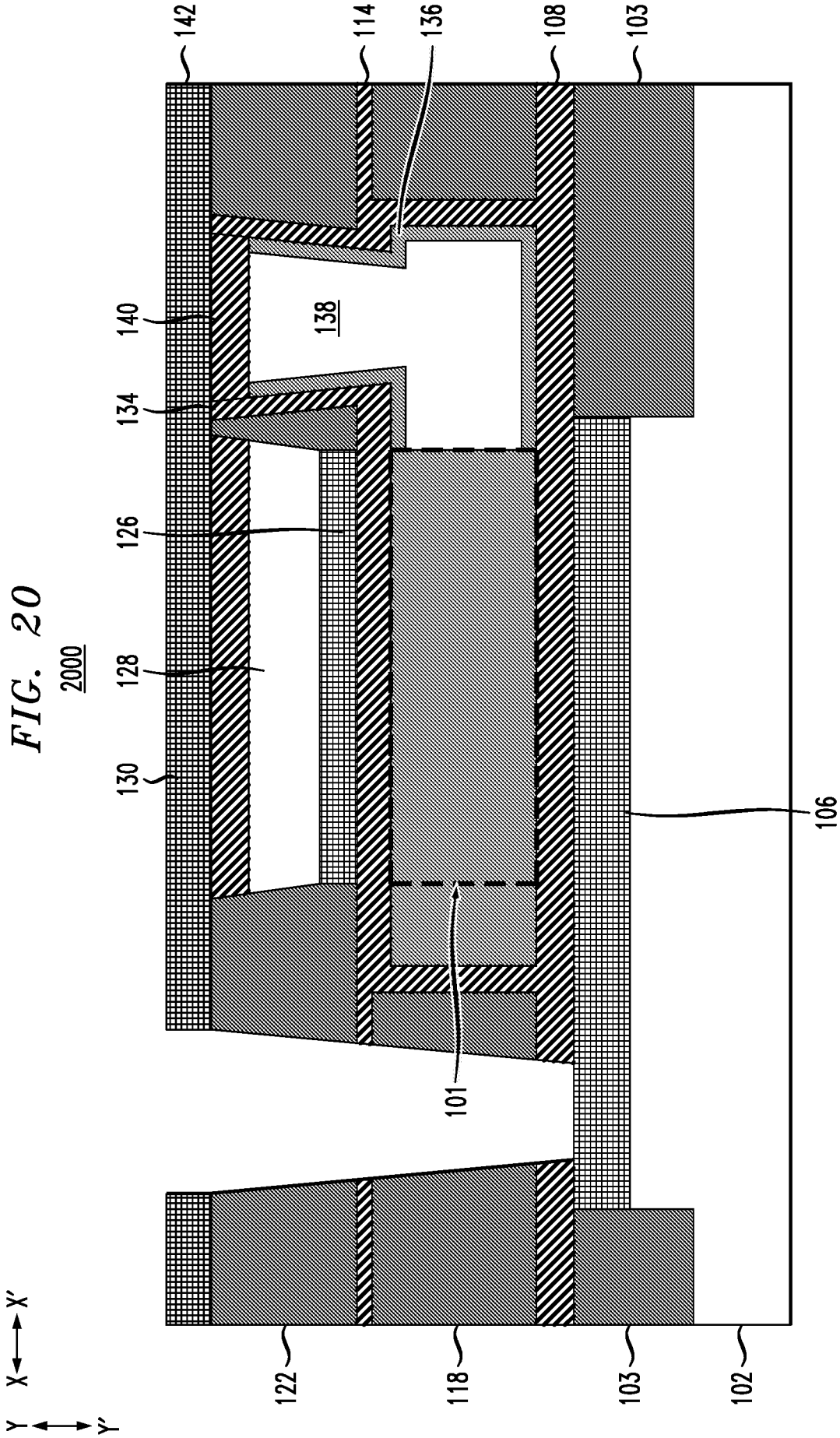
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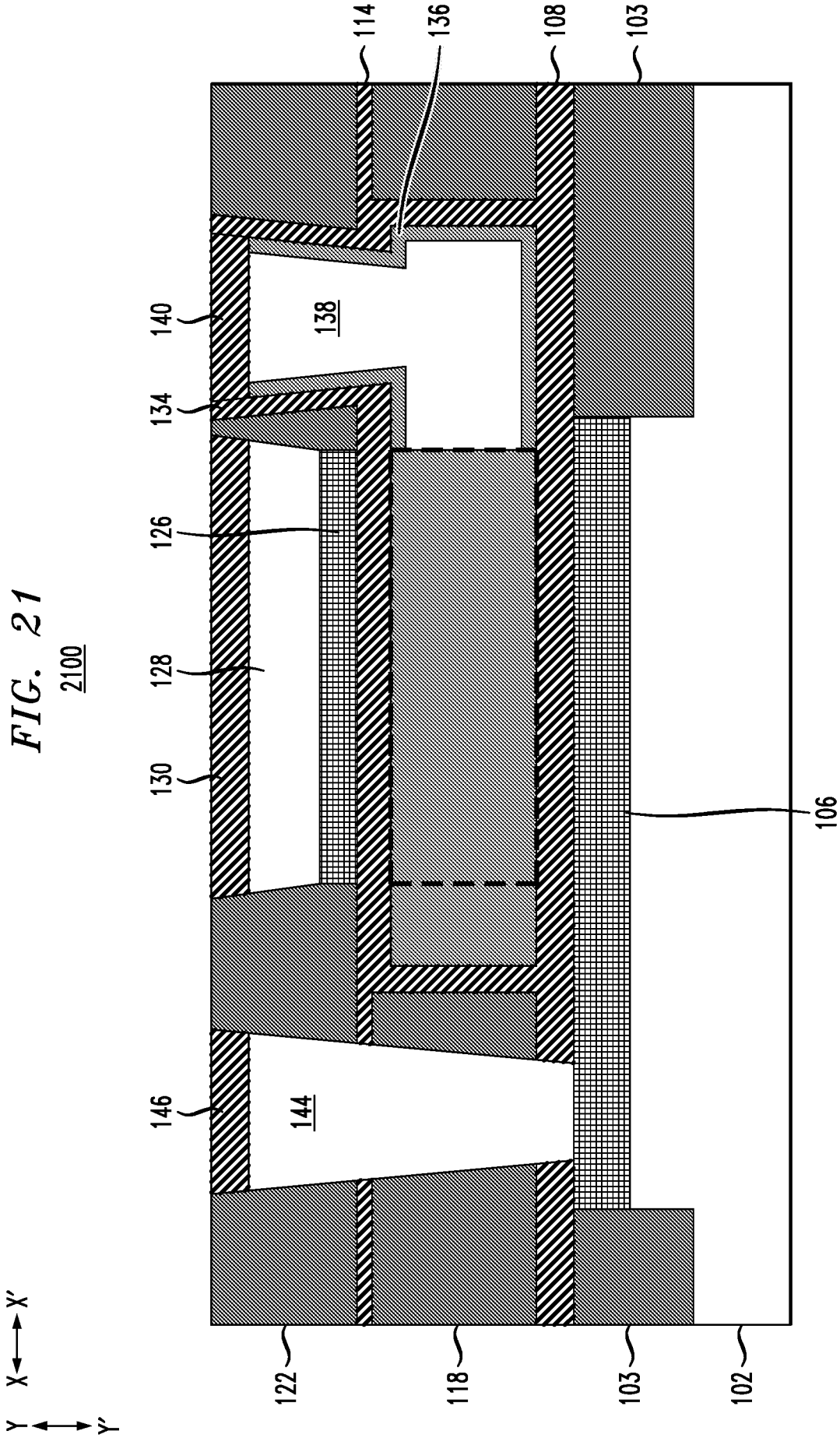
FIG. 21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X
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Y
Y'

FIG. 22

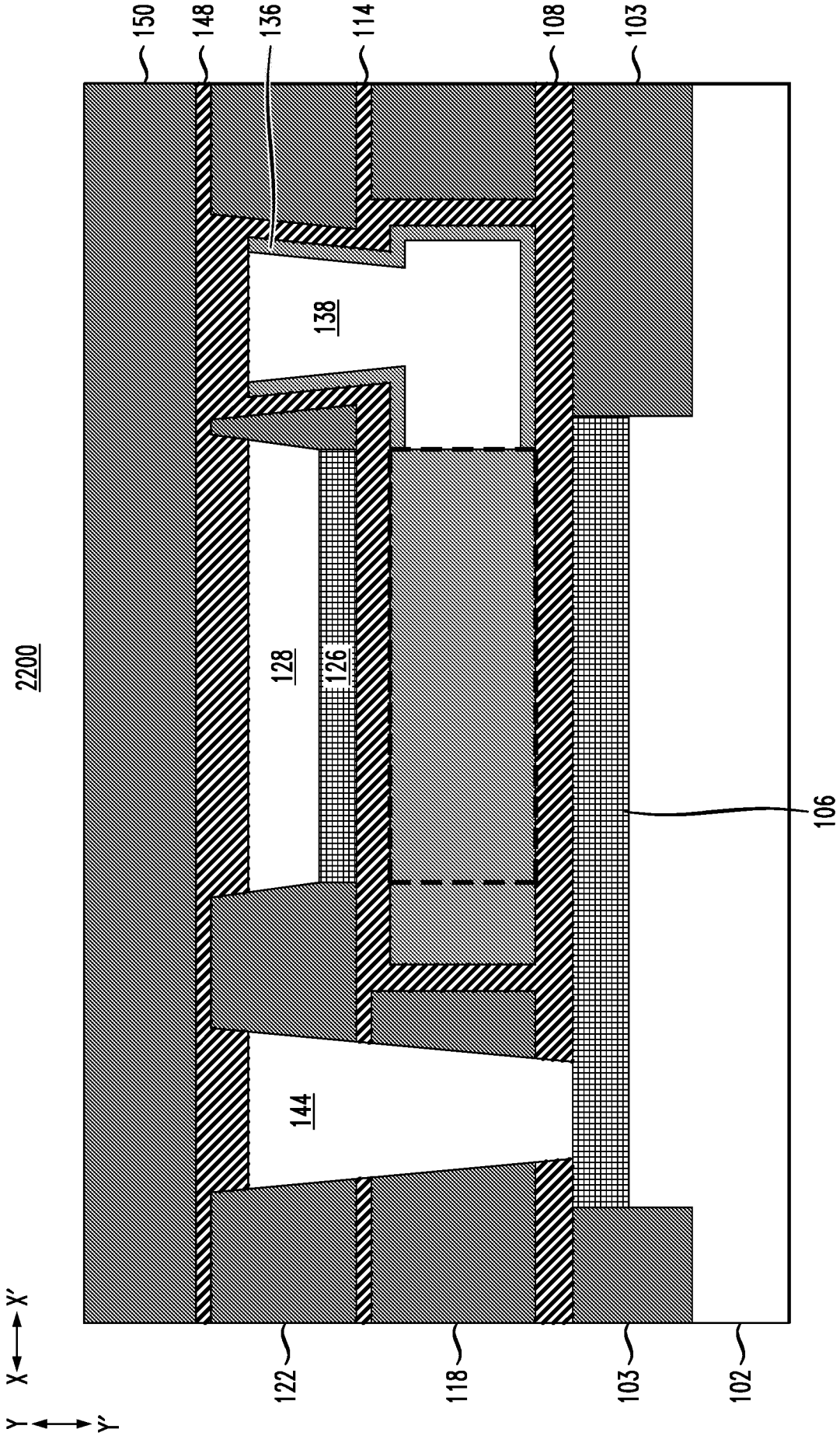
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FIG. 23

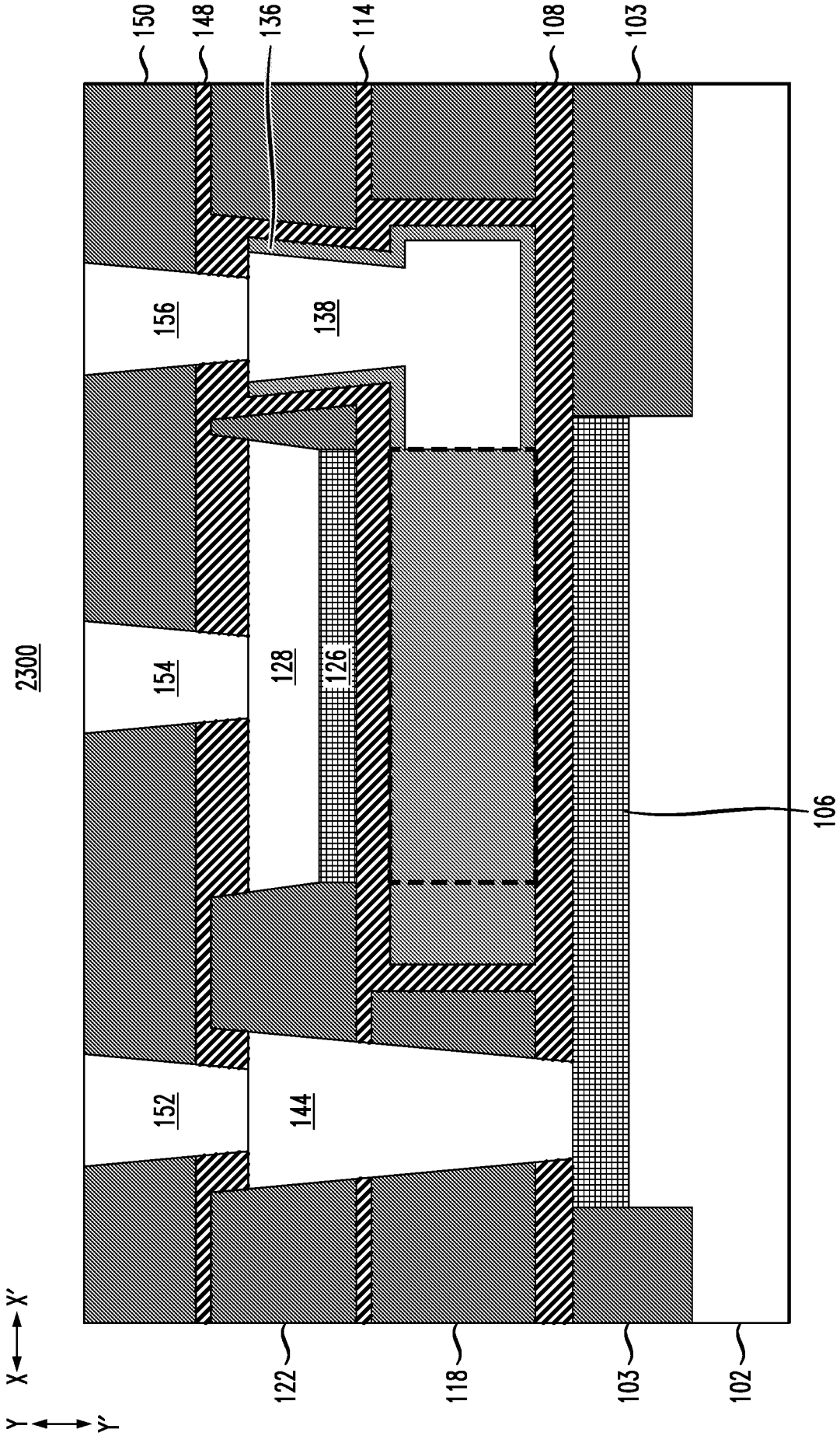
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FIG. 24

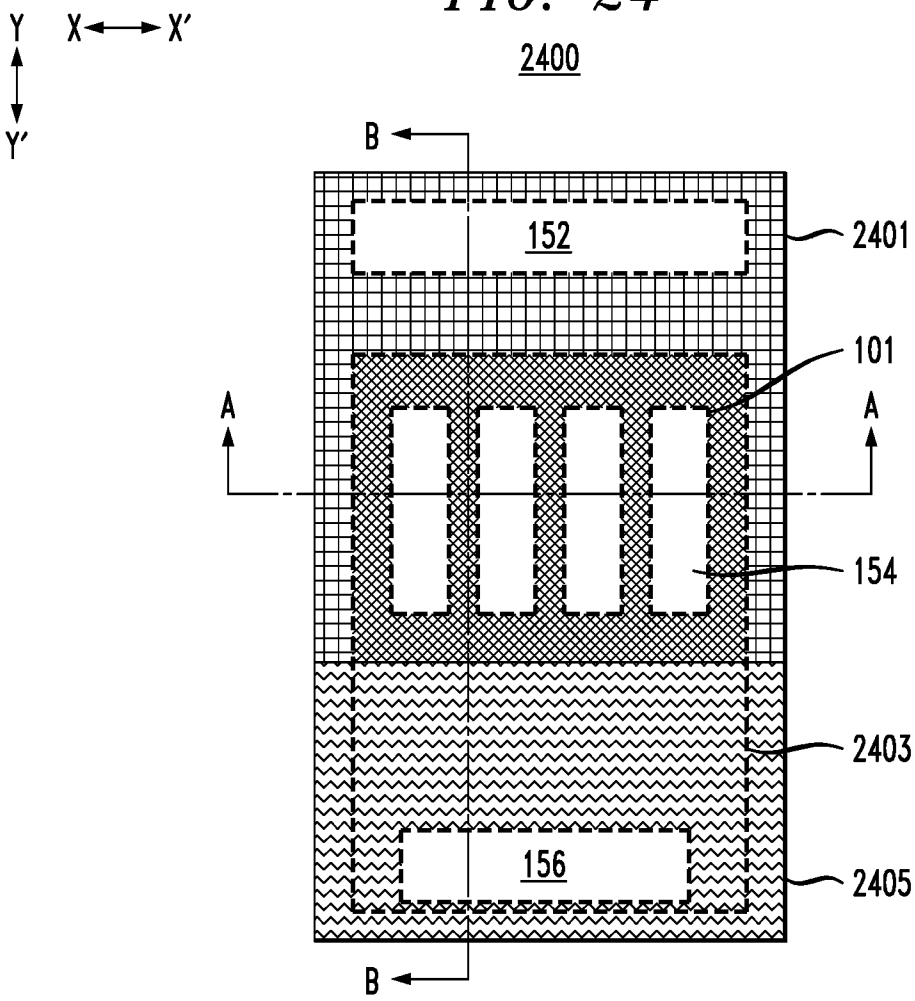


FIG. 25

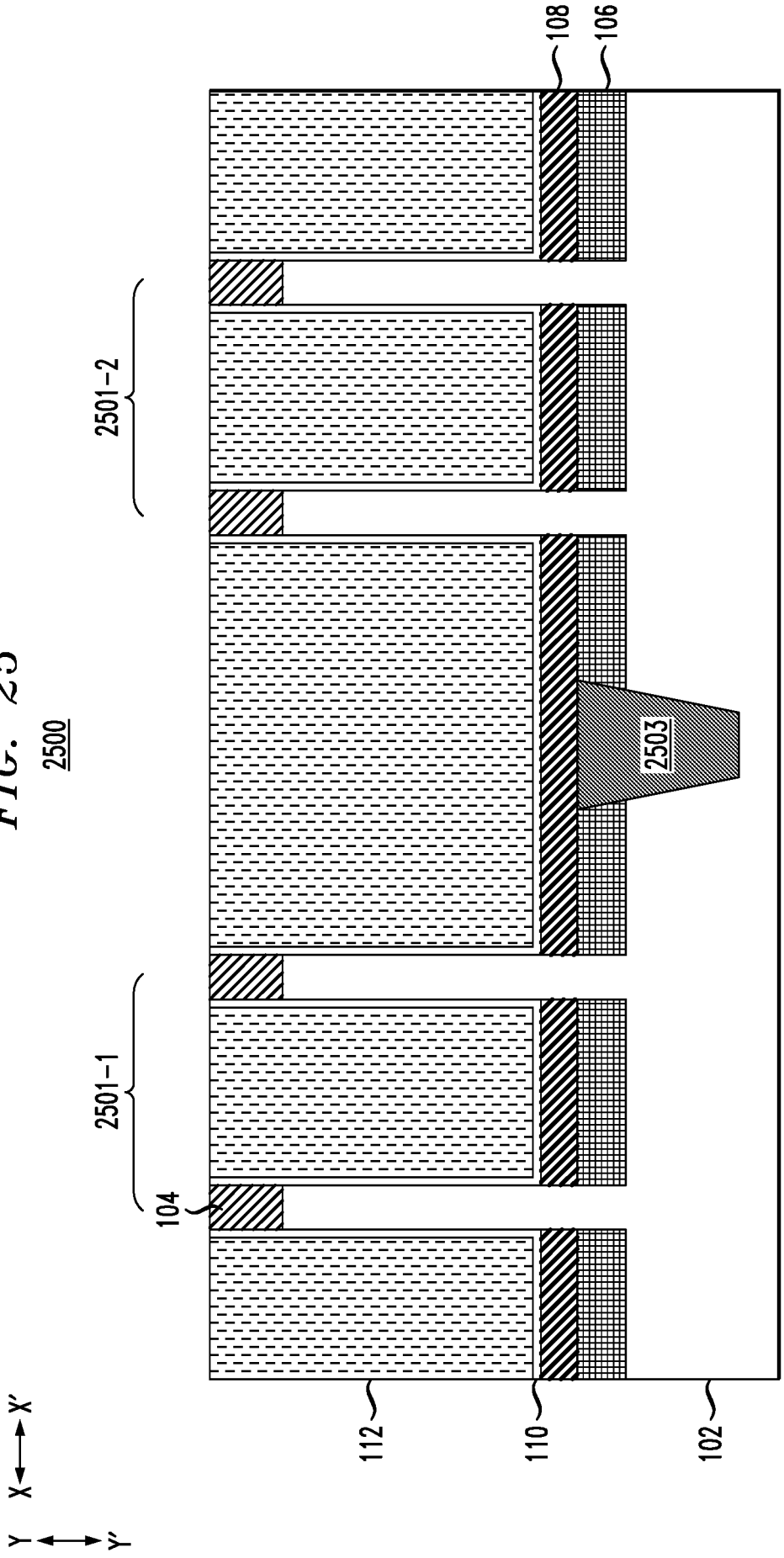


FIG. 26

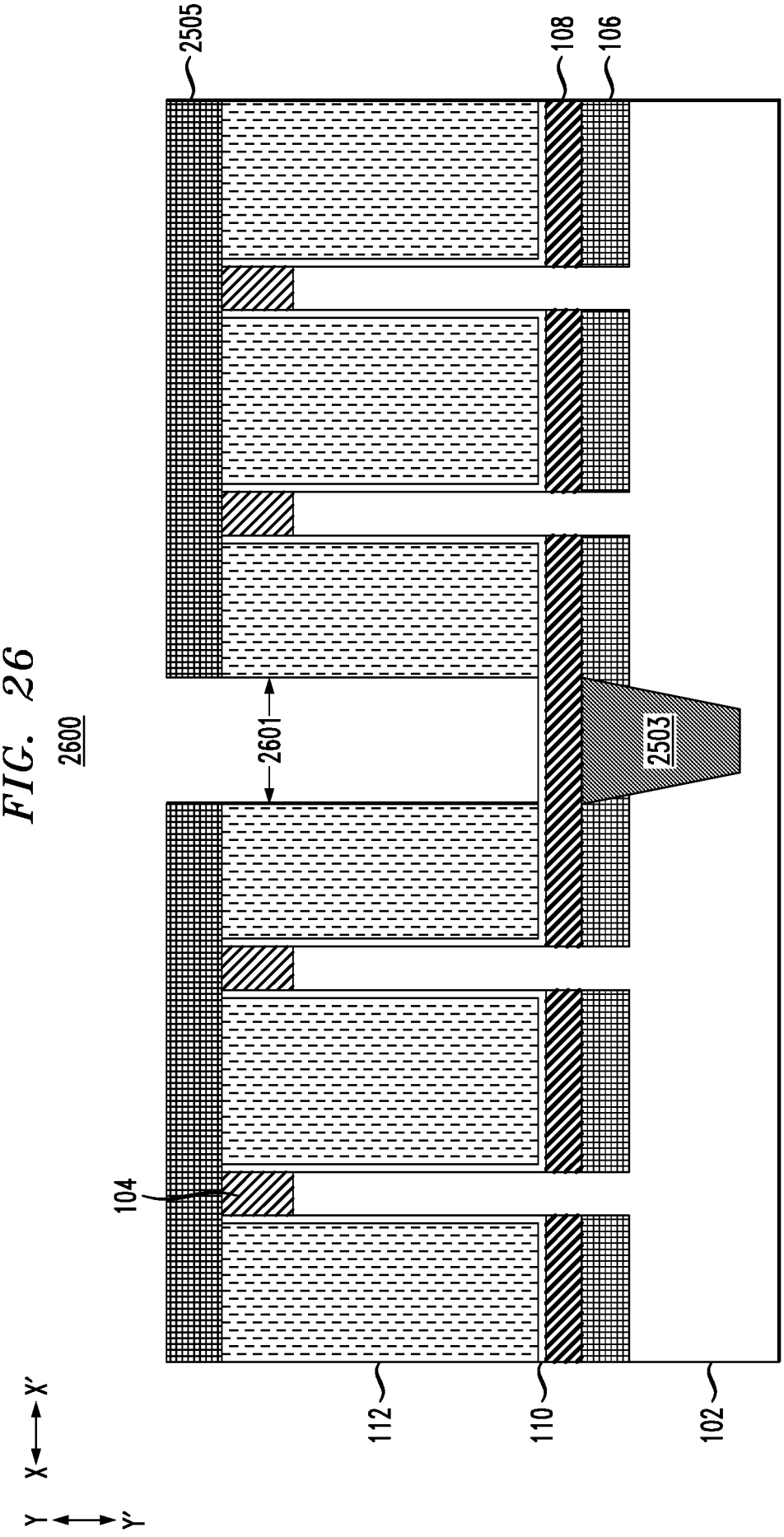


FIG. 27

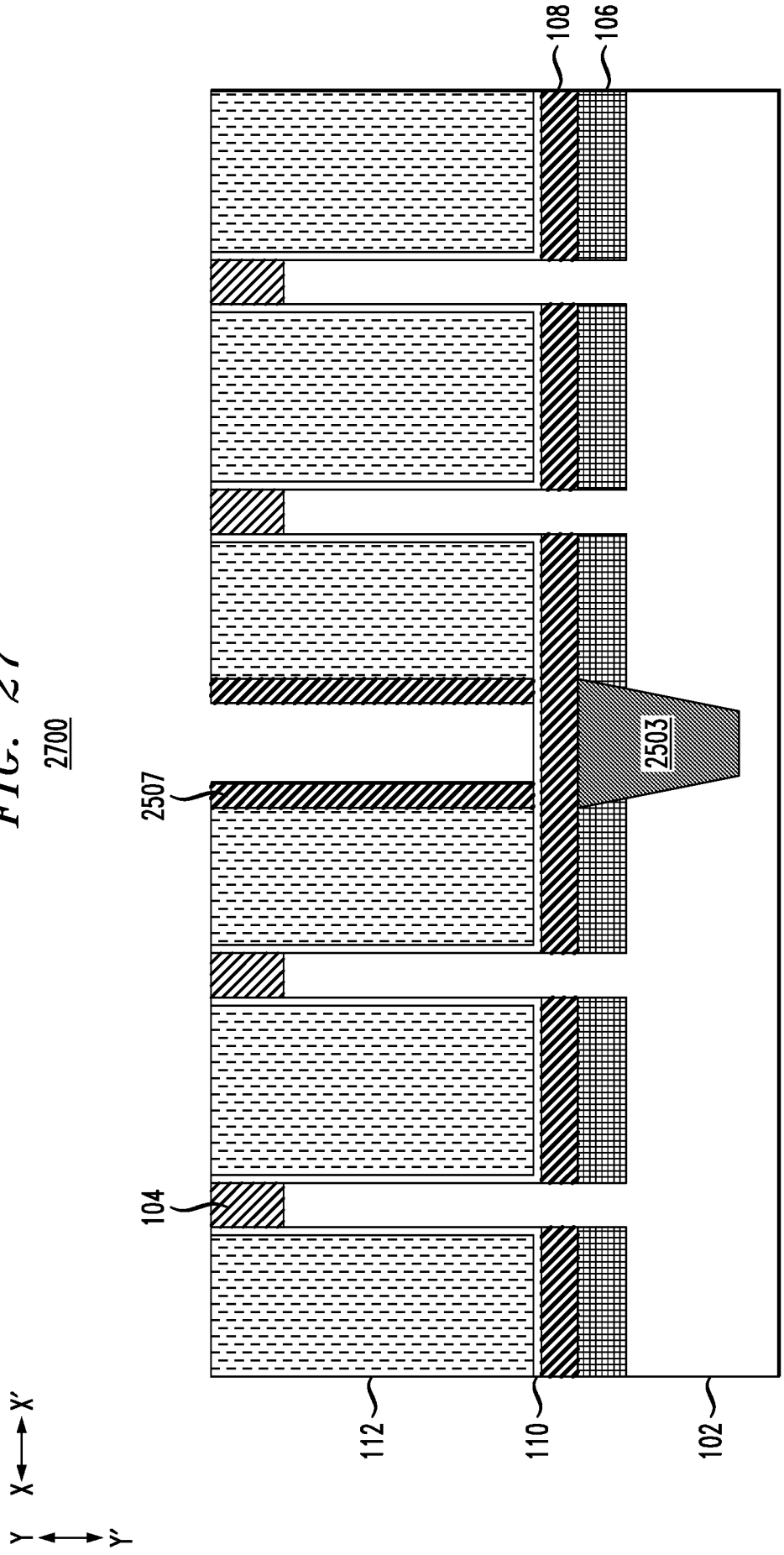


FIG. 28

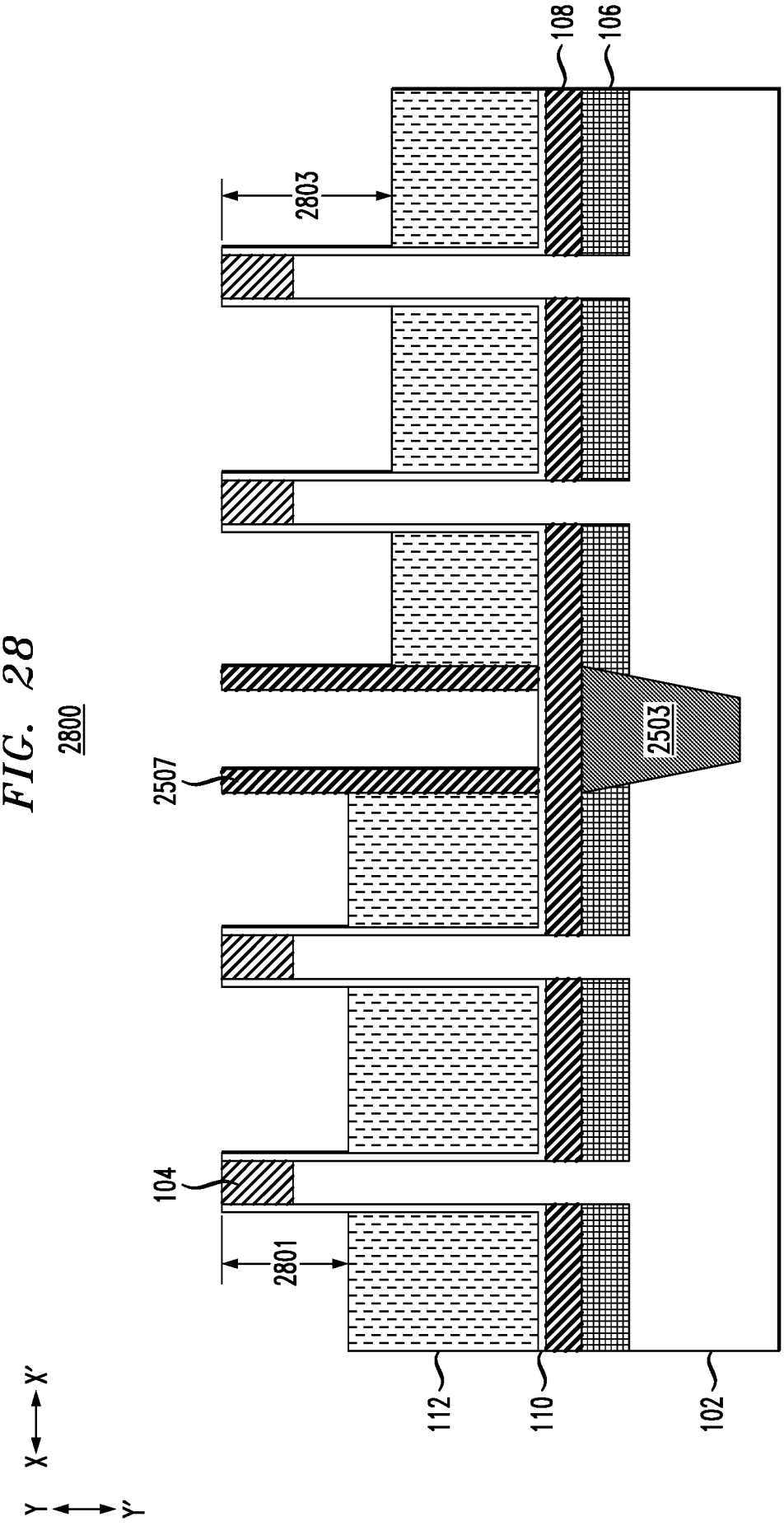


FIG. 29

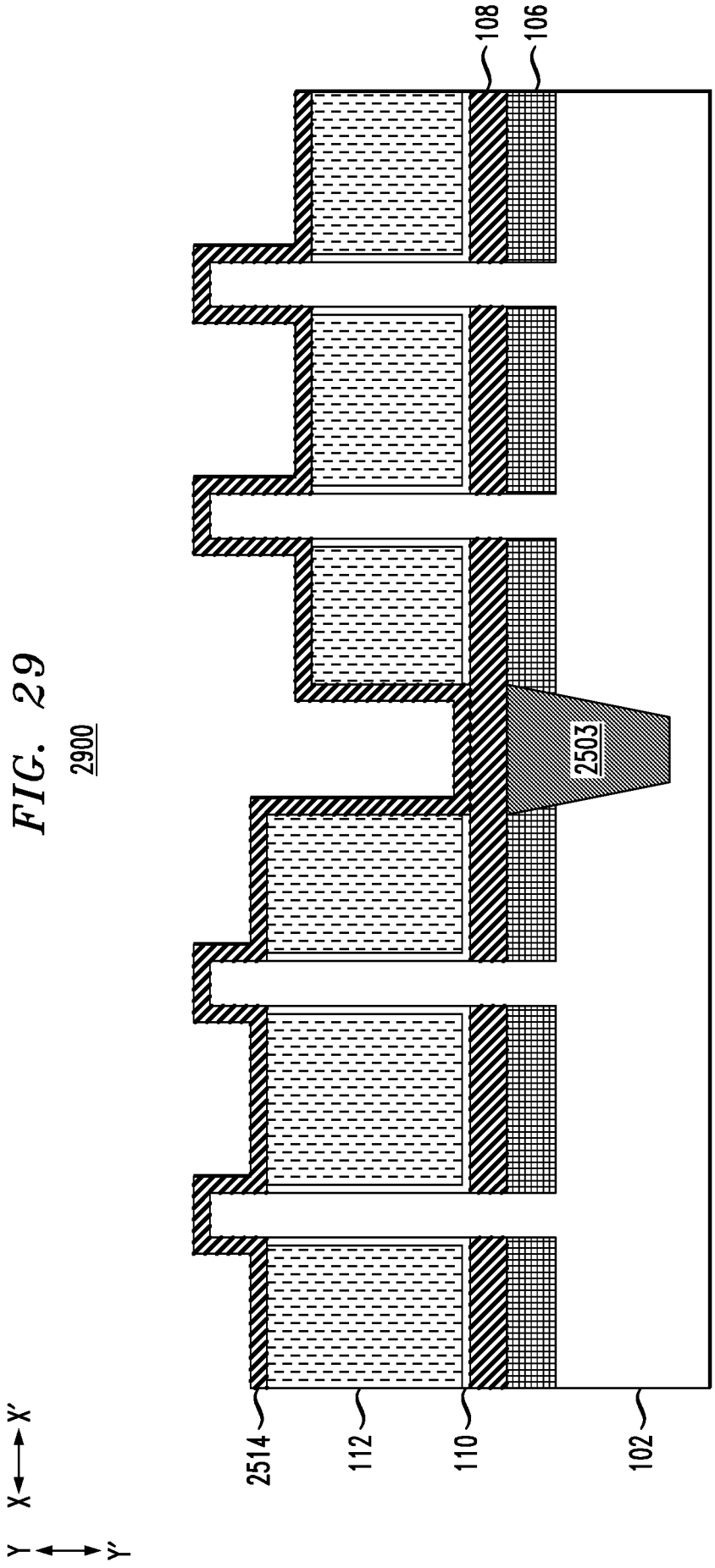


FIG. 30

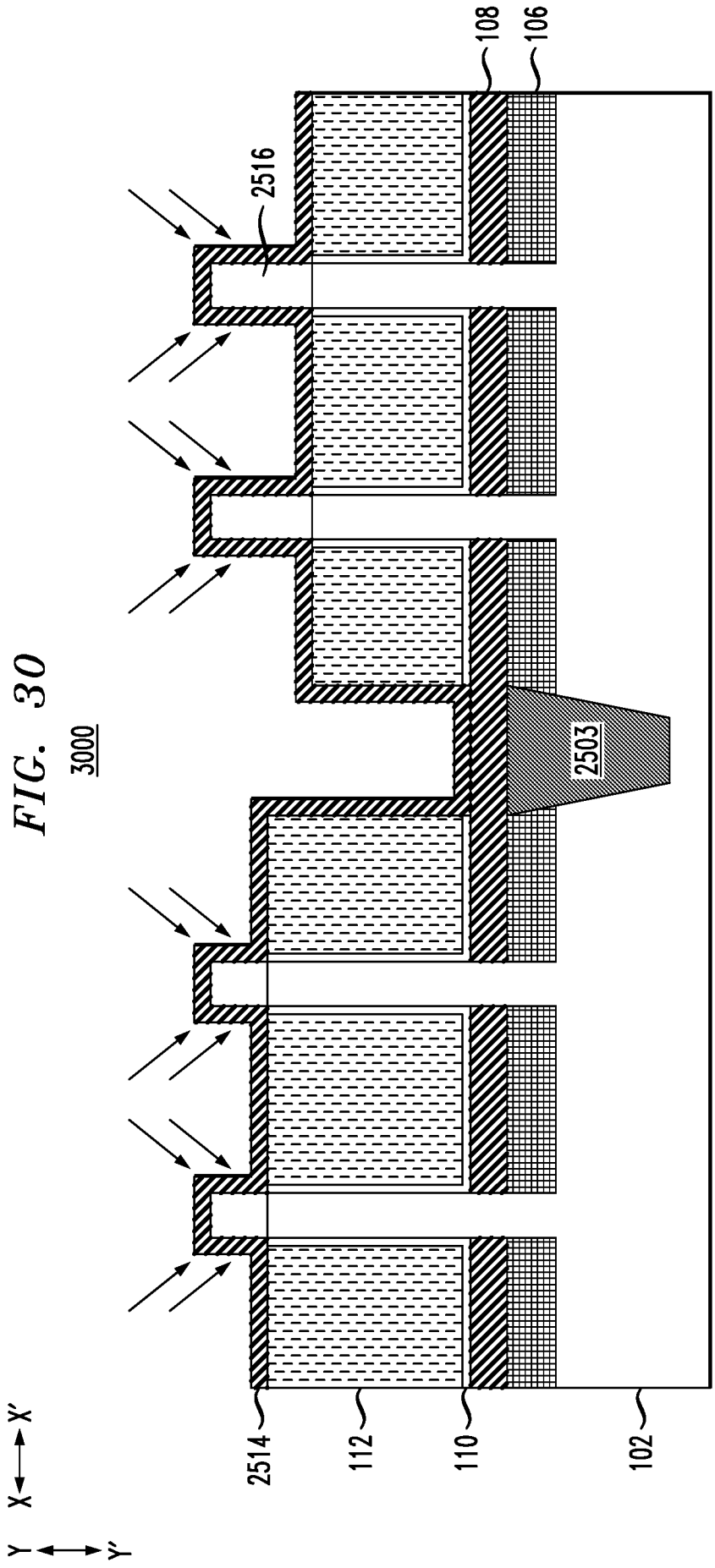


FIG. 31

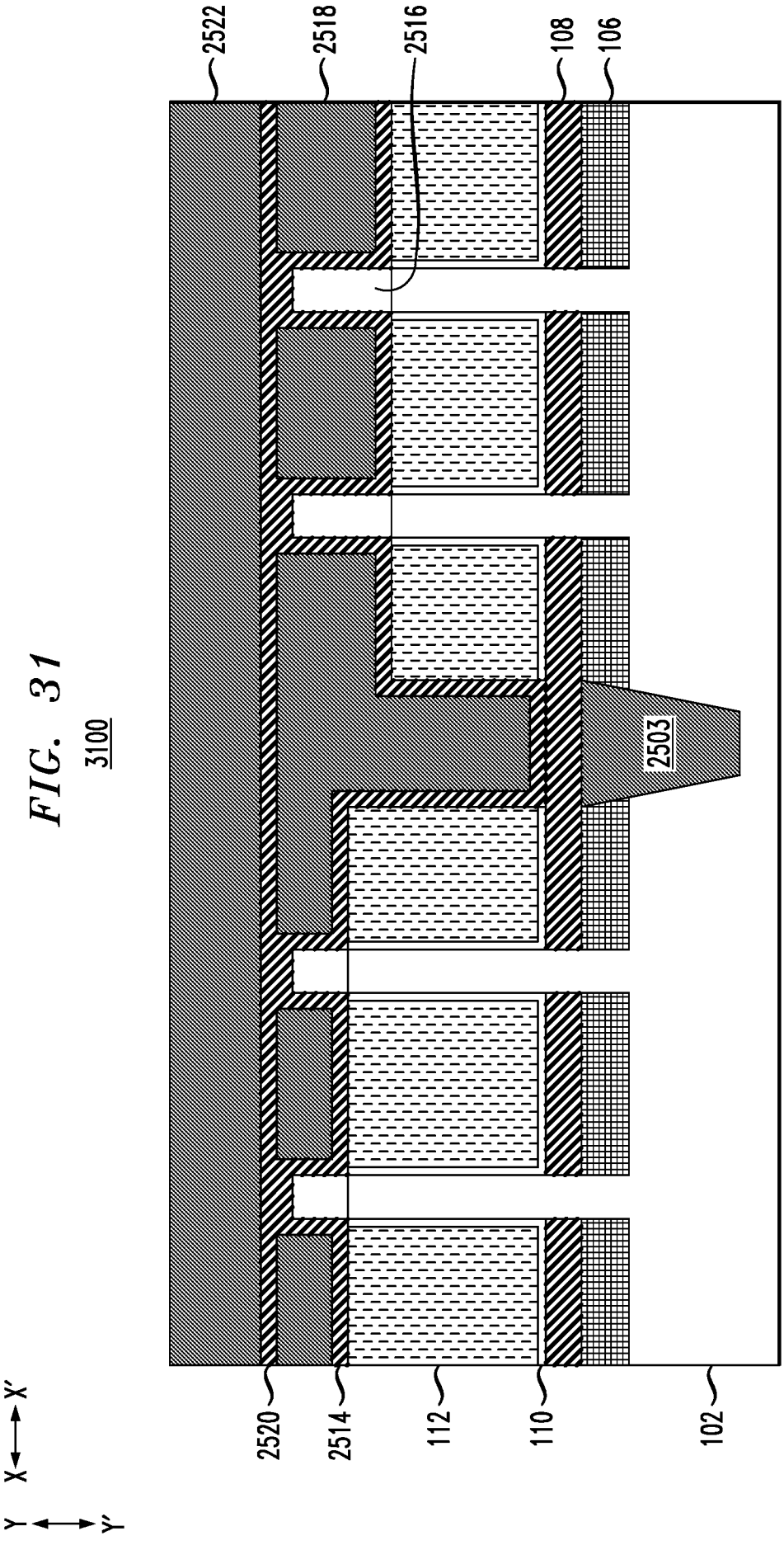
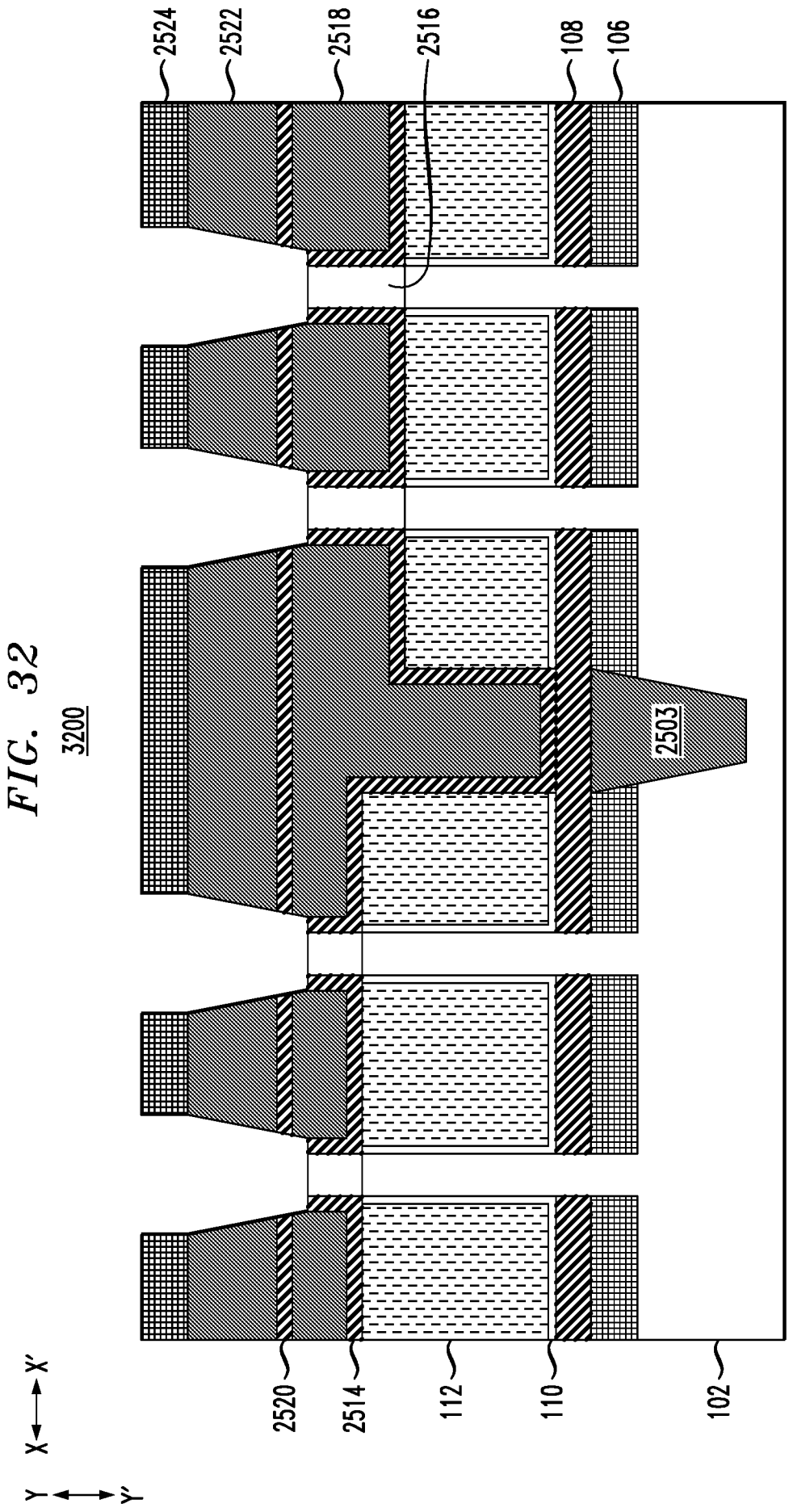


FIG. 32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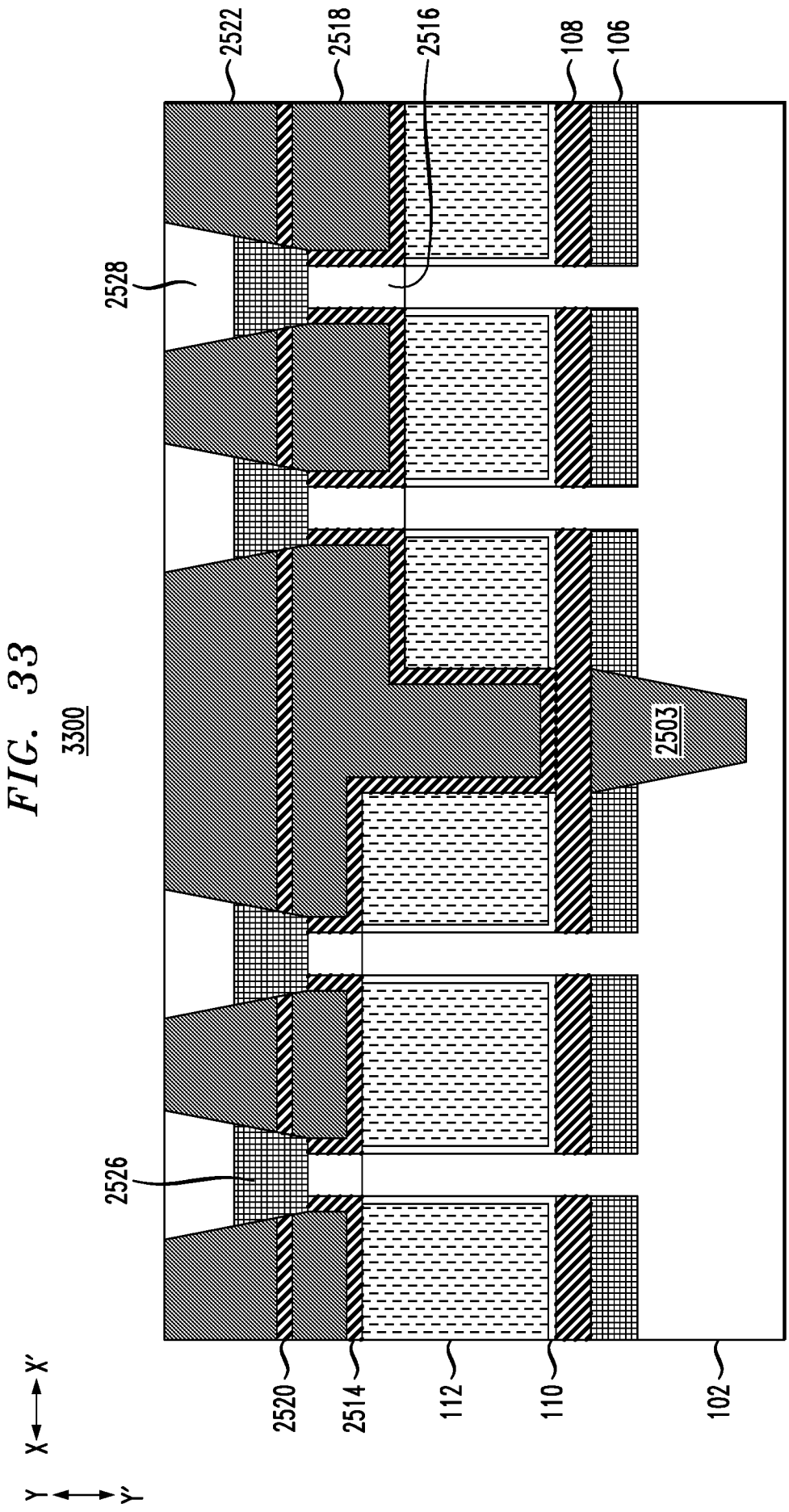
2514
112
110
102
X
X'
Y
Y'

FIG. 33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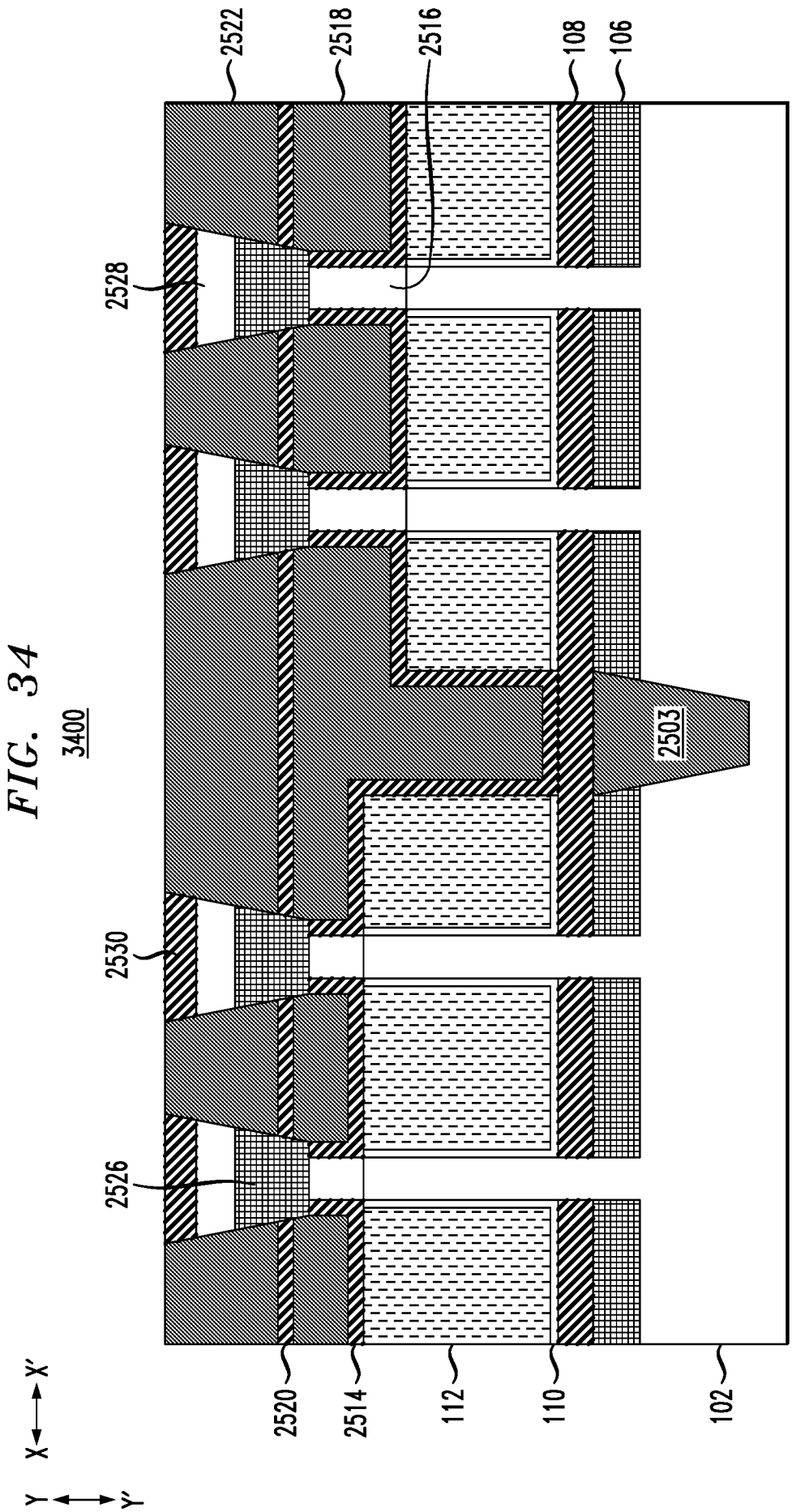
Y
Y'

FIG. 34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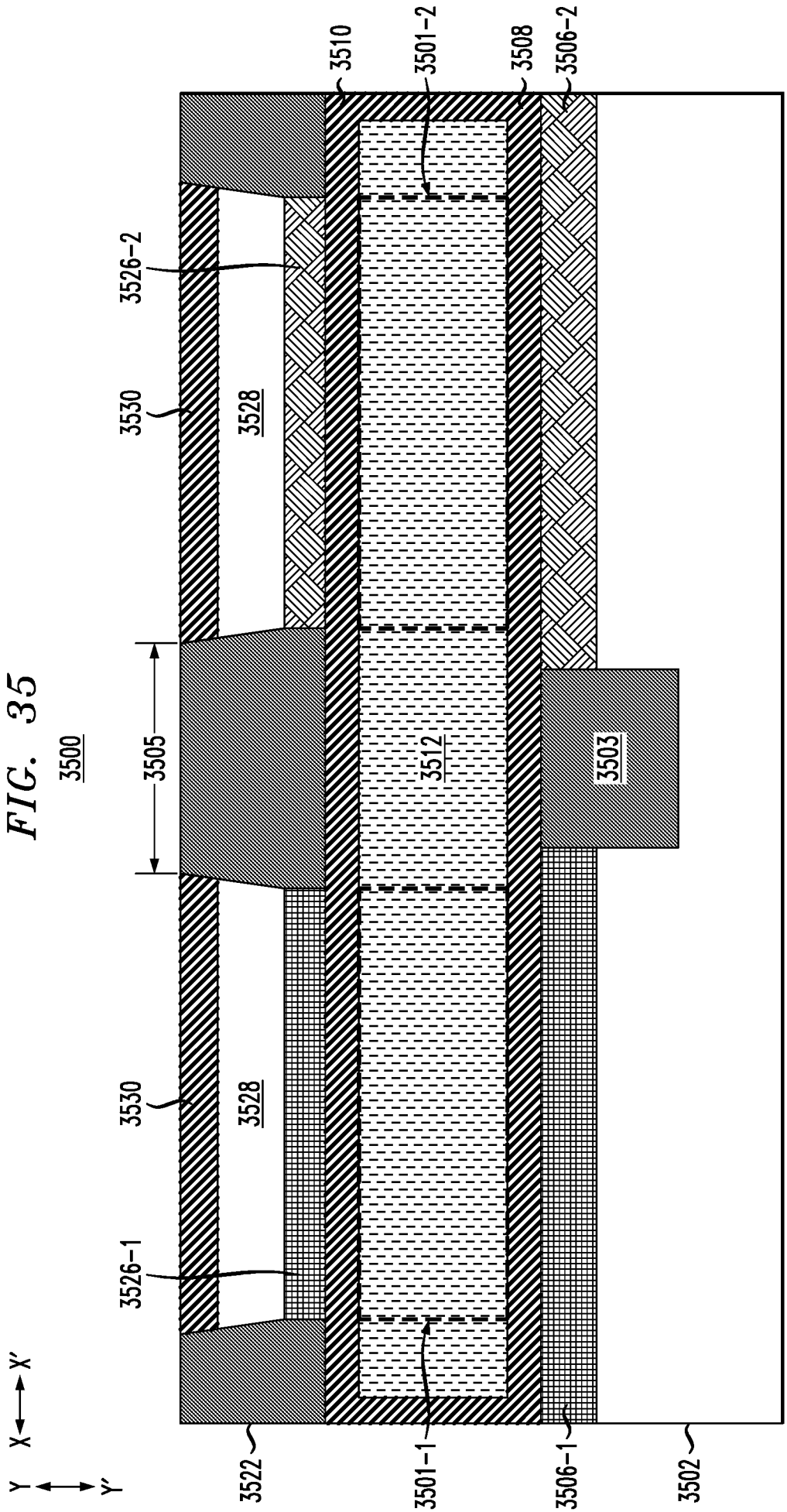
Y
Y'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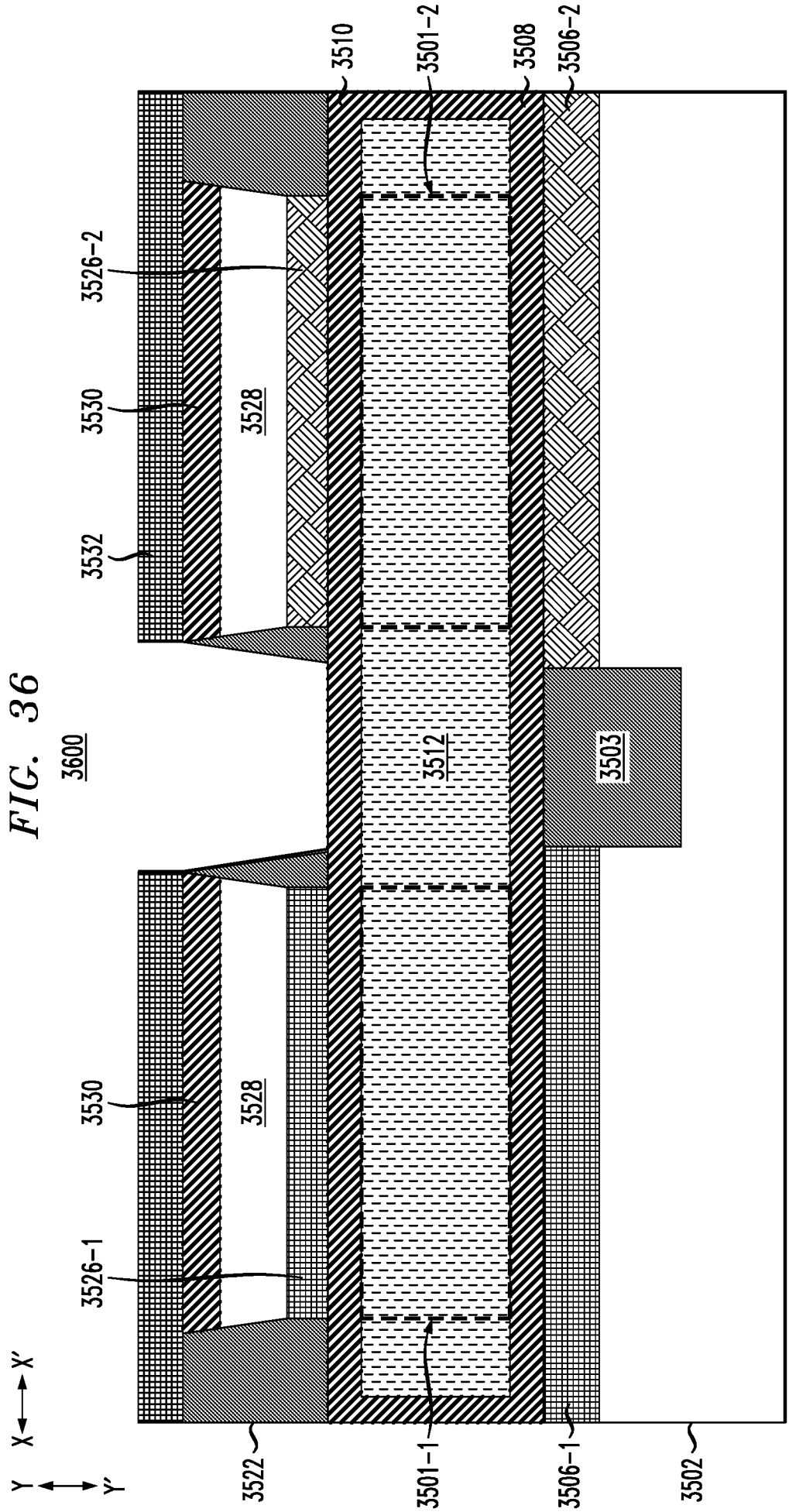
3506-1
3502
X
X'
Y
Y'

FIG. 35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X'
Y
Y'
3522
3501-1
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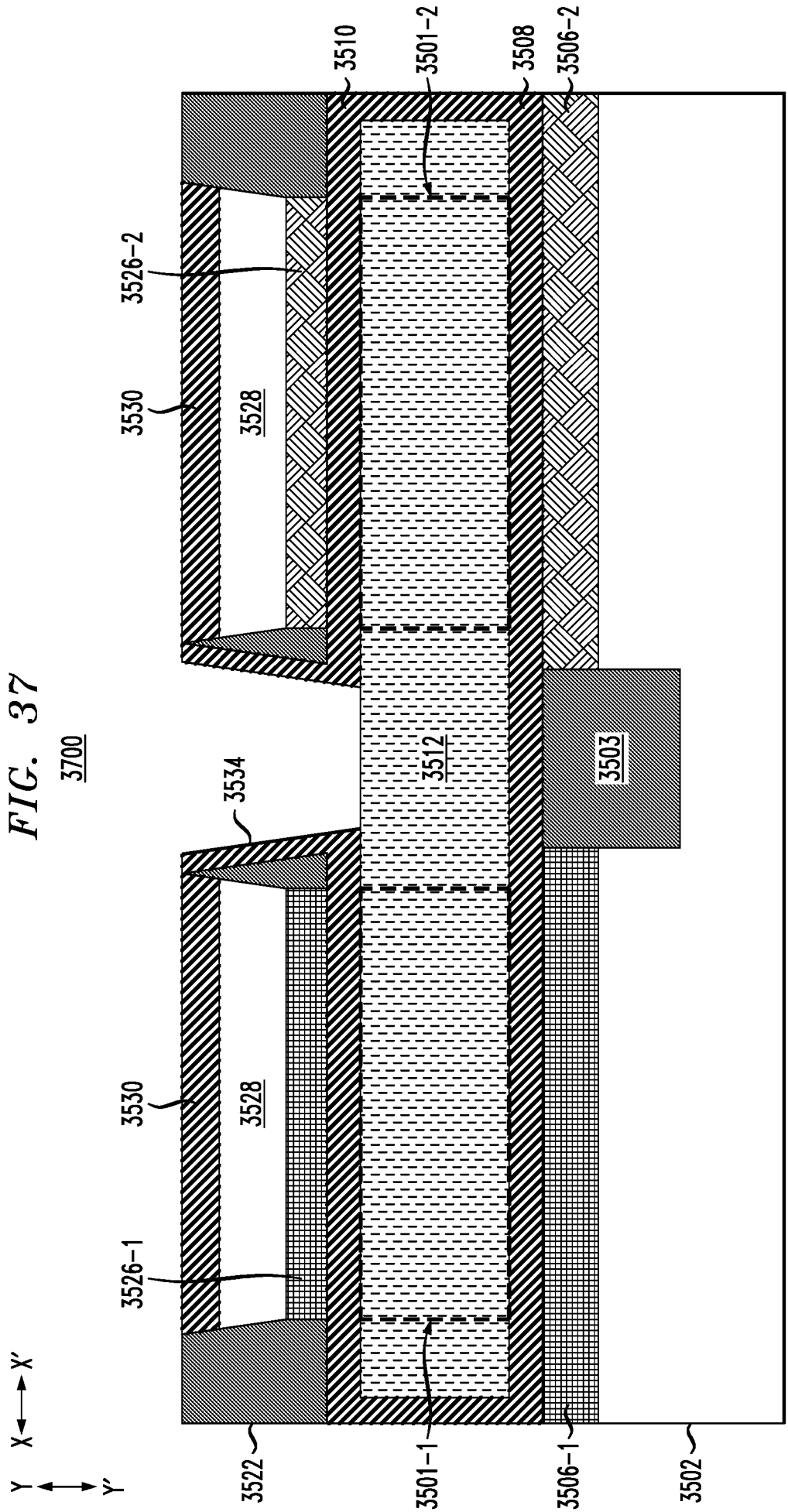
FIG. 36
3600

FIG. 37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Y'
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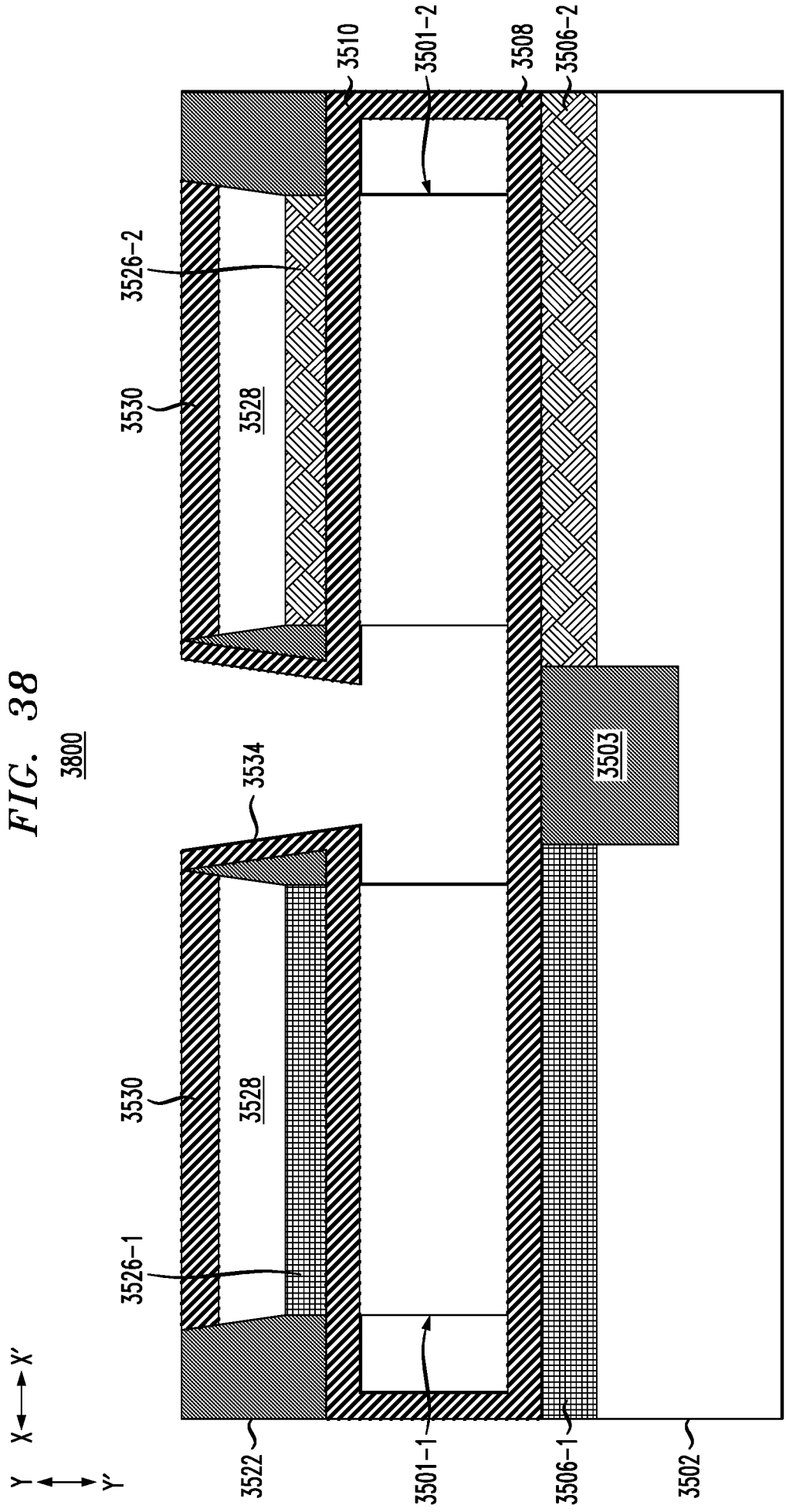
3502

FIG. 38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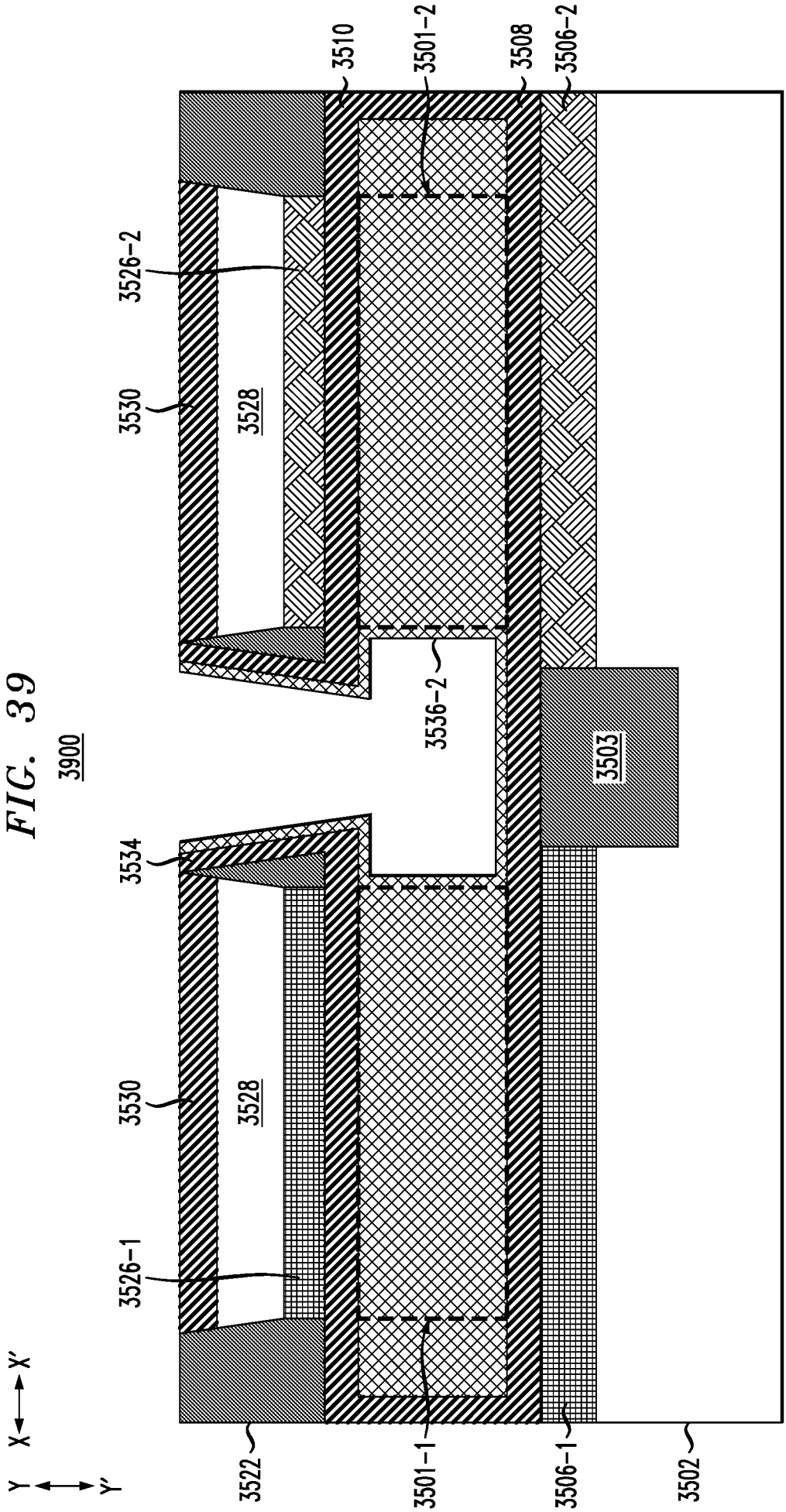
X
X'
Y
Y'
3522
3501-1
3506-1
3502

FIG. 39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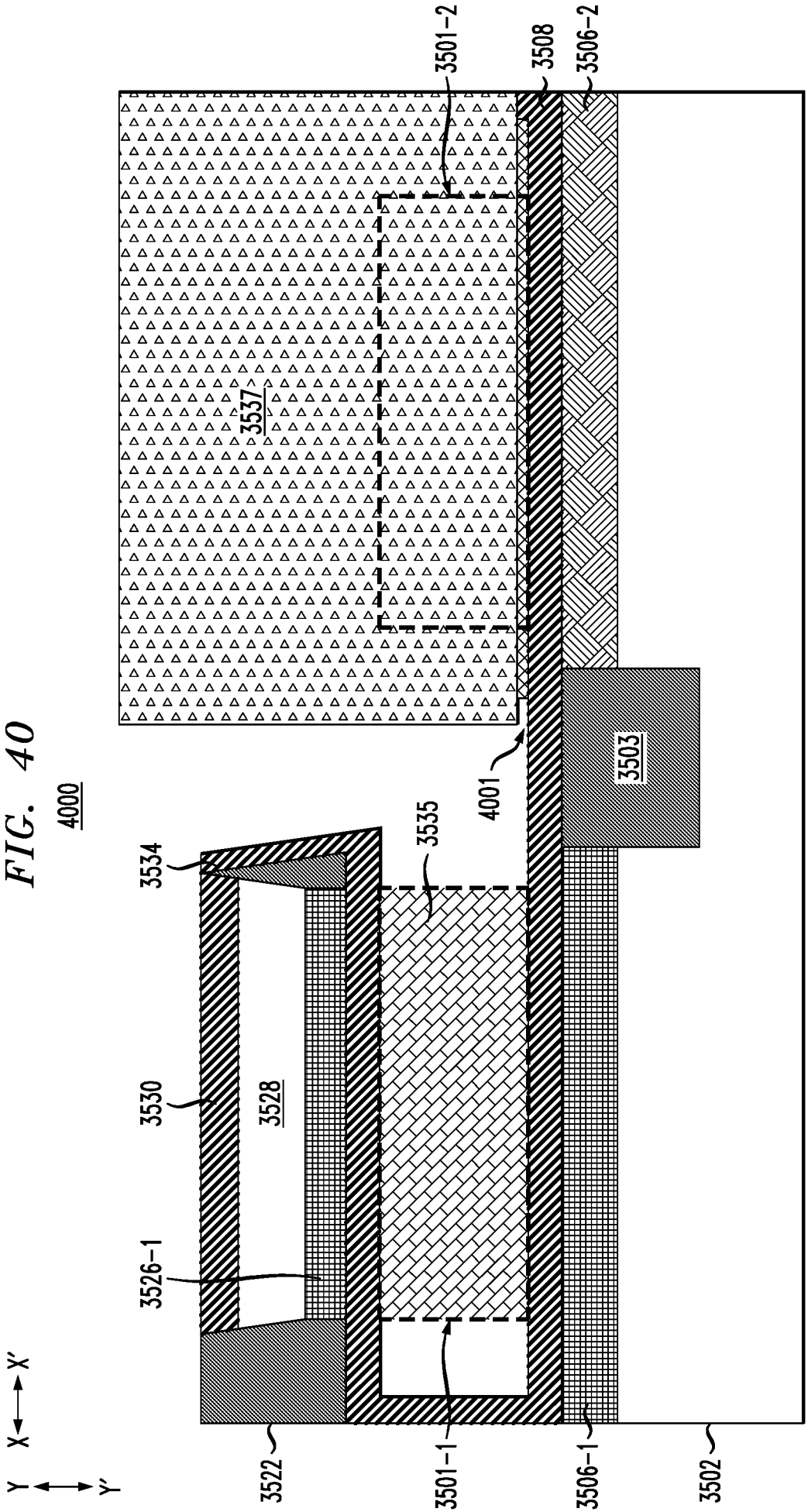
3506-1
3502
X
X'
Y
Y'

FIG. 40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Y
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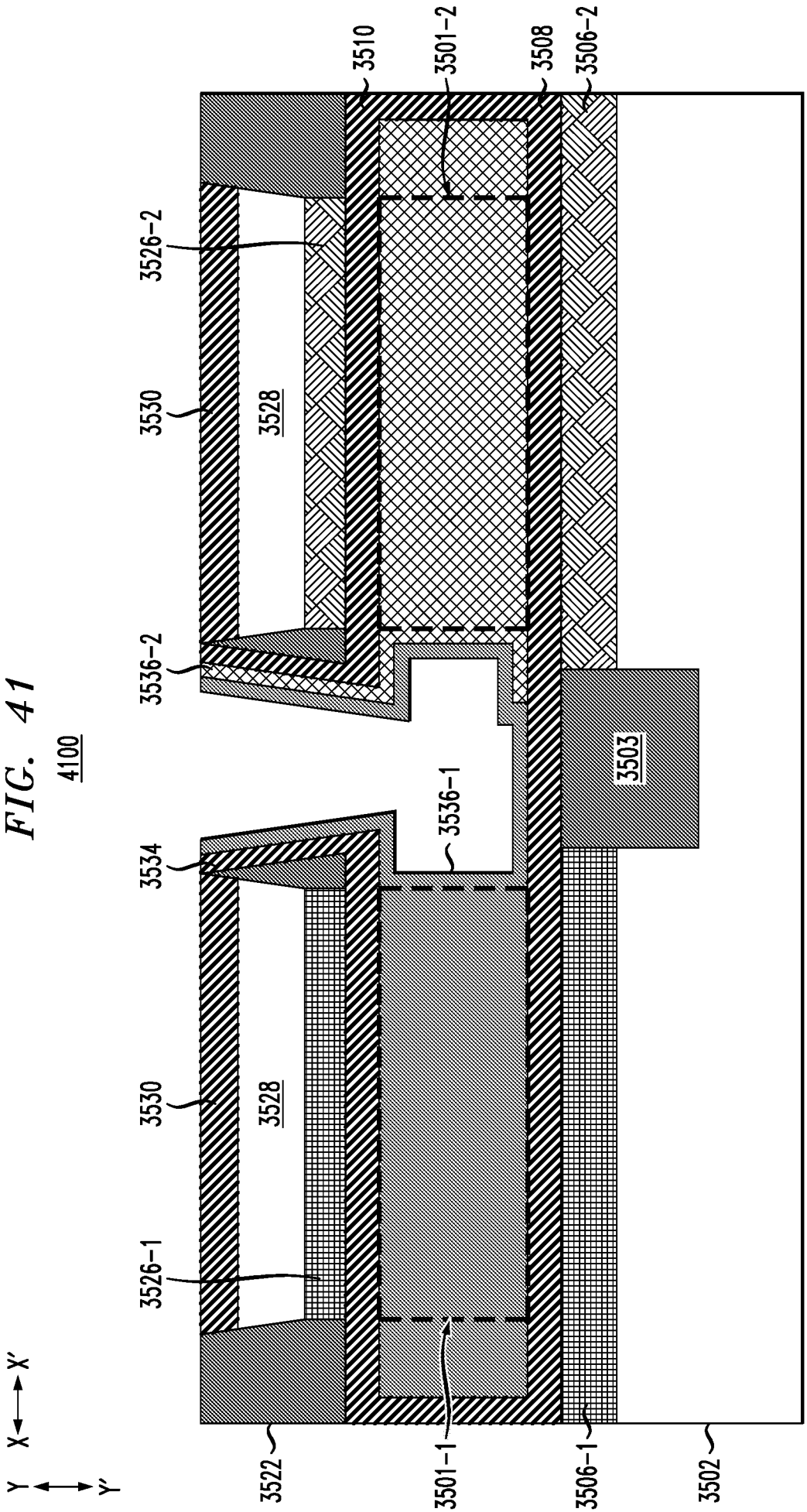
Y'
3522
3501-1
3506-1
3502

FIG. 41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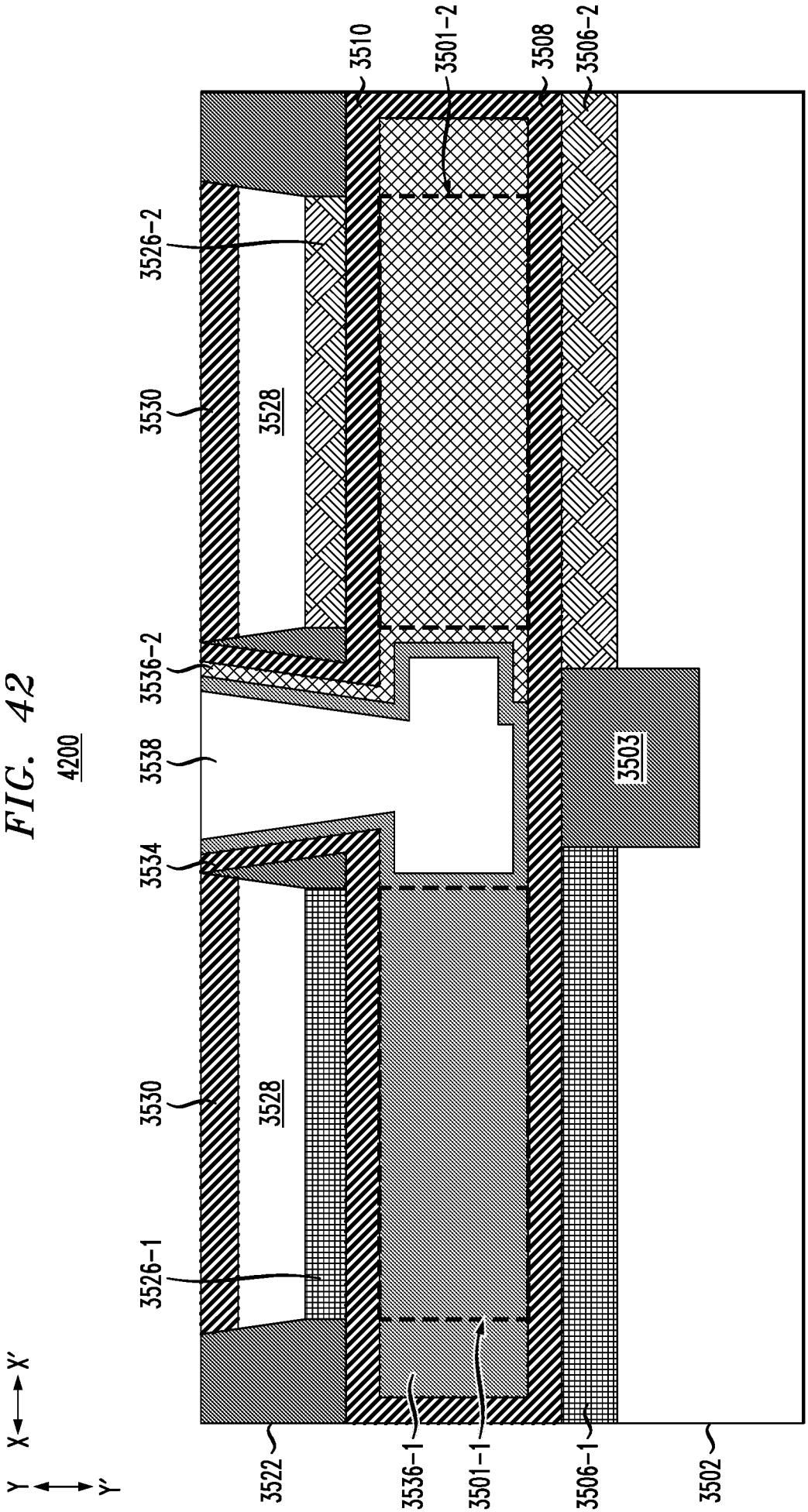
3526-1
3522
3501-1
3506-1
3502
X
X'
Y
Y'

FIG. 42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3506-1
3502
X
X'
Y
Y'

FIG. 43

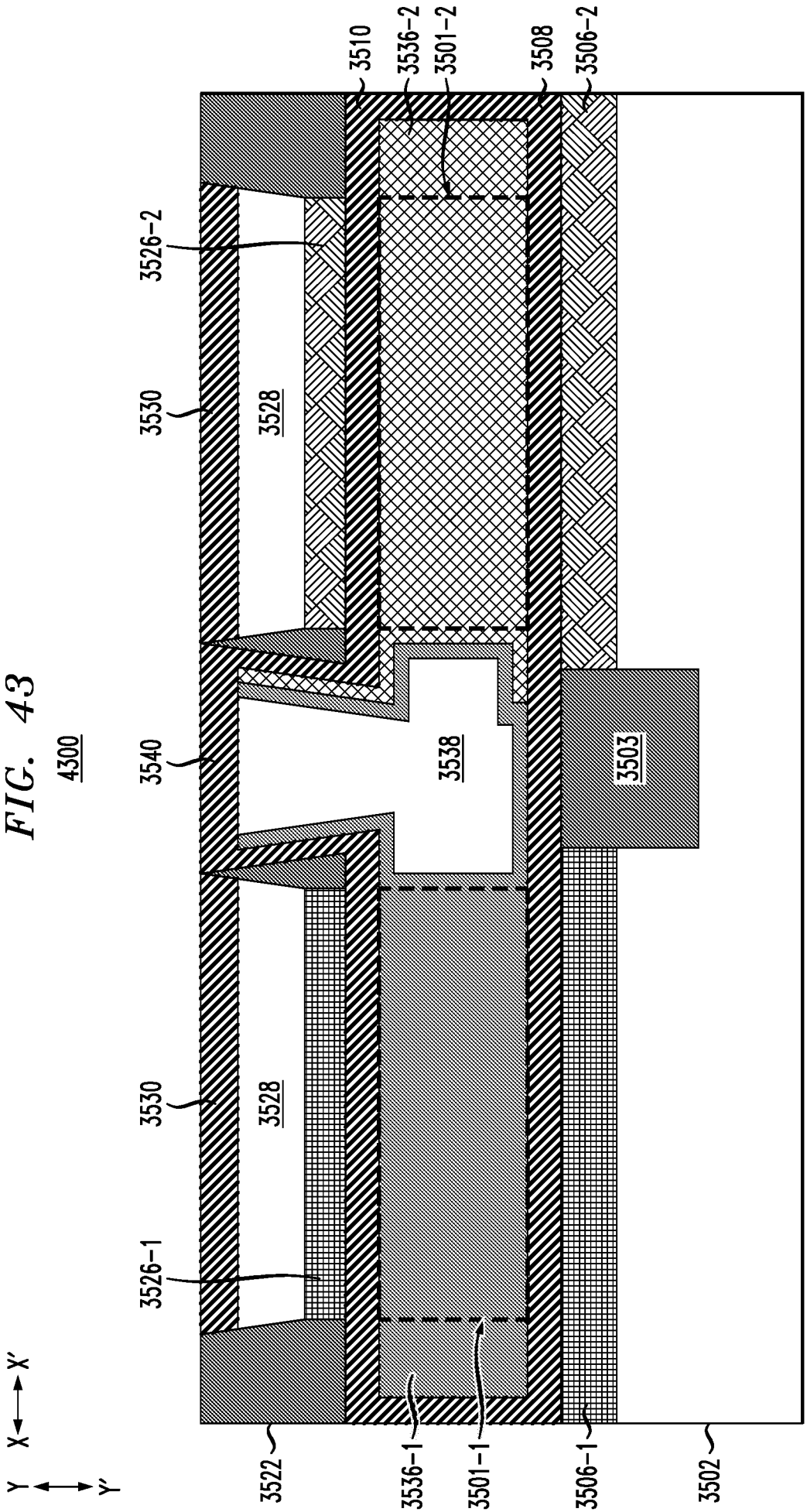
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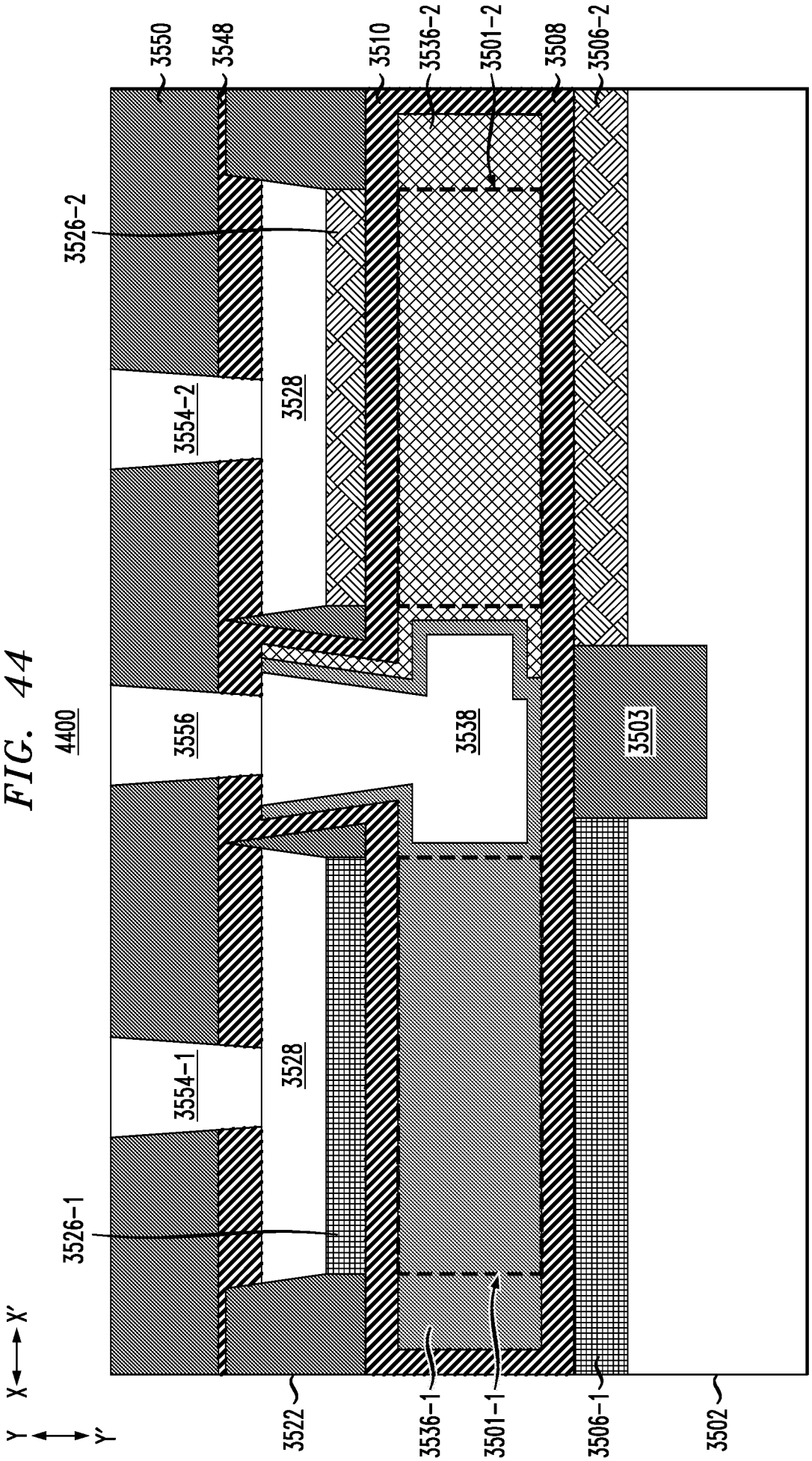
FIG. 44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3503
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Y
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X'
Y'
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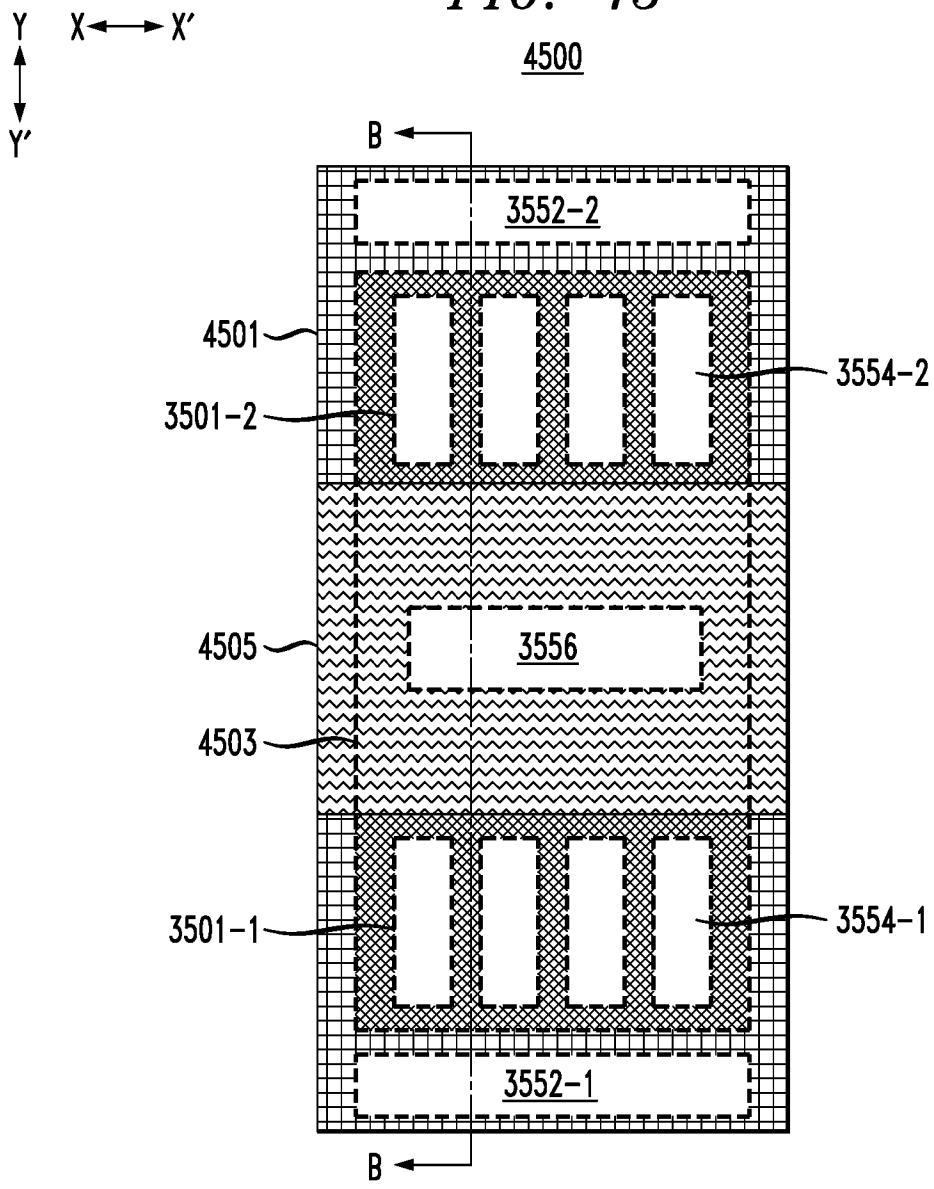
3536-1
3501-1
3506-1
3502

FIG. 45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B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2018/060735

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/41(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI, SIPOABS, DWPI, CNTXT, USTXT: semiconductor, fin, surface, substrate, vertical, transport, field, effect, transistor, VTFET, replacement, metal, gate, RMG, self-aligned, contact, layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 103972067 A (GLOBALFOUNDRIES INC. ET AL.) 06 August 2014 (2014-08-06) the whole document	1-20
A	CN 105261645 A (UNITED MICROELECTRONICS CORPORATION) 20 January 2016 (2016-01-20) the whole document	1-20
A	US 9048254 B2 (UNITED MICROELECTRONICS CORPORATION) 02 June 2015 (2015-06-02) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 April 2019	**28 May 2019**
Name and mailing address of the ISA/CN **National Intellectual Property Administration, PRC** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China** Facsimile No. **(86-10)62019451**	Authorized officer **ZHONG,Yangxue** Telephone No. **86-010-62411634**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/IB2018/060735

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	103972067	A	06 August 2014	US	2014217482	A1	07 August 2014
				US	8946793	B2	03 February 2015
				TW	201432821	A	16 August 2014
				CN	103972067	B	17 May 2017
				TW	I508192	B	11 November 2015
CN	105261645	A	20 January 2016	US	9224864	B1	29 December 2015
				US	2016020323	A1	21 January 2016
US	9048254	B2	02 June 2015	US	9397189	B2	19 July 2016
				US	2011127589	A1	02 June 2011
				US	2015249142	A1	03 September 2015