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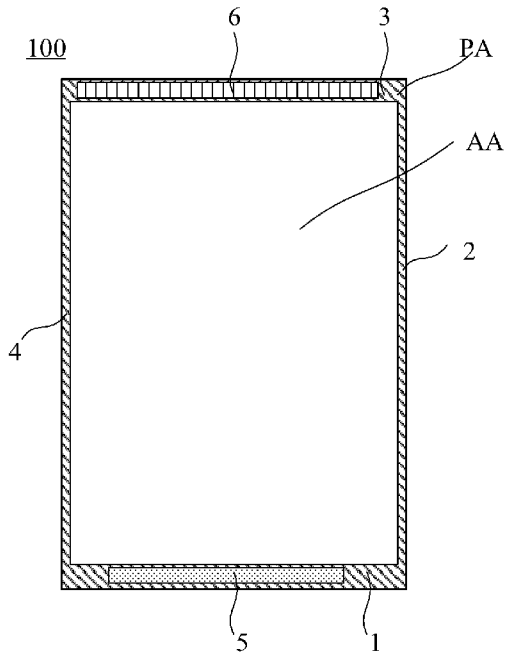

FIG. 1

(57) Abstract: A display panel includes a display area and a peripheral area surrounding the display area. The peripheral area comprises a first area (1), a second area (2), a third area (3) opposite to the first area (1), and a fourth area (4) opposite to the second area (2). The display panel may further include a data driving integrated circuit (5) provided in the first area (1), a gate drive circuit (6) provided in the third area (3), and a plurality of signal transmission lines (22) arranged in at least one of the second area (2) and the fourth area (4). The configuration of the data driving integrated circuit (5) and the gate drive circuit (6) makes it possible to manufacture a display panel with a narrow bezel.

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ARRAY SUBSTRATE, METHOD OF FABRICATING ARRAY SUBSTRATE, DISPLAY DEVICE, AND METHOD OF FABRICATING DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[1] This application claims the benefit of the filing date of Chinese Patent Application No. 201710979875.4 filed on October 19, 2017, the entire disclosure of which is hereby incorporated by reference.

TECHNICAL FIELD

[2] The present disclosure generally relates to the field of display technology, and in particular, to a display panel and a display device.

BACKGROUND

[3] A current trend in the field of display technology is a "narrow bezel" or even a "bezel-less" display. A conventional display device (for example, an organic light emitting diode (OLED) display device) may comprise an array substrate that comprises a display region and a periphery region surrounding the display region. The display region is provided with a plurality of pixel structures, whereas the periphery region is provided with a plurality of lines for loading drive signals to individual pixel structures. The width of the periphery region constitutes the "bezel." In order to reduce the width of the bezel, the "gate on array" (GOA) technology has been proposed, where a gate drive circuit is formed in the periphery region of the array substrate.

BRIEF SUMMARY

[4] One embodiment of the present disclosure is a display panel. The display panel may comprise a display area; and a peripheral area surrounding the display area, the peripheral area comprising a first area, a second area, a third area opposite to the first area, and a fourth area opposite to the second area. The display panel may further comprise a data driving integrated circuit provided in the first area, a gate drive circuit provided in the third area, and a plurality of signal transmission lines arranged in at least one of the second area and the fourth area. The plurality of signal transmission lines may extend in a first direction, and may be electrically connected to the gate drive circuit and configured to provide time sequence signals to the gate drive circuit.

[5] In at least some embodiments, the display panel may further comprise a plurality of gate connecting lines arranged in the display area and extending in the first direction, and a plurality of gate lines arranged in the display area and extending in a second direction. The first direction and the second direction may be substantially perpendicular to each other.

[6] In at least some embodiments, the display panel may further comprise a substrate, a light shielding layer provided on one side of the substrate, a buffer layer provided on a side of the light shielding layer opposite from the substrate, a gate insulating layer provided on a side of the buffer layer opposite from the substrate, and at least one through-hole extending through the buffer layer and the gate insulating layer. The plurality of signal transmission lines may be provided in a same layer as the light shielding layer. A plurality of gate lines may be provided on a side of the gate insulating layer opposite from the substrate. The plurality of gate lines may be electrically connected to the plurality of signal transmission lines through the at least one through-hole.

[7] In at least some embodiments, the display panel may further comprise a plurality of switches, the number of switches satisfying the relationship N x S, with N being a number of output terminals in the gate drive circuit, S being a number of gate connecting lines connected to one of the plurality of output terminals, and N and S each being a positive integer equal to or greater than 1. In at least some embodiments, each of the plurality of switches may comprise a first end and a second end. The first end of each of the plurality of switches may be electrically connected to at least one of the plurality of gate connecting lines. The second end of each of the plurality of switches may be electrically connected to an output terminal of the gate drive circuit that is connected to the at least one of the plurality of gate connecting lines.

[8] In at least some embodiments, the display panel may comprise an array of pixels. The display panel may comprise a same number of gate connecting lines as a number of rows in the array of pixels. Each of the gate connecting lines may be electrically connected to one of the rows in the array of pixels.

[9] In at least some embodiments, each of the plurality of switches may comprise a plurality of transistors. The display panel may further comprise a reset unit configured to perform a reset operation to at least one of (i) a gate connecting line connected to a (n+1)-th switch when a n-th switch is turned on and (ii) a gate connecting line connected to a (N x S)-th switch when

a first of the plurality of transistors in a switch is turned on, with n being a value that is smaller than a positive integer of (N x S).

[10] In at least some embodiments, the reset unit may comprise a plurality of transistors, the number of transistors in the reset unit being the same as the number of switches in the display panel.

[11] In at least some embodiments, each of the plurality of transistors of the reset unit may comprise a gate electrode, a source electrode, and a drain electrode. The gate electrode of an n-th transistor in the reset unit may be electrically connected to a first end of the corresponding n-th switch. The source electrode of the n-th transistor in the reset unit may be electrically connected to a predetermined voltage signal. The drain electrode of the n-th transistor may be electrically connected to a first end of the (n+1)-th switch.

[12] In at least some embodiments, the drain electrode of the first transistor in the reset unit may be electrically connected to a first end of the (N x S)-th transistor.

[13] Another embodiment of the present disclosure is a display device. The display device may comprise a display panel as described above.

BRIEF DESCRIPTION OF THE DRAWINGS

[14] The subject matter that is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other objects, features, and advantages of the present disclosure are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

[15] FIG. 1 shows a schematic diagram of a display panel according to an embodiment of the present disclosure;

[16] FIG. 2 shows a wiring diagram of a display panel according to an embodiment of the present disclosure;

[17] FIG. 3 shows a schematic cross-sectional view of the display panel illustrated in FIG. 2 along the line A-A;

[18] FIG. 4 shows a schematic cross-sectional view of the display panel illustrated in FIG. 2 along the line C-C;

[19] FIG. 5 shows a blown-up diagram of the dashed-line portion of the wiring diagram illustrated in FIG. 2;

[20] FIGS. 6 and 7 show schematic diagrams illustrating a connection between an output terminal and a signal transmission line according to embodiments of the present disclosure; and

[21] FIG. 8 shows a waveform diagram illustrating a time sequence signal according to an embodiment of the present disclosure.

[22] The various features of the drawings are not to scale as the illustrations are for clarity in facilitating one skilled in the art in understanding the invention in conjunction with the detailed description.

DETAILED DESCRIPTION

[23] Next, the embodiments of the present disclosure will be described clearly and concretely in conjunction with the accompanying drawings, which are described briefly above. The subject matter of the present disclosure is described with specificity to meet statutory requirements. However, the description itself is not intended to limit the scope of this disclosure. Rather, the inventors contemplate that the claimed subject matter might also be embodied in other ways, to include different steps or elements similar to the ones described in this document, in conjunction with other present or future technologies.

[24] While the present technology has been described in connection with the embodiments of the various figures, it is to be understood that other similar embodiments may be used or modifications and additions may be made to the described embodiments for performing the same function as the present technology without deviating therefrom. Therefore, the present technology should not be limited to any single embodiment, but rather should be construed in breadth and scope in accordance with the appended claims. In addition, all other embodiments obtained by one of ordinary skill in the art based on embodiments described in this document are considered to be within the scope of this disclosure.

[25] A current trend in the field of display technology is a “narrow bezel” or even a “bezel-less” display. A conventional display device (for example, an organic light emitting diode (OLED) display device) may comprise an array substrate that comprises a display region and a periphery region surrounding the display region. The display region is provided with a

plurality of pixel structures, whereas the periphery region is provided with a plurality of lines for loading drive signals to individual pixel structures. The width of the periphery region constitutes the "bezel." In order to reduce the width of the bezel, the "gate on array" (GOA) technology has been proposed, where a gate drive circuit is formed in the periphery region of the array substrate. However, conventional techniques for integrating the gate driving circuit onto the display panel make it difficult to reduce the amount of wiring in the display panel frame. The wirings still occupy a certain width, so as to limit the ability of conventional techniques to reduce the width of the display panel bezel. Therefore, there is a need to address the technical problem of further reducing the bezel width of a display panel.

[26] Embodiments of the present disclosure arrange the data driving integrated circuit and the gate drive circuit on opposite sides of a display panel, so that the number of components (for example, the gate and data lines) that need to be installed in the remaining sides of the display panel can be reduced and the width of the bezel corresponding to those remaining sides of the display panel can be narrowed. This makes it possible to realize a display panel with a narrow bezel.

[27] FIG. 1 shows a schematic diagram of a display panel according to an embodiment of the present disclosure. A display panel according to the present disclosure may be integrated into any display apparatus, including, but not limited to, a mobile phone, a tablet, a television, a computer, a display, a notebook computer, a digital photo frame, a navigation system, and any other products or components that provide a display function.

[28] As shown in FIG. 1, a display panel according to the present disclosure comprises a display area AA and a peripheral area PA surrounding the display area AA. The peripheral area PA includes a first area 1, a second area 2, a third area 3, and a fourth area 4. A data driving integrated circuit 5 is provided in one area of the peripheral area (for example, the first area 1 in the embodiment illustrated in FIG. 1) of the display panel. A gate drive circuit 6 is provided in an area of the peripheral area that is opposite from the data driving integrated circuit 5 (for example, the third area 3 in the embodiment illustrated in FIG. 1).

[29] The gate drive circuit 6 may be manufactured according to any suitable process known to a person of ordinary skill in the art, including the gate of array (GOA) technique.

[30] A plurality of signal transmission lines (22 in FIG. 5) are arranged in at least one of the remaining areas of the periphery area of the display panel (for example, in at least one of the second area 2 and the fourth area 4 in the embodiment illustrated in FIG. 1). The signal transmission lines 22 are arranged in a direction parallel to the second area 2 and/or the fourth area 4 of the display panel. The signal transmission lines 22 are configured to electrically connect to the gate drive circuit 6, and to provide time sequence signals to the gate drive circuit 6. More particularly, each signal transmission line 22 comprises a first component configured to transmit time sequence signals to the gate drive circuit 6, and a second component configured to transmit signals to a switch.

[31] It is understood that additional components and/or accessories may be provided within a display panel of the present disclosure without departing from the spirit and scope of the present disclosure. A person of ordinary skill in the art would readily appreciate that the configuration of a display panel is not limited to the embodiments shown in the figures, and a display panel may include any additional components that are typically found in a display panel and/or that are provided according to any particular purpose for which the display panel is intended. For example, in some embodiments, the display panel may further comprise a flexible circuit board electrically connected to the data driving integrated circuit 5; an electrostatic discharge unit; a fan-out unit provided between the data driving integrated circuit 5 and the first area 1; a cell test data line (CTD), and/or a data selector (MUX, Multiplexer). The display panel may also include a cell test VCOM signal line (CT VCOM) provided on a side of the source of the gate drive circuit 6 that is opposite from the third area 3, a touch metal wire electrostatic discharge unit (TX ESD unit), and/or a gate drive circuit electrostatic discharge unit (GOA ESD unit).

[32] In a display panel according to the present disclosure, the data driving integrated circuit 5 and the gate drive circuit 6 are provided on opposite portions of the display panel (for example, on the first area 1 and the third area 3, respectively, in the embodiment illustrated in FIG. 1). This configuration of the data driving integrated circuit 5 and the gate drive circuit 6 makes it possible to reduce the need to install wiring and/or other components in the remaining two areas of the display panel (for example, the second area 2 and the fourth area 4 in the embodiment illustrated in FIG. 1), so as to effectively reduce the widths of those two

areas of the display panel. This in turn makes it possible to significantly reduce the width of the bezel of the display panel.

[33] FIG. 2 shows a wiring diagram of a display panel according to an embodiment of the present disclosure. FIG. 3 shows a schematic cross-sectional view of the display panel illustrated in FIG. 2 along the line A-A. FIG. 4 shows a schematic cross-sectional view of the display panel illustrated in FIG. 2 along the line C-C.

[34] As shown in FIGS. 3 and 4, a display panel according to the present disclosure also includes a substrate 10, a light shielding layer 11 provided on one side of the substrate 10, and at least one gate connecting line 12 provided in the same layer as the light shielding layer 11. The gate connecting line 12 is configured to transmit gate driving signals from the gate drive circuit 6 to the gate line 15, so as to enable control of the transistor corresponding to each individual pixel in the display panel (for example, as shown in FIG. 2). In some embodiments, providing the gate connecting line 12 in the same layer as the light shielding layer 11 makes it possible for the gate drive circuit 6 to transmit gate driving signals to the gate line 15 through the gate connecting line 12, which drives the gate electrode and performs sequential scanning of each of the pixel rows in the display panel. In some embodiments, the gate connecting line 12 is arranged in a direction parallel to the signal transmission lines (22 in FIG. 5) provided in the periphery area of the display panel.

[35] A buffer layer 13 may be provided on a side of the gate connecting line 12 opposite from the substrate 10. In some embodiments, the buffer layer 13 covers at least a portion of the gate connecting line 12 and at least a portion of the substrate 10. A gate insulating layer 14 may be provided on a side on the buffer layer 13 opposite from the substrate 10. At least one gate line 15 is provided on a side of the gate insulating layer 14 opposite from the substrate 10. At least one through-hole 16 extends through the gate insulating layer 14 and the buffer layer 13. The gate line 15 is electrically connected to the gate connecting line 12 via the through-hole 16. In some embodiments, the gate line 15 is arranged in a direction perpendicular to the signal transmission lines (22 in FIG. 5) provided in the periphery area of the display panel.

[36] FIG. 3 shows a schematic cross-sectional view of the display panel illustrated in FIG. 2 along the line A-A. As shown in FIG. 3, the display panel may also include an active layer 17

provided on a side of the buffer layer 13 opposite from the substrate 10. A gate electrode 19 may be provided on a side of the gate insulating layer 14 opposite from the substrate 10. The gate electrode 19 may be configured to be electrically connected to the gate line 15. A passivation layer 18 may be provided on a side of the gate electrode 19 opposite from the substrate. A source electrode 20 and a drain electrode 21 may be provided on a side of the passivation layer 18 opposite from the substrate 10. At least one through-hole may be provided that extends through passivation layer 18 and at least a portion of the gate insulating layer 14. The source electrode 20 and the drain electrode 21 may be electrically connected to the active layer 17 via the through-hole in the passivation layer 18 and the gate insulating layer 14.

[37] FIG. 4 shows a schematic cross-sectional view of the display panel illustrated in FIG. 2 along the line C-C. As shown in FIG. 4, the gate line 15 may be arranged in a direction that is parallel to the first area 1 and the third area 3 of the display panel illustrated in FIG. 2. The gate connecting line 12 may be arranged in a direction that is perpendicular to the gate line 15, and electrically connected to the gate line 15 via the through-hole 16. The gate connecting line 12 is configured to transmit gate driving signals from the gate drive circuit 6 to the gate line 15, so as to enable control of the transistor corresponding to each individual pixel in the display panel (for example, as shown in FIG. 2). In some embodiments, providing the gate connecting line 12 in the same layer as the light shielding layer 11 makes it possible for the gate drive circuit 6 to transmit gate driving signals to the gate line 15 through the gate connecting line 12, which drives the gate electrode and performs sequential scanning of each of the pixel rows in the display panel.

[38] In some embodiments, the display panel may include an array having M rows and N columns of pixels, with M and N each being an integer greater than 1. M signal transmission lines 22 are provided for M rows of pixels, and each signal transmission line 22 is electrically connected to a corresponding gate line servicing one of the M rows of pixels. Electrically connecting each signal transmission line 22 with a corresponding gate line servicing one of the pixel rows makes it possible to transmit gate driving signal along one signal transmission line 22 to one gate line 15, so as to enable sequential scanning of each of the pixel rows in the display panel.

[39] In some embodiments, for an array substrate containing *N* columns of pixels, the array may be subdivided into regions containing *N* columns and/or *M* rows of pixels, and a signal transmission line 22 is provided for each region. This configuration makes it possible to uniformly distribute the signal transmission lines 22 in the array substrate, so as to simplify the design and construction of the wiring process.

[40] For example, FIG. 2 shows a wiring diagram of a display panel according to an embodiment of the present disclosure. As shown in FIG.2, each pixel may be a red pixel (R), a green pixel (G), or a blue pixel (B). In the array substrate shown in FIG. 2, the array is subdivided so that the ratio of the number of rows of pixels (*M*) to the number of columns (*N*) is 2 to 1. In that case, each column of pixels may be provided with two (2) gate connecting lines 12. As shown in FIG. 2, a first gate connecting line 12 is provided on one side of each column of red (R) pixels, and a second gate connecting line 12 is provided between each column of green (G) pixels and each column of blue (B) pixels. The gate connecting lines 12 are electrically connected to the gate lines 15 via the through-holes 16. There are no particular limitations on the configuration and arrangement of the gate connecting lines 12, and the gate connecting lines 12 may be arranged in any suitable manner known to a person of ordinary skill in the art, for example, depending on the intended purpose of the display panel.

[41] In some embodiments (for example, as shown in FIG. 1), the display panel is rectangular. The first area 1 and the second area 2 form a right angle of the rectangle, and the length of the first area 1 is shorter than the length of the second area 2. Similarly, the third area 3 and the fourth area 4 form another right angle of the rectangle, and the length of the third area 3 is shorter than the length of the fourth area 4. The first and third areas 1, 3 are on opposite sides of the rectangle from each other. Each row of pixels is arranged in a direction parallel to the first area 1 (and the third area 3).

[42] The gate drive circuit 6 includes a plurality of output terminals (Out_1 and Out_N in FIG. 5). For the purpose of illustration, the gate drive circuit 6 includes *N* output terminals electrically connected to *S* gate connecting lines 12. *N* and *S* are each a positive integer greater than 1.

[43] In the embodiment of the display panel illustrated in FIG. 1, the gate drive circuit 6 is provided on the third area 3, that is, on an area of the display panel having the shorter length, and each row of pixels is arranged in a direction parallel to the shorter third area 3. This results in the number of output terminals on the gate drive circuit 6 generally being smaller than the number (*M*) of signal transmission lines 22, because the length of the portion of the display panel on which the gate drive circuit 6 is provided affects the number of output terminals that can be installed. By electrically connecting each output terminal to *S* gate connecting lines 12, the present disclosure makes it possible to ensure that each signal transmission line 22 receives the gate driving signals from the gate drive circuit 6, so as to greatly improve the driving of each pixel's transistors.

[44] In some embodiments, the display panel may further include a plurality of switches. A switch may be implemented with a plurality of transistors. For example, the display panel may include *S* x *N* switches. Each switch comprises a first end, a second end, and a third end. The first end of a switch is electrically connected to a signal transmission line 22, which is in turn connected to an output terminal of the gate drive circuit. This output terminal is electrically connected to the second end of the switch 7.

[45] The display panel may further include a timing control unit. The timing control unit is configured to be electrically connected to the third end of a switch 7, and to generate time sequence signals for controlling the turning on and off of each output terminal and each of the *S* gate connecting line 12 that is connected to the output terminal.

[46] FIG. 5 shows a blown-up diagram of the dashed-line portion of the wiring diagram illustrated in FIG. 2, illustrating a connection between an output terminal (Out_1, Out_N) and a gate connecting line 12 according to an embodiment of the present disclosure. As shown in FIG. 5, *X* (number of signal transmission lines 22 connected to an output terminal) is 4, and there are *N* output terminals (OUT_1, OUT_2… OUT_N). As an illustrative example, OUT_1 is electrically connected to four (4) switches 7, each of the four switches 7 being electrically connected to a timing control unit 8. The timing control unit 8 transmits a time sequence signal, via a signal transmission line 22, to each switch 7, in order to turn ON or OFF the switch 7. When the switch 7 is turned ON, OUT_1 is configured to transmit gate drive signals along the gate connecting lines 12. Each output terminal is thus configured to

sequentially transmit gate drive signals along *S* gate connecting lines 12, and to control sequential driving of the pixels.

[47] In some embodiments, the display panel may further include a reset unit. When the $(n+1)^{th}$ switch 7 is turned on, the reset unit is configured to reset the signal transmission line 22 electrically connected to the n^{th} switch 7. When the first transistor in a switch 7 is turned ON, the reset unit is configured to reset the signal transmission line 22 electrically connected to the $(S \times N)^{th}$ switch. The value of *n* may be smaller than a positive integer of $(S \times N)$.

[48] FIG. 6 shows a schematic diagram illustrating a connection between an output terminal and a gate connecting line 12 according to another embodiment of the present disclosure. As shown in FIG. 6, the gate drive circuit 6 may be provided in an area of the peripheral area PA of the display panel opposite from the reset unit 9 (for example, in FIG. 6, the gate drive circuit 6 may be provided in third area 3 of the peripheral area PA, and the reset unit 9 may be provided in the first area 1 of the peripheral area PA). As shown in FIG. 9, a reset unit 9 is electrically connected to each switch 7. As an example, when the second switch is turned ON, the reset unit 9 is configured to reset the signal transmission line 22 electrically connected to the first switch. More generally, during scanning of the rows of pixels, when a particular row of pixels is turned ON, the previous row of pixels is turned OFF, and when the first row of pixels in a new frame is being scanned, the last row of pixels in the previous frame is turned OFF. This configuration of the display panel enables the sequential scanning of the rows of pixels.

[49] The reset unit 9 may include a plurality of transistors. Each transistor comprises a gate electrode, a source electrode, and a drain electrode. In some embodiments, the reset unit 9 includes the same number of transistors as the number of switches in the gate drive circuit 6. More particularly, the reset unit 9 may include $S \times N$ transistors. The gate electrode of the n^{th} transistor is electrically connected to the first end of the n^{th} switch. The source electrode of the n^{th} transistor is electrically connected to a predetermined voltage signal (for example, a low voltage signal (VGL)). The drain electrode of the n^{th} transistor is electrically connected to the first end of the $(n+1)^{th}$ switch. In addition, the drain electrode of the first of the plurality of transistors 90 is electrically connected to the first end of the $(S \times N)^{th}$ transistor.

[50] FIG. 7 shows a schematic diagram illustrating a connection between an output terminal and a gate connecting line 12 according to an embodiment of the present disclosure. As shown in FIG. 7, the switch 7 is composed of as plurality of transistors, and the reset unit 9 includes S x N transistors 90. The gate electrode of the n^{th} transistor is electrically connected to the first end of the n^{th} switch (for example, a drain electrode). The source electrode of the n^{th} transistor is electrically connected to a predetermined voltage signal (for example, a low voltage signal (VGL)). The drain electrode of the n^{th} transistor is electrically connected to the first end of the $(n+1)^{th}$ switch. More particularly, the drain electrode of the first transistor is electrically connected to the first end of the $(S \times N)^{th}$ switch. As shown in FIG. 7, the gate drive circuit 6 may be provided in an area of the peripheral area PA of the display panel opposite from the reset unit 9 comprising the transistors 90 (for example, in FIG. 7, the gate drive circuit 6 may be provided in third area 3 of the peripheral area PA, and the reset unit 9 may be provided in the first area 1 of the peripheral area PA).

[51] FIG. 8 shows a waveform diagram illustrating a time sequence signal according to an embodiment of the present disclosure. As shown in FIG. 8, a first timing control line L1 is connected to the first switch in a set of four (4) switches. A second timing control line L2 is connected to the second switch in a set of four (4) switches. A third timing control line L3 is connected to the third switch in a set of four (4) switches. A fourth timing control line L4 is connected to the fourth switch in a set of four (4) switches. High-voltage signals are transmitted to each of the four timing control lines L1, L2, L3, L4, and the timing of the high-voltage signals transmitted to different timing control lines does not overlap. Each high-voltage signal on each timing control line occupies 1/4 of a cycle.

[52] As shown in FIGS. 7 and 8, when the (n+1)th switch is turned ON, the (n+1)th transistor is also turned ON, and low-voltage signal is transmitted to the first end of the nth switch, so that the signal transmission line 22 corresponding to the nth switch becomes low voltage. When the first transistor of the switch is turned ON, the first transistor of the reset unit is turned ON, low-voltage signal is transmitted to the first end of the $(S \times N)^{th}$ switch, so that the signal transmission line corresponding to the $(S \times N)^{th}$ switch becomes low voltage.

[53] During scanning of the rows of pixels, a display panel according to the present disclosure is configured to turn ON a row of pixels and turn OFF the previous row of pixels, and turn

ON the first row of pixels in a new frame and turn OFF the last row of pixels in the previous frame. This configuration of the display panel enables the sequential scanning of the rows of pixels.

[54] In some embodiments, the display panel may include a touch metal line, a red pixel data line, a green pixel data line, and/or a blue pixel data line. The signal transmission lines are provided on a portion of the substrate that directly corresponds to the touch metal line, the red pixel data line, the green pixel data line, and/or the blue pixel data line.

[55] The touch metal line, the red pixel data line, the green pixel data line, and the blue pixel data line may shield light emitted by the display panel. Arranging the signal transmission lines on a portion of the substrate that directly corresponds to the touch metal line, the red pixel data line, the green pixel data line, and/or the blue pixel data line prevents the touch metal line, the red pixel data line, the green pixel data line, and/or the blue pixel data from causing excessive light shielding and reducing the transparency of the display panel.

[56] The present disclosure also provides a display device. The display device may be any device known to a person of ordinary skill in the art, including, but not limited to, a mobile phone, a tablet, a television, a computer, a display, a notebook computer, a digital photo frame, a navigation system, and any other products or components that provide a display function.

[57] It should be appreciated that changes could be made to the embodiments described above without departing from the inventive concepts thereof. It should be understood, therefore, that this invention is not limited to the particular embodiments disclosed, but it is intended to cover modifications within the spirit and scope of the present invention as defined by the appended claims.

CLAIMS

What is claimed is:

1. A display panel, comprising:

a display area; and

a peripheral area surrounding the display area, the peripheral area comprising a first area, a second area, a third area opposite to the first area, and a fourth area opposite to the second area,

wherein the display panel further comprises:

a data driving integrated circuit provided in the first area;

a gate drive circuit provided in the third area; and

a plurality of signal transmission lines arranged in at least one of the second area and the fourth area,

wherein the plurality of signal transmission lines extend in a first direction, and are electrically connected to the gate drive circuit and configured to provide time sequence signals to the gate drive circuit.

2. The display panel according to claim 1, further comprising:

a plurality of gate connecting lines arranged in the display area and extending in the first direction; and

a plurality of gate lines arranged in the display area and extending in a second direction,

wherein the first direction and the second direction are substantially perpendicular to each other.

3. The display panel according to any of the preceding claims, further comprising:

a substrate;

a light shielding layer provided on one side of the substrate;

a buffer layer provided on a side of the light shielding layer opposite from the substrate;

a gate insulating layer provided on a side of the buffer layer opposite from the substrate; and

at least one through-hole extending through the buffer layer and the gate insulating layer,

wherein the plurality of signal transmission lines are provided in a same layer as the light shielding layer,

wherein a plurality of gate lines are provided on a side of the gate insulating layer opposite from the substrate, and

wherein the plurality of gate lines are electrically connected to the plurality of signal transmission lines through the at least one through-hole.

4. The display panel according to any of the preceding claims, wherein the gate drive circuit comprises a plurality of output terminals, each output terminal being connected to at least a portion of the plurality of gate connecting lines.

5. The display panel according to any of the preceding claims,

wherein the display panel further comprises a plurality of switches, the number of switches satisfying the relationship N x S, with N being a number of output terminals in the gate drive circuit, S being a number of gate connecting lines connected to one of the plurality of output terminals, and N and S each being a positive integer equal to or greater than 1.

6. The display panel according to claim 5,

wherein each of the plurality of switches comprises a first end and a second end,

wherein the first end of each of the plurality of switches is electrically connected to at least one of the plurality of gate connecting lines, and

wherein the second end of each of the plurality of switches is electrically connected to an output terminal of the gate drive circuit that is connected to the at least one of the plurality of gate connecting lines.

7. The display panel according to any of the preceding claims,

wherein the display panel comprises an array of pixels,

wherein the display panel comprises a same number of gate connecting lines as a number of rows in the array of pixels, and

wherein each of the gate connecting lines is electrically connected to one of the rows in the array of pixels.

8. The display panel according to claim 5,

wherein each of the plurality of switches comprises a plurality of transistors, and

wherein the display panel further comprises a reset unit configured to perform a reset operation to at least one of (i) a gate connecting line connected to a (n+1)-th switch when a n-th switch is turned on and (ii) a gate connecting line connected to a (N x S)-th switch when a first of

the plurality of transistors in a switch is turned on, with n being a value that is smaller than a positive integer of (N x S).

9. The display panel according to claim 8, wherein the reset unit comprises a plurality of transistors, the number of transistors in the reset unit being the same as the number of switches in the display panel.

10. The display panel according to claim 9,

wherein each of the plurality of transistors of the reset unit comprises a gate electrode, a source electrode, and a drain electrode,

wherein the gate electrode of an n-th transistor in the reset unit is electrically connected to a first end of the corresponding n-th switch,

wherein the source electrode of the n-th transistor in the reset unit is electrically connected to a predetermined voltage signal, and

wherein the drain electrode of the n-th transistor is electrically connected to a first end of the (n+1)-th switch.

11. The display panel according to claim 10, wherein the drain electrode of the first transistor in the reset unit is electrically connected to a first end of the (N x S)-th transistor.

12. A display device, comprising the display panel according to any one of claims 1 to 11.

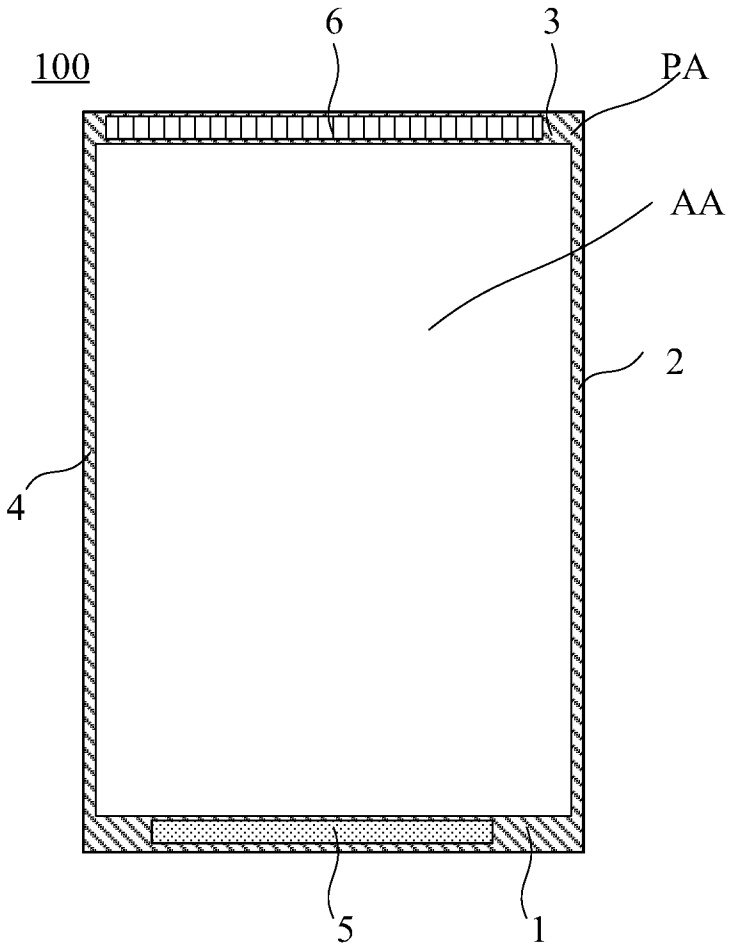

FIG. 1

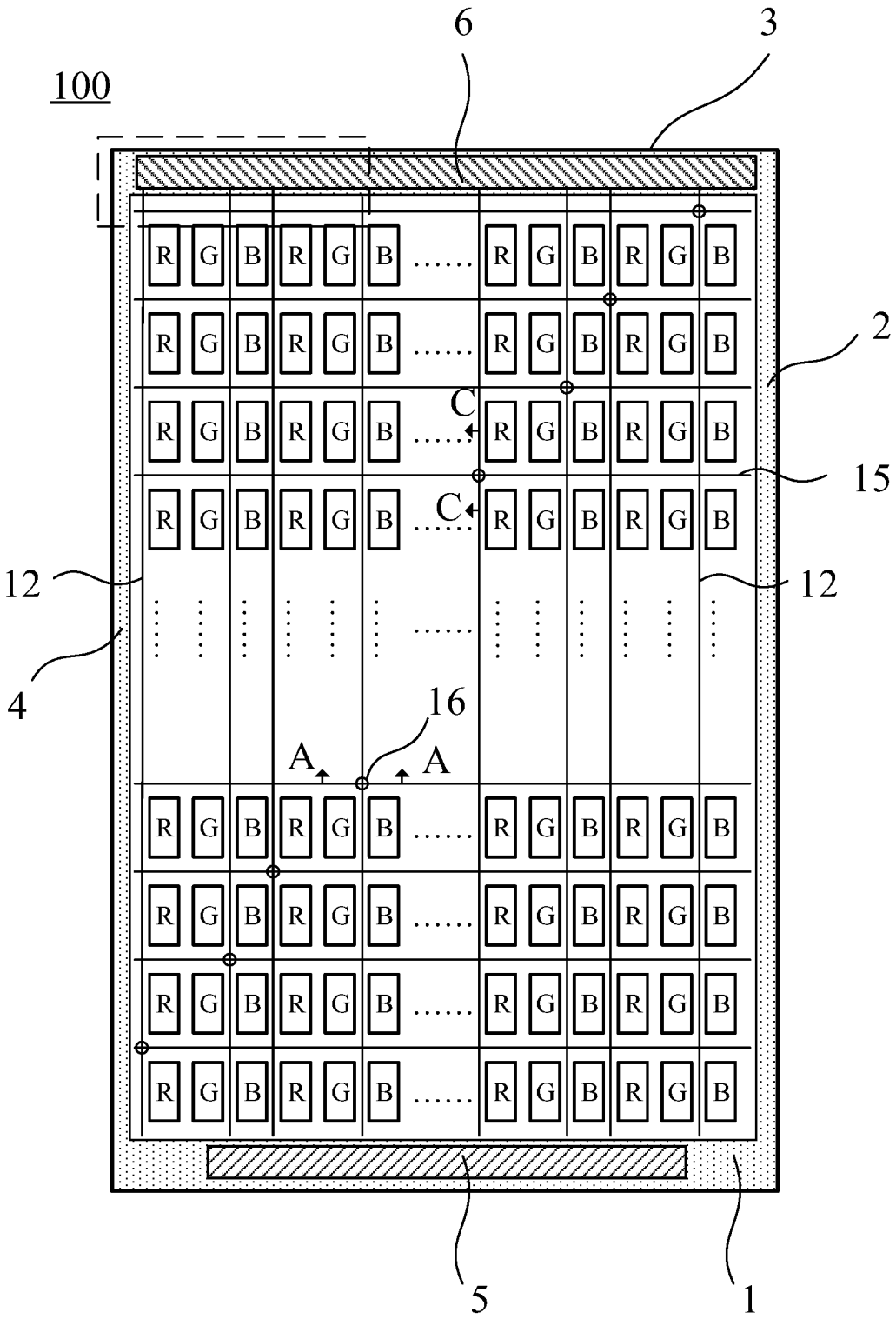

FIG. 2

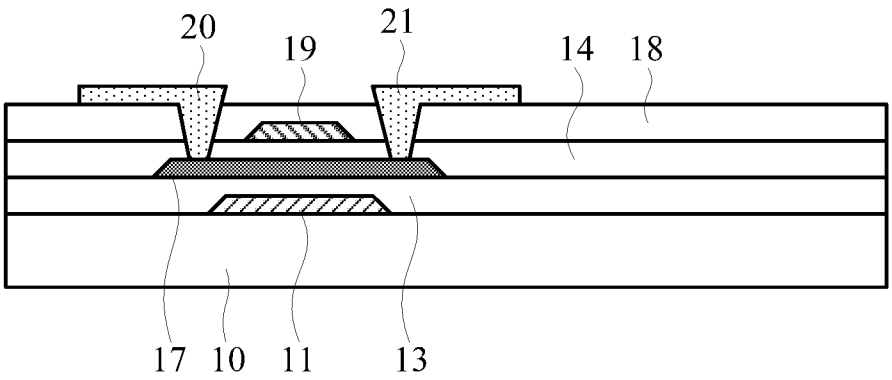

FIG. 3

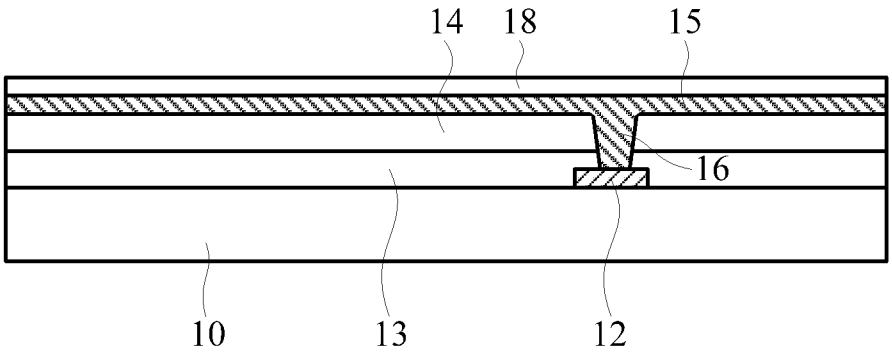

FIG. 4

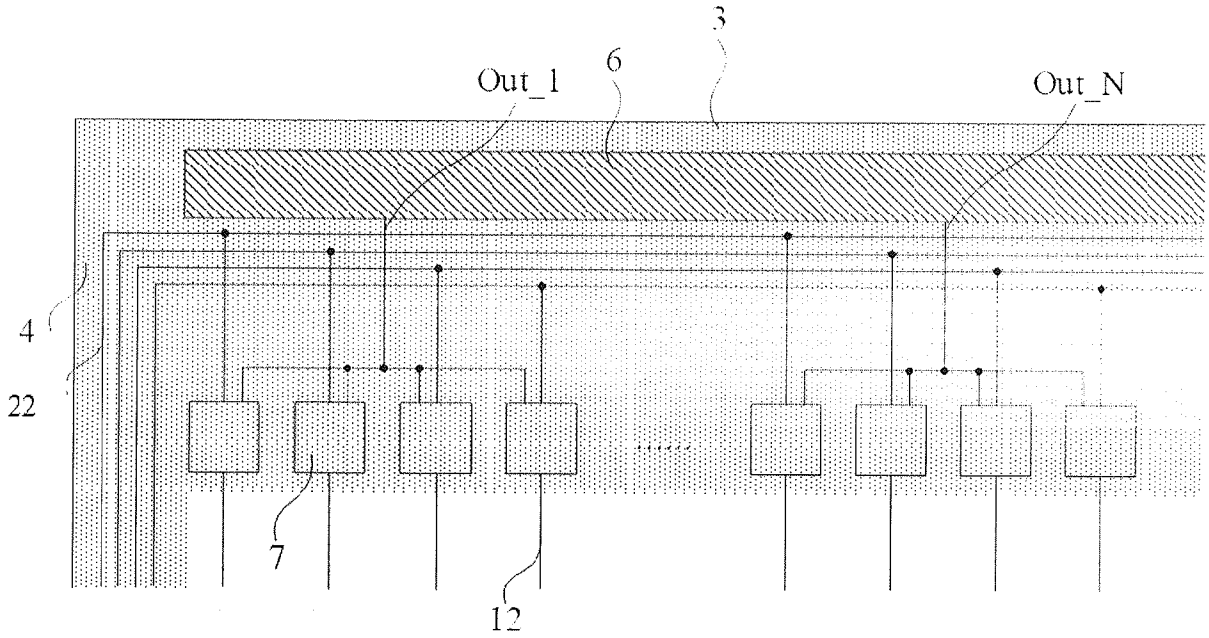

FIG. 5

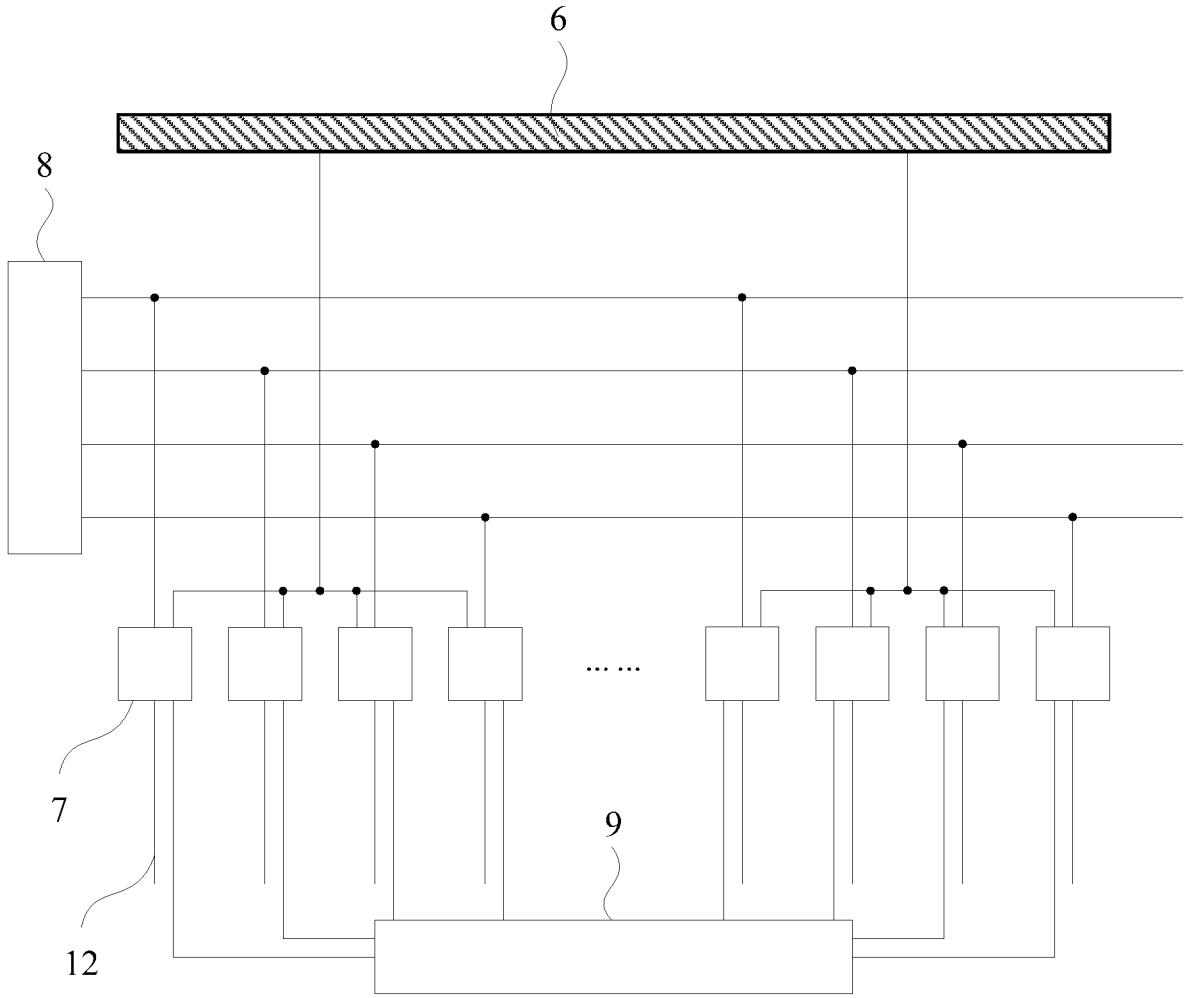

FIG. 6

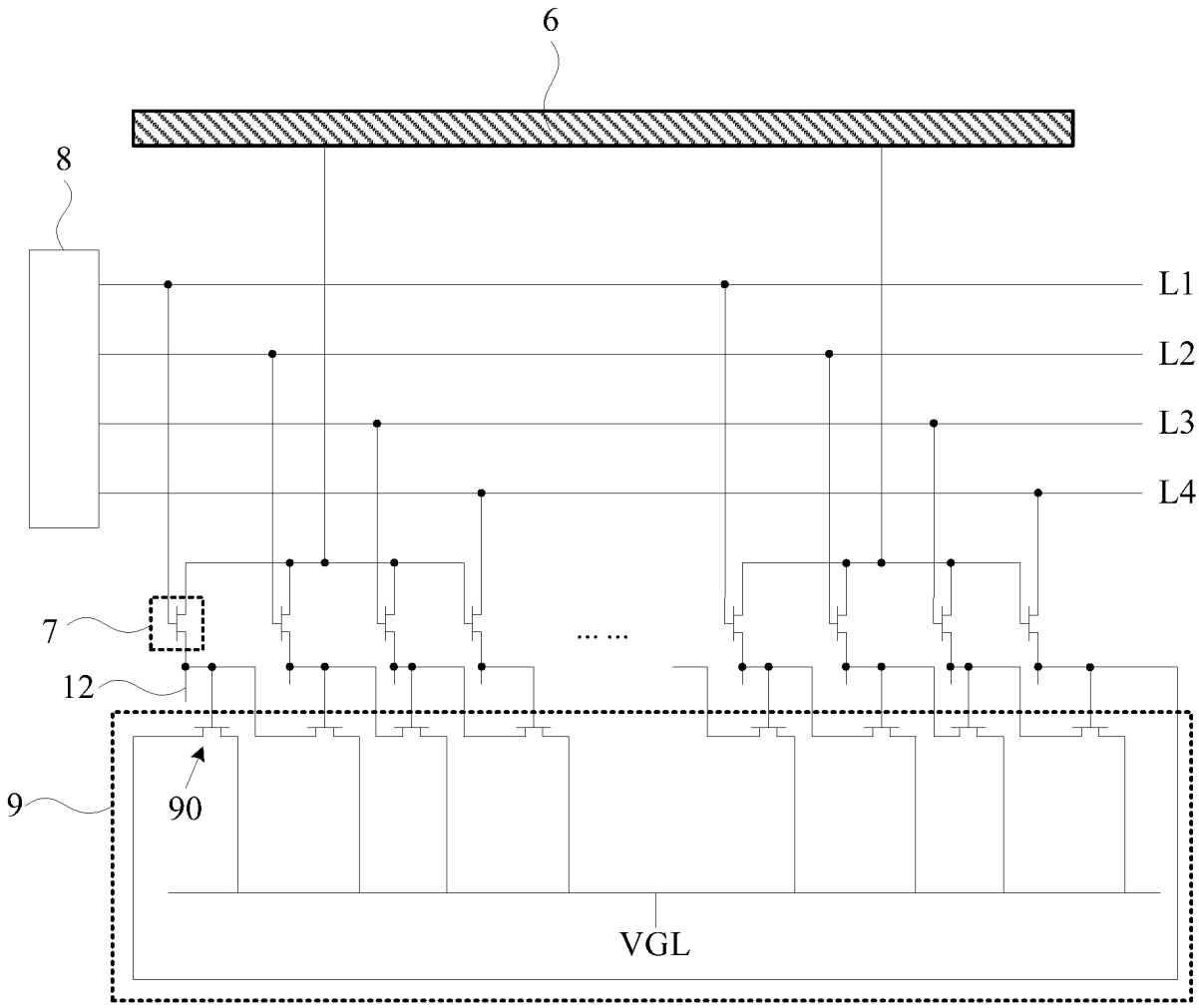

FIG. 7

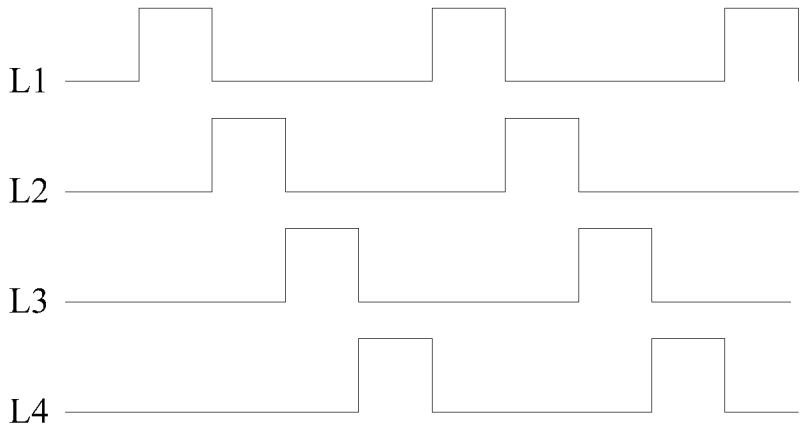

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2018/091025

A. CLASSIFICATION OF SUBJECT MATTER

G02F 1/1345(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI,CNPAT,EPODOC,WPI: BOE,display+,LCD?,circuit?,IC?,PCB?,PWB?,driv+,sid+, lateral,flank,edge,periphery, peripheries,peripheral,slim,narrow+ 1d boarder?, frame?,bezel

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP H08334740 A (MATSUSHITA ELECTRIC IND. CO., LTD.) 17 December 1996 (1996-12-17) description, paragraphs [0013]-[0024] and figures 1-3	1-12
PX	CN 107632474 A (BOE TECHNOLOGY GROUP CO., LTD. ET AL.) 26 January 2018 (2018-01-26) description, paragraphs [0043]-[0085] and figures 1-8	1-12
A	US 2007200993 A1 (SANYO EPSON IMAGING DEVICES CO.) 30 August 2007 (2007-08-30) the whole document	1-12
A	CN 105206232 A (KUNSHAN LONGTENG PHOTOELECTRICITY LTD.) 30 December 2015 (2015-12-30) the whole document	1-12
A	CN 104409037 A (XIAMEN TIANMA MICRO ELECTRONICS CO., LTD. ET AL.) 11 March 2015 (2015-03-11) the whole document	1-12

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 August 2018	**31 August 2018**

Name and mailing address of the ISA/CN	Authorized officer
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Facsimile No. **(86-10)62019451**	Telephone No. **86-(10)-53962360**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2018/091025

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
JP	H08334740	A	17 December 1996	None			
CN	107632474	A	26 January 2018	None			
US	2007200993	A1	30 August 2007	JP	4725358	B2	13 July 2011
				US	8031314	B2	04 October 2011
				JP	2007225953	A	06 September 2007
CN	105206232	A	30 December 2015	None			
CN	104409037	A	11 March 2015	CN	104409037	B	28 July 2017