Abstract: An apparatus includes a first interconnect and a first barrier structure. The first barrier structure is in contact with a dielectric material. The apparatus further includes a first protective structure in contact with the first barrier structure and an etch stop layer. An airgap is defined at least in part by the first protective structure and the etch stop layer.
SEMICONDUCTOR DEVICE HAVING AN AIRGAP DEFINED AT LEAST PARTIALLY BY A PROTECTIVE STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATIONS
[0001] The present application claims priority from commonly owned U.S. Non-Provisional Patent Application No. 14/444,104 filed on July 28, 2014, the contents of which are expressly incorporated herein by reference in their entirety.

FIELD
[0002] The present disclosure is generally related to a semiconductor device having an airgap defined at least partially by a protective structure.

DESCRIPTION OF RELATED ART
[0003] Advances in technology have resulted in smaller apparatuses and more powerful computing devices. For example, there currently exist a variety of portable personal computing devices, including wireless computing devices, such as portable wireless telephones, personal digital assistants (PDAs), and paging devices that are small, lightweight, and easily carried by users. More specifically, portable wireless telephones, such as cellular telephones and internet protocol (IP) telephones, can communicate voice and data packets over wireless networks. Further, many such wireless telephones include other types of devices that are incorporated therein. For example, a wireless telephone can also include a digital still camera, a digital video camera, a digital recorder, and an audio file player. Also, such wireless telephones can process executable instructions, including software applications, such as a web browser application, that can be used to access the Internet. As such, these wireless telephones can include significant computing capabilities.

[0004] Portable personal computing devices, such as wireless computing devices, may include multiple semiconductor devices. As a semiconductor device of the portable personal computing devices becomes smaller and more powerful, a capacitance (e.g., a parasitic capacitance) between interconnects of the semiconductor device may increase. To prevent the capacitance from interfering with the functioning of the semiconductor device, the semiconductor device may have an airgap defined between interconnects of a same layer. An etch process may be used as part of a formation of the airgap between two interconnects. However, the etch process may be destructive to (i.e., damage) the
interconnects. For example, the etch process may cause damage to a barrier structure (e.g., a barrier layer) or a conductive material of an interconnect.

SUMMARY
[0005] Techniques to form an airgap between multiple interconnects, where the airgap is defined at least in part by a protective structure coupled to one of the multiple interconnects are disclosed. The techniques include forming a trench in one or more layers of a semiconductor device, such as in one or more dielectric layers of the semiconductor device. A protective layer is formed (e.g., conformally deposited) in the trench prior to forming an interconnect in the trench. The protective layer may be in contact with a particular dielectric layer of the semiconductor device, such that the protective layer may protect the interconnect in the trench when the particular dielectric layer is etched. The interconnect may be formed in the trench such that the protective layer contacts an outer surface of the interconnect (e.g., a surface of a barrier layer of the interconnect).

[0006] After the interconnect is formed in the trench, an etch process may be performed to remove the particular dielectric layer. For example, the particular dielectric layer may be removed to establish a cavity between the interconnect (coupled to the protective layer) and another interconnect. The protective layer protects the interconnect from damage caused by the etch process used to remove the particular dielectric material. An etch stop layer may be deposited (e.g., non-conformally deposited) on the interconnect and the other interconnect to close an opening of the cavity to establish an airgap. The airgap may be defined by the protective layer (e.g., a protective structure) and one or more other structures or layers of the semiconductor device, such as one or more etch stop layers and/or another protective layer coupled to the other interconnect, as illustrative, non-limiting examples. By including the protective layer, the interconnect is protected during the etch process used to establish the cavity. As such, the semiconductor device may exhibit higher reliability as compared to semiconductor devices that do not include a protective layer.

[0007] In a particular embodiment, an apparatus includes a first interconnect. The first interconnect includes a first barrier structure. The first barrier structure is in contact with a dielectric material. The apparatus further includes a first protective structure in
contact with the first barrier structure and an etch stop layer. An airgap is defined at least in part by the first protective structure and the etch stop layer.

[0008] In another particular embodiment, a method includes depositing a protective layer in a trench. The method further includes etching the protective layer to define a first protective structure on a sidewall of the trench. The method also includes etching a dielectric material to expose an etch stop layer. A cavity is defined at least in part by the first protective structure and the etch stop layer.

[0009] In another particular embodiment, an apparatus includes means for resisting diffusion of a conductive material of an interconnect into a dielectric layer of a semiconductor device. The means for resisting the diffusion is in contact with the dielectric layer. The apparatus further includes means for defining an airgap. The means for defining is in contact with the means for resisting.

[0010] In another particular embodiment, a non-transitory computer-readable medium includes processor-executable instruction. The processor executable instructions, when executed by a processor, cause the processor to initiate formation of a semiconductor device. Forming the semiconductor device includes depositing a protective layer in a trench. Forming the semiconductor device further includes etching the protective layer to define a first protective structure on a sidewall of the trench. Forming the semiconductor device also includes etching a dielectric material to expose an etch stop layer. A cavity is defined at least in part by the first protective structure and the etch stop layer.

[0011] One particular advantage provided by at least one of the disclosed embodiments is reduced capacitance between interconnects (due to the airgap between the interconnects) while protecting one or more of the interconnects from degradation during an etch process performed as part of formation of the airgap as compared to devices that do not include a protective structure.

[0012] Other aspects, advantages, and features of the present disclosure will become apparent after review of the entire application, including the following sections: Brief Description of the Drawings, Detailed Description, and the Claims.
BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 is a diagram of a semiconductor device having an airgap defined at least partially by a protective structure;

[0014] FIG. 2 is a first illustrative diagram of at least one stage of a particular embodiment of a process of fabricating a semiconductor device having an airgap defined at least partially by a protective structure;

[0015] FIG. 3 is a second illustrative diagram of at least one stage of the particular embodiment of the process of fabricating the semiconductor device after performing a trenching operation;

[0016] FIG. 4 is a third illustrative diagram of at least one stage of the particular embodiment of the process of fabricating the semiconductor device after depositing a protective layer;

[0017] FIG. 5 is a fourth illustrative diagram of at least one stage of the particular embodiment of the process of fabricating the semiconductor device after an etch process;

[0018] FIG. 6 is a fifth illustrative diagram of at least one stage of the particular embodiment of the process of fabricating the semiconductor device after a deposition process;

[0019] FIG. 7 is a sixth illustrative diagram of at least one stage of the particular embodiment of the process of fabricating the semiconductor device after deposition of one or more conductive layers;

[0020] FIG. 8 is a seventh illustrative diagram of at least one stage of the particular embodiment of the process of fabricating the semiconductor device after a planarization operation;

[0021] FIG. 9 is an eighth illustrative diagram of at least one stage of the particular embodiment of the process of fabricating the semiconductor device after an etch process;

[0022] FIG. 10 is a ninth illustrative diagram of at least one stage of the particular embodiment of the process of fabricating the semiconductor device after deposition of an etch stop layer;
[0023] FIG. 11 is a flow diagram of an illustrative embodiment of a method of forming a semiconductor device having an airgap defined at least partially by a protective structure;

[0024] FIG. 12 is a block diagram of a device including the semiconductor device of FIG. 1; and

[0025] FIG. 13 is a data flow diagram of an illustrative embodiment of a manufacturing process to fabricate a device including the semiconductor device of FIG. 1.

DETAILED DESCRIPTION

[0026] Particular embodiments of the present disclosure are described below with reference to the drawings. In the description, common features are designated by common reference numbers.

[0027] Referring to FIG. 1, a diagram of a semiconductor device 100 having an airgap defined at least in part by a protective structure is shown. The semiconductor device 100 includes multiple layers and/or materials. For example, the semiconductor device 100 may include an etch stop layer 108, an airgap etch stop layer 104, and a dielectric material 102. The semiconductor device 100 may further include a first portion 120 (e.g., a first region) and a second portion 150 (e.g., a second region).

[0028] The semiconductor device 100 may include one or more conductive structures, such as one or more interconnects that electrically couple multiple devices of the semiconductor device 100, such as by routing power/signals to and from the multiple devices. For example, the first portion 120 of the semiconductor device 100 may include a first interconnect 130 that includes a conductive structure 136 (e.g., a conductive material), a liner structure 134 (e.g., a liner layer), and a barrier structure 132 (e.g., a barrier layer), as illustrative non-limiting examples. The liner structure 134 may be positioned between the barrier structure 132 and the conductive structure 136. In some embodiments, the first interconnect 130 may include additional structures/layers, such as one or more additional conductive structures, one or more additional liner structures, one or more additional barrier structures, one or more buffer structures, one or more spacer structures, or any combination thereof.

[0029] The second portion 150 of the semiconductor device 100 may include a second interconnect 160 that includes a second conductive structure 166, a second liner
The first interconnect 130 may be coupled to a first contact 110 and the second interconnect 160 may be coupled to a second contact 140.

[0030] One or more protective structures may be coupled to the first interconnect 130. For example, a protective structure 122 and a protective structure 124 may be coupled to the first interconnect 130. To illustrate, the protective structures 122, 124 may be coupled to (e.g., touching) an outer structure, such as an outer layer, of the first interconnect 130. The outer structure of the first interconnect 130 may include the barrier structure 132. The protective structure 122 may be coupled to a first portion of the barrier structure 132 and the protective structure 124 may be coupled to a second portion of the barrier structure 132. The first portion and/or the second portion of the barrier structure 132 may correspond to or be associated with sidewall portions of the barrier structure 132. For example, the first portion may correspond to a surrounding sidewall of a line portion of the first interconnect 130, such as within a metal layer, and the second portion may correspond to a surrounding sidewall of a via portion of the first interconnect 130, such as within an interlayer dielectric.

[0031] One or more protective structures may be coupled to an outer structure (e.g., an outer layer) of the second interconnect 160. For example, the outer structure of the second interconnect 160 may include the second barrier structure 162. A protective structure 152 may be coupled to a first portion of the barrier structure 162 and a protective structure 154 may be coupled to a second portion of the second barrier structure 162.

[0032] The first barrier structure 132 and/or the second barrier structure 162 may be in contact with the dielectric material 102. For example, a particular portion of the first barrier structure 132 may be in contact with a horizontal surface of the dielectric material 102. The particular portion of the first barrier structure 132 may be located between the first portion of the first barrier structure 132 in contact with the protective structure 122 and the second portion the first barrier structure 132 in contact with protective structure 124. A particular portion of the second barrier structure 162 may be in contact with another horizontal surface of the dielectric material 102. The particular portion of the second barrier structure 162 may be located between the first portion of the second barrier structure 162 in contact with the protective structure 152 and the
second portion of the second barrier structure 162 in contact with the protective
structure 154.

[0033] The semiconductor device 100 may have an airgap 170 defined therein. For
example, as illustrated in FIG. 1, the airgap 170 may be defined by one or more of the
etch stop layer 108, the airgap etch stop layer 104 (e.g., an etch stop layer (ESL)), the
first protective structure 122, and the protective structure 152. Additionally, the airgap
170 may be defined by one or more other structures or layers of the semiconductor
device 100. For example, in some embodiments, the airgap 170 may be further defined
by a second dielectric layer, one or more additional etch stop layers, one or more
additional protective structures, etc. A capacitance between the first interconnect 130
and the second interconnect 160 (e.g., across the airgap) may be less than if a dielectric
material, instead the airgap 170, were positioned between the first interconnect 130 and
the second interconnect 160.

[0034] During operation of the semiconductor device 100, one or more electrical
charges (e.g., charges provided in response to an alternating current (AC) voltage or a
direct current (DC) voltage from a signal/power source) may be applied to the first
interconnect 130, the second interconnect 160, or both. For example, a charge may be
applied by a source, such as a signal/current source or a voltage source, at the first
contact 110 and/or at the second contact 140. A charge applied to the first contact 110
may pass through the first interconnect 130 to another circuit coupled to the first
interconnect 130. Likewise, a charge applied to the second contact 140 may pass
through the second interconnect 160 to another circuit coupled to the second
interconnect 160.

[0035] Although the semiconductor device 100 is depicted as having two interconnects
(e.g., the first interconnect 130 and the second interconnect 160), in other embodiments
the semiconductor device 100 may include more than two or less than two
interconnects. Likewise, in some embodiments, the semiconductor device 100 may
include multiple airgaps defined as described with reference to the airgap 170.
Although not shown in FIG. 1, the semiconductor device 100 may include one or more
additional layers and/or one or more additional structures. To illustrate, a seed layer
(e.g., a seed structure) may be positioned between the liner structure 134 and the
conductive structure 136, as an illustrative, non-limiting example. The seed layer and
the conductive structure 136 may be the same material, such as a conductive material (e.g., copper).

[0036] In some embodiments, the first interconnect 130 may not include the first barrier structure 132 and/or the first liner structure 134. For example, in an embodiment where the first interconnect 130 does not include the first barrier structure 132, the first liner structure 134 may be the outer structure (of the first interconnect 130) that is in contact with the protective structure 122, with the dielectric material 102, and with the protective structure 124. As another example, in an embodiment where the first interconnect 130 does not include the barrier structure 132 and the liner structure 134, the first conductive structure 136 may be in contact with the dielectric material 102.

Similarly, the second interconnect 160 may not include the second barrier structure 162 and/or the second liner structure 164. Alternatively or additionally, the first interconnect 130 and/or the second interconnect 160 may include one or more additional structures or layers. For example, the first interconnect 130 may include a buffer layer positioned between the first liner structure 134 and the first barrier structure 132. As another example, the buffer layer may be the outer structure of the first interconnect 130, such that the buffer layer is positioned between the protective structures 122, 124 and the first barrier structure 132. As another example, the first interconnect 130 may include one or more spacers located between the first barrier structure 132 and the protective structure 122 and/or between the first barrier structure 132 and the protective structure 124.

Similarly, the second interconnect 160 may include one or more buffer layers, one or more spacers, or a combination thereof. In each embodiment, one or more protective structures may at least in part define an airgap. For example, one or more protective structures may constitute a boundary of the airgap (in one or more directions). To illustrate, the protective structure 122 may at least partially define (e.g., constitute a boundary of) the airgap 170. The airgap 170 may be further defined (e.g., bounded) by the protective structure 152, the etch stop layer 108, and the airgap etch stop layer 104.

[0037] By defining (e.g., establishing) the airgap 170 at least in part by the protective structure 122, the semiconductor device 100 may have a reduced capacitance between the first interconnect 130 and/or the second interconnect 160 as compared to semiconductor devices that do not include the airgap 170, such as semiconductor devices that have a dielectric material positioned between interconnects instead of an
airgap. The protective structure 122 may protect the first interconnect 130 during the formation of the airgap 170, thereby increasing reliability of the first interconnect 130 and increasing a yield count associated with the semiconductor device as compared to semiconductor devices that do not include a protective structure.

[0038] Referring to FIG. 2, a first illustrative diagram of at least one stage of a process of fabricating a semiconductor device having an airgap defined at least in part by a protective structure is depicted and generally designated 200. The semiconductor device may correspond to the semiconductor device 100 of FIG. 1. The semiconductor device is depicted after deposition of a first dielectric material 202 (e.g., a first dielectric layer), deposition of an airgap etch stop layer 204, deposition of a second dielectric 206 (e.g., a second dielectric layer), and deposition of a hardmask 212 (e.g., titanium nitride (TiN)). The first dielectric material 202 and the airgap etch stop layer 204 (e.g., an etch stop layer (ESL)) may correspond to the dielectric material 102 and the airgap etch stop layer 104 of FIG. 1, respectively.

[0039] The first dielectric material 202 may be a same material as or a different material than the second dielectric material 206. For example, one or both of the first dielectric material 202 and the second dielectric material 206 may include an oxide material, a low k dielectric material, or a combination thereof.

[0040] The airgap etch stop layer 204 may include one or more materials resistive to an etch process. For example, the airgap etch stop layer 204 may include silicon nitride (SiN), silicon carbon nitride (SiCN), silicon carbide (SiC), another protective material (e.g., resistant to the etch process used to etch the second dielectric material 206), or any combination thereof. In a particular embodiment, a thickness of the airgap etch stop layer 204 is less than 10 nanometers.

[0041] The semiconductor device may include a first portion 220 (e.g., a first region) and a second portion 250 (e.g., a second region). For example, the first portion 220 and the second portion 250 may correspond to the first portion 120 and the second portion 150 of FIG. 1, respectively. The first portion 220 may be associated with a first interconnect and the second portion 250 may be associated with a second interconnect. The formation of the first interconnect and the second interconnect are described further with reference to FIGS. 3-8. The first portion 220 may include a contact 210 and the second portion 250 of the semiconductor device may include a second contact 240. The
contact 210 and the second contact 240 may correspond to the first contact 110 and the second contact 140 of FIG. 1, respectively. The contacts 210, 240 may be coupled to one or more structures of another layer, such as a lower layer (not shown), of the semiconductor device or may be used to couple the semiconductor device to another device. In some embodiments, the contacts 210, 240 may be included in a metal layer (Mx), and the first dielectric material 202 is positioned on the metal layer (Mx). Although the contacts 210, 240 are depicted as internal to the first dielectric material 202, the contacts may be external to the first dielectric material 202 in other embodiments. The contacts 210, 240 may include a conductive material, such as a metal (e.g., copper or aluminum), another conductive material, such as a metal alloy, or any combination thereof, as illustrative, non-limiting examples. Although two contacts are illustrated in FIG. 2, the semiconductor device 200 may include more than or less than two contacts. After the first dielectric material 202, the airgap etch stop layer 204, the second dielectric material 206, and the hardmask 212 are deposited, a trenching operation may be applied to one or more of the layers of the semiconductor device to form one or more trenches.

[0042] Referring to FIG. 3, a second illustrative diagram of at least one stage of the process of fabricating the semiconductor device after performing a trenching operation is depicted and generally designated 300. The trenching operation may form one or more trenches. For example, the trenching operation may form a first trench 372 in the first portion 220 of the semiconductor device and a second trench 374 in the second portion 250 of the semiconductor device. The first trench 372 may expose a surface of the first contact 210 and the second trench 374 may expose a surface of the second contact 240. The trenching operation may include one or more etch operations to remove portions of the hardmask 212, the second dielectric material 206, the airgap etch stop layer 204, and the first dielectric material 202 to form the first trench 372 and the second trench 374. The trenching operation may be performed as part of a damascene process, such as a dual damascene process. For example, the trenching operation may be performed as part of a process to form a via in the first dielectric material 202, a conductive line (e.g., a metal line, such as a copper line) in the second dielectric material 206, or both.
Referring to FIG. 4, a third illustrative diagram of at least one stage of the process of fabricating the semiconductor device, after depositing a protective layer is depicted and generally designated 400. A protective layer 476 may be deposited (e.g., conformally deposited) on exposed structures (e.g., exposed surfaces) of the semiconductor device. For example, the protective layer 476 may be deposited on exposed portions (e.g., sidewalls and horizontal surfaces) of the hardmask 212, of the second dielectric material 206, of the airgap etch stop layer 204, and of the first dielectric 202. The protective layer 476 may include or be associated with the protective structures 122, 124, 152, 154 of FIG. 1.

The protective layer 476 may include silicon nitride (SiN), silicon carbon nitride (SiCN), silicon carbide (SiC), another protective material (e.g., a material resistive to the etch process), or any combination thereof, as illustrative, non-limiting examples. For example, the protective layer 476 may be resistive to an etch process performed to remove the second dielectric material 206, as described further herein.

Referring to FIG. 5, a fourth illustrative diagram of at least one stage of the process of fabricating the semiconductor device, after performing an etch process, is depicted and generally designated 500. The semiconductor device may include one or more protective structures. For example, the semiconductor device may include a protective structure 522 on a first portion (e.g., a sidewall) of the first trench 372, a protective structure 524 on a second portion of the first trench 372, a protective structure 552 on a first portion of the second trench 374, and a protective structure 554 on a second portion of the second trench 374. The protective structures 522-554 may correspond to the protective layer 476 of FIG. 4 after the etch process has been performed.

The etch process may have removed horizontal portions (e.g., horizontally exposed surfaces, such as lateral surfaces) of the protective layer 476. For example, the etch process may have included a directional etch process used to remove a first portion of the protective layer 476 to expose a horizontal surface 580 of the hardmask 212, to remove a second portion of the protective layer 476 to expose a first horizontal surface 582 of the first dielectric material 202, and to remove a third portion of the protective layer 476 to expose a horizontal surface 584 of the first contact 210. Removal of the first portion, the second portion, and the third portion of the protective layer 476 defines
the protective structure 522 and the protective structure 524. The directional etch process may further include removal of a fourth portion of the protective layer 476 to expose a second horizontal surface 586 of the first dielectric material 202 and removal of a fifth portion of the protective layer 476 to expose a horizontal surface 588 of the second contact 240. Removal of the fourth portion and the fifth portion of the protective layer 476 may include the protective structure 552 and the protective structure 554. The protective structures 522, 524, 552, 554 may correspond to the protective structures 122, 124, 152, 154 of FIG. 1. In a particular embodiment, the etch process used to etch the protective layer 476 may be an anisotropic etch process.

[0047] Referring to FIG. 6, a fifth illustrative diagram of at least one stage of the process of fabricating the semiconductor device, after performing one or more deposition processes, is depicted and generally designated 600. As illustrated in FIG. 6, a barrier material may be deposited on the semiconductor device to form a barrier layer 678. A liner material may be deposited on the barrier layer 678 to form a liner 680 (e.g., a liner layer). For example, the liner 680 may include or may be associated with the liner structures 134, 164 of FIG. 1.

[0048] The barrier layer 678 may be in contact with the one or more protective structures 522, 524, 552, 554, the first dielectric material 202, and the hardmask 212. The barrier layer 678 may resist diffusion of a conductive material (described herein with reference to FIG. 7) into a dielectric layer. The barrier layer 678 may include tantalum (Ta), titanium nitride (TiN), another material to prevent diffusion of a conductive material, or any combination thereof. Although FIG. 6 shows the barrier layer 678 in contact with the one or more protective structures 522, 524, 552, 554, in other embodiments, one or more additional structures and/or layers may be positioned between the barrier layer 678 and the one or more protective structures 522, 524, 552, 554. For example, one or more buffer layers may be formed between one or more of the protective structures 522, 524, 552, 554 and the barrier layer 678. As an additional example, one or more spacers (e.g., separating structures, passivation structures, etc.) may be formed between one or more of the protective structures 522, 524, 552, 554 and the barrier layer 678.

[0049] The liner 680 may include a material, such as tantalum (Ta), as an illustrative, non-limiting example. Although FIG. 6 shows the liner 680 in contact with the barrier
layer 678, in other embodiments, one or more additional structures and/or layers (e.g., a buffer layer, a spacer, etc.) may be positioned between the liner 680 and the barrier layer 678.

[0050] Referring to FIG. 7, a sixth illustrative diagram of at least one stage of the process of fabricating the semiconductor device, after deposition of one or more conductive layers, is depicted and generally designated 700. As illustrated in FIG. 7, one or more conductive materials may be deposited on the liner 680 to form a conductive layer 736. To illustrate, the conductive material may be deposited in the first trench 372 and in the second trench 374. The conductive material may fill the trenches 372, 374. The barrier layer 678 of FIG. 6 may protect the protective structures 522, 524, 552, 554 and/or the dielectric material 202 from diffusion of the conductive material. In a particular embodiment, the conductive layer 736 includes a metal and may be deposited using an electroplating process. The electroplating process may be facilitated by a seed layer deposited at least on one or more exposed surfaces of the first trench 372 and/or one or more exposed surfaces of the second trench 274. For example, the seed layer may be deposited on the liner 680. The seed layer may include a material that attracts a material of the conductive layer 736 under electroplating conditions. The seed layer and the conductive layer 736 may include a same material or a different material. For example, the conductive layer 736 and/or the seed layer may include a metal (e.g., aluminum or copper), a metal alloy, another conductive material, or any combination thereof. In a particular embodiment, the conductive layer 736 and the seed layer include copper.

[0051] Although FIG. 7 depicts the barrier layer 678 and the liner 680 as being positioned between the conductive layer 732 and the first contact 210, in other embodiments, an additional operation (e.g., an etch or a punch through) may be performed before deposition of the conductive layer 736, such that the conductive layer 736 (and/or the seed layer) may be in contact with the first contact 210. Similarly, the additional operation may be performed such that the conductive layer 736 (and/or the seed layer) may be in contact with the second contact 240.

[0052] Referring to FIG. 8, a seventh illustrative diagram of at least one stage of the process of fabricating the semiconductor device, after performance of a planarization operation, is depicted and generally designated 800. The planarization operation, such
as a chemical mechanical planarization (CMP) process, may remove one or more portions of the hardmask 212, the second dielectric 206, the barrier layer 678, the liner 680 of FIG. 6, and/or the conductive layer 736 of FIG. 7. The planarization operation may define a first interconnect 830 and a second interconnect 860. The first interconnect 830 may be associated with the first portion 220 of the semiconductor device and the second interconnect 860 may be associated with the second portion 250 of the semiconductor device. For example, the planarization operation may define a first barrier structure 832, a first liner structure 834, and a first conductive structure 836 associated with the first interconnect 830. As another example, the planarization operation may further define a second barrier structure 862, a second liner structure 864, and a second conductive structure 866 associated with the second interconnect 860.

[0053] Portions of the interconnects 830, 860 may be associated with vias and portions of the interconnects 830, 860 may be associated with a line (e.g., a trace), such as a metal line of the semiconductor device. For example, portions (e.g., lower/narrow portions) of the interconnects 830, 860 formed in the first dielectric material 202 may be associated with vias and portions (e.g., upper/wide portions) of the interconnects 830, 860 formed in the second dielectric material 206 may be associated with lines (e.g., metal lines). Although FIG. 8 depicts both the first interconnect 830 and the second interconnect 860 as having trace portions (upper/wide portions) and via portions (lower/narrow portions), in other embodiments, one or both of the first interconnect 830 or the second interconnect 860 may not include a via portion or may not include a line portion.

[0054] The first interconnect 830 may include or correspond to the first interconnect 130 of FIG. 1 and the second interconnect 860 may include or correspond to the second interconnect 160 of FIG. 1. To illustrate, the first barrier structure 832, the first liner structure 834, and the first conductive structure 836 may correspond to the first barrier structure 132, the first liner structure 134, and the first conductive structure 136, respectively, of FIG. 1. The second barrier structure 852, the second seed structure 854, and the second conductive structure 856 may correspond to the second barrier structure 162, the second liner structure 164, and the second conductive structure 156, respectively, of FIG. 1.
[0055] Referring to FIG. 9, an eighth illustrative diagram of at least one stage of the process of fabricating the semiconductor device, after performing one or more etch operations, is depicted and generally designated 900. The one or more etch operations may form a cavity 984 associated with an airgap, as described further herein. For example, during the one or more etch processes, a portion of the hardmask 212 and a portion of the second dielectric material 206 of FIG. 2 may be removed to form the cavity 984. The cavity 984 may be positioned between the first interconnect 830 and the second interconnect 860 and may include an opening 986. The cavity 984 may expose a portion (e.g., a sidewall) of the protective structure 522, a portion of the protective structure 552, and a portion (e.g., a horizontal surface) of the airgap etch stop layer 204.

[0056] During the one or more etch operations, the protective structures 522, 524, 552, 554 may protect the first interconnect 830 and the second interconnect 860, respectively, from damage (e.g., deterioration) caused by the etch process. For example, the protective structures 522, 524, 552, 554 may be resistant to the one or more etch operations used to remove the portion of the second dielectric material 206. The protective structure 522 may protect the first barrier structure 832 and the protective structure 552 may protect the second barrier structure 862 during the etch process. By protecting the first interconnect 830 and the second interconnect 860, reliability of the first interconnect 830 and the second interconnect 860 may be increased, thereby increasing a yield count associated with the semiconductor device as compared to semiconductor devices that do not include protective structures.

[0057] In some embodiments, the one or more etch operations may remove at least a portion of the airgap etch stop layer 204. Removal of the portion of the airgap etch stop layer 204 may also remove a portion of the first dielectric 202 and expose a surface of the first dielectric 202. The protective structures 522, 524, 552, 554 may be resistant to the one or more etch operations used to remove the portion of the airgap etch stop layer 204 and the portion of the first dielectric 202.

[0058] Referring to FIG. 10, a ninth illustrative diagram of at least one stage of the process of fabricating the semiconductor device, after deposition of an etch stop layer, is depicted and generally designated 900. As depicted in FIG. 10, an etch stop layer 1008 may be deposited (e.g., non-conformally deposited) on the semiconductor device to
form an airgap 1040. For example, the etch stop layer 1008 may seal the opening 986 of the cavity 984 of FIG. 9 to form the airgap 1040. Using an angled directional deposition process to deposit the etch stop layer 1008 in combination with a small size of the cavity 984 may prevent or reduce the amount of material of the etch stop layer 1008 that enters the cavity 984 during the deposition process, thereby forming the airgap 1040. The airgap 1040 may correspond to the airgap 170 of FIG. 1.

[0059] The etch stop layer 1008 may include a material that is resistant to one or more etch processes that may be applied to the semiconductor device. For example, the etch stop layer 1008 may be a low k layer and/or an etch stop layer. The etch stop layer 1008 may include silicon nitride (SiN), silicon carbon nitride (SiCN), silicon carbide (SiC), another material that is resistive to the one or more etch processes, or a combination thereof, as illustrative, non-limiting examples. Accordingly, the airgap 1040 may be at least partially defined by the protective structure 522, the airgap etch stop layer 204 (e.g., a first etch stop layer), the protective structure 552, the etch stop layer 1008 (e.g., a second etch stop layer), or a combination thereof. For example, the airgap 1040 may be bounded in three dimensions by components of the semiconductor device. The protective structure 522, the airgap etch stop layer 204, the protective structure 552, the etch stop layer 1008, another structure/layer of the semiconductor device, or a combination thereof may constitute at least a portion of the boundary of the airgap 1040. Although FIG. 10 depicts the etch stop layer 1008 as being in contact with the first interconnect 830 and the second interconnect 860, in some embodiments, a particular layer or a particular structure (e.g., a protection layer or a protection structure distinct from the protective layer 476 of FIG. 4 and distinct from the protective structures 522, 524, 552, 554 of FIG. 5), such as cobalt tungsten phosphide (CoWP) may be deposited over a surface of the first interconnect 830 and over a surface of the second interconnect 860 after the chemical mechanical planarization process described with reference to FIG. 7. The particular layer may be positioned between the etch stop layer 1008 and one or more of the first interconnect 830 and the second interconnect 860. In some embodiments, a portion of the particular layer may constitute at least a portion of the boundary of the airgap 1040.

[0060] The semiconductor device may advantageously include one or more of the protective structures 522, 524, 552, 554 that form a boundary of (e.g., define), at least in
part, the airgap 1040. The airgap 1040 may reduce a capacitance between the first interconnect 830 and the second interconnect 860 as compared to a semiconductor device that does not include an airgap (e.g., has a dielectric material) between interconnects. Additionally, one or more of the protective structures 522, 524, 552, 554 may protect the first interconnect 830 and the second interconnect 860 during formation of the airgap 1040, such as during an etch process to remove the second dielectric material 206.

[0061] Referring to FIG. 11, a flow diagram of an illustrative embodiment of a method 1100 of forming a semiconductor device having an airgap defined at least partially by a protective structure is depicted. For example, the semiconductor device may include the semiconductor device 100 of FIG. 1 or the semiconductor device formed according to the process described with reference to FIGS. 2-10. The airgap may include or correspond to the airgap 170 of FIG. 1 or the airgap 1040 of FIG. 10.

[0062] The method 1100 may include depositing a protective layer in a trench, at 1102. For example, referring to FIG. 4, the protective layer 476 may be deposited in the first trench 372.

[0063] The method 1100 may further include etching the protective layer to define a first protective structure on a sidewall of the trench, at 1104. The first protective structure may correspond to any of the protective structures 122, 124, 152, 154 of FIG. 1 and/or any of the protective structures 522, 524, 552, 554 of FIG. 5. For example, referring to FIG. 5, the protective structures 522, 524, 552, 554 may be defined by etching the protective layer 476 of FIG. 4. Etching the protective layer may include removing one or more portions of the protective layer. To illustrate, an anisotropic etch process may be used to remove the one or more portions of the protective layer.

[0064] The method 1100 may also include etching a dielectric material to expose a first etch stop layer, at 1106. The first etch stop layer may correspond to the airgap etch stop layer 104 of FIG. 1 and/or the airgap etch stop layer 204 of FIG. 2. A cavity may be defined at least in part by the first protective structure and the first etch stop layer. For example, referring to FIG. 9, the cavity 984 may be formed by etching the second dielectric material 206 of FIG. 8. Etching the second dielectric material 206 may expose the airgap etch stop layer 204. The cavity 984 may be defined at least in part by the protective structure 522 and the airgap etch stop layer 204. For example, the cavity may
be bounded at least in part by the protective structure 522 and the airgap etch stop layer 204.

[0065] The method 1100 may include depositing a second etch stop layer on the protective structure to close an opening of the cavity, at 1108. The second etch stop layer may correspond to the etch stop layer 108 of FIG. 1 and/or the etch stop layer 1008 of FIG. 1. For example, referring to FIG. 10, the etch stop layer 1008 may be deposited on the protective structure 522 to seal an opening (e.g., the opening 986 of the cavity 984 of FIG. 9). Closing the opening may define the airgap, such as the airgap 170 of FIG. 1 or the airgap 1040 of FIG. 10. Using an angled directional deposition process to deposit the second etch stop layer in combination with a small size of the cavity may prevent or reduce the amount of material of the second etch stop layer that enters the cavity during the deposition process, thereby forming the airgap.

[0066] The method 1100 may be used to define an airgap positioned between interconnects of a semiconductor device. The airgap may reduce a capacitance between the interconnects. Additionally, the airgap may be defined at least partially by a protective structure, such as the first protective structure. The protective structure may protect one or more of the interconnects during formation of the airgap, such as protecting an interconnect during etching of the dielectric material to expose the first etch stop layer.

[0067] The method of FIG. 11 may be implemented by a processing unit such as a central processing unit (CPU), a controller, a field-programmable gate array (FPGA) device, an application-specific integrated circuit (ASIC), a digital signal processor (DSP), another hardware device, firmware device, or any combination thereof. As an example, the method of FIG. 11 can be performed by one or more processors that execute instructions to control fabrication equipment.

[0068] In conjunction with one or more of the described embodiments of FIGS. 1-11, an apparatus is disclosed that may include means (e.g., a barrier layer) for resisting diffusion of a conductive material of an interconnect into a dielectric layer of a semiconductor device. The means for resisting diffusion may be in contact with the dielectric layer. The means for resisting diffusion may correspond to the first barrier structure 132 of FIG. 1, the second barrier structure 162 of FIG. 1, the first barrier
structure 832 of FIGS. 8-10, the second barrier structure 862 of FIGS. 8-10, one or more other structures configured to resist diffusion, or any combination thereof.

[0069] The apparatus may also include means for defining an airgap. The means for defining an airgap may be in contact with the means for resisting. The means for defining an airgap may correspond to the protective structure 122, the airgap etch stop layer 104, the etch stop layer 108, the protective structure 152 of FIG. 1, the airgap etch stop layer 204 of FIGS. 2-10, the protective structure 522, the protective structure 552 of FIGS. 5-10, the etch stop layer 1008 of FIG. 10, one or more other structures configured to define an airgap, or any combination thereof.

[0070] In conjunction with the described embodiments of FIGS. 1-11, a method is disclosed that may include a first step for depositing a protective layer in a trench. The first step may correspond to the process described with reference to FIG. 4, to the method 1100 of FIG. 11 at 1102, to one or more other processes configured to deposit a protective layer in a trench, or any combination thereof.

[0071] The method may also include a second step for etching the protective layer to define a first protective structure on a sidewall of the trench. The second step may correspond to the process described with reference to FIG. 5, to the method 1100 of FIG. 11 at 1104, to one or more other processes configured to etch a protective layer to define a protective structure on a sidewall of a trench, or any combination thereof.

[0072] The method may also include a third step for etching a dielectric material to expose an etch stop layer. The third step may correspond to the process described with reference to FIG. 9, to the method 1100 of FIG. 11 at 1106, to one or more other processes configured to etch a dielectric material, or any combination thereof.

[0073] Referring to FIG. 12, a block diagram of a particular illustrative embodiment of an electronic device 1200, such as a wireless communication device is depicted. The electronic device 1200 may include the semiconductor device 100 of FIG. 1, a semiconductor device formed according to the process illustrated by FIGS. 2-10, a semiconductor device formed using the method of FIG. 11, or a combination thereof.

[0074] The electronic device 1200 includes a processor 1210, such as a digital signal processor (DSP), coupled to a memory 1232. The processor 1210 may include a semiconductor device 1264. For example, the semiconductor device 1264 may be the
semiconductor device 100 of FIG. 1, a semiconductor device formed according to the
process illustrated by FIGS. 2-10, a semiconductor device formed using the method of
FIG. 11, or a combination thereof. To illustrate, the processor 1210 may be constructed
in such a way that components of the processor 1210 may be electrically connected by
structures, such as the first interconnect 130 and/or the second interconnect 160 of FIG.
1. The processor 1210 may further be constructed in such a way that the processor 1210
includes one or more of the protective structures 122, 124, 152, 154. An airgap, such as
the airgap 170 of FIG. 1, may be positioned between components/structures of the
processor 1210, such as the first interconnect 130 and/or the second interconnect 160.

[0075] The memory 1232 includes instructions 1268 (e.g., executable instructions) such
as computer-readable instructions or processor-readable instructions. The instructions
1268 may include one or more instructions that are executable by a computer, such as
the processor 1210.

[0076] FIG. 12 also shows a display controller 1226 that is coupled to the processor
1210 and to a display 1228. A coder/decoder (CODEC) 1234 can also be coupled to the
processor 1210. A speaker 1236 and a microphone 1238 can be coupled to the CODEC
1234.

[0077] FIG. 12 also indicates that a wireless interface 1240, such as a wireless
controller, can be coupled to the processor 1210 and to an antenna 1242. In a particular
embodiment, the processor 1210, the display controller 1226, the memory 1232, the
CODEC 1234, and the wireless interface 1240 are included in a system-in-package or
system-on-chip device 1222. In a particular embodiment, an input device 1230 and a
power supply 1244 are coupled to the system-on-chip device 1222. Moreover, in a
particular embodiment, as illustrated in FIG. 12, the display 1228, the input device 1230,
the speaker 1236, the microphone 1238, the antenna 1242, and the power supply 1244
are external to the system-on-chip device 1222. However, each of the display 1228, the
input device 1230, the speaker 1236, the microphone 1238, the antenna 1242, and the
power supply 1244 can be coupled to a component of the system-on-chip device 1222,
such as an interface or a controller. Although the semiconductor device 1264 is
depicted as being included in the processor 1210, the semiconductor device 1264 may
be included in another component of the device 1200 or a component coupled to the
device 1200. For example, the semiconductor device 1264 may be included in the
memory 1232, the wireless interface 1240, the power supply 1244, the input device 1230, the display 1228, the display controller 1226, the CODEC 1234, the speaker 1236, or the microphone 1238. To illustrate, one or more of the components of the electronic device 1200 may include a semiconductor device that is constructed in such a way that components of the semiconductor device may be electrically connected by structures/interconnects (e.g., corresponding to the first interconnect 130 of FIG. 1 and/or to the second interconnect 160). The interconnects may be used to route power/signals between circuits of the semiconductor device. The interconnects may be separated by an airgap (e.g., the airgap 170 of FIG. 1) and may be protected by one or more protective structures (e.g., the protective structure 522 and/or the protective structure 552).

[0078] One or more of the disclosed embodiments may be implemented in a system or an apparatus, such as the electronic device 1200, that may include a communications device, a fixed location data unit, a mobile location data unit, a mobile phone, a cellular phone, a satellite phone, a computer, a tablet, a portable computer, or a desktop computer. Alternatively or additionally, the electronic device 1200 may include a set-top box, an entertainment unit, a navigation device, a personal digital assistant (PDA), a monitor, a computer monitor, a television, a tuner, a radio, a satellite radio, a music player, a digital music player, a portable music player, a video player, a digital video player, a digital video disc (DVD) player, a portable digital video player, any other device that stores or retrieves data or computer instructions, or a combination thereof.

As another illustrative, non-limiting example, the system or the apparatus may include remote units, such as hand-held personal communication systems (PCS) units, portable data units such as global positioning system (GPS) enabled devices, meter reading equipment, or any other device that stores or retrieves data or computer instructions, or any combination thereof.

[0079] The foregoing disclosed devices and functionalities may be designed and configured into computer files (e.g. RTL, GDSII, GERBER, etc.) stored on computer-readable media. Some or all such files may be provided to fabrication handlers who fabricate devices based on such files. Resulting products include semiconductor wafers that are then cut into semiconductor die and packaged into a semiconductor chip. The
chips are then employed in devices described above. FIG. 13 depicts a particular
illustrative embodiment of an electronic device manufacturing process 1300.

[0080] Physical device information 1302 is received at the manufacturing process 1300,
such as at a research computer 1306. The physical device information 1302 may
include design information representing at least one physical property of a
semiconductor device, such as the semiconductor device 100 of FIG. 1, a semiconductor
device formed according to the process illustrated by FIGS. 2-10, a semiconductor
device formed using the method of FIG. 11, or a combination thereof. For example, the
physical device information 1302 may include physical parameters, material
characteristics, and structure information that is entered via a user interface 1304
coupled to the research computer 1306. The research computer 1306 includes a
processor 1308, such as one or more processing cores, coupled to a computer-readable
medium (e.g., a non-transitory computer-readable medium), such as a memory 1310.
The memory 1310 may store computer-readable instructions that are executable to cause
the processor 1308 to transform the physical device information 1302 to comply with a
file format and to generate a library file 1312.

[0081] In a particular embodiment, the library file 1312 includes at least one data file
including the transformed design information. For example, the library file 1312 may
include a library of semiconductor devices including a device that includes the
semiconductor device 100 of FIG. 1, a semiconductor device formed according to the
process illustrated by FIGS. 2-10, a semiconductor device formed using the method of
FIG. 11, or a combination thereof, that is provided for use with an electronic design
automation (EDA) tool 1320.

[0082] The library file 1312 may be used in conjunction with the EDA tool 1320 at a
design computer 1314 including a processor 1316, such as one or more processing
cores, coupled to a memory 1318. The EDA tool 1320 may be stored as processor
executable instructions at the memory 1318 to enable a user of the design computer
1314 to design a circuit including the semiconductor device 100 of FIG. 1, a
semiconductor device formed according to the process illustrated by FIGS. 2-10, a
semiconductor device formed using the method of FIG. 11, or a combination thereof.
For example, a user of the design computer 1314 may enter circuit design information
1322 via a user interface 1324 coupled to the design computer 1314. The circuit design
information 1322 may include design information representing at least one physical property of a semiconductor device, such as the semiconductor device 100 of FIG. 1, a semiconductor device formed according to the process illustrated by FIGS. 2-10, a semiconductor device formed using the method of FIG. 11, or a combination thereof. To illustrate, the circuit design property may include identification of particular circuits and relationships to other elements in a circuit design, positioning information, feature size information, interconnection information, or other information representing a physical property of a semiconductor device.

[0083] The design computer 1314 may be configured to transform the design information, including the circuit design information 1322, to comply with a file format. To illustrate, the file format may include a database binary file format representing planar geometric shapes, text labels, and other information about a circuit layout in a hierarchical format, such as a Graphic Data System (GDSII) file format. The design computer 1314 may be configured to generate a data file including the transformed design information, such as a GDSII file 1326 that includes information describing the semiconductor device 100 of FIG. 1, a semiconductor device formed according to the process illustrated by FIGS. 2-10, a semiconductor device formed using the method of FIG. 11, or a combination thereof, in addition to other circuits or information. To illustrate, the data file may include information corresponding to a system-on-chip (SOC) that includes the semiconductor device 100 of FIG. 1, a semiconductor device formed according to the process illustrated by FIGS. 2-10, a semiconductor device formed using the method of FIG. 11, or a combination thereof, and that also includes additional electronic circuits and components within the SOC.

[0084] The GDSII file 1326 may be received at a fabrication process 1328 to manufacture the semiconductor device 100 of FIG. 1, a semiconductor device formed according to the process illustrated by FIGS. 2-10, a semiconductor device formed using the method of FIG. 11, or a combination thereof, according to transformed information in the GDSII file 1326. For example, a device manufacture process may include providing the GDSII file 1326 to a mask manufacturer 1330 to create one or more masks, such as masks to be used with photolithography processing, illustrated as a representative mask 1332. The mask 1332 may be used during the fabrication process to generate one or more wafers 1333, which may be tested and separated into dies, such
as a representative die 1336. The die 1336 includes a circuit including a device that includes the semiconductor device 100 of FIG. 1, a semiconductor device formed according to the process illustrated by FIGS. 2-10, a semiconductor device formed using the method of FIG. 11, or a combination thereof. To illustrate, the first interconnect 130 and one or more of the protective structures 122, 124, 152, 154 may be integrated into the die 1336.

[0085] For example, the fabrication process 1328 may include a processor 1334 and a memory 1335 to initiate and/or control the fabrication process 1328. The memory 1335 may include executable instructions such as computer-readable instructions or processor-readable instructions. The executable instructions may include one or more instructions that are executable by a computer such as the processor 1334.

[0086] The fabrication process 1328 may be implemented by a fabrication system that is fully automated or partially automated. For example, the fabrication process 1328 may be automated according to a schedule. The fabrication system may include fabrication equipment (e.g., processing tools) to perform one or more operations to form a semiconductor device. For example, the fabrication equipment may be configured to deposit one or more materials, etch one or more protective materials, etch one or more dielectric materials, etch one or more etch stop layers, perform a chemical mechanical planarization process, etc.

[0087] The fabrication system (e.g., an automated system that performs the fabrication process 1328) may have a distributed architecture (e.g., a hierarchy). For example, the fabrication system may include one or more processors, such as the processor 1334, one or more memories, such as the memory 1335, and/or controllers that are distributed according to the distributed architecture. The distributed architecture may include a high-level processor that controls or initiates operations of one or more low-level systems. For example, a high-level portion of the fabrication process 1328 may include one or more processors, such as the processor 1334, and the low-level systems may each include or may be controlled by one or more corresponding controllers. A particular controller of a particular low-level system may receive one or more instructions (e.g., commands) from a particular high-level system, may issue sub-commands to subordinate modules or process tools, and may communicate status data back to the particular high-level. Each of the one or more low-level systems may be associated
with one or more corresponding pieces of fabrication equipment (e.g., processing tools). 
In a particular embodiment, the fabrication system may include multiple processors that 
are distributed in the fabrication system. For example, a controller of a low-level 
system component may include a processor, such as the processor 1334.

[0088] Alternatively, the processor 1334 may be a part of a high-level system, 
subsystem, or component of the fabrication system. In another embodiment, the 
processor 1334 includes distributed processing at various levels and components of a 
fabrication system.

[0089] Thus, the processor 1334 may include processor-executable instructions that, 
when executed by the processor 1334, cause the processor 1334 to initiate or control 
formation of a semiconductor device, the semiconductor device formed by depositing a 
protective layer in a trench, etching the protective layer to define a first protective 
structure on a sidewall of the trench, and etching a dielectric material to expose an etch stop layer.

[0090] The executable instructions included in the memory 1335 may enable the 
processor 1334 to initiate formation of a semiconductor device such as the 
semiconductor device 100 of FIG. 1, a semiconductor device formed according to the 
process illustrated by FIGS. 2-10, a semiconductor device formed using the method of 
FIG. 11, or a combination thereof. In a particular embodiment, the memory 1335 is a 
non-transient computer-readable medium storing computer-executable instructions that 
are executable by the processor 1334 to cause the processor 1334 to initiate formation of a 
semiconductor device in accordance with at least a portion of any of the processes 
illustrated FIGS. 2-10, at least a portion of the method of FIG. 11, or any combination 
thereof. For example, the computer executable instructions may be executable to cause the processor 1334 to initiate formation of the semiconductor device, such as the 
semiconductor device 100 of FIG. 1. The semiconductor device may be formed by 
depositing a protective layer in a trench, etching the protective layer to define a first 
protective structure on a sidewall of the trench, and etching a dielectric material to expose an etch stop layer.

[0091] As an illustrative example, the processor 1334 may initiate or control a first step 
for depositing a protective layer in a trench. For example, the processor 1334 may be 
embedded in or coupled to one or more controllers that control one or more pieces of
fabrication equipment to perform the first step for depositing a protective layer in a
trench. The processor 1334 may control the first step for depositing a protective layer in
a trench by controlling one or more processes as described by the method 1100 of FIG. 11 at 1102, by one or more other processes configured to deposit a protective layer in a
trench, or any combination thereof.

[0092] The processor 1334 may also control a second step for etching the protective
layer to define a first protective structure on a sidewall of the trench. For example, the
processor 1334 may be embedded in or coupled to one or more controllers that control
one or more pieces of fabrication equipment to perform the second step for etching the
protective layer to define a first protective structure on a sidewall of the trench. The
processor 1334 may control the second step perform the second step for etching the
protective layer to define a first protective structure on a sidewall of the trench by
controlling one or more processes as described by the method 1100 of FIG. 11 at 1104,
by one or more other processes configured to etch a protective layer to define a
protective structure on a sidewall of a trench, or any combination thereof.

[0093] The processor 1334 may also control a third step for etching a dielectric material
to expose an etch stop layer. For example, the processor 1334 may be embedded in or
coupled to one or more controllers that control one or more pieces of fabrication
equipment to perform the third step for etching a dielectric material to expose an etch
stop layer. The processor 1334 may control the third step for etching a dielectric
material to expose an etch stop layer by controlling one or more processes as described
by the method 1100 of FIG. 11 at 1106, by one or more other processes configured to
etch a dielectric material, or any combination thereof.

[0094] The die 1336 may be provided to a packaging process 1338 where the die 1336
is incorporated into a representative package 1340. For example, the package 1340 may
include the single die 1336 or multiple dies, such as a system-in-package (SiP)
arrangement. The package 1340 may be configured to conform to one or more
standards or specifications, such as Joint Electron Device Engineering Council (JEDEC)
standards.

[0095] Information regarding the package 1340 may be distributed to various product
designers, such as via a component library stored at a computer 1346. The computer
1346 may include a processor 1348, such as one or more processing cores, coupled to a
memory 1350. A printed circuit board (PCB) tool may be stored as processor executable instructions at the memory 1350 to process PCB design information 1342 received from a user of the computer 1346 via a user interface 1344. The PCB design information 1342 may include physical positioning information of a packaged semiconductor device on a circuit board, the packaged semiconductor device corresponding to the package 1340 including the semiconductor device 100 of FIG. 1, a semiconductor device formed according to the process illustrated by FIGS. 2-10, a semiconductor device formed using the method of FIG. 11, or a combination thereof.

[0096] The computer 3946 may be configured to transform the PCB design information 3942 to generate a data file, such as a GERBER file 3952 with data that includes physical positioning information of a packaged semiconductor device on a circuit board, as well as layout of electrical connections such as traces (e.g., metal lines) and vias, where the packaged semiconductor device corresponds to the package 3940 including the semiconductor device 100 of FIG. 1, a semiconductor device formed according to the process illustrated by FIGS. 2-10, a semiconductor device formed using the method of FIG. 11, or a combination thereof. In other embodiments, the data file generated by the transformed PCB design information may have a format other than a GERBER format.

[0097] The GERBER file 1352 may be received at a board assembly process 1354 and used to create PCBs, such as a representative PCB 1356, manufactured in accordance with the design information stored within the GERBER file 1352. For example, the GERBER file 1352 may be uploaded to one or more machines to perform various steps of a PCB production process. The PCB 1356 may be populated with electronic components including the package 1340 to form a representative printed circuit assembly (PCA) 1358.

[0098] The PCA 1358 may be received at a product manufacture process 1360 and integrated into one or more electronic devices, such as a first representative electronic device 1362 and a second representative electronic device 1364. For example, the first representative electronic device 1362, the second representative electronic device 1364, or both, may include or correspond to the wireless communication device 1200 of FIG. 12. As an illustrative, non-limiting example, the first representative electronic device 1362, the second representative electronic device 1364, or both, may include a
communications device, a fixed location data unit, a mobile location data unit, a mobile
phone, a cellular phone, a satellite phone, a computer, a tablet, a portable computer, or a
desktop computer. Alternatively or additionally, the first representative electronic
device 1362, the second representative electronic device 1364, or both, may include a
set top box, an entertainment unit, a navigation device, a personal digital assistant
(PDA), a monitor, a computer monitor, a television, a tuner, a radio, a satellite radio, a
music player, a digital music player, a portable music player, a video player, a digital
video player, a digital video disc (DVD) player, a portable digital video player, any
other device that stores or retrieves data or computer instructions, or a combination
thereof, into which the semiconductor device 100 of FIG. 1, a semiconductor device
formed according to the process illustrated by FIGS. 2-10, a semiconductor device
formed using the method of FIG. 11, or a combination thereof, is integrated. As another
illustrative, non-limiting example, one or more of the electronic devices 1362 and 1364
may include remote units, such as mobile phones, hand-held personal communication
systems (PCS) units, portable data units such as personal data assistants, global
positioning system (GPS) enabled devices, navigation devices, fixed location data units
such as meter reading equipment, or any other device that stores or retrieves data or
computer instructions, or any combination thereof. Although FIG. 13 illustrates remote
units according to teachings of the disclosure, the disclosure is not limited to these
illustrated units. Embodiments of the disclosure may be suitably employed in any
device which includes active integrated circuitry including memory and on-chip
circuitry.

[0099] A device that includes the semiconductor device 100 of FIG. 1, a semiconductor
device formed according to the process illustrated by FIGS. 2-10, a semiconductor
device formed using the method of FIG. 11, or a combination thereof, may be fabricated,
processed, and incorporated into an electronic device, as described in the illustrative
process 1300. One or more aspects of the embodiments disclosed with respect to FIGS.
1-13 may be included at various processing stages, such as within the library file 1312,
the GDSII file 1326 (e.g., a file having a GDSII format), and the GERBER file 1352
(e.g., a file having a GERBER format), as well as stored at the memory 1310 of the
research computer 1306, the memory 1318 of the design computer 1314, the memory
1350 of the computer 1346, the memory of one or more other computers or processors
(not shown) used at the various stages, such as at the board assembly process 1354, and
also incorporated into one or more other physical embodiments such as the mask 1332, the die 1336, the package 1340, the PCA 1358, other products such as prototype circuits or devices (not shown), or any combination thereof. Although various representative stages of production from a physical device design to a final product are depicted, in other embodiments fewer stages may be used or additional stages may be included. Similarly, the process 1300 may be performed by a single entity or by one or more entities performing various stages of the process 1300.

[00100] Although one or more of FIGS. 1-13 may illustrate systems, apparatuses, and/or methods according to the teachings of the disclosure, the disclosure is not limited to these illustrated systems, apparatuses, and/or methods. Embodiments of the disclosure may be suitably employed in any device that includes integrated circuitry including memory, a processor, and on-chip circuitry.

[00101] Although one or more of FIGS. 1-13 may illustrate systems, apparatuses, and/or methods according to the teachings of the disclosure, the disclosure is not limited to these illustrated systems, apparatuses, and/or methods. One or more functions or components of any of FIGS. 1-13 as illustrated or described herein may be combined with one or more other portions of another of FIGS. 1-13. Accordingly, no single embodiment described herein should be construed as limiting and embodiments of the disclosure may be suitably combined without departing form the teachings of the disclosure.

[00102] Those of skill would further appreciate that the various illustrative logical blocks, configurations, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software executed by a processor, or combinations of both. Various illustrative components, blocks, configurations, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or processor executable instructions depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present disclosure.
The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in random access memory (RAM), flash memory, read-only memory (ROM), programmable read-only memory (PROM), erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), registers, hard disk, a removable disk, a compact disc read-only memory (CD-ROM), or any other form of non-transient storage medium known in the art. For example, a storage medium may be coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an application-specific integrated circuit (ASIC). The ASIC may reside in a computing device or a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a computing device or user terminal.

The previous description of the disclosed embodiments is provided to enable a person skilled in the art to make or use the disclosed embodiments. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the principles defined herein may be applied to other embodiments without departing from the scope of the disclosure. Thus, the present disclosure is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope possible consistent with the principles and novel features as defined by the following claims.
CLAIMS:

1. An apparatus comprising:
a first interconnect comprising a first barrier structure, wherein the first barrier structure is in contact with a dielectric material; and
a first protective structure in contact with the first barrier structure and a first etch stop layer, wherein an airgap is defined at least in part by the first protective structure and the first etch stop layer.

2. The apparatus of claim 1, wherein the first interconnect further comprises a liner structure and a conductive structure, the liner structure in contact with the barrier structure, and wherein the conductive structure is in contact with the liner structure.

3. The apparatus of claim 2, wherein the conductive structure comprises copper (Cu).

4. The apparatus of claim 2, wherein the liner structure comprises tantalum (Ta).

5. The apparatus of claim 1, wherein a thickness of the first etch stop layer is less than 10 nanometers.

6. The apparatus of claim 1, wherein the first protective structure comprises silicon nitride (SiN), silicon carbon nitride (SiCN), silicon carbide (SiC), or a combination thereof.

7. The apparatus of claim 1, wherein the first barrier structure comprises tantalum (Ta), titanium nitride (TiN), or a combination thereof.

8. The apparatus of claim 1, further comprising:
a second interconnect, wherein the second interconnect includes a second conductive structure and a second barrier structure; and
a second protective structure in contact with the second barrier structure and in contact with the first etch stop layer.
9. The apparatus of claim 8, further comprising a second etch stop layer, wherein the airgap is further defined by the second protective structure and the second etch stop layer.

10. The apparatus of claim 1, further comprising:
a third protective structure in contact with the first barrier structure; and
a fourth protective structure in contact with a second barrier structure.

11. The apparatus of claim 1, wherein the first interconnect and the first protective structure are integrated into at least one semiconductor die.

12. The apparatus of claim 1, wherein the first interconnect and the first protective structure are integrated into a mobile phone, a cellular phone, a portable computer, a radio, a satellite radio, a communication device, a portable music player, a portable digital video player, a navigation device, a personal digital assistant (PDA), a mobile location data unit, or a combination thereof.

13. The apparatus of claim 1, wherein the first interconnect and the first protective structure are integrated into a set top box, an entertainment unit, a fixed location data unit, a desktop computer, a display device, a tuner, a media player, or a combination thereof.

14. A method comprising:
depositing a protective layer in a trench;
etching the protective layer to define a first protective structure on a sidewall of the trench; and
etching a dielectric material to expose a first etch stop layer, wherein a cavity is defined at least in part by the first protective structure and the first etch stop layer.

15. The method of claim 14, further comprising depositing a second etch stop layer on the first protective structure and on one or more other structures of a semiconductor device to close an opening of the cavity, wherein closing the opening of the cavity defines an airgap.
16. The method of claim 14, wherein depositing the protective layer in the trench comprises depositing the protective layer on a horizontal surface of the trench and on the sidewall of the trench.

17. The method of claim 14, further comprising forming an interconnect in the trench, wherein forming the interconnect comprises forming a barrier layer on the first protective structure.

18. The method of claim 17, wherein forming the interconnect further comprises forming a seed layer on the barrier layer, depositing a metal on the seed layer, and performing a chemical mechanical planarization operation to define the interconnect.

19. The method of claim 14, wherein etching the dielectric material exposes a portion of the first protective structure.

20. The method of claim 14, wherein etching the protective layer is performed using an anisotropic etch process.

21. The method of claim 14, further comprising forming a first interconnect and forming a second interconnect, wherein the cavity is positioned between the first interconnect and the second interconnect.

22. The method of claim 14, further comprising forming a second protective structure on a second sidewall of a second trench, wherein the second protective structure further defines the cavity.

23. The method of claim 22, wherein etching the dielectric material exposes a portion of the second protective structure.

24. The method of claim 14, wherein depositing the protective layer, etching the protective layer, and etching the dielectric material are initiated at a controller of a fabrication system.
25. An apparatus comprising:
means for resisting diffusion of a conductive material of an interconnect into a
dielectric layer of a semiconductor device, wherein the means for
resisting the diffusion is in contact with the dielectric layer; and
means for defining an airgap, wherein the means for defining is in contact with
the means for resisting.

26. The apparatus of claim 25, wherein the means for defining the airgap
includes a first protective structure coupled to the means for resisting, one or more etch
stop layers, and a second protective structure associated with another interconnect, and
wherein the means for resisting diffusion includes a barrier structure.

27. The apparatus of claim 25, wherein the means for resisting and the means
for defining are integrated into a mobile phone, a cellular phone, a portable computer, a
radio, a satellite radio, a communication device, a portable music player, a portable
digital video player, a navigation device, a personal digital assistant (PDA), a mobile
location data unit, or a combination thereof.

28. The apparatus of claim 25, wherein the means for resisting diffusion and the
means for defining an airgap are integrated into a set top box, an entertainment unit, a
fixed location data unit, a desktop computer, a display device, a tuner, a media player,
or a combination thereof.

29. A non-transitory computer-readable medium comprising processor-
executable instruction that, when executed by a processor, cause the processor to:
initiate formation of a semiconductor device, the semiconductor device formed
by:
  depositing a protective layer in a trench;
etching the protective layer to define a first protective structure on a
  sidewall of the trench; and
  etching a dielectric material to expose a first etch stop layer, wherein a
cavity is defined at least in part by the first protective structure
  and the first etch stop layer.
30. The non-transitory computer-readable medium of claim 29, wherein the semiconductor device is further formed by depositing a second etch stop layer to close an opening of the cavity, wherein closing the opening of the cavity defines an airgap.
1100

Deposit a protective layer in a trench

1104

Etch the protective layer to define a first protective structure on a sidewall of the trench

1106

Etch a dielectric material to expose a first etch stop layer, where a cavity is defined at least in part by the first protective structure and the first etch stop layer

1108

Deposit a second etch stop layer on the protective structure to close an opening of the cavity, where closing the opening of the cavity defines an airgap

FIG. 11
# A. CLASSIFICATION OF SUBJECT MATTER

**INV.** H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal , WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<th>Category</th>
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<th>Relevant to claim No.</th>
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- **X** Special categories of cited documents:
  - "A" document defining the general state of the art which is not considered to be of particular relevance
  - "E" earlier application or patent but published on or after the international filing date
  - "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
  - "O" document referring to an oral disclosure, use, exhibition or other means
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- **T** later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

- **X** document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

- **Y** document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

- **A** document member of the same patent family

### Date of the actual completion of the international search

29 September 2015

### Date of mailing of the international search report

06/10/2015

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