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(54) Title: III-N SEMICONDUCTOR LAYER ON SI SUBSTRATE

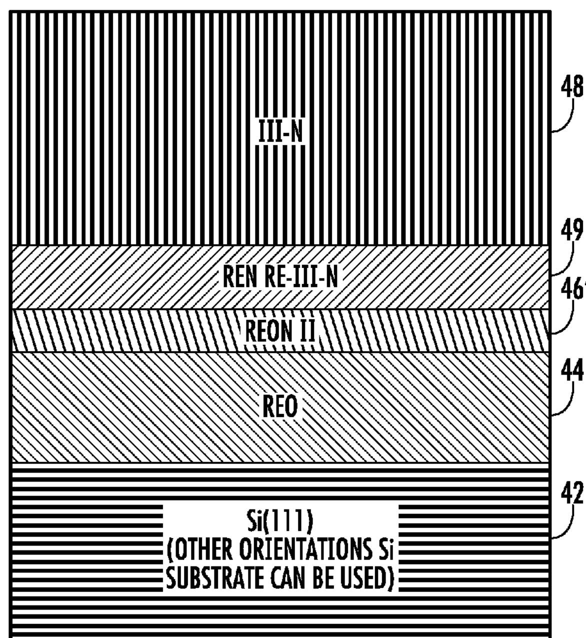

FIG. 10

(57) **Abstract**: A method of growing III-N semiconducting material on a silicon substrate including the steps of growing a layer of epitaxial rare earth oxide on a single crystal silicon substrate and modifying the surface of the layer of epitaxial rare earth oxide with nitrogen plasma. The method further includes the steps of growing a layer of low temperature epitaxial gallium nitride on the modified surface of the layer of epitaxial rare earth oxide and growing a layer of bulk epitaxial III-N semiconductive material on the layer of low temperature epitaxial gallium nitride.

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III-N SEMICONDUCTOR LAYER ON Si SUBSTRATE

Field of the Invention

This invention relates in general to the growth of semiconductor layers of III-N material on a silicon substrate and more specifically to III-N epitaxial growth on a modified REO buffer on a silicon substrate.

Background of the Invention

GaN or other III-N semiconductor based electronics and optoelectronics need low cost and scalable substrates. GaN or other III-N semiconductors grown on a silicon substrate is generally considered to be the most cost efficient technology. However, it is known that growing a III-N material, such as GaN, on a silicon substrate is difficult due in large part to the large crystal lattice mismatch (-16.9%) and the huge difference in thermal expansion coefficients (56%) between silicon and GaN. Also, final tinsel stress arises during III-N growth on Silicon and subsequent cooling of the structure. Thus, some type of buffer layer or layers is generally formed on the silicon substrate and the III-N material is grown on the buffer layer.

Generally, the prior art buffer layers, such as an AlN buffer, do no adequately reduce the strain in the silicon substrate or the III-N due to crystal lattice mismatch. In the prior art, various attempts are disclosed for the growth of different devices including III-V materials on silicon and other substrates. In some copending United States Patent Applications rare earth nitrides and rare earth oxy-nitrides are used in buffer layers, all of which are at least partially successful. Some specific applications and patents include: (A31) entitled "Rare Earth Oxy-Nitride Buffered III-N On Silicon", serial No. 13/196,919, filed on 08/03/2011; (A41) entitled "Nucleation of III-N On REO Templates", serial No. 13/845,426, filed on 03/18/2013; (A62) entitled "Modification Of REO By Subsequent III-N EPI Process", Patent No. 8,501,635, issued 08/06/2013; (A65) entitled "III-N Material Grown On REN Epitaxial Buffer On Si Substrate", serial No. 13/939,721, filed on 07/11/2013; and (A67) entitled "REN Semiconductor Layer Epitaxially Grown on REAlN/REO Buffer on Si Substrate", serial No. 14/161,925,filed on 01/23/2014, and all incorporated herein by reference.

It would be highly advantageous, therefore, to remedy the foregoing and other deficiencies inherent in the prior art and copending applications.

Summary of the Invention

The desired objects and aspects of the instant invention are achieved in accordance with a preferred method of growing III-N semiconducting material on a silicon substrate including the steps of growing a layer of epitaxial rare earth oxide on 5 a single crystal silicon substrate and modifying the surface of the layer of epitaxial rare earth oxide with nitrogen plasma. The method further includes the steps of growing a layer of low temperature epitaxial gallium nitride on the modified surface of the layer of epitaxial rare earth oxide and growing a layer of bulk epitaxial III-N semiconductive material on the layer of low temperature epitaxial gallium nitride.

10 The desired objects and aspects of the instant invention are further realized in accordance with a specific embodiment of III-N semiconducting material on a silicon substrate including a single crystal layer of rare earth oxide positioned on a single crystal silicon substrate and the surface of the single crystal layer of rare earth oxide is terminated with nitrogen atoms forming a nitrogen atom template. A single crystal 15 layer of low temperature GaN is positioned on the nitrogen atom template and a single crystal epitaxial bulk semiconductor III-N layer is positioned on the single crystal layer of low temperature GaN.

The desired objects and aspects of the instant invention are further realized in accordance with a specific method of growing III-N semiconducting material on a 20 silicon substrate including epitaxially growing a first layer of rare earth oxide on the silicon substrate, the first layer of rare earth oxide being substantially lattice matched to the silicon substrate. Epitaxially growing a second layer of rare earth oxide on the first layer of rare earth oxide, the second layer of rare earth oxide having a different lattice constant then the first layer of rare earth oxide creating a stress in the second 25 layer of rare earth oxide. Nitridizing the second layer of epitaxial rare earth oxide with nitrogen plasma to form a nucleation layer and epitaxially growing a layer of III-N material on the nucleation layer of epitaxial rare earth oxide.

Brief Description of the Drawings

30 The foregoing and further and more specific objects and advantages of the instant invention will become readily apparent to those skilled in the art from the following detailed description of a preferred embodiment thereof taken in conjunction with the drawings, in which:

FIG. 1 is a simplified layer diagram illustrating a method and structure of growing single crystal III-N material on a silicon substrate with the new template, in accordance with the present invention;

FIG. 2 illustrates characteristic emission wavelengths of optical emission spectra of nitrogen plasma.

FIG. 3 is a chart illustrating the lattice constant (crystal spacing) of the lanthanide oxides (rare earth oxides);

FIG. 4 is a simplified layer diagram of first steps in another method and structure of growing single crystal III-N material on a silicon substrate, in accordance with the present invention;

FIG. 5 is a RHEED maxima curve in reciprocal space illustrating stress in the REO II layer of FIG. 4;

FIG. 6 is a graph illustrating the thickness of the REO II layer of FIG. 4 versus the reciprocal spacing;

FIG. 7 is a simplified layer diagram illustrating the nitridizing of the REO II layer of FIG. 4;

FIG. 8 is a simplified layer diagram of additional steps in the method and illustrated in FIG. 6;

FIG. 9 illustrates an XRD scan of the structure illustrated in FIG. 8; and

FIG. 10 is a simplified layer diagram of a modification to the structure illustrated in FIG. 8, in accordance with the present invention.

Detailed Description of the Drawings

Turning to FIG. 1, a simplified layer diagram is illustrated of a structure 10 representing apparatus and several steps in a process of growing single crystal III-N material on a silicon substrate 12, in accordance with the present invention. It will be understood that substrate 12 is or may be a standard well known single crystal wafer or portion thereof generally known and used in the semiconductor industry. Also, the term "substrate" simply refers to a supporting structure and may be a layer of silicon-containing material positioned on a base layer of other material such as an oxide or the like. Single crystal substrates, it will be understood, are not limited to any specific crystal orientation but could include (111) silicon, (110) silicon, (100) silicon, offcuts thereof, or any other orientation or variation known and used in the art. However,

throughout this disclosure substrate 12 is illustrated with a preferred (111) orientation because of the simplification of further operations.

In the present invention, as illustrated in FIG. 1, a buffer 14 of single crystal rare earth oxide (REO) is epitaxially grown on silicon substrate 12. Buffer 14 can include a single layer of REO substantially crystal lattice matched to silicon substrate 12 or multiple layers engineered to more closely mate silicon substrate 12 to a III-N semiconductor material. For example, at least a lower portion of buffer 14 can include a single crystal cubic REO material, such as Er_2O_3, with upper portions gradually or in a step function changing to hexagonal REO. For example, as illustrated in the chart of FIG. 3, Gd_2O_3 has a crystal lattice spacing (a) of 10.81Å, Er_2O_3 has a crystal lattice spacing (a) of 10.55Å, Nd_2O_3 has a crystal lattice spacing (a) of 11.08Å, and silicon has a double spacing (2a) of 10.86Å. In this example the lattice mismatch between Er_2O_3 and silicon is approximately -2%, herein referred to as "substantially" crystal lattice matched.

A nucleation layer or template 16 for the growth of III-N semiconductor material is formed by modifying the surface of REO buffer 14 with nitrogen plasma. The nitrogen plasma modifies the surface of REO buffer 14 by terminating the REO surface with nitrogen atoms (i.e. nitrogen atoms attaching to loose bonds) to form template 16 for the growth of III-N material thereon. In a preferred embodiment, the nitrogen plasma has an atomic-to-molecular ratio in a range of 2 to 4 and the substrate temperature during the nitrogen plasma modification is in a range of 550°C to 850°C. The atomic-to-molecular ratio is determined, in this specific method, from characteristic emission wavelengths of optical emission spectra of the nitrogen plasma, as illustrated, for example, in FIG. 2.

Once the nitrogen plasma modification is completed, a thin layer 18 of low temperature GaN is epitaxially grown on template 16. Layer 18 of low temperature GaN in this preferred embodiment is grown using the following parameters: a substrate temperature in a range of 450°C to 650°C (defined as "low temperature"); atomic-to-molecular nitrogen ratio in the plasma in a range of 2 to 4; and gallium vapor partial pressure of approximately $1x10^{-6}$ Torr. Layer 18 of low temperature GaN helps in the later epitaxial growth of bulk III-N material at higher temperature.

With thin layer 18 of low temperature GaN completed a layer 20 of bulk III-N semiconductor material is epitaxially grown on layer 18. In this preferred embodiment and using GaN as an example of the III-N material, layer 18 is

epitaxially grown using the following parameters: a substrate temperature in a range of 800°C to 950°C; a gallium partial pressure of approximately 2.5×10^{-6} Torr; and an atomic-to-molecular nitrogen ratio in the plasma in a range of 2 to 4.

Because of the crystal matching of template 16 and layer 18 of low temperature GaN, layer 20 of bulk III-N semiconducting material can be epitaxially grown relatively thick with very low or no fractures or stress. Thus, structure 10 can be used for the growth of III-N (e.g. GaN, AlN) semiconductor layers used in, for example, photonic devices. As an example, a III-N LED structure (not shown) could be formed in/on layer 20. Layer 20 is illustrated as a single layer for convenience but it should be understood that the III-N LED structure could include the growth of one or more typical layers, including for example, i-GaN, n-GaN, active layers such as InGaN/GaN, electron blocking layers, p-GaN, and other inter-layers used in the formation and performance of LED (especially photonic LED) devices.

Thus, in the present novel process, buffer 14 including one or more layers of single crystal REO is first epitaxially grown on silicon substrate 12. Nitrogen plasma is used to modify the surface of REO buffer 14 by terminating the REO surface with nitrogen atoms to form template 16 for the growth of III-N material. A thin layer 18 of low temperature GaN is epitaxially grown on template 16 and layer 20 of bulk III-N material is grown epitaxially on layer 18. Layer 20 may be an active semiconductor layer for the formation of various semiconductor devices or additional layers may be epitaxially grown on layer 20. Also, because of the reduced stress, layer 20 can be grown sufficiently thick to form electronic of photonic devices therein.

Turning now to FIG. 4, a simplified layer diagram is illustrated of first steps in another method and structure of growing single crystal III-N material on a silicon substrate, in accordance with the present invention. During the modification of the REO surface with N-plasma, metal bonds are broken and oxygen is replaced with nitrogen atoms. Generally, oxygen-metal ionic bonds are strong and for this reason the nitridation process requires substantial processing time. It has been found that the oxygen-metal ionic bonds can be weakened by introducing stress into the REO layer.

As an example of introducing stress into the REO layer, the gadolinium oxide lattice constant is larger than the lattice constant of erbium oxide, as illustrated in the chart of FIG. 3. Erbium oxide (Er_2O_3) grown on gadolinium oxide (Gd_2O_3) is under tensile stress before it relaxes after reaching critical thickness. The critical thickness

of a layer depends on the stress and the layer growth process conditions (*e.g.* temperature, growth rate, etc.)

Referring again to FIG. 4, the growth rate of a strained oxide layer is illustrated. A single crystal silicon substrate 42 is provided. Single crystal substrates, as explained above, are not limited to any specific crystal orientation but could include (111) silicon, (110) silicon, (100) silicon, offcuts thereof, or any other orientation or variation known and used in the art. A first rare earth oxide (REO I) layer 44 is epitaxially grown on substrate 42 so as to be a relaxed oxide layer with a thickness of >50nm. It should be understood that layer 44 can be a single layer or it can be a multilayered relaxed REO template.

Next, a second rare earth oxide (REO II) layer 46 is epitaxially grown on layer 44. REO II layer 46 is a strained oxide layer with a lattice constant different from the lattice constant of REO I 44. As explained above, a typical example of rare earth oxides with different lattice constants is Erbium oxide (Er_2O_3) grown on gadolinium oxide (Gd_2O_3), which is under tensile stress. The thickness of REO II layer 46 must be below 10nm in order to maintain stress in its crystal structure. The stress in REO II layer 46 is evaluated by the change of its lattice constant indicated by distance of the RHEED (reflecting high energy electron diffraction) maxima in reciprocal space as illustrated in FIG. 5. The distance between maxima is designated with arrow 47. A higher distance between the maxima corresponds to smaller lattice constant in real space. The relationship between the thickness of REO II layer 46 and reciprocal spacing is illustrated in the graph of FIG. 6, with a not saturated curve indicating a not relaxed layer.

Referring additionally to FIG. 7, stressed REO II layer 46 is nitridized or modified with an N-plasma. The nitridized modification of REO II layer 46 is illustrated in FIG. 7 as REON II, designated 46' to indicate the modification. As explained above, because REO II layer 46 is stressed the nitridization is easier as compared to a relaxed REO layer.

A layer 48 of III-N semiconductor material can be epitaxially grown directly on REON II layer 46'. The crystal structure of REON II layer 46' is close enough to the crystal structure of III-N semiconductor material, such as GaN, so that a relatively thick layer can be grown with a tolerable amount of stress. Referring additionally to FIG. 9, an XRD-scan is illustrated of the structure illustrated in FIG. 8. The X-ray diffraction 2Θ-ω scan is of the FWHM structure of the GaN (0002) peak: 0.46 degree.

Turning now to FIG. 10, a simplified layer diagram is illustrated of a modification to the structure illustrated in FIG. 8, in accordance with the present invention. In this modification, a rare earth nitride (REN) and rare earth III nitride (RE-III-N) layer 49 is epitaxially grown on the nitridized REON II layer 46' and forms a nucleation-buffer layer which subsequently serves as a substrate for the epitaxial growth of III-N layer 48, such as GaN semiconductor material. It should be understood that the low temperature GaN followed by the bulk epitaxial layer of GaN structure illustrated and described in conjunction with FIG. 1 can also be incorporated into the present structure, or the Structure of FIG. 8, if desired.

Thus, new and improved methods for the growth of single crystal semiconducting III-N and, optionally, subsequent III-N material and new and improved structures grown on a silicon substrate are disclosed. The new and improved methods for the III-N material include specifically the nitrogen termination of the surface of a REO buffer using nitrogen plasma. Further, it has been found that the nucleation process can be more easily and quickly performed in stressed rare earth oxide layers. The subsequent epitaxial growth of a layer of low temperature GaN aids in the subsequent growth of a bulk III-N semiconducting material.

Various changes and modifications to the embodiments herein chosen for purposes of illustration will readily occur to those skilled in the art. To the extent that such modifications and variations do not depart from the spirit of the invention, they are intended to be included within the scope thereof which is assessed only by a fair interpretation of the following claims.

Having fully described the invention in such clear and concise terms as to enable those skilled in the art to understand and practice the same, the invention claimed is:

CLAIMS

1. A method of growing III-N semiconducting material on a silicon substrate comprising the steps of:

providing a single crystal silicon substrate;

growing a layer of epitaxial rare earth oxide on the silicon substrate, the layer of epitaxial rare earth oxide having a surface;

terminating the surface of the layer of epitaxial rare earth oxide with nitrogen forming a nitrogen atom template;

growing a layer of III-N material on the nitrogen terminated surface of the layer of epitaxial rare earth oxide; and

growing a layer of bulk epitaxial III-N semiconductive material on the layer of III-N material.

2. The method as claimed in claim 1 wherein the step of growing the layer of III-N material includes epitaxially growing one of GaN and AlN.

3. The method as claimed in claim 1 wherein the step of terminating the surface of the layer of epitaxial rare earth oxide with nitrogen includes modifying the surface with nitrogen plasma.

4. The method as claimed in claim 3 wherein the step of modifying the surface of the layer of epitaxial rare earth oxide with the nitrogen plasma includes using the following parameters: the nitrogen plasma has an atomic-to-molecular ratio in a range of 2 to 4 and the substrate temperature during the nitrogen plasma modification is in a range of 550°C to 850°C.

5. The method as claimed in claim 21 wherein the step of growing the layer of low temperature epitaxial gallium nitride includes using the parameters: a substrate temperature in a range of 450°C to 650°C; atomic-to-molecular nitrogen ratio in the plasma in a range of 2 to 4; and gallium vapor partial pressure of approximately $1x10^{-6}$ Torr.

6. The method as claimed in claim 1 wherein the step of growing the layer of bulk epitaxial III-N semiconductive material includes using the parameters: a substrate temperature in a range of 800°C to 950°C; a gallium vapor partial pressure of approximately $2.5x10^{-6}$ Torr; and an atomic-to-molecular nitrogen ratio in the plasma in a range of 2 to 4.

7. The method as claimed in claim 1 wherein the step of growing the layer of epitaxial rare earth oxide on the silicon substrate includes growing one of a single layer and a multilayer REO buffer.

8. The method as claimed in claim 1 wherein the step of growing the layer of epitaxial rare earth oxide on the silicon substrate includes epitaxially growing a first rare earth oxide layer substantially lattice matched to the silicon substrate and epitaxially growing a second rare earth oxide layer with a different lattice constant on the first rare earth oxide layer so that the second rare earth oxide layer is stressed.

9. The method as claimed in claim 8 wherein the step of epitaxially growing the second rare earth oxide layer includes growing the second rare earth oxide layer with a thickness below 10nm to maintain stress in the crystal structure.

10. A method of growing III-N semiconducting material on a silicon substrate comprising the steps of:

providing a single crystal silicon substrate;

epitaxially growing a first layer of rare earth oxide on the silicon substrate, the first layer of rare earth oxide being substantially lattice matched to the silicon substrate;

epitaxially growing a second layer of rare earth oxide on the first layer of rare earth oxide, the second layer of rare earth oxide having a different lattice constant then the first layer of rare earth oxide creating a stress in the second layer of rare earth oxide;

nitridizing the second layer of epitaxial rare earth oxide with nitrogen to form a nucleation layer; and

epitaxially growing a layer of III-N material on the nucleation layer of epitaxial rare earth oxide.

11. The method as claimed in claim 10 wherein the step of epitaxially growing the second layer of rare earth oxide includes growing the second layer of rare earth oxide with a thickness below 10nm.

12. The method as claimed in claim 10 wherein the step of epitaxially growing the first layer of rare earth oxide includes growing the first layer of rare earth oxide with a thickness above 50nm.

13. The method as claimed in claim 10 wherein the step of epitaxially growing the first layer of rare earth oxide on the silicon substrate includes growing one of a single layer and a multilayer REO buffer.

14. A method of growing III-N semiconducting material on a silicon substrate comprising the steps of:

providing a single crystal silicon substrate;

epitaxially growing a first layer of rare earth oxide on the silicon substrate, the first layer of rare earth oxide being substantially lattice matched to the silicon substrate;

epitaxially growing a second layer of rare earth oxide on the first layer of rare earth oxide, the second layer of rare earth oxide having a different lattice constant then the first layer of rare earth oxide creating a stress in the second layer of rare earth oxide;

nitridizing the second layer of epitaxial rare earth oxide with nitrogen to form a nucleation layer;

epitaxially growing a nucleation-buffer layer of REN RE-III-N material on the nucleation layer of epitaxial rare earth oxide; and

epitaxially growing a layer of III-N material on the nucleation-buffer layer of epitaxial rare earth oxide.

15. A method of growing III-N semiconducting material on a silicon substrate comprising the steps of:

providing a single crystal silicon substrate;

growing a layer of epitaxial rare earth oxide on the silicon substrate, the layer of epitaxial rare earth oxide having a surface;

modifying the surface of the layer of epitaxial rare earth oxide with a nitrogen plasma using the following parameters: the nitrogen plasma has an atomic-to-molecular ratio in a range of 2 to 4 and the substrate temperature during the nitrogen plasma modification is in a range of 550°C to 850°C;

growing a layer of low temperature epitaxial gallium nitride on the modified surface of the layer of epitaxial rare earth oxide using the parameters: a substrate temperature in a range of 450°C to 650°C; atomic-to-molecular nitrogen ratio in the plasma in a range of 2 to 4; and gallium vapor partial pressure of approximately $1x10^{-6}$ Torr; and

growing a layer of bulk epitaxial III-N semiconductive material on the layer of low temperature epitaxial gallium nitride using the parameters: a substrate temperature in a range of 800°C to 950°C; a gallium vapor partial pressure of approximately $2.5x10^{-6}$ Torr; and an atomic-to-molecular nitrogen ratio in the plasma in a range of 2 to 4.

16. III-N semiconducting material on a silicon substrate comprising:

a single crystal silicon substrate;

a first epitaxial layer of rare earth oxide positioned on the silicon substrate, the first layer of rare earth oxide being substantially lattice matched to the silicon substrate;

a second epitaxial layer of rare earth oxide positioned on the first epitaxial layer of rare earth oxide, the second epitaxial layer of rare earth oxide having a different lattice constant then the first epitaxial layer of rare earth oxide with a stress in the second epitaxial layer of rare earth oxide;

the second layer of epitaxial rare earth oxide being nitridized with nitrogen to form a nucleation layer; and

an epitaxial layer of III-N material positioned on the nucleation layer of epitaxial rare earth oxide.

17. The III-N semiconducting material on the silicon substrate as claimed in claim 16 wherein the first epitaxial layer of rare earth oxide includes single crystal gadolinium oxide (Gd_2O_3) and the second epitaxial layer of rare earth oxide includes single crystal erbium oxide (Er_2O_3).

18. III-N semiconducting material on a silicon substrate comprising:

a single crystal silicon substrate;

a single crystal layer of rare earth oxide positioned on the silicon substrate and having a surface;

the surface of the single crystal layer of rare earth oxide being terminated with nitrogen atoms forming a nitrogen atom template;

a single crystal layer of III-N material positioned on the nitrogen atom template; and

a single crystal epitaxial bulk semiconductor III-N layer positioned on the single crystal layer of III-N material.

19. The III-N semiconducting material on the silicon substrate as claimed in claim 18 wherein the single crystal epitaxial rare earth oxide layer includes a rare earth oxide with a cubic crystal structure.

20. The III-N semiconducting material on the silicon substrate as claimed in claim 18 wherein the single crystal epitaxial rare earth oxide with the cubic crystal structure includes single crystal erbium oxide (Er_2O_3).

21. The method as claimed in claim 1 wherein the step of growing the layer of epitaxial III-N semiconducting material includes growing low temperature epitaxial bulk gallium nitride.

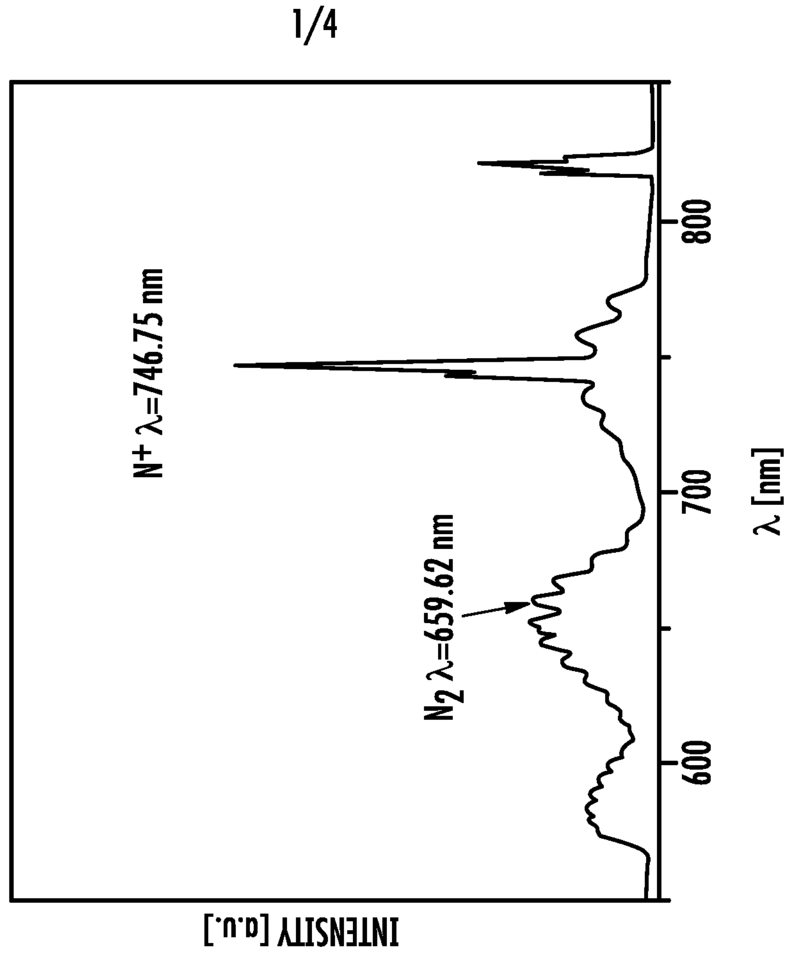

FIG. 2

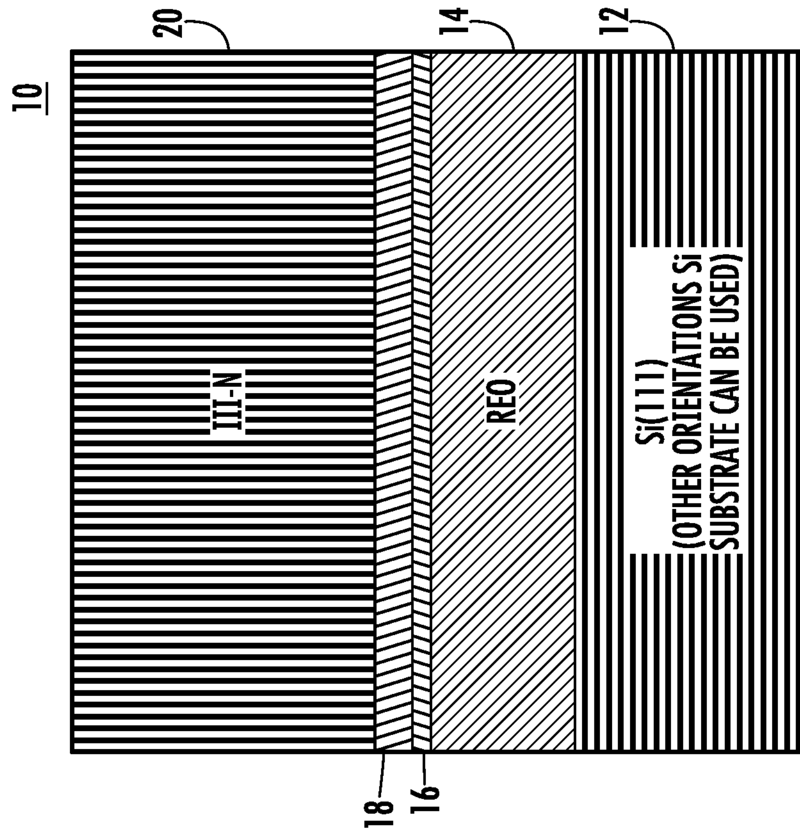

FIG. 1

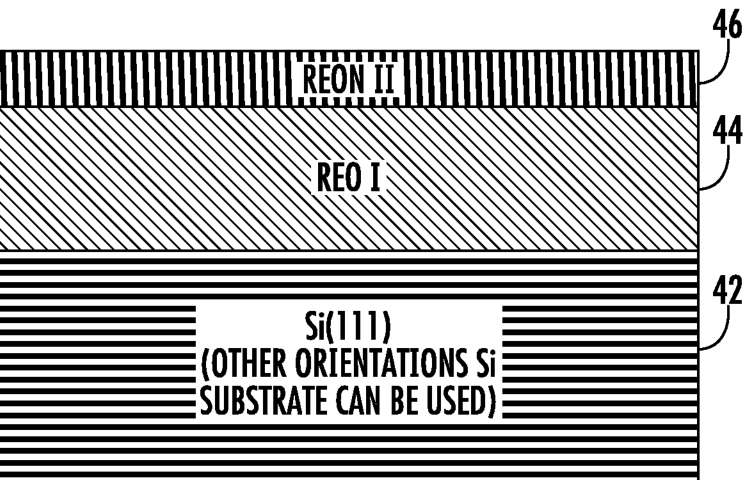

FIG. 4

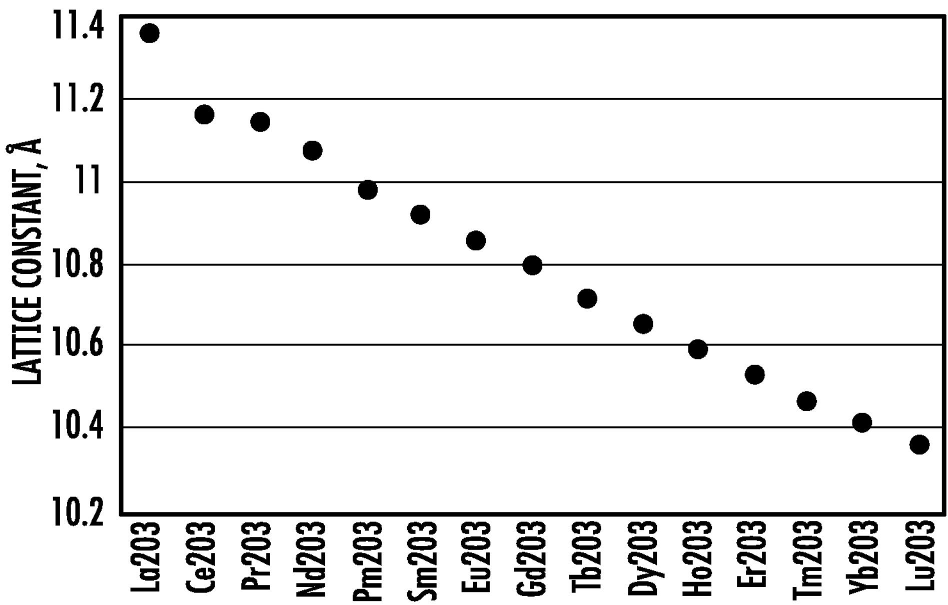

FIG. 3

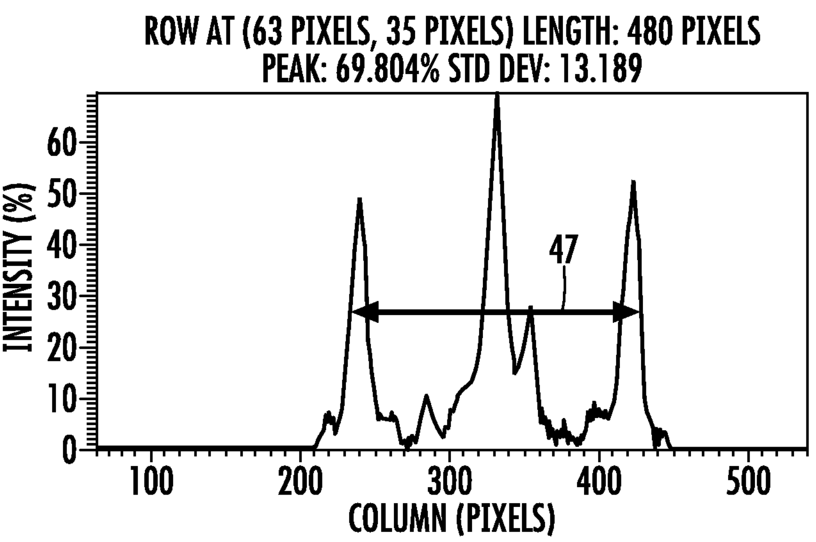

FIG. 5

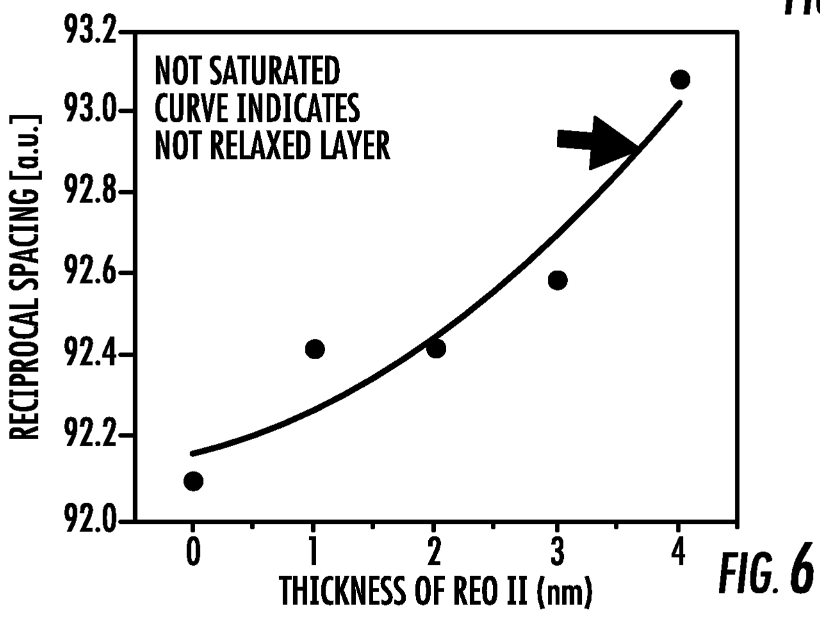

FIG. 6

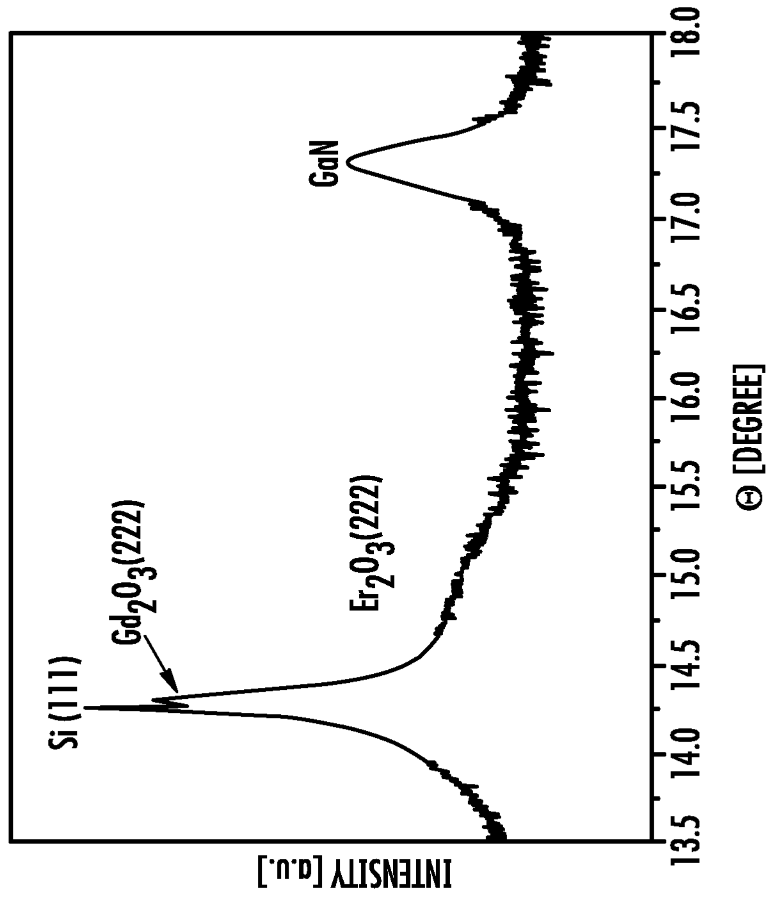

FIG. 9

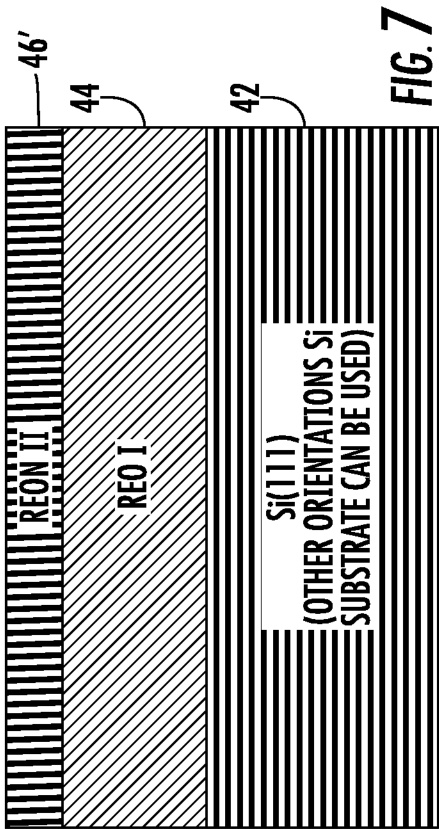

FIG. 7

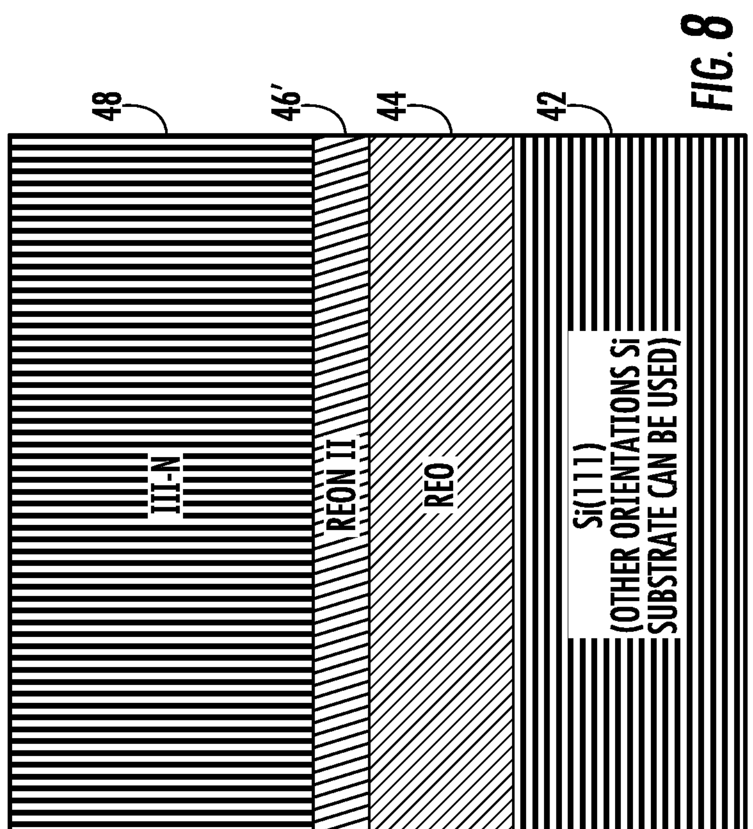

FIG. 8

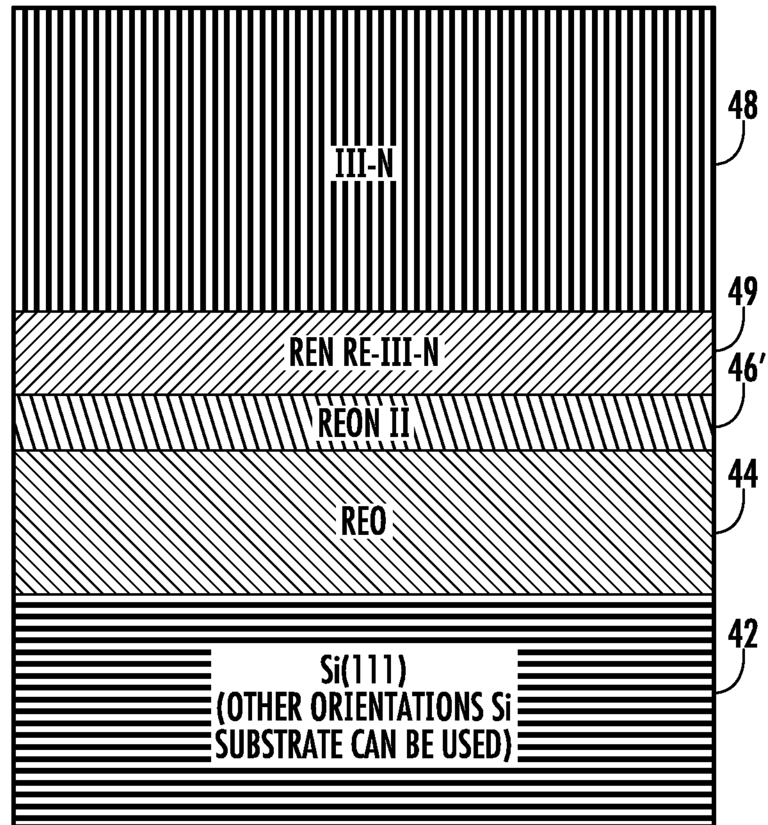

FIG. 10

INTERNATIONAL SEARCH REPORT PCT/US2015/014034 23.04.2015

International application No.
PCT/US15/14034

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 29/12, 21/20, 29/20 (2015.01)
CPC - H01L 29/2003, 21/02156, 21/0254
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8): H01L 29/12, 21/20, 29/20, 21/36; B32B 9/04 (2015.01)
CPC: H01L 29/2003, 21/02156, 21/0254, 21/02502, 21/02381

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatSeer (US, EP, WO, JP, DE, GB, CN, FR, KR, ES, AU, IN, CA, INPADOC Data); ProQuest; IP.com; Google/Google Scholar; grow, deposit, III-N, AlN, GaN, gallium nitride, rare earth oxide, REO, gadolinium oxide, erbium oxide, Gd2O3, Er2O3, epitaxal, layer, silicon, Si, substrate, single crystal, monocrystalline, nitrogen plasma, nitridation, nucleation, buffer, lattice, temperature, pressure, flux, atom

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013/0032858 A1 (CLARK, A et al.) 07 February 2013; paragraphs [0014]-[0015], [0023]; figure 2; claims 1, 15, 21	1-21
Y	US 2011/0189860 A1 (PORSHNEV, P) 04 August 2011; paragraphs [0024], [0026]; claims 1-2	1-21
Y	EP 2 610 895 A1 (NATIONAL UNIVERSITY CORPORATION NAGOYA UNIVERSITY, et al.) 03 July 2013; paragraph [0054]; figures 3, 5; claim 5	6, 15
Y	US 2010/0065815 A1 (BOJARCZUK, JR., NA et al.) 18 March 2010; paragraphs [0012], [0041], [0055]; claim 1	9, 11-12
Y	US 8,012,442 B2 (CLARK, RD et al.) 06 September 2011; claim 1	14
Y	US 2013/0248853 A1 (ARKUN, E et al.) 26 September 2013; abstract; paragraphs [0021]-[0022]; claim 5	17
Y	US 7,011,706 B2 (HIGUCHI, T et al.) 14 March 2006; claims 1-3	19-20
Y	US 7,964,482 B2 (LIETEN, R et al.) 21 June 2011; abstract; column 12, lines 62-63; column 13, lines 8-10	5, 15, 21
A	US 8,636,844 B1 (DARGIS, R et al.) 28 January 2014; entire document	1-21
A	US 2012/0183767 A1 (DARGIS, R et al.) 19 July 2012; entire document	1-21

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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