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(71) Applicant: **KONINKLIJKE PHILIPS N.V.** [NL/NL]; High Tech Campus 5, NL-5656 AE Eindhoven (NL).

(72) Inventors: **GRILLOT, Patrick Nolan**; c/o High Tech Campus 5, NL-5656 AE Eindhoven (NL). **WILDESON, Isaac Harshman**; c/o High Tech Campus 5, NL-5656 AE Eindhoven (NL). **NSHANIAN, Tigran**; c/o High Tech Campus 5, NL-5656 AE Eindhoven (NL). **DEB, Parijat Pramil**; c/o High Tech Campus 5, NL-5656 AE Eindhoven (NL).

(74) Agents: **VAN EEUWIJK, Alexander Henricus Walterus** et al.; High Tech Campus Building 5, NL-5656 AE Eindhoven (NL).

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(54) **Title**: REDUCING OR ELIMINATING NANOPIPE DEFECTS IN III-NITRIDE STRUCTURES

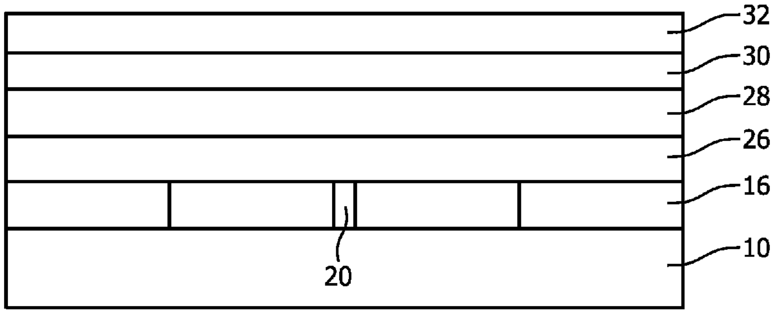


FIG. 3

(57) **Abstract**: Embodiments of the invention include a III-nitride light emitting layer disposed between an n-type region and a p-type region, a III-nitride layer including a nanopipe defect, and a nanopipe terminating layer disposed between the III-nitride light emitting layer and the III-nitride layer comprising a nanopipe defect. The nanopipe terminates in the nanopipe terminating layer.

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# Reducing or eliminating nanopipe defects in III-nitride structures

## Field of the invention

The present invention relates to reducing or eliminating nanopipe defects in III-nitride structures.

## Background

Semiconductor light-emitting devices including light emitting diodes (LEDs), resonant cavity light emitting diodes (RCLEDs), vertical cavity laser diodes (VCSELs), and edge emitting lasers are among the most efficient light sources currently available. Materials systems currently of interest in the manufacture of high-brightness light emitting devices capable of operation across the visible spectrum include Group III-V semiconductors, particularly binary, ternary, and quaternary alloys of gallium, aluminum, indium, and nitrogen, also referred to as III-nitride materials. Typically, III-nitride light emitting devices are fabricated by epitaxially growing a stack of semiconductor layers of different compositions and dopant concentrations on a sapphire, silicon carbide, III-nitride, or other suitable substrate by metal-organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), or other epitaxial techniques. The stack often includes one or more n-type layers doped with, for example, Si, formed over the substrate, one or more light emitting layers in an active region formed over the n-type layer or layers, and one or more p-type layers doped with, for example, Mg, formed over the active region. Electrical contacts are formed on the n- and p-type regions.

III-nitride devices are often grown on sapphire, Si, or SiC substrates. Due to differences in lattice constant and coefficient of thermal expansion between the substrate material and the III-nitride semiconductor material, defects are formed in the semiconductor during growth, which may limit the efficiency of III-nitride devices.

## Summary

It is an object of the invention to reduce or eliminate nanopipe defects in a III-nitride structure.

Embodiments of the invention include a III-nitride light emitting layer disposed between an n-type region and a p-type region, a III-nitride layer including a nanopipe defect, and a nanopipe terminating layer disposed between the III-nitride light emitting layer and the III-nitride layer comprising a nanopipe defect. The nanopipe terminates in the nanopipe terminating layer.

Embodiments of the invention include a III-nitride light emitting layer disposed between an n-type region and a p-type region, and a III-nitride layer that may be doped with an acceptor. The n-type region is disposed between the III-nitride layer doped with an acceptor and the light emitting layer. The acceptor may be, for example, magnesium.

A method according to embodiments of the invention includes growing a III-nitride layer over a growth substrate, the III-nitride layer including a nanopipe defect, growing a nanopipe terminating layer over the III-nitride layer, and growing a III-nitride light emitting layer over the nanopipe terminating layer. The nanopipe terminates in the nanopipe terminating layer.

## Brief description of the drawings

Fig. 1 illustrates a III-nitride nucleation layer grown on a substrate.

Fig. 2 illustrates the formation of a nanopipe in a high temperature layer and an active region grown over the structure illustrated in Fig. 1.

Fig. 3 illustrates a III-nitride structure including a nanopipe termination structure.

Fig. 4 illustrates a nanopipe termination structure including multiple acceptor-doped layers.

Fig. 5 illustrates a nanopipe termination structure including an acceptor-doped layer and an additional layer.

Fig. 6 illustrates a superlattice nanopipe termination structure.

Fig. 7 illustrates the structure of Fig. 3 formed into a flip chip device.

Fig. 8 illustrates a nanopipe termination structure incorporated into an electrostatic discharge protection circuit.

Fig. 9 is a circuit diagram of the structure illustrated in Fig. 8.

## Detailed description

Figs. 1 and 2 illustrate the formation of a type of defect referred to herein as a nanopipe. Nanopipes are particularly problematic defects because of their large size - often several microns long, and several tens or hundreds of angstroms in diameter. For example, in III-nitride material a nanopipe may be at least 10 Å wide in some embodiments and no more than 500 Å wide in some embodiments. In some materials, such as SiC, nanopipes may be 1 micron wide, or even wider. Nanopipes may be caused by impurities such as oxygen, silicon, magnesium, aluminum, and indium in GaN films. Nanopipes may also be related to impurities or defects on the substrate surface, such as scratches, or nanopipes may be present in the substrate itself, and may continue from the substrate into the III-nitride material grown on the substrate. Nanopipes often form in III-nitride devices at a density of $\sim 10^6$ $cm^{-2}$, which is much lower than the dislocation density in typical III-nitride devices, which may vary from $\sim 10^7$ $cm^{-2}$ to $\sim 10^{10}$ $cm^{-2}$.

In Fig. 1, a low temperature nucleation layer 12, often GaN or AlN, is deposited on a substrate 10, which may be, for example, sapphire, SiC, Si, a composite substrate, or any another suitable substrate. Nucleation layer 12 is often a polycrystalline or amorphous layer, deposited at a temperature less than 800 °C, for example. The nucleation layer 12 is then annealed at a temperature higher than the deposition temperature. When the nucleation layer 12 is annealed, the nucleation layer forms small separated islands 14 of the nucleation layer on the substrate.

In Fig. 2, a high temperature III-nitride layer 16, often GaN, is grown over nucleation layer 12 to decrease the density of threading dislocations in the device, and to create a smooth, uniform surface on which the active region and other device layers may be grown. High temperature layer 16 initially nucleates on the islands 14, resulting in individual islands 18A, 18B, 18C, and 18D, which eventually coalesce into a smooth, uniform film. Most of the boundaries between islands coalesce to form a smooth uniform film, but these boundaries, such as the boundary between islands 18A and 18B or the boundary between islands 18C and 18D, may contain one or more dislocations, thus giving rise to a threading dislocation density $\sim 10^7$ $cm^{-2}$ to $\sim 10^{10}$ $cm^{-2}$. While most of the islands coalesce, gaps remain between some islands, and these gaps form long narrow defects commonly referred to as nanopipes. One such nanopipe 20 is illustrated in Fig. 2 between islands 18B and 18C. In III-nitride devices such as LEDs, a light emitting or active region 22 is grown above the high temperature layer 16. Nanopipe 20 may propagate near or into active region 22 to form a damaged area 24. These damaged areas in the active region can lead to poor LED performance and poor reliability, and are thus undesirable.

In embodiments of the invention, a structure that prevents a nanopipe from propagating into a later-grown layer, or that reduces the size of the nanopipe, referred to herein as a “nanopipe termination structure” or NTS, is grown before the active region. Fig. 3 illustrates a III-nitride structure including an NTS. In Fig. 3, a high temperature layer 16, often an undoped or n-type GaN layer, is grown over a nucleation layer (not shown) on a substrate, as described above in Figs. 1 and 2. The high temperature layer may include one or more nanopipes 20. An NTS 26 is grown over high temperature layer 16, which includes nanopipes 20. At least a part of NTS 26 may be not intentionally doped, doped with acceptors such as magnesium, or doped with donors such as Si.

An n-type region 28 is grown over NTS 26, followed by active region 30, followed by a p-type region 32. Examples of suitable light emitting regions 30 include a single thick or thin light emitting layer, or a multiple quantum well light emitting region including multiple thin or thick light emitting layers separated by barrier layers. The light emitting layers in active region 30, in a device that emits visible light, are typically InGaN. The light emitting layers in active region 30, in a device that emits UV light, may be GaN or AlGaN. Each of the n-type region 28 and the p-type region 32 may include multiple layers of different composition, thickness, and dopant concentration, including layers that are not intentionally doped, or layers of the opposite conductivity type. In one example, n-type region 28 includes at least one n-type GaN layer doped with Si, active region 30 includes InGaN quantum well layers separated by GaN barrier layers, and p-type region 32 includes at least one p-type GaN or AlGaN layer doped with Mg.

In some embodiments, NTS 26 is a low temperature GaN layer. For example, a low temperature GaN NTS may be grown at a temperature approximately 100 to 200 °C below the growth temperature of high temperature GaN layer 16. This low temperature GaN NTS may be at least 10 nm thick in some embodiments, no more than 40 nm thick in some embodiments, 25 nm thick in some embodiments, at least 100 nm thick in some embodiments, no more than 1 micron thick in some embodiments, and 0.5 micron thick in some embodiments. The low temperature GaN layer is a substantially single crystal layer, and it may be doped or undoped.

In some embodiments, NTS 26 is a III-nitride layer that includes aluminum, such as AlN, AlGaN, AlBGaN, or AlInGaN. The composition x in an $Al_xGa_{1-x}N$ NTS may be at least 0.1 in some embodiments, no more than 0.5 in some embodiments, at least 0.2 in some embodiments, and no more than 0.3 in some embodiments. In one example, an $Al_xGa_{1-x}N$ NTS layer is 150 Å thick at x = 0.25. The upper limit on thickness and composition are determined by the cracking threshold for growth of AlGaN on GaN, so AlN may be used if NTS 26 is sufficiently thin to avoid cracking. As a result, the maximum allowable thickness decreases as the Al composition increases. The thickness of an aluminum-containing NTS may be at least 50 Å thick in some embodiments, no more than 0.5 μm thick in some embodiments, at least 100 Å thick in some embodiments, and no more than 500 Å thick in some embodiments. An aluminum-containing NTS may be undoped or doped with an acceptor such as magnesium. In some embodiments, the aluminum-containing layer includes at least some minimal thickness that is not doped with Si, or is not doped n-type. For example, this minimal thickness is at least 2 nm in some embodiments and at least 5 nm in some embodiments.

In some embodiments, NTS 26 is a III-nitride layer doped with acceptor defects. Magnesium is the preferred acceptor, although other acceptor defects may also be used. Other potential candidates for these acceptor defects include carbon, beryllium, or native defects. A magnesium-doped NTS 26 may be, for example, any suitable III-nitride material including GaN, InGaN, AlGaN, or AlInGaN. In some embodiments, a magnesium-doped NTS 26 may be grown immediately after annealing nucleation layer 12, such that high temperature layer 16, which is often undoped, is omitted. The magnesium concentration may range from $1x10^{17}$ $cm^{-3}$ to $1x10^{20}$ $cm^{-3}$ in some embodiments and from $1x10^{17}$ $cm^{-3}$ to $1x10^{19}$ $cm^{-3}$ in some embodiments. The magnesium dopants in this layer do not need to be activated after growth.

In some embodiments, the concentration of magnesium in a magnesium-doped NTS 26 is graded. As used herein, the term "graded" when describing the dopant concentration in a layer or layers in a device is meant to encompass any structure that achieves a change in dopant concentration in any manner other than a single step in composition. Each graded layer may be a stack of sublayers, each of the sublayers having a different dopant concentration than either sublayer adjacent to it. If the sublayers are of resolvable thickness, the graded layer is a step-graded layer. In some embodiments, the sublayers in a step-graded layer may have a thickness ranging from several tens of angstroms to several thousands of angstroms. In the limit where the thickness of individual sublayers approaches zero, the graded layer is a continuously-graded region. The sublayers making up each graded layer can be arranged to form a variety of profiles in dopant concentration versus thickness, including, but not limited to, linear grades, parabolic grades, and power-law grades. Also, graded layers or graded regions are not limited to a single grading profile, but may include portions with different grading profiles and one or more portions with substantially constant dopant concentration. For example, in a graded magnesium-doped NTS 26, the magnesium concentration may increase in a linear fashion as the NTS 26 is grown, such that the concentration of magnesium is higher in a portion of NTS 26 closer to the active region than in a portion of NTS 26 further from the active region.

In some embodiments, NTS 26 includes multiple layers. Figs. 4, 5, and 6 illustrate nanopipe termination structures with multiple layers.

Fig. 4 illustrates an NTS 26 with multiple layers doped with magnesium or any other suitable acceptor. Each of layers 40, 42, and 44 may have a different dopant concentration. For example, layer 40 may have a magnesium concentration between zero (not doped with Mg) and $2x10^{18}$ $cm^{-3}$, layer 42 may have a magnesium concentration between $1x10^{17}$ $cm^{-3}$ and $1x10^{20}$ $cm^{-3}$ in some embodiments and between $2x10^{17}$ $cm^{-3}$ and $5x10^{19}$ $cm^{-3}$ in some embodiments, and layer 44 may have a magnesium concentration between zero (not doped with Mg) and $1x10^{19}$ $cm^{-3}$. The layer in NTS 26 closest to active region 30 may have the highest dopant concentration in some embodiments. The layer in NTS 26 closest to growth substrate 10 may have the lowest dopant concentration in some embodiments. Though Fig. 4 illustrates three layers, an NTS with multiple acceptor-doped layers may include more or fewer than three layers. Layers 40, 42, and 44 may have the same composition, though they need not. For example, layers 40, 42, and 44 may be GaN, InGaN, AlGaN, AlN, or AlInGaN.

In Fig. 5, NTS 26 includes at least two layers 46 and 48. Layer 46 is grown on high temperature, nanopipe-containing layer 16. Layer 46 may be doped with magnesium or another acceptor. Layer 46 is often GaN, although it may be InGaN, AlGaN, or AlInGaN. Layer 48 is grown over layer 46. Layer 48 may include aluminum and/or indium. For example, layer 48 may be AlGaN, InGaN, or AlInGaN. Alternatively, layer 48 may be a GaN layer grown at a temperature 100 to 200 °C below the temperature of high temperature layer 16. The low temperature GaN layer may be doped or undoped. An active region 30 is grown over layer 48. Active region 30 may be grown in direct contact with layer 48, or may be spaced apart from layer 48 by, for example, an n-type region 28 as illustrated in Fig. 3.

In Fig. 6 NTS 26 is a superlattice. The superlattice may be doped or undoped. The superlattice includes multiple pairs of layers 50 and 52. Layers 50 and 52 alternate. Though three layer pairs are illustrated, more or fewer layer pairs can be used. An active region 30 is grown over the super lattice. Active region 30 may be grown in direct contact with the superlattice, or may be spaced apart from the superlattice by, for example, an n-type region 28 as illustrated in Fig. 3. Though the superlattice is illustrated beginning with a layer 50 in direct contact with high temperature layer 16 and terminating with a layer 52 disposed beneath active region 30, the superlattice may begin or terminate with either a layer 50 or a layer 52, and the superlattice may include incomplete layer pairs. In one embodiment, layers 50 are GaN and layers 52 are $Al_aGa_{1-a}N$ with an aluminum composition a between 0.05 and 1. In one embodiment, layers 50 are GaN and layers 52 are AlN. In some embodiment, layers 50 are $Al_bGa_{1-b}N$ and layers 52 are $Al_cGa_{1-c}N$, where $b \neq c$ in one embodiment, $b > c$ in some embodiments, and $b < c$ in some embodiments. In one embodiment, layers 50 and 52 may have compositions $b = 0.05$ and $c = 1$. Strain compensated layer pairs may also be used, where one of the layers 50 and 52 is compressively strained, such as by using InGaN or another indium containing layer, and the other of layers 50 and 52 is under tensile strain, such as by using AlGaN, AlN, or AlInGaN. Each of layers 50 and 52 may be, for example, at least 1 nm thick in some embodiments and no more than 50 nm thick in some embodiments. The total thickness of the superlattice may be at least 10 nm thick in some embodiments and no more than 1000 nm thick in some embodiments.

In some embodiments, NTS 26 is spaced apart from active region 30. For example, NTS 26, which may be any of the NTSs described above, may be spaced apart from the active region 30 by n-type region 28. NTS 26 may be spaced at least 500 nm from the active region 30 in some embodiments, at least 1 micron from the active region 30 in some embodiments, and no more than 5 microns from the active region 30 in some embodiments. NTS 26 is grown before the active region of the device, such that NTS 26 is included in the template on which the active region 30 is grown. After growth, the orientation may be maintained, such that the NTS is located below the active region, or the device may be flipped over, such that the NTS is located above the active region.

In some embodiments, the active region is disposed between an n-type region and a p-type region. Metal contacts are formed on the n- and p-type regions in order to forward bias the active region. In some embodiments, no metal contacts are formed on the NTS such that the NTS is not intentionally electrically active in the device, meaning that the NTS is not in the direct path of electrons and holes flowing through the semiconductor structure from the contacts. Some current may inadvertently flow into or through the NTS in some embodiments.

The semiconductor structures illustrated in Figs. 3, 4, 5, and 6 may be formed into any appropriate device. Fig. 7 illustrates one example of an appropriate device, a flip chip. The semiconductor structure 70 may include one or more of a nucleation layer 12, high temperature layer 16, NTS 26, n-type region 28, active region 30, and p-type region 32, and may include any combination of these structures or features of these structures described above. A metal p-contact 60 is formed on the p-type region. If a majority of light is directed out of the semiconductor structure through a surface opposite the p-contact, the p-contact 60 may be reflective. A flip chip device may be formed by patterning the semiconductor structure by standard photolithographic operations and etching the semiconductor structure to remove a portion of the entire thickness of the p-type region and a portion of the entire thickness of the light emitting region, to form a mesa which reveals a surface of the n-type region on which a metal n-contact 62 is formed. The p- and n-contacts are electrically isolated from each other by a gap 64, which may be filled with a dielectric material. The mesa and p- and n-contacts may be formed in any suitable manner. Forming the mesa and p- and n-contacts is well known to a person of skill in the art. Substrate 10 may be removed or thinned, or may remain part of the device, as illustrated in Fig. 7. If substrate 10 is removed, any or all of nucleation layer 12, high temperature layer 16, and NTS 26 may be removed or thinned.

In some embodiments, metal contacts may be formed on both the NTS and the high temperature region, such that the NTS may form part of a secondary electrical protection circuit, such as an electrostatic discharge protection circuit. Fig. 8 illustrates a cross section of a device including an NTS that forms part of an electrostatic discharge protection circuit. Fig. 9 is a circuit diagram of the structure illustrated in Fig. 8. In the device of Figs. 8 and 9, the NTS 26 is electrically connected to the n-type region 28, and the p-type region 32 is electrically connected to the high temperature layer 16, such that the NTS 26 and high temperature layer 16 form an electrostatic discharge (ESD) protection diode connected anti-parallel to the diode formed by the n-type and p-type regions 28 and 32 that surround the active region 30. First and second metal contacts 64 and 66 are formed on NTS 26 and high temperature layer 16 respectively, as illustrated in Fig. 8. Mesas, in addition to the mesa which exposes the n-type region on which contact 62 is formed, may be etched to expose NTS 26 on which contact 64 is formed, and to expose high temperature layer 16 on which contact 66 is formed. The electrical connection 80 between contacts 62 and 64 and the electrical connection 82 between contacts 60 and 66 may be metal layers formed on the chip with appropriate dielectric isolation layers, or may be formed on a mount through external circuitry.

The LED in Figs. 8 and 9 includes n-type region 28, active region 30, and p-type region 32. The LED is forward biased by applying current to metal contacts 60 and 62, electrically connected to p-type region 32 and n-type region 28, respectively. The ESD protection diode includes high temperature layer 16 and NTS 26, which are connected to metal contacts 66 and 64, respectively.

Fig. 9 is a circuit diagram of the device illustrated in Fig. 8. LED 90 and electrostatic discharge protection diode 88 are illustrated in Fig. 9. Arrow 84 illustrates current flow during normal LED operation. Arrow 86 illustrates current flow during an electrostatic discharge event.

Though in the examples below the semiconductor light emitting device are III-nitride LEDs that emits blue or UV light, semiconductor light emitting devices besides LEDs such as laser diodes may be within the scope of the invention.

Having described the invention in detail, those skilled in the art will appreciate that, given the present disclosure, modifications may be made to the invention without departing from the spirit of the inventive concept described herein. Therefore, it is not intended that the scope of the invention be limited to the specific embodiments illustrated and described.

CLAIMS:

1. A device comprising:

a III-nitride light emitting layer disposed between an n-type region and a p-type region; and

a III-nitride layer doped with an acceptor, wherein the n-type region is disposed between the III-nitride layer doped with an acceptor and the light emitting layer.

2. The device of claim 1 further comprising a layer comprising a nanopipe defect, wherein the III-nitride layer doped with an acceptor is disposed between the layer comprising a nanopipe defect and the light emitting layer, wherein the nanopipe defect terminates in the III-nitride layer doped with an acceptor.

3. The device of claim 1 wherein the acceptor is magnesium.

4. The device of claim 3 where the III-nitride layer doped with an acceptor is electrically connected in common with the n-type layer.

5. The device of claim 1 wherein the III-nitride layer doped with an acceptor is a first magnesium-doped layer, the device further comprising a second magnesium doped layer disposed between the first magnesium-doped layer and the light emitting layer.

6. The device of claim 5 wherein the first magnesium-doped layer is doped to a lower magnesium concentration than the second magnesium-doped layer.

7. The device of claim 1 further comprising a layer comprising aluminum disposed between the III-nitride layer doped with an acceptor and the III-nitride light emitting layer.

8. The device of claim 1 wherein the III-nitride light emitting layer is spaced at least 1 micron from the III-nitride layer doped with an acceptor.

9. A device comprising:

a III-nitride light emitting layer disposed between an n-type region and a p-type region;

a III-nitride layer comprising a nanopipe defect; and

a nanopipe terminating layer disposed between the III-nitride light emitting layer and the III-nitride layer comprising a nanopipe defect, wherein the nanopipe terminates in the nanopipe terminating layer.

10. The device of claim 9 wherein the nanopipe terminating layer comprises aluminum.

11. The device of claim 10 wherein the nanopipe terminating layer contains magnesium.

12. The device of claim 9 wherein the nanopipe terminating layer comprises a superlattice, the superlattice comprising a plurality of alternating first and second layers.

13. The device of claim 12 wherein the first layers are GaN and the second layers are $Al_xGa_{1-x}N$ where $0 < x \leq 1$.

14. The device of claim 12 wherein the first layers are $Al_bGa_{1-b}N$ and the second layers are $Al_cGa_{1-c}N$, wherein $b \neq c$.

15. The device of claim 9 wherein the III-nitride light emitting layer is spaced at least 1 micron from the nanopipe terminating layer.

16. The device of claim 9 wherein the nanopipe terminating layer is electrically connected in common with the n-type layer.

17. The device of claim 9 wherein the nanopipe terminating layer is electrically connected in common with the n-type layer.

18. The device of claim 9 wherein the nanopipe terminating layer comprises part of an electrostatic discharge protection circuit.

19. A method comprising:

growing a III-nitride layer over a growth substrate, wherein the III-nitride layer comprises a nanopipe defect;

growing a nanopipe terminating layer over the III-nitride layer, wherein the nanopipe terminates in the nanopipe terminating layer; and

growing a III-nitride light emitting layer over the nanopipe terminating layer.

20. The method of claim 19 wherein the III-nitride layer is grown at a first temperature and the nanopipe terminating layer is grown at a second temperature, wherein the second temperature is 100 to 200 °C less than the first temperature.

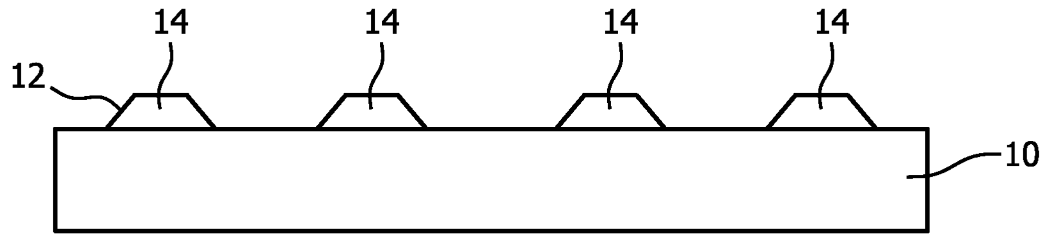


FIG. 1

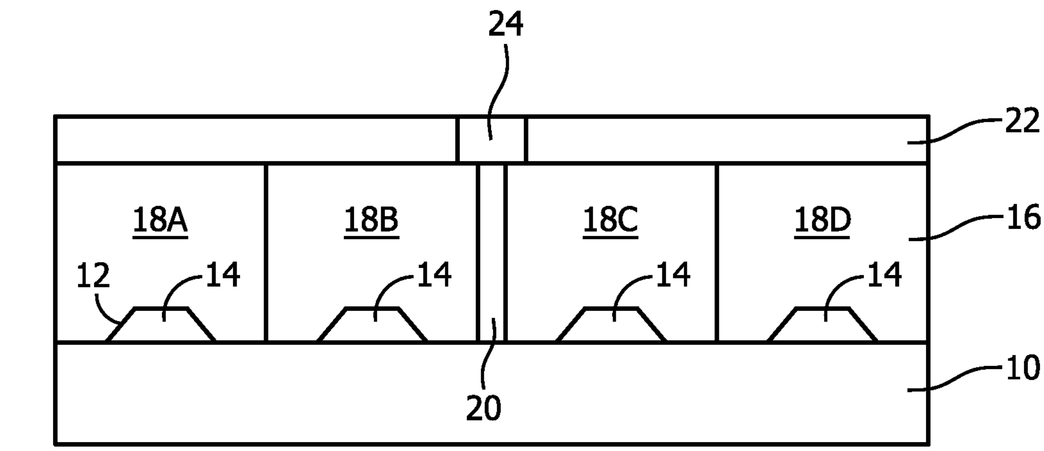


FIG. 2

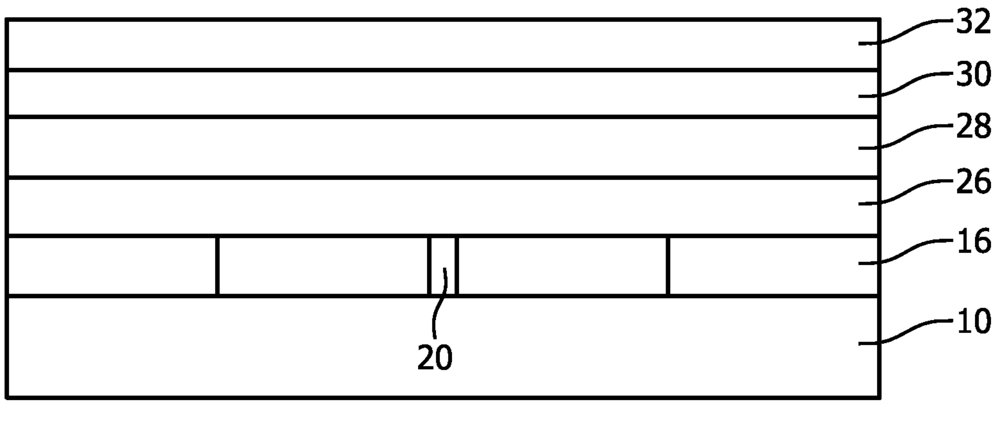


FIG. 3

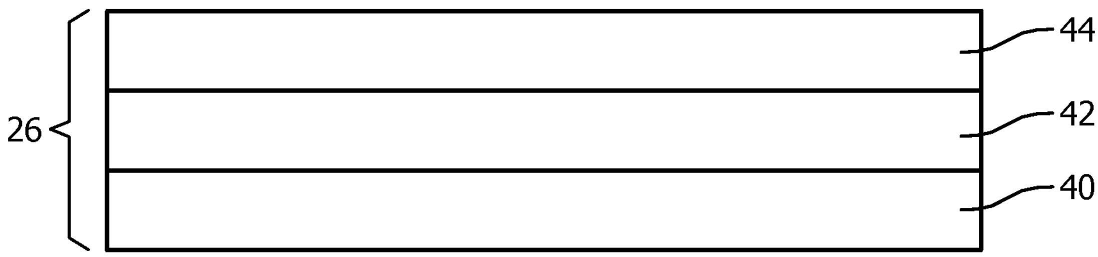


FIG. 4

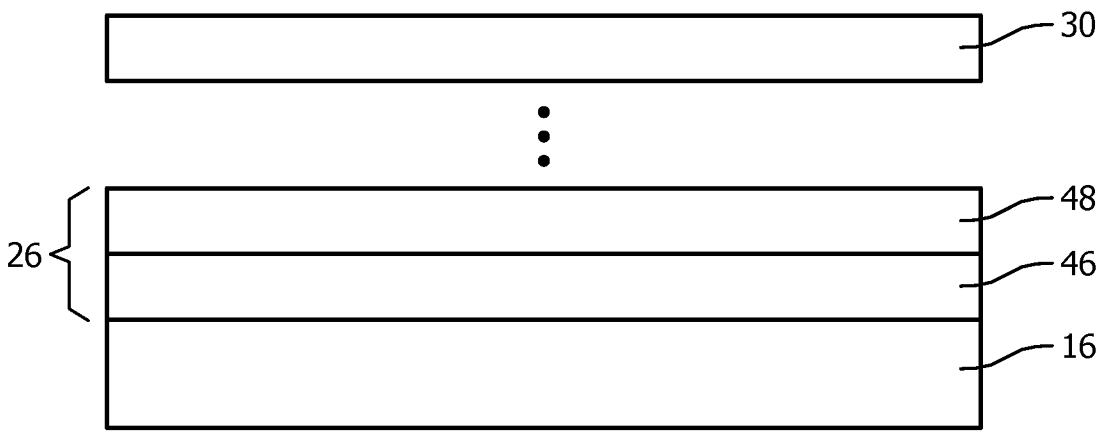


FIG. 5

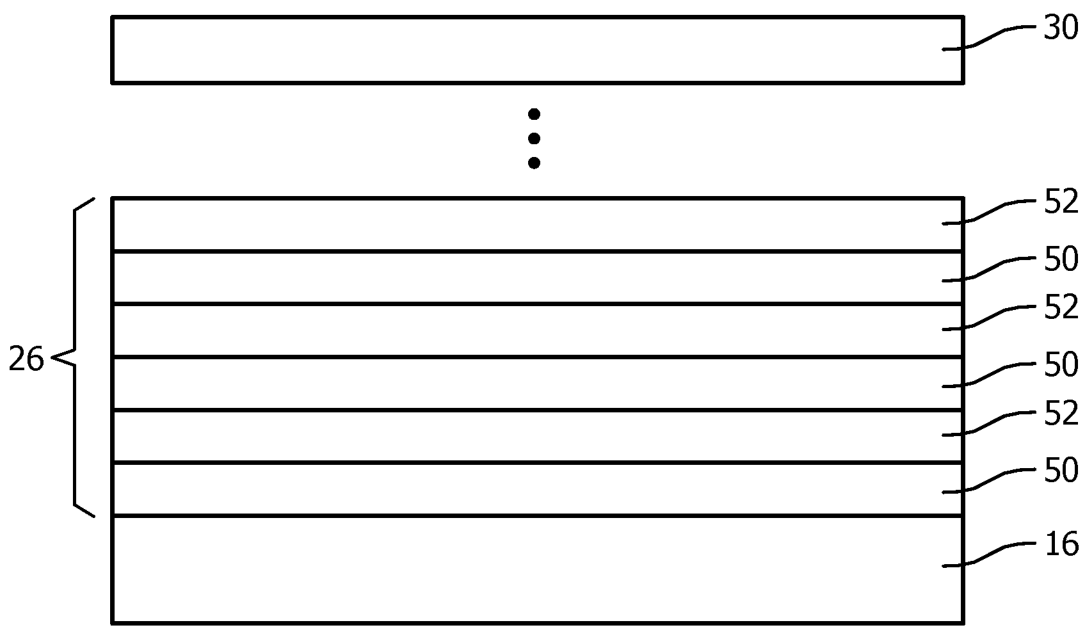


FIG. 6

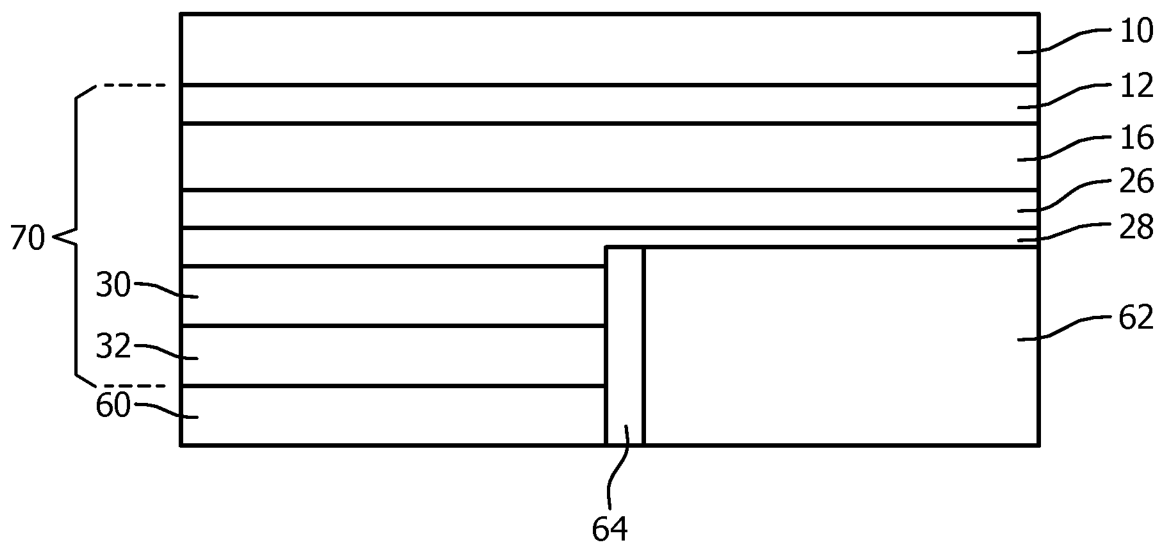


FIG. 7

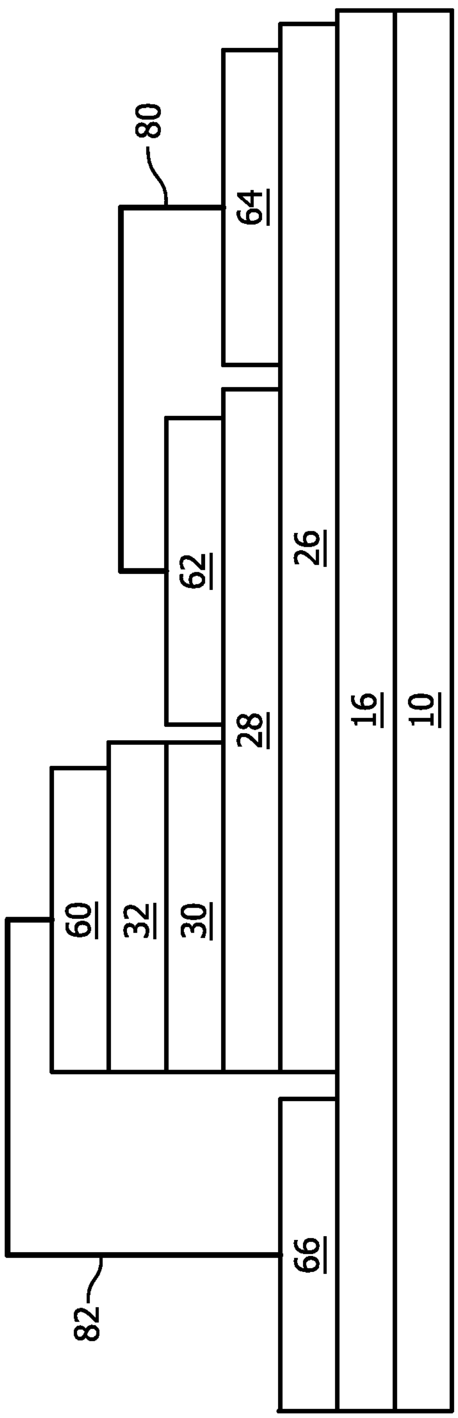
80
64
62
26
28
60
32
30
16
10
66
82

FIG. 8

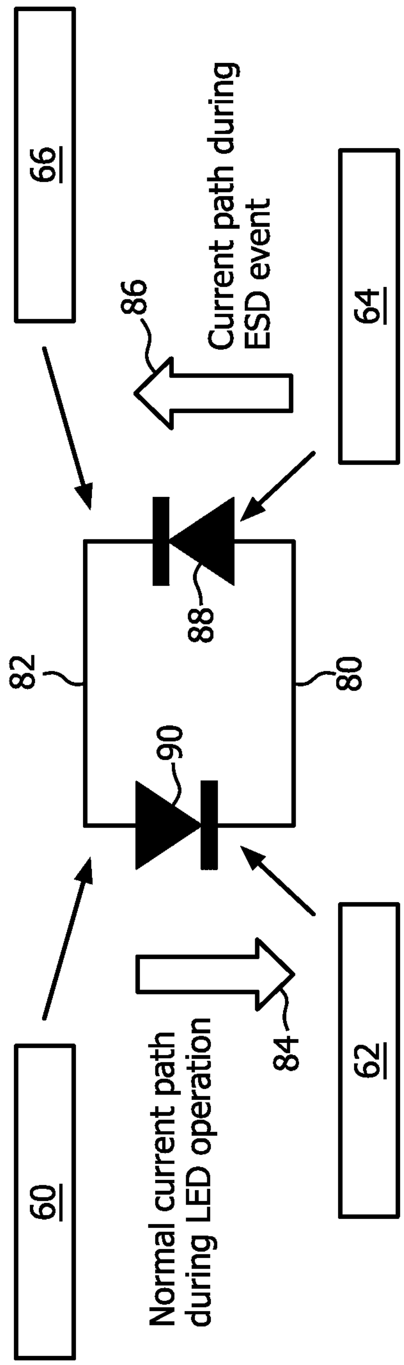
66
86
Current path during ESD event
64
82
88
80
90
60
Normal current path during LED operation
84
62

FIG. 9

# INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2013/055446

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L33/00 H01L33/02 H01L33/12
ADD. H01L33/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 6 194 742 B1 (KERN R SCOTT [US] ET AL) 27 February 2001 (2001-02-27) column 2, line 63 - column 3, line 57; figure 3 | 1,3,4,8 |
| X | DE 10 2009 060749 A1 (OSRAM OPTO SEMICONDUCTORS GMBH [DE]) 7 July 2011 (2011-07-07) | 9,10, 15-20 |
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 5 November 2013 | 12/11/2013 |

| Name and mailing address of the ISA/ | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040,<br>Fax: (+31-70) 340-3016 | Ott, André |

# INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2013/055446

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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International application No
PCT/IB2013/055446

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