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RELAY SHIFT REGISTER

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This invention relates to a relay circuit organization, and more particularly pertains to a relay shift register.

In various code pulse systems, it frequently is desirable to place a serially received train of code pulses into a storage device for later use or to make it available for decoding purposes. Also, such a stored code is often required to be transformed again to its original serial form in which the code pulses appear in a time-spaced pattern. These functions are all performed efficiently by an organization known as a shift register. Shift registers of the electronic type have been developed in various forms using electronic tubes of the evacuated and gas discharge type and of the grid glow type. According to the present invention, however, it is proposed to provide a shift register comprising electromagnetic relays, with only one relay required for each code digit to be stored.

Described briefly, the first of the bank of relays in the shift register has applied to it the sequence of code pulses constituting a received code. On each pulse period that a code pulse is actually received, the relay is actuated; when no code pulse is received, the relay remains in its original dropped away condition. In the interval between the first and second pulse periods, the information as to the condition of the first relay is transferred to a storage capacitor, and the first relay is at the same time restored to its initial state so that it can be selectively actuated again in accordance with whether a code pulse is received on the second pulse period. At the time of the second pulse period, not only is the first shift register relay selectively actuated, but the storage capacitor associated with the first relay is then connected to a winding of the second relay so as to selectively actuate this second relay. Therefore, actuation of the second relay is dependent upon whether the first relay had been picked up in the first pulse period.

A storage capacitor is associated with each of the various shift register relays so that, in a manner similar to that just described, the condition of each relay on a particular pulse period is transferred to the next relay on the next pulse period. Thus, a serially received code of pulses applied to the first relay is sequentially stepped into the shift register. When the whole code has been received, the last-received digit is then stored in the first shift register relay while the first code pulse received has, in the mean while, been stepped through all the relays and is then stored in the last relay of the shift register. The permutation of the conditions of the relays then provide information as to the intelligence then stored. Also, by continuing to shift the then-stored code, the code may be shifted out of the shift register. An output relay may be selectively actuated in accordance with the character of the successive digits as they are stepped out of the register so that the selective actuation of this output relay represents the stored code in its serial form.

An object of this invention, therefore, is to provide a shift register circuit organization comprising only a single electromagnetic relay for each code digit to be stored.

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An additional object of this invention is to provide a shift register having one relay for each stored digit of a code and including also capacitors associated with each relay for temporarily storing during the interval between successive pulse periods the code character placed in the relay on the preceding pulse period.

An additional object of this invention is to provide a relay shift register having an output relay whose selective actuations provide a serial code representing the stored digits when a stored code is stepped out of the shift register.

Other objects, purposes and characteristic features of this invention will be apparent from the accompanying drawing and also pointed out as the description of the invention progresses.

In describing this invention in detail, reference will be made to the accompanying drawing in which:

Fig. 1 illustrates a relay shift register; and

Fig. 2 is a code chart for illustrating the manner of operation of this invention.

To simplify the illustration and facilitate the explanation of this invention, the various parts and circuits that constitute the embodiment of this invention are shown diagrammatically and certain conventional illustrations are used. The drawing has been made to make it easy to understand the principles and manner of operation rather than to illustrate the specific construction and arrangement of parts that would be used in practice. The various relays and their contacts are shown in a conventional manner, and symbols are used to indicate connections to the opposite terminals of batteries or other sources of direct current instead of showing all the wiring connections to these terminals.

Fig. 1 shows a typical relay shift register having five shift register relays designated SR1 to SR5 inclusive, providing for the storage of a code constituting five spaced pulse periods. Each of these relays is of the neutral type having two independent windings, and the energization of either winding causes the relay armature to pick up.

A serially received code is applied to the shift register from the input coding means 10. This input coding means provides for the operation of the pulse coding relay PCR and the pulse demarcating relay PDR in the manner designated in Fig. 2. For each pulse of one kind, termed for convenience a "mark," the pulse coding relay PCR is picked up. On each pulse period that the opposite type of character is received, the relay PCR remains dropped away. This type of character may conveniently be termed a "space." In Fig. 2, the relay PCR is shown as being selectively actuated in accordance with a code constituting the following successive characters; mark, mark, space, mark, mark.

The pulse demarcating relay PDR operates on each pulse period, regardless of the type of character then being received, thereby demarcating the beginning and end of each pulse period. The input coding means 10 is illustrated in Fig. 2 as causing relay PCR, when operated on a particular pulse period, to pick up in coincidence with the pulse demarcating relay PDR. In other words, if a mark pulse is received on a particular pulse period, the relay PCR picks up at the same time that the relay PDR picks up. This coincidence in operation of the relays PCR and PDR is not required for proper operation, however. It is only necessary that there be some overlap in their operation so that if relay SR1 is picked up by the picking up of relay PCR, a stick circuit to hold relay SR1 picked up will be established by picking up relay PDR before relay PCR drops away. Furthermore, it has been shown that the interval between successive pulse periods is equal in duration to each pulse period. This equality is not essential, however, and it will be apparent as the description of the invention progresses

that the interval between successive pulse periods may vary widely and independently of the length of the pulse periods themselves and that it is not essential for the duration of the pulse periods nor of the intervals between them to be of uniform duration throughout the reception of a particular code.

When the shift register is in a passive state, i.e. a code is neither being stepped into or out of the shift register, the relay D is dropped away since it is then not being intermittently energized through front contact 11 of relay PDR. As a result, each of the contacts 12—16 of relay D are closed thereby providing a direct shunt from wire 17 to each of the wires 18—22. The purpose of providing this shunt is to discharge the capacitors associated with each relay after a code has been fully stored in the shift register as will later be apparent. When it is desired to step a new code into the shift register, it is necessary that these shunts be removed. Thus, the picking up of relay D upon the first actuation of relay PDR, results in opening of all of these back contacts 12—16 to cause the removal of these shunts. Relay D has slow release characteristics so that the intermittent operation of relay PDR during a code stepping operation causes relay D to remain picked up.

Assuming that the first code digit received is a mark as illustrated in Fig. 2, the picking up of the pulse coding relay PCR in response to this mark results in the closing of front contact 23 which causes energy to be applied to the lower winding of relay SR1 so that this relay picks up. Relay PDR picks up at this time also which causes the closure of its front contact 24 so that a stick circuit is immediately established through front contact 25 of relay SR1 to energize the upper winding of this relay.

As soon as relay SR1 has picked up, a circuit is completed to charge capacitor 26. This charging circuit extends from (+) and includes front contact 27 of relay PDR, capacitor 26, front contact 28 of relay SR1, and current limiting resistor 29, to (-). The time constant provided in this circuit is sufficiently short to insure that capacitor 26 will be fully charged in the interval of the pulse period during which the stick circuit maintains relay SR1 in its picked-up condition.

At the end of the pulse period, relay PCR drops away, thereby opening its front contact 23 which deenergizes the lower winding of relay SR1. At the same time, the stick circuit effective on the upper winding is also deenergized by the opening of front contact 24 of the pulse demarcating relay PDR. When this happens, relay SR1 drops away. This causes back contact 28 of relay SR1 to close so that capacitor 26 is then connected directly in parallel with capacitor 30. Capacitor 30 is initially discharged as was capacitor 26 prior to the reception of the first code pulse. The now charged capacitor 26 transfers some of its charge to capacitor 30, and such transfer continues until the voltage across the two capacitors 26 and 30 is equal. In effect, capacitor 30 now stores the information that relay SR1 was picked up on the last preceding pulse period by a mark pulse received in the input code.

Fig. 2 indicates that on the second pulse period another mark is received. As before, this results in the picking up of relay SR1 so that capacitor 26 can again be charged. The closing of front contact 27 of relay PDR now not only provides for the completion of the charging circuit for capacitor 26 but also causes the charged capacitor 30 to be connected across the lower winding of relay SR2. More specifically, the charging of capacitor 26 resulted in a voltage across this capacitor causing its right-hand terminal to become positive with respect to its left-hand terminal. In the "off" period between successive pulse periods, the capacitor 30 also became charged with a polarity causing its right-hand terminal to become positive with respect to its left-hand terminal. Upon the closure of front contact 27 of relay PDR, a circuit is completed causing current to flow from the positive or

right-hand terminal of capacitor 30 over wire 17, front contact 27, to the (+) terminal, and from this (+) terminal, through the lower winding of relay SR2, to the left-hand terminal of capacitor 30. This flow of current from left to right through the lower winding of relay SR2 causes it to be picked up. Immediately upon its picking up, a stick circuit is completed through its front contact 31 to hold it energized throughout that pulse period.

As a result, during the second pulse period, the character that was stored in relay SR1 on the first pulse period is transferred to relay SR2 in the sense that this relay will be picked up during the second pulse period if relay SR1 had been picked up during the first pulse period in response to the code received on that pulse period.

As soon as relay SR2 picks up on the second pulse period, its capacitor 32 is charged through the closed front contact 33 of relay SR2. Thus, at the end of the second pulse period, both capacitors 26 and 32 are charged so they store the information that the relays SR1 and SR2 were both in picked-up conditions during the second pulse period.

For the typical code shown in Fig. 2, a space character is shown for the third pulse period. This is illustrated diagrammatically by showing that the relay PCR does not pick up on the third pulse period. Consequently, there is no circuit completed on this third pulse period to energize relay SR1 so that this relay remains in its released condition. The picking up of relay PDR to demarcate the beginning of the third pulse period causes the charged capacitor 30 to be connected across the lower winding of relay SR2 so that this relay will again be picked up. The closure of front contact 27 also causes the charged capacitor 34 to be connected across the lower winding of relay SR3 so that this relay is also picked up. In this third pulse period, therefore, the relay SR1 does not become picked up but the two relays SR2 and SR3 are picked up.

With the picking up of relays SR2 and SR3, the capacitors 32 and 35 associated with these relays, respectively, become charged. Since relay SR1 is not picked up, however, the capacitor 26 cannot become charged. At the end of the third pulse period, therefore, when relays SR2 and SR3 are dropped away, the charge on the capacitors 32 and 35 is transferred partially to the parallel capacitors 34 and 36, respectively. Since capacitor 26 is not charged, however, the capacitor 30 cannot become charged. As a result, at the beginning of the fourth pulse period, the closure of front contact 27 of relay PDR, which causes the capacitors 30, 34 and 36 to be connected across the windings of relays SR2, SR3 and SR4, respectively, will result in the picking up of the two relays SR3 and SR4 but cannot result in the picking up of relay SR2 since the capacitor 30 has no charge which can provide the required energy for picking up relay SR2.

On the fourth pulse period, relay SR1 also is picked up since Fig. 2 indicates that a mark occurs on the fourth pulse period. In a manner similar to that described, the status of each relay is shifted on the fifth pulse period to the relay immediately adjoining it on the right. For the five shift register relays shown in Fig. 1, the occurrence of a fifth pulse period indicates that a complete code for filling the shift register has been received. The first code character occurring on the first pulse period is stored in relay SR5 and the last character received on the fifth pulse period is then stored in relay SR1. The other code characters are stored in the intermediate relays SR2—SR4.

When the full code is stored in the shift register, the pulse demarcating relay is maintained in its picked-up condition so that current can be supplied through its front contact 24 to hold any shift register relay then picked up in that condition for as long as desired. The shift register is cleared out by releasing relay PDR which opens the stick circuits for the relays and causes them all to drop away.

If it is desired to transfer the code stored in the shift register relays out of the shift register, this is readily

accomplished by actuating the pulse demarcating relay PDR to demarcate successive pulse periods. From the description already given, it is clear that for each picking up and successive dropping away of relay PDR, the condition of each shift register relay will be transferred to the one on its right. For example, for the code assumed to be stored in the shift register according to Fig. 2, the dropping away of relay PDR the first time results in a transfer of charge between the two capacitors associated with any shift register relay if that relay was picked up in accordance with the code then stored. With relay SR5 picked up as a result of a mark having occurred as the first element of the code as shown in Fig. 2, the dropping away of relay PDR causes the shifting of contact 60 of relay SR5 and thus causes the charged capacitor 37 to transfer some of its charge to the associated parallel capacitor 38. The subsequent picking up of relay PDR then causes the shifting of the code, at which time the charged capacitor 38 is connected across a lower winding of the output relay OR through front contact 27 of relay PDR so that relay OR will be picked up. At the same time, the fact that relay SR4 had been picked up in response to the received code results in the picking up of relay SR5. Relay SR4, however, is not reenergized when the shifting takes place because the third code character received on the third pulse period had been a space as previously registered by relay SR3 being deenergized, requiring that this relay SR3 remain dropped away and fail to charge capacitor 35. Therefore, just as occurred when the code was originally stepped into the shift register, the first actuation of relay PDR transfers the condition of each relay to the next relay on the right so that relay OR is selectively actuated successively according to the condition of relay SR5 during the preceding step. This causes the relay OR to repeat the code characters successively, being picked up for mark characters, and remaining dropped away for space characters. Relay OR applies an output through its front contact 39 from the battery 40 to output terminals 41. The output terminals 41 may be connected to any type of control or communication apparatus.

Each subsequent actuation of relay PDR steps the code along one more digit with the result that relay OR is operated alternately between its two conditions according to the code stored in the shift register. In such a stepping out operation, the relay PCR is not operated so that relay SR1 is not picked up at any time. Consequently, when the code character originally stored in relay SR1 has been stepped through the shift register and finally is stored in the output relay OR, the shift register has been entirely cleared of its stored code so that all its relays are released.

As an alternative, it is possible to feed another code into the shift register in the same manner as the first by selectively energizing the relay PCR on each of the pulse periods as demarcated by the pulse demarcating relay PDR. In that event, the originally stored code is stepped out of the shift register by the intermittent actuation of relay PDR and a new code is at the same time stepped into the shift register according to the selective actuation of relay PCR.

As still another alternative, it is possible to step a stored code out of the shift register to thereby make it available as a time spaced code and yet conclude such an operation with the original code still stored in the shift register. Thus, the intermittent operation of the output relay may, as it selectively closes its front contact 39, cause energy to be applied from battery 40 to the output terminal 41. At the same time, if the lever 42 is moved to its right-hand position, each closure of front contact 43 of relay OR will cause energy to be applied over wire 44 to the lower winding of relay SR1. In this way, the output code appearing sequentially in relay OR is fed back into the shift register via relay SR1 so that when the entire code has been stepped through relay OR, it has, at the same

time, been fed back into the shift register so that it will appear again in the relays SR1—SR5.

It is at times desirable to place an entire code simultaneously in the shift register rather than to feed it in as a time-spaced code through relay PCR. To accomplish this, the parallel code read-in circuits 45 are provided. These provide for the selective energization of the wires 46—50 in accordance with the code pattern that is to be established in the shift register. Energization of any wire, such as wire 49, results in the picking up of the associated relay, such as relay SR4. A code placed in the shift register in this manner can be stepped out of the shift register through operation of the pulse demarcating relay PDR exactly in the manner already described.

Any stepping operation of the shift register, whether it involves the placing of a time spaced code in the shift register or the stepping of a code out of the shift register involves the operation of the pulse demarcating relay PDR. While this occurs, the intermittent closure of front contact 11 provides intermittent energization of relay D. Since this relay is provided with slow release characteristics, it remains picked up during such stepping operation. However, as soon as the code stepping has ceased, the relay D drops away and closes all its back contacts 12—16. The closure of these contacts connects the wire 17 to each of the wires 18—22 to thereby short circuit all of the capacitors associated with the shift register relays. This discharges all these capacitors so that subsequent operation of the shift register will not be improperly affected by spurious charges retained in any of the capacitors.

Various operating rates of the shift register may be employed, and the particular value selected is dependent upon the characteristics of the relays, the capacitors, and the voltage employed. Thus, the length of a pulse period must be sufficient to charge the capacitor such as capacitor 26 and also to permit the picking up of any relay such as relay SR2 in response to the charge appearing on a corresponding capacitor such as capacitor 30. The pulse period must also be long enough so that a charged capacitor will not only be able to pick up the relay for the next succeeding digit but will also result in effectively discharging such capacitor so that it will not be effective to operate the relay on the next pulse period if such operation is not called for according to the code. The interval between successive pulse periods must be long enough to permit the required transfer of charge from one capacitor to the other, such as from capacitor 26 to the corresponding capacitor 30.

Having described a relay shift register as one specific embodiment of our invention, we desire it to be understood that various other forms, adaptations and modifications can be made to the structure shown to meet the requirements of practice without departing from the spirit or scope of this invention.

What we claim is:

1. A relay shift register for a multiple digit code having pulses appearing selectively on successive time-spaced pulse periods comprising, an electromagnetic relay for each pulse period of said code, circuit means responsive to each of said pulses for selectively energizing or maintaining deenergized a first of said relays, stick circuit means including a contact operated by each relay effective to maintain said relay energized when once picked up on a pulse period only throughout the duration of that pulse period, a source of direct current, a first capacitor provided for each relay and becoming charged from said source through a contact of the associated relay closed when the associated relay is picked up, a second capacitor provided for each relay and being connected in multiple with said first capacitor for the associated relay through a contact of the associated relay closed when the associated relay is dropped away, circuit means effective during each pulse period to connect said second capacitor associated with each relay through the winding of the next one of said

relays of the register in a predetermined order, whereby storage of selected code digits serially applied to a first relay of the shift register is stepped sequentially through said relays at a rate comparable to the rate of reception of the time-spaced pulses.

2. A relay shift register for a multi-digit code comprising pulses appearing selectively during successive time-spaced pulse periods of said code and including, an electromagnetic relay for each pulse period of said code, circuit means responsive to each of said pulses for selectively energizing or maintaining deenergized the first of the said relays, stick circuit means including a contact operated by each relay effective to maintain said relay energized when once picked up during a pulse period only throughout the duration of said pulse period, first and second storage capacitors provided for the respective magnetic relays, a source of direct current energy, said first capacitor associated with each relay becoming charged from said source through a contact of the associated relay when the associated relay is picked up, said first capacitor being connected in parallel with said second capacitor for the associated relay through a contact of the associated relay closed when the associated relay is dropped away at the end of a pulse period, circuit means effective on each pulse period to connect said second capacitor across a winding of the next succeeding relay thereby causing said next relay to pick up only if said second capacitor is then in a charged condition, whereby a distinctive code serially applied to the first of said shift register relays is stepped sequentially through said relays one at a time as the respective digits of the code are applied to said first relay.

3. In a shift register for registering a plurality of pulse periods during which distinctive code pulses appear selectively, an electromagnetic relay for each pulse period of said code, input circuit means for selectively energizing or maintaining deenergized the first of said relays on each pulse period on which a code pulse occurs, pulse demarcating circuit means effective to provide a stick circuit including a contact operated by each relay effective to maintain said relay energized when once picked up on a pulse period only throughout the duration of that pulse period, first and second storage capacitors provided for the respective electromagnetic relays, a source of direct current energy, said first capacitor being charged by said direct current source through a contact of its associated relay closed when the associated relay is picked up, said first capacitor being connected in parallel with said second capacitor for the associated relay through a contact of the associated relay closed when the associated relay is dropped away at the end of a pulse period by said pulse demarcating means, said pulse demarcating circuit means being also effective to connect said second capacitor across the winding of the next associated relay during a pulse period thereby causing said next relay to pick up only if said second capacitor had received a charge from said first capacitor in the interval between said pulse period and the immediately preceding pulse period, whereby on each pulse period the particular condition of said shift register relay representative of storage of a code element is transferred to the next succeeding relay.

4. A relay shift register for registering a multi-digit code having pulses appearing selectively on successive time-spaced pulse periods and comprising, an electromagnetic relay for each of said pulse periods, circuit

means responsive to each of said pulses for energizing or maintaining deenergized the first of said relays selectively in accordance with the code digit appearing during that pulse, stick circuit means including a contact operated by each relay effective to maintain said relay energized when once picked up on a pulse period only throughout the duration of that pulse period, first and second storage capacitors provided for the respective electromagnetic relays, a source of direct current energy, said first capacitor being charged by said source through a contact of the associated relay closed when the associated relay is picked up, said first capacitor being connected in parallel with said second capacitor through a contact of the associated relay closed when the associated relay is dropped away, circuit means effective on each pulse period to connect said second capacitor across a winding of the next succeeding relay thereby causing said next relay to pick up only if said second capacitor is then in a charged condition, and an output relay having connected across its winding on each pulse period said second capacitor associated with the last of said shift register relays, whereby a distinctive code serially applied to the first of said shift register relays is stepped sequentially through said relays one at a time on successive pulse periods and on successive pulse periods said output relay is selectively actuated in accordance with the input code originally applied to the first of said shift register relays.

5. A shift register for a multi-digit code comprising pulses appearing selectively on successive spaced pulse periods of said code and including, an electromagnetic relay for each of said pulse periods, circuit means for selectively actuating said relays in accordance with a particular code desired to be stored in said relays, pulse demarcating circuit means effective to provide a stick circuit including a contact operated by each relay effective to maintain said relay energized when once picked up on a pulse period only throughout the duration of said pulse period, a source of direct current energy, a first capacitor provided for each relay and becoming charged by said direct current source through a contact of the associated relay closed when the associated relay is picked up, a second capacitor also provided for each relay and connected in parallel with said first capacitor through a contact of the associated relay closed when the associated relay is dropped away at the end of a pulse period, circuit means effective on each pulse period to connect said second capacitor provided for each relay across a winding of the next relay to thereby cause the actuation of said relay only if said second capacitor is then in a charged condition, and circuit means governed by said pulse demarcating circuit means and being effective when said pulse demarcating circuit means is not intermittently actuated during a code shifting operation to shunt said first and said second capacitors associated with said relays to thereby discharge said capacitors.

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