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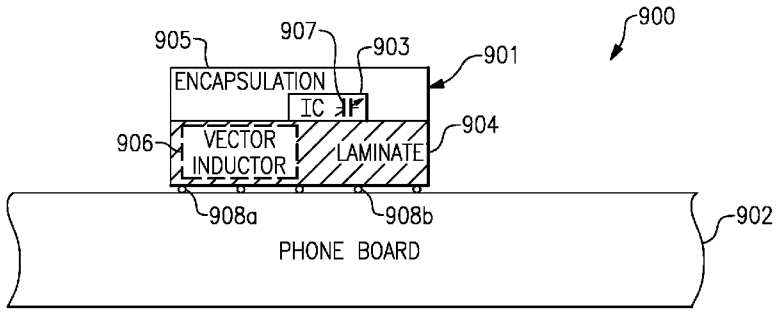


FIG.19

(57) Abstract: Apparatus and methods for tunable filters are provided. In certain configurations, a tunable filter includes a semiconductor die attached to a laminated substrate, such as a substrate of a multi-chip module (MCM). The tunable filter includes a vector inductor implemented using two or more conductors arranged on different conductive layers of the laminated substrate. The vector inductor's conductors are inductively coupled to one another and electrically connected in parallel to provide the vector inductor with high quality factor (Q-factor). The semiconductor die includes a variable capacitor that is electrically connected with the vector inductor to operate as a tunable resonator. Additionally, a frequency characteristic of the tunable filter, such as a passband, can be controlled by selecting a capacitance value of the variable capacitor, thereby tuning a resonance of the resonator.

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APPARATUS AND METHODS FOR TUNABLE FILTERS

BACKGROUND

Field

[0001] Embodiments of the invention relate to electronic systems and, in particular, to tunable filters for radio frequency (RF) electronics.

Description of the Related Technology

[0002] A radio frequency (RF) system can include filters for filtering RF signals. For example, an RF front-end can include one or more filtering structures, such as surface acoustic wave (SAW) filters, bulk acoustic wave (BAW) filters, and/ or thin film bulk acoustic resonators (FBARs).

[0003] The filters can be used to provide filtering to particular RF bands or channels. For example, the filters can have a fixed filtering characteristic versus frequency, such as a passband positioned to pass a particular band or channel while attenuating other bands or channels.

SUMMARY

[0004] In one aspect, a tunable filter includes a laminated substrate and a semiconductor die. The laminated substrate includes a first vector inductor. The first vector inductor includes a stack of conductors including two or more conductors arranged on different conductive layers of the laminated substrate. Each of the different conductive layers is separated by a dielectric. The two or more conductors are electrically connected to one another along a first side of the stack, and the two or more conductors are electrically connected to one another along a second side of the stack opposite the first side. The semiconductor die is attached to the laminated substrate, and includes a first variable capacitor. The first variable capacitor and the first vector inductor are electrically connected to operate as a first tunable resonator.

[0005] In another aspect, a radio frequency system includes a phone board and a multi-chip module attached to the phone board. The multi-chip module includes a laminated

substrate including a first vector inductor integrated therein. The first vector inductor includes a stack of conductors including two or more conductors arranged on different conductive layers of the laminated substrate. Each of the different conductive layers is separated by a dielectric. The two or more conductors are electrically connected to one another along a first side of the stack, and the two or more conductors are electrically connected to one another along a second side of the stack opposite the first side. The multi-chip module further includes a semiconductor die attached to the laminated substrate, and the semiconductor die includes a first variable capacitor. The first variable capacitor and the first vector inductor are electrically connected to operate as a first tunable resonator.

[0006] In another aspect, a tunable filter is provided. The tunable filter includes a substrate, a first surface mount inductor attached to the substrate, and a semiconductor die attached to the substrate. The semiconductor die includes a first variable capacitor array and a bias voltage generation circuit configured to bias the first variable capacitor array to control a capacitance of the first variable capacitor array. The first variable capacitor array includes a first plurality of metal oxide semiconductor (MOS) variable capacitor cells. The first plurality of MOS variable capacitor cells includes a first MOS variable capacitor cell including a first MOS capacitor and a second MOS capacitor. The first MOS capacitor and the second MOS capacitor are arranged in an anti-series configuration or in an anti-parallel configuration. The first variable capacitor array and the first surface mount inductor are electrically connected to operate as a first tunable resonator.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figure 1 is a schematic diagram of one embodiment of a radio frequency (RF) system.

[0008] Figure 2A is a schematic diagram of a tunable filter according to one embodiment.

[0009] Figure 2B is a schematic diagram of a tunable filter according to another embodiment.

[0010] Figure 2C is a schematic diagram of a tunable filter according to another embodiment.

[0011] Figure 3A is a schematic diagram of one embodiment of a tunable resonator array.

[0012] Figure 3B is a schematic diagram of another embodiment of a tunable resonator array.

[0013] Figure 4A is a cross section of a portion of a vector inductor according to one embodiment.

[0014] Figure 4B is a cross section of a vector inductor according to one embodiment.

[0015] Figure 5A is a perspective view of a vector inductor according to one embodiment.

[0016] Figure 5B is a plan view of a conductor of the vector inductor of Figure 5A.

[0017] Figure 6 is a plan view of a conductor of a vector inductor according to another embodiment.

[0018] Figure 7A is a cross section of a laminated substrate according to one embodiment.

[0019] Figure 7B is a cross section of a laminated substrate according to another embodiment.

[0020] Figure 8A is a plan view of a tunable filter according to one embodiment.

[0021] Figure 8B is a cross-section of the tunable filter of Figure 8A taken along the lines 8B-8B.

[0022] Figure 8C is a circuit diagram of the tunable filter of Figure 8A.

[0023] Figure 9A is a plan view of a tunable filter according to another embodiment.

[0024] Figure 9B is a cross-section of the tunable filter of Figure 9A taken along the lines 9B-9B.

[0025] Figure 9C is a circuit diagram of the tunable filter of Figure 9A.

[0026] Figure 9D is a plan view of a conductor of a vector inductor of the tunable filter of Figure 9A.

[0027] Figure 10A is a plan view of a tunable filter according to another embodiment.

[0028] Figure 10B is a cross-section of the tunable filter of Figure 10A taken along the lines 10B-10B.

[0029] Figure 10C is a circuit diagram of the tunable filter of Figure 10A.

[0030] Figure 11A is a plan view of a tunable filter according to another embodiment.

[0031] Figure 11B is a cross-section of the tunable filter of Figure 11A taken along the lines 11B-11B.

[0032] Figure 11C is a circuit diagram of the tunable filter of Figure 11A.

[0033] Figure 12 is a schematic diagram of an integrated circuit (IC) according to one embodiment.

[0034] Figures 13A and 13B are graphs of two examples of capacitance versus bias voltage.

[0035] Figure 14A is a schematic diagram of a variable capacitor cell according to one embodiment.

[0036] Figure 14B is a schematic diagram of a variable capacitor cell according to another embodiment.

[0037] Figure 15A is a schematic diagram of a metal oxide semiconductor (MOS) variable capacitor cell according to one embodiment.

[0038] Figure 15B is a schematic diagram of a MOS variable capacitor cell according to another embodiment.

[0039] Figure 16A is a graph of gain versus frequency for one example of a bandpass filter.

[0040] Figure 16B is a graph of gain versus frequency for one embodiment of a tunable filter.

[0041] Figure 16C is a graph of gain versus frequency for another embodiment of a tunable filter.

[0042] Figure 17A is a graph of gain versus frequency for another embodiment of a tunable filter.

[0043] Figure 17B is a graph of gain versus frequency for another embodiment of a tunable filter.

[0044] Figure 18 is a schematic diagram of a tunable filter according to another embodiment.

[0045] Figure 19 is a schematic diagram of another embodiment of an RF system.

DETAILED DESCRIPTION OF EMBODIMENTS

[0046] The following detailed description of certain embodiments presents various descriptions of specific embodiments of the invention. However, the invention can be embodied in a multitude of different ways as defined and covered by the claims. In this description, reference is made to the drawings in which like reference numerals may indicate identical or functionally similar elements.

[0047] Provided herein are apparatus and methods for tunable filters. In certain configurations, a tunable or programmable filter includes a semiconductor die attached to a laminated substrate, such as a substrate of a multi-chip module (MCM). The tunable filter includes a vector inductor implemented using two or more conductors arranged on different conductive layers of the laminated substrate. The vector inductor's conductors are inductively coupled to one another and electrically connected in parallel to provide the vector inductor with high quality factor (Q-factor). The semiconductor die includes a variable capacitor that is electrically connected with the vector inductor to operate as a tunable resonator. Additionally, a frequency characteristic of the tunable filter, such as a passband, can be controlled by selecting a capacitance value of the variable capacitor to tune a resonance of the resonator.

[0048] The tunable filter can be used to avoid the rigidity of a passive filtering structure. For example, in certain implementations, the tunable filter can have a frequency response characteristic that can be digitally programmed, thereby allowing the tunable filter to provide filtering for one or more frequency channels. The tunable filter can be used to reduce cost, size, and/or power of a variety of RF systems, such as RF front-ends. For example, the programmable filter can enable a mobile device such as a handset to operate using a common platform across operators and/or to operate using additional bands without re-design or a

change to hardware components. Thus, the tunable filter can facilitate faster time to market and/or reduce inventory or distribution costs. Furthermore, the tunable filter can operate over a wide range of frequencies, including frequency bands or channels associated with the proliferation of long term evolution (LTE) communications.

[0049] In certain configurations, the tunable filter can be used to provide filtering for two or more frequency carriers to provide carrier aggregation. For example, the tunable filter can two or more tunable resonators tuned to different frequency carriers, such that the tunable filter passes channels associated with two or more carriers.

[0050] The tunable filters herein can exhibit enhanced performance, such as finer frequency tuning and/or asymmetric rejection of out-of-band signals relative to certain conventional filters. For example, the tunable filter's vector inductor can include conductors inductively coupled to one another with high mutual inductance and electrically connected in parallel with one another to provide low resistance. Additionally, mutual coupling between the conductors in the stack can result in the vector inductor having an overall inductance that is similar to that of a self-inductance of an individual conductor in the stack. Accordingly, in certain implementations, a number of conductors in the vector inductor's stack may not affect the overall inductance of the vector inductor, but a vector inductor with a large number of conductors in a stack can have a lower resistance and higher Q-factor. Thus, including a vector inductor in a tunable filter can improve tuning performance.

[0051] In certain configurations, the variable capacitor is implemented using a variable capacitor array and a bias voltage generation circuit. The variable capacitor array can include a plurality of metal oxide semiconductor (MOS) variable capacitor cells, which include one or more pairs of MOS capacitors implemented in anti-parallel and/or anti-series configurations. The bias voltage generation circuit generates bias voltages for biasing the variable capacitor array, and can bias the MOS capacitors of a particular MOS variable capacitor cell at a voltage level selected from discrete number of two or more bias voltage levels associated with high linearity. For example, in certain implementations, the bias voltage generation circuit can bias a particular MOS capacitor either at a first bias voltage level associated with an accumulation mode of the MOS capacitor or at a second bias voltage level associated an inversion mode of the MOS capacitor.

[0052] The variable capacitor array can have a relatively small size, a relatively high Q-factor, a relatively high linearity, and/or a relatively low insertion loss. Thus, including a variable capacitor array in a resonator can provide finer frequency tuning and/or enhanced rejection of out-of-band signals.

[0053] Figure 1 is a schematic diagram of one embodiment of a radio frequency (RF) system 10. The RF system 10 includes a programmable duplexer 1, an antenna 2, a receive terminal RX, and a transmit terminal TX. The RF system 10 can represent a portion of a wireless device, such as a smart phone or handset. Accordingly, although not illustrated in Figure 1 for clarity, the RF system 10 can include additional components and/or circuitry.

[0054] As shown in Figure 1, the programmable duplexer 1 includes a first tunable filter 3 and a second tunable filter 4. The first tunable filter 3 includes an input electrically connected to the antenna 2 and an output electrically connected to the receive terminal RX. The first tunable filter 3 further includes a first variable capacitor 5 and a first vector inductor 7, which are electrically connected to operate as a first tunable resonator. The capacitance of the first variable capacitor 5 can control a filtering characteristic of the first tunable filter 3, such as the location in frequency of a passband. The second tunable filter 4 includes an input electrically connected to the transmit terminal TX and an output electrically connected to the antenna 2. The second tunable filter 4 further includes a second variable capacitor 6 and a second vector 8, which are electrically connected to operate as a second tunable resonator. The second variable capacitor's capacitance can be selected to control a filtering characteristic of the second tunable filter 4.

[0055] A wireless device such as a smart phone, tablet, or laptop computer can communicate over multiple frequency bands using one or more common or shared antennas. A desire to transmit at wider bandwidth and/or over different communications networks has increased a demand for the number of bands that a wireless device can communicate over. For example, a wireless device may be specified to operate using one or more of a variety of communications standards including, for example, GSM/EDGE, IMT-2000 (3G), 4G, Long Term Evolution (LTE), Advanced LTE, IEEE 802.11 (Wi-Fi), Mobile WiMAX, Near Field Communication (NFC), Global Positioning System (GPS), GLONASS, Galileo, Bluetooth, and the like. Proprietary standards can also be applicable. The complexities of multi-band

communication can be further exacerbated in configurations in which the wireless device is specified to use carrier aggregation.

[0056] Certain conventional wireless devices can include a multi-throw switch and a duplexer associated with each of the frequency bands, and the multi-throw switch can be used to selectively couple an antenna to a duplexer associated with a particular band. The duplexers can provide band filtering using, for example, passive filtering structures, such as a surface acoustic wave (SAW) filters, bulk acoustic wave (BAW) filters, and/ or thin film bulk acoustic resonators (FBARs). The multi-throw switch can be used to electrically couple the antenna to a duplexer associated with a frequency band that the wireless device is transmitting and/or receiving over at a particular time instance.

[0057] In the illustrated configuration, the programmable duplexer 1 can be configured to filter a particular frequency band by programming the first and second tunable filters 3, 4 using a control signal CNTL. For example, in certain embodiments, the capacitance value of the first variable capacitor 5 can be controlled using the control signal CNTL to control a frequency location of a passband of the first tunable filter 3, and the capacitance value of the second variable capacitor 6 can be controlled using the control signal CNTL to control a frequency location of a passband of the second tunable filter 4.

[0058] Accordingly, the programmable duplexer 1 can be used to provide the RF system 10 with multi-band capability, while avoiding a need for using a multi-throw switch and a duplexer for each frequency band. Including the programmable duplexer 1 in the RF system 10 can reduce insertion loss in transmit and/or receive paths by eliminating a need for a multi-throw switch. Furthermore, the programmable duplexer 1 can have smaller area relative to a configuration including a multi-throw switch and multiple duplexers. Thus, a wireless device that includes the programmable duplexer 1 can have a smaller form factor and/or lower cost.

[0059] In the illustrated configuration, the capacitance values of the first and second variable capacitors 5, 6 can be controlled using the control signal CNTL. In one embodiment, the control signal CNTL is received by the programmable duplexer 1 over an interface, such as a serial peripheral interface (SPI) or Mobile Industry Processor Interface radio frequency front end (MIPI RFFE) interface. Although two examples of interfaces have

been provided, other interfaces can be used. Although Figure 1 illustrates the first and second variable capacitors 5, 6 as receiving a common control signal CNTL, other configurations are possible, such as implementations in which the first and second variable capacitors 5, 6 are controlled using separate control signals. In certain configurations, the first variable capacitor 5 and/or the second variable capacitor 6 are implemented using one or more ICs that include variable capacitor arrays.

[0060] The first and second vector inductors 7, 8 can provide higher Q-factor and/or smaller area relative to certain other inductive structures, such as spiral or coil inductors. Although the RF system 10 illustrates one example of a system that can include one or more vector inductors, the vector inductors described herein can be used in other systems.

[0061] Figure 2A is a schematic diagram of a tunable filter 20 according to one embodiment. The tunable filter 20 includes a tunable input impedance matching network 11, a tunable resonator 13, a tunable output impedance matching network 15, and a control circuit 18. The tunable filter 20 further includes an RF input IN and an RF output OUT.

[0062] The tunable filter 20 illustrates one embodiment of a tunable filter suitable for implementing the first and/or second tunable filters 3, 4 shown in Figure 1. However, the tunable filter 20 can be used in other systems and/or the first and/or second tunable filters 3, 4 can be implemented in other ways.

[0063] The tunable input impedance matching network 11 can receive an RF input signal on the RF input IN, and can generate an impedance transformed signal for the tunable resonator 13. Thus, the tunable input impedance matching network 11 can provide an impedance transformation from input to output. For example, in one embodiment, the input impedance transformer 11 transforms an input impedance Z_{IN} of about 50 Ω to an output impedance of about Z_L, where Z_L is less than 50 Ω, for example, 8 Ω.

[0064] Transforming the input impedance of the tunable filter 20 in this manner can result in the impedance transformed signal having a smaller voltage level relative to a voltage level of the RF input signal received at the RF input IN. For example, when the tunable filter 20 has an input impedance Z_L, the voltage level of the impedance transformed

signal can be smaller than the voltage level of the RF input signal by a factor of about $\sqrt{Z_{IN}/Z_L}$.

[0065] The tunable input matching network 11 receives an input matching control signal from the control circuit 18. The input matching control signal can be used for a variety of purposes, including, for example, to control input impedance to enhance performance for a particular band, or under varying voltage standing wave ratio (VSWR). In certain configurations, the input matching control signal can also be used to control a ratio of impedance transformation provided by the tunable input matching network 11.

[0066] As shown in Figure 2A, the tunable resonator 13 can receive the impedance transformed signal from the tunable input matching network 11, and can be used to generate a filtered signal for the tunable output matching network 15. The tunable resonator 13 receives a resonator control signal, which can be used to control one or more resonant frequencies of the tunable resonator. By controlling the resonance of the tunable resonator 13, the tunable filter 20 can achieve a desired gain versus frequency response. In certain configurations, the resonator control signal is used to control a capacitance of a variable capacitor, thereby controlling the tunable resonator's resonant frequency.

[0067] The output impedance matching network 15 receives the filtered signal from the tunable resonator 13, and generates the RF output signal on the RF output OUT. In certain configurations, the output impedance matching network 15 can provide an impedance transformation from the impedance Z_L to an output impedance Z_{OUT} that is greater than Z_L. In certain implementations, the output impedance Z_{OUT} can be selected to be about 50 Ω. The tunable output matching network 15 receives an output matching control signal from the control circuit 18. The output matching control signal can be used for a variety of purposes, including, for example, to control output impedance to enhance output matching and/or to control a ratio of impedance transformation provided by the tunable output matching network 15.

[0068] Although the tunable filter's input impedance Z_{IN} and output impedance Z_{OUT} can be the same in certain configurations, for instance, about 50 Ω, the teachings herein are also applicable to configurations in which a tunable filter's input impedance Z_{IN} and output impedance Z_{OUT} are different.

[0069] As shown in Figure 2A, the control circuit 18 can include a calibration circuit 19, which can be used to control provide calibration to the tunable resonator 13, the tunable input matching network 11, and/or the tunable output matching network 15. In certain configurations, the calibration circuit 19 can be used to compensate for variation of the tunable resonator 13, the tunable input matching network 11, and/or the tunable output matching network 15, such as variation associated with processing and/or temperature. For example, the control circuit 18 can generate control signals that can be used to select capacitance values of variable capacitors of the tunable filter 20, and the calibration circuit 19 can be used to adjust the value of the control signals to provide compensation. In certain configurations, the calibration can be band and/or carrier specific to compensate for variation in the errors across frequency.

[0070] The tunable resonator 13 can be used to narrow-band match the tunable filter 20 to a particular frequency band or carrier. Thus, in contrast to certain passive filtering structures, such as SAW filters, BAW filters, and/or FBARs, the tunable filter 20 can exhibit greater frequency selectivity and lower insertion loss when tuned to a particular frequency. The selectivity can be enhanced by using high Q-factor vector inductors and/or high Q-factor variable capacitors in the tunable resonator 13.

[0071] For instance, the tunable filter 20 can include vector inductors that include a stack of mutually coupled inductors electrically connected in parallel to provide low resistance and high Q-factor, which in turn can lower the tunable filter's insertion loss and enhance the tunable filter's frequency selectivity. Additionally, the tunable filter 20 can include a variable capacitor array including MOS variable capacitor cell that include on or more pairs of MOS capacitors implemented in anti-parallel and/or anti-series configurations. Additionally, the MOS capacitors of a particular MOS variable capacitor cell can be biased at selected voltage levels to provide high linearity, and can operate without requiring switches in RF signal paths to control active capacitor cells. Thus, the variable capacitor array can have a relatively high Q and a relatively low insertion loss, and thus can lower insertion loss and increase frequency selectivity when included in a tunable filter.

[0072] Although including vector inductors and variable capacitor arrays can enhance performance of the tunable filter 20, various implementations of the tunable input

matching network 11, the tunable resonator 13, and the tunable output matching network 15 are possible to achieve a specific performance desired for a particular RF system and/or application.

[0073] In one embodiment, the tunable input matching network 11 is implemented using a combination of a surface mount technology (SMT) inductor and a variable capacitor array, using a combination of a vector inductor and any suitable variable capacitor, and/or using a combination of a vector inductor and a variable capacitor array. Additionally, in one embodiment, the tunable resonator 13 is implemented using a combination of an SMT inductor and a variable capacitor array, using a combination of a vector inductor and any suitable variable capacitor, and/or using a combination of a vector inductor and a variable capacitor array. Furthermore, in one embodiment, the tunable output matching network 15 is implemented using a combination of an SMT inductor and a variable capacitor array, using a combination of a vector inductor and any suitable variable capacitor, and/or using a combination of a vector inductor and a variable capacitor array.

[0074] Figure 2B is a schematic diagram of a tunable filter 30 according to another embodiment. The tunable filter 30 includes a tunable input impedance matching network 31, a tunable resonator 33, a tunable output impedance matching network 35, and a control circuit 18.

[0075] The tunable filter 30 of Figure 2B is similar to the tunable filter 20 of Figure 2A, except that the tunable filter 30 of Figure 2B illustrates a specific implementation of the tunable input impedance matching network 31, the tunable resonator 33, and the tunable output impedance matching network 35.

[0076] In particular, the illustrated tunable input impedance matching network 31 includes a first vector inductor 21 and a first variable capacitor array 24. Additionally, the illustrated tunable resonator 33 includes a second vector inductor 22, a second variable capacitor array 25, and an RF signal processing circuit 27, which can be used to process RF signals in a wide variety of ways. Furthermore, the illustrated output impedance matching network 35 includes a third vector inductor 23 and a third variable capacitor array 26.

[0077] Including vector inductors and/or variable capacitor arrays in a tunable filter can increase the tunable filter's Q-factor, enhance the tunable filter's frequency

selectivity, and/or lower the tunable filter's insertion loss. For example, vector inductors and variable capacitor arrays can have high Q-factor and low resistance, and thus can provide narrow-band selectivity and a relatively small amount of signal loss.

[0078] Although Figure 2B illustrates a configuration in which each of the tunable input impedance matching network 31, the tunable resonator 33, and the tunable output impedance matching network 35 includes a vector inductor and a variable capacitor array, other configurations are possible. For example, one or more of the vector inductors can be omitted in favor of using a surface mount inductor. Additionally, one or more of the variable capacitor arrays can be omitted in favor of using other variable capacitance structures. Furthermore, the teachings herein are applicable to configurations in which the tunable input impedance matching network 31, the tunable resonator 33, and/or the tunable output impedance matching network 35 includes multiple vector inductors and/or multiple variable capacitor arrays.

[0079] Additional details of the tunable filter 30 can be similar to those described earlier.

[0080] Figure 2C is a schematic diagram of a tunable filter 40 according to another embodiment. The tunable filter 40 includes a first tunable input impedance matching network 11a, a second tunable input impedance matching network 11b, a third tunable input impedance matching network 11c, a first tunable resonator 13a, a second tunable resonator 13b, a third tunable resonator 13c, a first tunable output impedance matching network 15a, a second tunable output impedance matching network 15b, a third tunable output impedance matching network 15c, and a control circuit 18. The tunable filter 40 further includes a first RF input IN1, a second RF input IN2, a third RF input IN3, a first RF output OUT1, a second RF output OUT2, and a third RF output OUT3.

[0081] Although Figure 2C illustrates a tunable filter that provides filtering on three RF signal pathways, the tunable filter can be adapted to provide filtering of more or fewer RF signal pathways.

[0082] The first tunable input impedance matching network 11a can provide input matching and/or impedance transformation for the first RF input IN1. Similarly, the second tunable input impedance matching network 11b can be used to provide input matching and/or

impedance transformation for the second RF input IN2, and the third tunable input impedance matching network 11c can be used to provide input matching and/or impedance transformation for the third RF input IN3. The control circuit 18 can be used to control input impedance matching and/or to control ratios of impedance transformation provided by the tunable input matching networks 11a-11c.

[0083] The first tunable output impedance matching network 15a can provide output matching and/or impedance transformation for the first RF output OUT1. Similarly, the second tunable output impedance matching network 15b can be used to provide output matching and/or impedance transformation for the second RF output OUT2, and the third tunable output impedance matching network 15c can be used to provide output matching and/or impedance transformation for the third RF output OUT3. The control circuit 18 can be used to control output impedance matching and/or to control ratios of impedance transformation provided by the tunable output matching networks 15a-15c.

[0084] As shown in Figure 2C, the first tunable resonator 13a can provide filtering between the first RF input IN1 and the first RF output OUT1. Additionally, the second tunable resonator 13b can provide filtering between the second RF input IN2 and the second RF output OUT2, and the third tunable resonator 13c can provide filtering between the third RF input IN3 and the third RF output OUT3. The control circuit 18 can be used to control one or more resonant frequencies of the tunable resonators 13a-13c to achieve a desired gain versus frequency response.

[0085] Additional details of the tunable filter 40 can be similar to those described earlier.

[0086] Although Figures 2A-2C illustrate embodiments of tunable filters that include input and output impedance matching networks, the teachings herein are also applicable to configurations of tunable filters in which the input and/or output impedance matching networks are omitted.

[0087] Figure 3A is a schematic diagram of one embodiment of a tunable resonator array 50. The tunable resonator array 50 includes a first tunable resonator 51a, a second tunable resonator 51b, and a third tunable resonator 51c.

[0088] The first tunable resonator 51a includes a cascade of a first tunable series resonator 61, a second tunable series resonator 62, and a third tunable series resonator 63 between a first RF input I_1 and a first RF output O_1. Additionally, the second tunable resonator 51b includes a cascade of a fourth tunable series resonator 64, a fifth tunable series resonator 65, and a sixth tunable series resonator 66 between a second RF input I_2 and a second RF output O_2. Furthermore, the third tunable resonator 51c includes a cascade of a seventh tunable series resonator 67, an eighth tunable series resonator 68, and a ninth tunable series resonator 69 between a third RF input I_3 and a third RF output O_3.

[0089] Although the tunable resonator array 50 of Figure 3A is illustrated as including three tunable resonators, the tunable resonator array 50 can be adapted to include more or fewer tunable resonators. Additionally, although the tunable resonators 51a-51c are illustrated as including a cascade of three tunable series resonators, other configurations are possible, such as configurations including more or fewer tunable series resonators, and/or a combination of tunable series resonators and parallel series resonators.

[0090] As shown in Figure 3A, the tunable resonator array 50 receives the control signal CNTL, which can be used to control a variable capacitance associated with the first to ninth tunable series resonators 61-69. By controlling the tunable series resonators' capacitances, a frequency response of the tunable resonator array 50 can be tuned. Although Figure 3A illustrates a configuration in which the first to ninth tunable series resonators 61-69 are controlled using a common control signal, the teachings herein are also applicable to configurations in which two or more control signals are used to tune resonators.

[0091] The tunable resonator array 50 can be used in a tunable filter, such as the tunable filter 40 of Figure 2C. For example, the tunable resonator array 50 can be used to implement the tunable resonators 13a-13c of Figure 2C.

[0092] Additional details of the tunable resonator array 50 can be similar to those described earlier.

[0093] Figure 3B is a schematic diagram of another embodiment of a tunable resonator array 70. The tunable resonator array 70 includes a first tunable resonator 71a, a second tunable resonator 71b, and a third tunable resonator 71c.

[0094] The tunable resonator array 70 of Figure 3B is similar to the tunable resonator array 50 of Figure 3A, except that the tunable resonator array 70 includes a different configuration of tunable resonators 71a-71c. In particular, in contrast to the tunable resonators 51a-51c of Figure 3A which each include a cascade of tunable series resonators, the illustrated tunable resonators 71a-71c each include a cascade of tunable parallel resonators.

[0095] For example, the first tunable resonator 71a includes a cascade of a first tunable parallel resonator 81, a second tunable parallel resonator 82, and a third tunable parallel resonator 83. Additionally, the second tunable resonator 71b includes a cascade of a fourth tunable parallel resonator 84, a fifth tunable parallel resonator 85, and a sixth tunable parallel resonator 86. Furthermore, the third tunable resonator 71c includes a cascade of a seventh tunable parallel resonator 87, an eighth tunable parallel resonator 88, and a ninth tunable parallel resonator 89.

[0096] Although the tunable resonator array 70 of Figure 3B is illustrated as including three tunable resonators, the tunable resonator array 70 can be adapted to include more or fewer tunable resonators. Additionally, although the tunable resonators 71a-71c are illustrated as including a cascade of three tunable parallel resonators, other configurations are possible, such as configurations including more or fewer tunable parallel resonators. Moreover, the teachings herein are applicable to configurations in which a tunable resonator array includes both series tunable resonators and parallel tunable resonators.

[0097] Additional details of the tunable resonator array 70 can be similar to those described earlier.

[0098] Figure 4A is a cross section of a portion of a vector inductor according to one embodiment. The portion of the vector inductor or inductive structure 90 includes a first conductor 102a and a second conductor 102b, which are separated by a first dielectric region 104a.

[0099] As shown in Figure 4A, a first terminal A is electrically connected to a first end of the first conductor 102a and to a first end of the second conductor 102b. Additionally, a second terminal B is electrically connected to a second end of the first conductor 102a and to a second end of the second conductor 102b.

[0100] The inductive structure 90 has been annotated to include a voltage V_{AB} between the first terminal A and the second terminal B and to illustrate a current i flowing therethrough. As shown in Figure 4A, a first current having a magnitude about equal to $i/2$ can flow through the first conductor 102a, and a second current having a magnitude about equal to $i/2$ can flow through the second conductor 102b.

[0101] In certain configurations, the voltage V_{AB} across the inductive structure 90 can be given by Equation 1 below, where L is equal to the self-inductance of the first conductor 102a and of the second conductor 102b, and M is equal to the mutual inductance between the first and second conductors 102a, 102b.

Equation 1

$$V_{AB} = L\frac{d\frac{i}{2}}{dt} + M\frac{d\frac{i}{2}}{dt} = \left(\frac{L}{2} + \frac{M}{2}\right)\frac{di}{dt}$$

[0102] The mutual inductance M between a first inductor of self-inductance L_1 and a second inductor of self-inductance L_2 can be about equal to $k\sqrt{L_1 * L_2}$, where k is the coupling coefficient between the inductors. In the illustrated configuration, the first and second conductors 102a, 102b have about equal self-inductance L, and thus the mutual inductance M can be about equal to $k*L$, where k is equal to the coupling coefficient between the first and second conductors 102a, 102b. Accordingly, in certain implementations, the voltage V_{AB} across the inductive structure 90 can be given by Equation 2 below.

Equation 2

$$V_{AB} = \left(\frac{L}{2} + \frac{kL}{2}\right)\frac{di}{dt} \approx L\frac{di}{dt} \quad \text{for } k \approx 1$$

[0103] Accordingly, a pair of conductors each having a self-inductance L, can have an overall inductance that is also about equal to L when the conductors are tightly coupled, such as when the conductors are mutually coupled with a relatively high coupling coefficient, for example, a coupling coefficient of at least 0.9.

[0104] In certain implementations, the dielectric regions between adjacent conductors can be relatively thin, such that adjacent conductors exhibit a high degree of mutual coupling. In one embodiment, a thickness t_1 of the first dielectric region 104a is selected to be in the range of about 8 μm to about 50 μm. In certain configurations, the dielectric regions between conductors have a thickness that is less a thickness of the conductors. For example, in one embodiment, the conductors have a thickness t_2 that is in the range of about 16 μm to about 32 μm. Although examples of specific thicknesses of conductors and dielectric regions have been provided, other configurations are possible.

[0105] Although an overall inductance of the pair of conductors can be about equal to a self-inductance of an individual one of the conductors, the resistance of the inductive structure 90 can be smaller than a resistance of an individual conductor. For example, when the first and second conductors 102a, 102b each have a resistance *R*, an overall resistance between the first terminal A and the second terminal B can be about equal to *R*/2.

[0106] When additional conductors are added to the stack, resistance can further decrease. However, the overall inductance can remain about equal to *L* when the conductors are tightly coupled to one another via mutual induction.

[0107] Figure 4B is a cross section of a vector inductor 95 according to one embodiment. The vector inductor 95 is illustrated as including a first conductor 102a, a second conductor 102b, and a third conductor 102c, with the first and second conductors 102a, 102b separated by a first dielectric region 104a and with the second and third conductors 102b, 102c separated by a second dielectric region 104b. However, as indicated by the ellipses, the vector inductor 95 can include *N* conductors. *N* can vary in a broad range.

[0108] In one embodiment, a vector inductor includes a stack of *N* conductors, where *N* is selected to be in the range of about 2 conductors and about 16 conductors. As used herein, a first conductor in a stack of *N* conductors can be referred to as a lowermost conductor in the stack, while the last or *N*th conductor in the stack can be referred to as an uppermost conductor in the stack. In one embodiment, a vector inductor includes a stack of three or more conductors.

[0109] As shown in Figure 4B, the conductors 102a-102c can be arranged vertically in a stack. Additionally, adjacent conductors in the stack can be tightly coupled to one another via inductive coupling to achieve a high amount of mutual inductance. In one embodiment, adjacent conductors in a vector inductor's stack are configured to have a coupling coefficient k that is at least 0.5, or more particularly, 0.9 or greater.

[0110] Tightly coupling the conductors via inductive coupling can result in the vector inductor 95 having an overall inductance that is similar to a self-inductance of an individual conductor in the stack. However, the conductors can be electrically connected in parallel, and thus an Ohmic loss of the vector inductor 95 can decrease with an increase in the number of conductors in the stack. Accordingly, the Q-factor of a vector inductor can be increased by including additional conductors in the stack.

[0111] Moreover, a configuration including multiple conductors arranged in a stack can also provide higher conductivity for radio frequency (RF) signals relative to a configuration including a single solid conductor of similar dimension. For example, implementing the conductors in a stack can provide a greater amount of conductor surface area relative to a single solid conductor, and thus the vector inductor can provide high conductivity in the presence of skin effect.

[0112] The vector inductor 95 can also be implemented in a relatively small area relative to certain inductors of similar inductance and/or resistivity. For example, in one embodiment, the vector inductor 95 includes N conductors of self-inductance L. When the conductors of the vector inductor 95 are tightly coupled, an overall inductance of the vector inductor 95 can be about equal to L. In contrast, an inductor that operates without mutual coupling can have an overall size that is a factor of about N times greater to achieve a similar inductance. Furthermore, since the conductors are arranged in a vertical stack, the conductors can occupy an area that is about a factor of $1/N$ smaller relative to a planar configuration. The net result of mutual coupling and vertical integration can result in a reduction of size by a factor of about N^2 relative to an inductor that is implemented without layering and without mutual coupling.

[0113] In certain configurations, the vector inductor 95 can be configured to have high mutual inductance between adjacent conductors in part by using a dielectric material

between the conductors that has a relatively high permittivity. As persons having ordinary skill in the art will appreciate, relative permittivity ε_r, can correspond to a ratio of the permittivity of a specific medium relative to the permittivity of free space ε_0. In one embodiment, the dielectric is implemented using a dielectric material having a relative permittivity ε_r that is in the range of about 2.7 to about 10. However, other configurations are possible.

[0114] In certain configurations, the dielectric regions disposed between adjacent conductors can have low dielectric loss. For example, in one embodiment, the dielectric loss tangent (tan δ) of the dielectric regions can be selected to be much less than 1, for instance, 0.00002 or less. As persons having ordinary skill in the art will appreciate, an electromagnetic field in a dielectric can include a reactive or lossless component and a resistive or lossy component, and a dielectric with low dielectric loss tangent can have a reactive component that is much greater in magnitude than the resistive component. A dielectric with low dielectric loss tangent can also be associated with a relatively small amount of heat dissipation. Thus, selecting a dielectric with low dielectric loss tangent can aid in integrating a vector inductor in applications having stringent heat dissipation specifications, such as in certain wireless device applications.

[0115] In one embodiment, the dielectric regions comprise HL832, HL970, and/or HL972 series. Although various examples of dielectric materials have been provided, other dielectric materials are possible.

[0116] In certain configurations, a thickness of the vector inductor's dielectric regions is substantially the same. Additionally, in certain configurations, a thickness of the vector inductor's conductors is substantially the same. However, other configurations are possible, including, for example, configurations in which the thicknesses of dielectric regions are different and/or configurations in which the thicknesses of conductors are different.

[0117] In certain configurations, the vector inductor's conductors can be implemented as individual strips or patches of conductive material, such as elongated strips of metal. For example, the vector inductor's conductors can be implemented to have a substantially rectangular shape when from viewed from above the conductor stack. Configuring the conductors in a substantially rectangular shape can reduce or eliminate curves

and angles to provide a relatively straight path for electron flow, which in turn can provide high Q-factor. However, as will be described in detail below, other configuration are possible, including, for example, configurations in which the vector inductor's conductors are curved to aid in providing a connection to a variable capacitor to provide a parallel resonator.

[0118] Certain conventional inductors are implemented in a coil or spiral shape. However, a path for current flow in such structures can be steeply curved or angled. Thus, electrons associated with currents flowing through such inductors may tend to localize along the innermost edge of the coil or spiral at high frequencies, which can degrade the inductor's Q-factor.

[0119] Although increasing a size of an inductor's conductor may increase Q-factor, such an approach can undesirably increase the inductor's area. Additionally, an ability to increase Q-factor by increasing conductor size may be limited by the skin effect. As persons having ordinary skill in the art will appreciate, the skin effect is a tendency of a radio frequency signal propagating via a conductor to have a current density near the surface of the conductor, rather than through an entire thickness of the conductor.

[0120] The vector inductors herein can have a relatively high Q-factor, a relatively high linearity, and/or a relatively low insertion loss. Additionally, the vector inductors can have a relatively high inductance per unit area, and thus can occupy a relatively small physical space or area.

[0121] In certain configurations, a vector inductor can be integrated into a laminated substrate, such as a substrate of a multi-chip module (MCM).

[0122] The vector inductor can be configured to operate in an inductor-capacitor (LC) resonator with a variable capacitor. Additionally, the capacitance of the variable capacitor can be selected to provide frequency tuning to a tunable filter.

[0123] Figure 5A is a perspective view of a vector inductor 100 according to one embodiment. The vector inductor 100 includes first to sixteenth conductors 102a-102p, respectively. The vector inductor 100 further includes first to fifteenth dielectric regions 104a-104o, respectively. The vector inductor 100 further includes conductive sidewalls 108, a first terminal 118, and a second terminal 119.

[0124] Although the vector inductor 100 is illustrated as including sixteen conductors, the teachings herein are applicable to vector inductors including more or fewer conductors.

[0125] Although not illustrated in Figure 5A for clarity of the figures, the vector inductor 100 is implemented within a laminated substrate, such as a substrate of a multi-chip module (MCM). Additionally, the first to sixteenth conductors 102a-102p can correspond to conductive layers of the laminated substrate.

[0126] Figure 5B is a plan view of a conductor 102 of the vector inductor 100 of Figure 5A. The conductor 102 can correspond to an overhead view of any of the conductors 102a-102p of Figure 5A.

[0127] As shown in Figure 5B, the conductor 102 has a substantially rectangular shape when viewed from above the vector inductor's stack. Configuring the conductor 102 in this manner can enhance conductivity at high frequencies by providing a relatively straight path for current flow, which in turn can increase Q-factor.

[0128] In one embodiment, the conductor 102 has a height X_1 in the range of about 250 μm to about 2,000 μm, and a width X_2 in the range of about 1000 μm to about 10,000 μm. However, other configurations are possible.

[0129] While sharp angles for corners and straight lines are illustrated in the figures, those of ordinary skill in the art will appreciate that in actual embodiments, particularly with miniaturized embodiments, corners can be rounded and the "lines" can be other than straight.

[0130] Figure 6 is a plan view of a conductor 112 of a vector inductor according to another embodiment.

[0131] The conductor 112 of Figure 6 is similar to the conductor 102 of Figure 5B, except that the conductor 112 of Figure 6 further includes a first stub 113a and a second stub 113b, which are located on opposite ends of a conductive body 111.

[0132] The first and second stubs 113a, 113b can aid in providing impedance matching to components and/or other circuitry that is electrically connected to a vector inductor.

[0133] As shown in Figure 6, the conductor 112 includes the conductive body 111, which can have a height X_1 and a width X_2 similar to that of conductor 112 of Figure 5B. Additionally, the conductor 112 can have a stub height X_3 and a stub width X_4. In one embodiment, the stub height X_3 is in the range of about 100 μm to about 1,000 μm, and the stub width X_4 is in the range of 100 μm to about 1,000 μm. However, other configurations are possible.

[0134] Figure 7A is a cross section of a laminated substrate 150 according to one embodiment. The laminated substrate 150 includes dielectric 154 and first to eighth conductors 152a-152h, which have been implemented as a vector inductor 160. As shown in Figure 7A, the laminated substrate 150 further includes vias 158, which operate as conductive sidewalls of the vector inductor 160 to electrically connect adjacent conductors to one another along the ends of the conductors.

[0135] Although the laminated substrate 150 illustrates a vector inductor that includes eight conductors in the vector inductor's conductor stack, the teachings herein are applicable to configurations including more or fewer conductors in a stack.

[0136] The illustrated laminated substrate 150 includes a top surface 151a, which includes a first top surface inductor terminal 168a and a second top surface inductor terminal 169a. Additionally, the illustrated laminated substrate 150 includes a bottom surface 151b, which includes a first bottom surface inductor terminal 168b and a second bottom surface inductor terminal 169b.

[0137] Accordingly, the illustrated laminated substrate 150 includes a vector inductor that can be electrically connected to other circuitry on the top and/or bottom surfaces of the substrate.

[0138] Configuring the laminated substrate 150 in this manner can facilitate providing electrical connections between the vector inductor 160 and other components or circuitry. For example, integrated circuits (ICs) and/or surface mount components can be attached to the laminated substrate's top and bottom surfaces, and can be electrically connected to the vector inductor 160 using traces or other electrical connections.

[0139] Additionally, providing both top and bottom terminals for a vector inductor can reduce an electrical length between the vector inductor's terminals and an innermost conductor in the vector inductor's stack.

[0140] Figure 7B is a cross section of a laminated substrate 170 according to another embodiment.

[0141] The laminated substrate 170 of Figure 7B is similar to the laminated substrate 150 of Figure 7A, except that the laminated substrate 170 includes a vector inductor 180 that includes a conductor stack with tapered sides 175a, 175b. In particular, rather than including a stack of conductors of substantially the same width, the illustrated configuration includes a stack of conductors that are tapered in width with the uppermost and bottommost conductors having a longer width relative to conductors in the middle of the stack.

[0142] Configuring the conductors 152a-152h in this manner can help balance differences in mutual coupling between conductors in the stack and/or to balance a flow of current through the conductors relative to one another. For example, when the conductors are not tapered, the innermost conductor of the stack may have a larger amount of mutual coupling relative to the stack's outermost conductors, and thus the innermost conductor may have a larger overall inductance and smaller current flow relative to the outermost conductors. Thus, the conductors in the stack can be tapered to compensate for differences in mutual coupling between conductors to provide substantially the same amount of current flow in each of the conductors in the vector inductor's stack. In certain embodiments, tapering is also used to compensate for differences in electrical length between the vector inductor's terminals and a particular conductor in the stack.

[0143] Accordingly, the illustrated configuration includes conductors that are tapered to balance a flow of current through the conductors relative to one another.

[0144] Figure 8A is a plan view of a tunable filter 200 according to one embodiment. Figure 8B is a cross-section of the tunable filter 200 of Figure 8A taken along the lines 8B-8B. Figure 8C is a circuit diagram of the tunable filter 200 of Figure 8A.

[0145] The tunable filter 200 includes a laminated substrate 201 including a vector inductor 202 formed therein. The tunable filter 200 further includes a semiconductor die or

integrated circuit (IC) 203 attached to the laminated substrate 201. The tunable filter 200 further includes conductive balls 221a-221c, which can be used to provide electrical connections from the laminated substrate 201 to other components of an RF system. For example, in certain configurations, the tunable filter 200 is implemented as a multi-chip module (MCM), and the conductive balls 221a-221c can provide electrical connections to a phone board.

[0146] For clarity of the figures, only certain structures of the tunable filter 200 have been shown. However, persons having ordinary skill in the art will appreciate that the tunable filter 200 can include additional circuitry and/or structures. For example, the tunable filter 200 can include surface mount components, additional ICs, additional conductors and vias, input and/or output impedance matching networks, additional tunable resonators, and/or additional conductive balls or other structures for providing external electrical connections. Such details have been omitted from the figures for clarity.

[0147] Electrical connections between the IC 203 and the laminated substrate 201 can be made in a variety of ways. For example, in certain configurations, the IC 203 can be attached to the laminated substrate 201 in a flip-chip configuration in which the IC 203 is bumped to the laminated substrate 201. Thus, the IC 203 can be electrically connected to the laminated substrate 201 using bumps, pillars, and/or bars in certain implementations. However, other configurations are possible, such as implementations in which electrical connections are provided between the IC 203 and the laminated substrate 201 using wire bonds.

[0148] The illustrated vector inductor 202 includes a stack of conductors including a first conductor 211, a second conductor 212, a third conductor 213, a fourth conductor 214, and a fifth conductor 215 arranged on different conductive layers of the laminated substrate 201. Additionally, vias 218 have been used to electrically connect the stack of conductors along a first side and along a second side opposite the first side. Although Figure 8B illustrates the vector inductor 202 as including five conductors in the stack, the vector inductor 202 can include more or fewer conductors in the stack. Additionally, although Figure 8B illustrates the vector inductor 202 as being implemented using inner-conductors of the laminated substrate 201, the teachings herein are applicable to configurations in which a

vector inductor is implemented in part using a top surface conductor and/or a bottom surface conductor of a laminated substrate.

[0149] The IC 202 includes a variable capacitor 204 and a control circuit 205. The control circuit 205 can be used to control a capacitor of the variable capacitor 205. In certain embodiments, the variable capacitor 204 is implemented using a variable capacitor array and the control circuit 205 is implemented using a bias voltage generation circuit. Examples of variable capacitor arrays and bias voltage generation circuits will be described in detail further below with reference to Figures 12-15B.

[0150] In the illustrated configuration, the variable capacitor 204 and the vector inductor 202 are electrically in series with one another to operate as a series resonator. As shown in Figures 8A-8C, a first terminal of the vector inductor 202 located on a first side of the laminated substrate 201 is electrically connected to the first conductive ball 221a, which serves as a first RF input I_1. Additionally, a second terminal of the vector inductor 202 located on a second side of the laminated substrate 202 is electrically connected to a first end of the variable capacitor 204 using the conductor 207. Additionally, a second end of the variable capacitor 204 is electrically connected to the second conductive ball 221b, which serves as a first RF output O_1. The electrical connection between the second end of the variable capacitor 204 and the second conductive ball 221b can be provided by an electrical path 208 through the laminated substrate 201, which is schematically depicted by a dashed line in Figure 8B for clarity of the figures.

[0151] The illustrated embodiment uses the first conductive ball 221a as an RF input and the second conductive ball 221b as an RF output of the series resonator. In another embodiment, the first conductive ball 221a serves as an RF output and the second conductive ball 221b serves as an RF input.

[0152] Additional details of the tunable filter 200 can be similar to those described earlier.

[0153] Figure 9A is a plan view of a tunable filter 230 according to another embodiment. Figure 9B is a cross-section of the tunable filter 230 of Figure 9A taken along the lines 9B-9B. Figure 9C is a circuit diagram of the tunable filter 230 of Figure 9A.

[0154] The tunable filter 230 includes a laminated substrate 235 including a vector inductor 232 formed therein. The tunable filter 230 further includes the semiconductor die 203, which is attached to laminated substrate 235. The tunable filter 230 further includes conductive balls 221a-221d. As persons having ordinary skill in the art will appreciate, the tunable filter 230 can include additional circuitry and/or structures not shown.

[0155] In the illustrated configuration, the variable capacitor 204 and the vector inductor 232 are electrically in parallel with one another to operate as a parallel resonator.

[0156] The vector inductor 232 of Figures 9A-9B is similar to the vector inductor 202 of Figures 8A-8B, except that the vector inductor 232 includes a curved shaped. The curved shape can aid in connecting the vector inductor 232 in parallel with the variable capacitor 204. Additionally, the curved shaped can generate stronger magnetic field concentration and provide higher inductance. Additional details of the vector inductor 232 can be similar to those described earlier.

[0157] As shown in Figures 9A-9C, a first terminal of the vector inductor 232 is electrically connected to the first conductive ball 221a, which serves as a first RF input I_1. Additionally, a second terminal of the vector inductor 232 is electrically connected to the second conductive ball 221b, which serves as a first RF output O_1.

[0158] Additional details of the tunable filter 230 can be similar to those described earlier.

[0159] Figure 9D is a plan view of the first conductor 211 of the vector inductor 232. As shown in Figure 9D, the first conductor 211 includes a first end 219a and a second end 219b opposite the first end. The first conductor 211 has a height X_1 and a width X_2.

[0160] Figure 10A is a plan view of a tunable filter 250 according to another embodiment. Figure 10B is a cross-section of the tunable filter 250 of Figure 10A taken along the lines 10B-10B. Figure 10C is a circuit diagram of the tunable filter 250 of Figure 10A.

[0161] The tunable filter 250 includes a laminated substrate 241 including a first vector inductor 202a, a second vector inductor 202b, a third vector inductor 202c, and a fourth vector inductor 202d formed therein. The vector inductors 202a-202d can have a similar structure as the vector inductor 202 of Figures 8A-8C. The tunable filter 250 further includes a semiconductor die 245, which is attached to laminated substrate 241. The

semiconductor die 245 includes a control circuit 205, a first variable capacitor 204a, a second variable capacitor 204b, a third variable capacitor 204c, and a fourth variable capacitor 204d. In certain configurations, the variable capacitors 204a-204d are implemented as variable capacitor arrays, and the control circuit 205 is implemented as a bias voltage generation circuit. The tunable filter 250 further includes conductive balls 221a-221e, a first ground isolation structure 257a, a second ground isolation structure 257b, a third ground isolation structure 257c, a fourth ground isolation structure 257d, and a fifth ground isolation structure 257e. As persons having ordinary skill in the art will appreciate, the tunable filter 250 can include additional circuitry and/or structures not shown.

[0162] In the illustrated configuration, the first vector inductor 202a and the first variable capacitor 204a are electrically in series with one another between a first RF input I_1 and an intermediate node of the tunable filter 250. Additionally, the second variable capacitor 204b and the second vector inductor 202b are electrically in series with one another between the intermediate node and a first RF output O_1. Furthermore, the third variable capacitor 204c and the third vector inductor 202c are electrically in series with one another between the intermediate node and ground GND. Additionally, the fourth variable capacitor 204d and the fourth vector inductor 202d are electrically in series with one another between the intermediate node and ground GND. As shown in Figure 10B, a first terminal of the first vector inductor 202a is electrically connected to the first conductive ball 221a, which serves as the first RF input I_1. Additionally, a first terminal of the second vector inductor 202b is electrically connected to the second conductive ball 221b, which serves as the first RF output O_1. Furthermore, a first terminal of the third vector inductor 202c is electrically connected to the third conductive ball 221c and a first terminal of the fourth vector inductor 202d is electrically connected to the fourth conductive ball 221d. The third and fourth conductive balls 221c, 221d are electrically connected to ground GND in this configuration.

[0163] As shown in Figure 10A, the first ground isolation structure 257a is positioned between the first and fourth vector inductors 202a, 202d. Additionally, the second ground isolation structure 257b is positioned between the second and fourth vector inductors 202b, 202d. Furthermore, the third ground isolation structure 257c is positioned between the second and third vector inductors 202b, 202c. Additionally, the fourth ground isolation

structure 257d is positioned between the first and third vector inductors 202a, 202c. In certain embodiments, the tunable filter 250 further includes the fifth ground isolation structure 257e is positioned beneath the semiconductor die 245.

[0164] The ground isolation structures 257a-257e can be implemented using vias and conductors that are electrically connected to ground. For example, a particular ground isolation structure can be electrically connected to a column of vias and conductors that extend through the laminated substrate 241. The ground isolation structures 257a-257e can help prevent magnetic and/or electric fields of the vector inductors 202a-202d from interfering with one another. In certain configurations, the ground isolation structures 257a-257e can be electrically connected to ground GND using conductive balls. For example, in the illustrated configuration, the fifth ground isolation structure 257e is electrically connected to ground GND using the fifth conductive ball 221e.

[0165] Additional details of the tunable filter 250 can be similar to those described earlier.

[0166] Figure 11A is a plan view of a tunable filter 270 according to another embodiment. Figure 11B is a cross-section of the tunable filter 270 of Figure 11A taken along the lines 11B-11B. Figure 11C is a circuit diagram of the tunable filter 270 of Figure 11A.

[0167] The tunable filter 270 includes a laminated substrate 261 including a first vector inductor 232a, a second vector inductor 232b, a third vector inductor 232c, and a fourth vector inductor 232d formed therein. The tunable filter 270 further includes a semiconductor die 263, which is attached to laminated substrate 261. The semiconductor die 263 includes the control circuit 205 and first to fourth variable capacitors 204a-204d. In certain configurations, the variable capacitors 204a-204d are implemented as variable capacitor arrays, and the control circuit 205 is implemented as a bias voltage generation circuit. The tunable filter 270 further includes conductive balls 221a-221g. As persons having ordinary skill in the art will appreciate, the tunable filter 270 can include additional circuitry and/or structures not shown.

[0168] In the illustrated configuration, the first vector inductor 232a and the first variable capacitor 204a are electrically in parallel with one another between a first RF input I_1 and an intermediate node of the tunable filter 270. Additionally, the second variable capacitor

204b and the second vector inductor 232b are electrically in parallel with one another between the intermediate node and a first RF output O_1. Furthermore, the third variable capacitor 204c and the third vector inductor 232c are electrically in parallel with one another between the intermediate node and ground GND. Additionally, the fourth variable capacitor 204d and the fourth vector inductor 232d are electrically in parallel with one another between the intermediate node and ground GND. As shown in Figure 11B, a first terminal of the first vector inductor 232a is electrically connected to the first conductive ball 221a, which serves as the first RF input I_1. Additionally, a first terminal of the second vector inductor 232b is electrically connected to the second conductive ball 221b, which serves as the first RF output O_1.

[0169] As shown in Figure 11A, the conductive balls 221c-221f can be positioned between the vector inductors 232a-232d. In certain configurations, the conductive balls 221c-221f are electrically connected to ground isolation structures used to isolate the vector inductors 232a-232d from one another in a manner similar to that described earlier. In certain embodiments, a ground isolation structure can also be positioned beneath the semiconductor die 263 and electrically connected to ground GND using the conductive ball 221g.

[0170] Additional details of the tunable filter 270 can be similar to those described earlier.

[0171] Figure 12 is a schematic diagram of an integrated circuit (IC) or semiconductor die 460 according to one embodiment. The IC 460 includes a first variable capacitor array 461, a second variable capacitor array 462, a third variable capacitor array 463, and a bias voltage generation circuit 464. The IC 460 includes a first RF input RF_{IN1}, a second RF input RF_{IN2}, a third RF input RF_{IN3}, a first RF output RF_{OUT1}, a second RF output RF_{OUT2}, and a third RF output RF_{OUT3}.

[0172] The first variable capacitor array 461 includes a first variable capacitor cell 471a, a second variable capacitor cell 471b, and a third variable capacitor cell 471c. The first to third capacitors cells 471a-471c are electrically connected in parallel between the first RF input RF_{IN1} and the first RF output RF_{OUT1}. The second variable capacitor array 462 includes a first variable capacitor cell 472a, a second variable capacitor cell 472b, and a third variable capacitor cell 472c. The first to third capacitors cells 472a-472c are electrically

connected in parallel between the second RF input RF_{IN2} and the second RF output RF_{OUT2}. The third variable capacitor array 463 includes a first variable capacitor cell 473a, a second variable capacitor cell 473b, and a third variable capacitor cell 473c. The first to third capacitors cells 473a-473c are electrically connected in parallel between the third RF input RF_{IN3} and the third RF output RF_{OUT3}.

[0173] Although Figure 12 illustrates the IC 460 as including three variable capacitor arrays, the IC 460 can be adapted to include more or fewer variable capacitor arrays. In other embodiments, the IC 460 can include between about 1 and about 16 variable capacitor arrays. However, other configurations are possible.

[0174] Additionally, although Figure 12 illustrates each variable capacitor array as including three variable capacitor cells, the variable capacitor arrays can be adapted to include more or fewer variable capacitor cells. In one embodiment the IC 460 includes between about 6 and about 12 variable capacitor cells. However, a variable capacitor array can be adapted to include other numbers of variable capacitor cells.

[0175] The bias voltage generation circuit 464 receives the control signal CNTL, and generates a first bias voltage V_{BIAS1}, a second bias voltage V_{BIAS2}, and a third bias voltage V_{BIAS3}. As shown in Figure 12, the first bias voltage V_{BIAS1} is provided to the first variable capacitor cell 471a of the first variable capacitor array 461, to the first variable capacitor cell 472a of the second variable capacitor array 462, and to the first variable capacitor cell 473a of the third variable capacitor array 463. Additionally, the second bias voltage V_{BIAS2} is provided to the second variable capacitor cell 471b of the first variable capacitor array 461, to the second variable capacitor cell 472b of the second variable capacitor array 462, and to the second variable capacitor cell 473b of the third variable capacitor array 463. Furthermore, the third bias voltage V_{BIAS3} is provided to the third variable capacitor cell 471c of the first variable capacitor array 461, to the third variable capacitor cell 472c of the second variable capacitor array 462, and to the third variable capacitor cell 473c of the third variable capacitor array 463.

[0176] The bias voltage generation circuit 464 can be used to control the voltage levels of the first, second, and third bias voltages V_{BIAS1}-V_{BIAS3} to control the capacitances of the first to third variable capacitor arrays 461-463.

[0177] In one embodiment, the illustrated variable capacitor cells are implemented using MOS capacitors. Additionally, the first to third bias voltages V_{BIAS1}-V_{BIAS3} can be used to bias the MOS capacitors at two or more bias voltages associated with a small amount of capacitance variation, and thus with high linearity. For example, in one embodiment, the first to third bias voltages V_{BIAS1}-V_{BIAS3} can be controlled to bias the MOS capacitors in in accumulation or inversion to control the overall capacitance of the arrays.

[0178] In certain configurations, the MOS capacitors can be fabricated using silicon on insulator (SOI) processes. However, other configurations are possible, including, for example, implementations in which the MOS capacitors are fabricated using deep sub-micron (DSM) complementary metal oxide semiconductor (CMOS) processes.

[0179] In certain configurations herein, a variable capacitor cell can include one or more pairs of MOS capacitors implemented using anti-parallel and/or anti-series configurations. Configuring a variable capacitor cell in this manner can help reduce a variation in the cell's capacitance in the presence of RF signals.

[0180] As shown in Figure 12, the bias voltage generation circuit 464 receives the control signal CNTL, which can be used to select the voltage levels of the first, second, and third bias voltages V_{BIAS1}-V_{BIAS3}. In certain configurations, each of the variable capacitor arrays 461-463 includes weighted banks of capacitors cells. For example, in one embodiment, the first variable capacitor cell 471a, the second variable capacitor cell 471b, and the third variable capacitor cell 471c have different capacitance weights or sizes. For example, the variable capacitor cells of a particular variable capacitor array can increase in size by a scaling factor, such as 2. Thus, an overall capacitance of a particular variable capacitor array can be based on a sum of the capacitances of the array's MOS variable capacitor cells.

[0181] The IC 460 includes a first signal path from the first RF input RF_{IN1} to the first RF output RF_{OUT1} through the first variable capacitor array 461. Additionally, the IC 460 includes a second signal path from the second RF input RF_{IN2} to the second RF output RF_{OUT2} through the second variable capacitor array 462, and a third signal path from the third RF input RF_{IN3} to the third RF output RF_{OUT3} through the third variable capacitor array 463.

[0182] In certain embodiments, the IC 460 does not include any switches in the signal paths between the IC's inputs and outputs through the variable capacitor arrays. By

configuring the variable capacitor arrays in this manner, the variable capacitor arrays can have lower insertion loss and/or higher linearity relative to a configuration in which capacitance is provided by selecting discrete capacitors via switches.

[0183] As shown in Figure 12, multiple variable capacitor arrays can be fabricated on a common IC, and can share control signals but receive different RF signals. However, other configurations are possible, such as implementations in which the variable capacitor arrays receive separate control signals.

[0184] Figures 13A and 13B are graphs of two examples of capacitance versus bias voltage. Figure 13A includes a first graph 491 of capacitance versus voltage, and Figure 13B includes a second graph 492 of capacitance versus voltage.

[0185] The first graph 491 includes a high frequency capacitance-voltage (CV) plot 493 for one example of an n-type MOS capacitor. As shown in the CV plot 493, the capacitance of the MOS capacitor can increase with bias voltage level. The increase in capacitance can be associated with the MOS capacitor transitioning between operating regions or modes. For example, at low bias voltage levels, the MOS capacitor can operate in an accumulation mode in which a majority carrier concentration near the gate dielectric / semiconductor interface is greater than a background majority carrier concentration of the semiconductor. Additionally, as the voltage level of the bias voltage increases, the MOS capacitor can transition from the accumulation mode to a depletion mode in which minority and majority carrier concentrations near the gate dielectric / semiconductor interface are less than the background majority carrier concentration. Furthermore, as the voltage level of the bias voltage further increases, the MOS capacitor can transition from the depletion mode to an inversion mode in which the minority carrier concentration near the gate dielectric / semiconductor interface is greater than the background majority carrier concentration.

[0186] The first graph 491 has been annotated to include an AC signal component 494 when biasing the MOS capacitor at a bias voltage level V_B. When the AC signal component 494 is not present, the MOS capacitor can have a capacitance C. However, as shown by in Figure 13A, the AC signal component494 can generate a capacitance variation 495. The capacitance variation 495 can be associated with a capacitance variation generated by the AC signal component 494.

[0187] With reference to Figure 5B, the second graph 492 includes the CV plot 493, which can be as described above. The second graph 492 has been annotated to include a first AC signal component 496 associated with biasing the MOS capacitor at a first bias voltage level V_{B1}, and a second AC signal component 497 associated with biasing the MOS capacitor at a second bias voltage level V_{B2}.

[0188] As shown in Figure 13B, the first AC signal component 496 can generate a first capacitance variation 498, and the second AC signal component 497 can generate a second capacitance variation 499.

[0189] When biased at the first bias voltage level V_{B1} or the second bias voltage level V_{B2}, the MOS capacitor can nevertheless have a capacitance that varies in the presence of AC signals. However, the first and second bias voltage levels V_{B1}, V_{B2} can be associated with DC bias points of the MOS capacitor having relatively small capacitance variation or change.

[0190] Accordingly, in contrast to the capacitance variation 495 of Figure 13A which has a relatively large magnitude, the first and second capacitance variations 498, 499 of Figure 13B have a relatively small magnitude.

[0191] In certain embodiments herein, a variable capacitor array includes MOS capacitors that are biased at bias voltages associated with small capacitance variation. By biasing the MOS capacitors in this manner, a variable capacitor array can exhibit high linearity.

[0192] Such a variable capacitor array can also have less capacitance variation when operated in a system using multiple frequency bands. For example, when included in a tunable filter, the variable capacitor array can provide relatively constant capacitance even when tuned to frequency carriers or bands that are separated by a wide frequency.

[0193] In certain embodiments, the first bias voltage level V_{B1} is selected to operate in the MOS capacitor in an accumulation mode, and the second bias voltage level V_{B2} is selected to operate the MOS capacitor in an inversion mode. In certain configurations, biasing a MOS capacitor in this manner can achieve a capacitance tuning range of 3:1 or more. However, other tuning ranges can be realized, including, for example, a tuning range associated with a particular manufacturing process used to fabricate the MOS capacitor.

[0194] Figure 14A is a schematic diagram of a variable capacitor cell 520 according to one embodiment. The variable capacitor cell 520 includes a first variable capacitor 521 and a second variable capacitor 522. The variable capacitor cell 520 further includes an RF input RF_{IN} and an RF output RF_{OUT}.

[0195] The first variable capacitor 521 includes an anode electrically connected to the RF input RF_{IN} and a cathode electrically connected to the RF output RF_{OUT}. The second variable capacitor 522 includes an anode electrically connected to the RF output RF_{OUT} and a cathode electrically connected to the RF input RF_{IN}.

[0196] In the illustrated configuration, an anode structure of the first and second variable capacitors 521, 522 is different than a cathode structure of the first and second variable capacitors 521, 522. For example, the first and second variable capacitors 521, 522 can be implemented by first and second MOS capacitors, respectively. Additionally, the first and second MOS capacitors can have anodes associated with transistor gates and cathodes associated with transistor source and/or drain regions.

[0197] The first and second variable capacitors 521, 522 have been implemented in an anti-parallel or inverse parallel configuration. Electrically connecting the first and second variable capacitors 521, 522 in this manner can enhance the robustness of the capacitors to capacitance variation in the presence of RF signals. For example, when the first and second variable capacitors are each biased with a particular bias voltage, the variable capacitors' capacitance may change when an RF input signal is received on the RF input RF_{IN}. However, a capacitance variation ΔC of the first and second variable capacitors 521, 522 can have about equal magnitude, but opposite polarity. For instance, in the presence of an RF input signal that generates a capacitance variation having a magnitude ΔC, the first variable capacitor 521 may have a capacitance $C_V + \Delta C$, while the second variable capacitor 522 may have a capacitance $C_V - \Delta C$. Since the first and second variable capacitors 521, 522 are electrically connected in parallel with one another, an overall capacitance of the first and second variable capacitors 521, 522 can be about equal to $2*C_V$.

[0198] Accordingly, the illustrated configuration can provide reduced capacitance variation in the presence of RF signals. Furthermore, the illustrated variable capacitor cell 520 can exhibit high linearity.

[0199] Figure 14B is a schematic diagram of a variable capacitor cell 530 according to another embodiment. The variable capacitor cell 530 includes the first and second variable capacitors 521, 522.

[0200] The variable capacitor cell 530 of Figure 14B is similar to the variable capacitor cell 520 of Figure 14A, except that the variable capacitor cell 530 includes a different arrangement of the first and second variable capacitors 521, 522. In particular, in contrast to the variable capacitor cell 520 of Figure 14A which implements the first and second variable capacitors 521, 522 in an anti-parallel configuration, the variable capacitor cell 530 of Figure 14B implements the first and second variable capacitors 521, 522 in an anti-series or inverse series configuration.

[0201] For example, the first variable capacitor 521 includes an anode electrically connected to the RF input RF_{IN}, and a cathode electrically connected to a cathode of the second variable capacitor 522. Additionally, the second variable capacitor 522 further includes an anode electrically connected to first and second variable capacitors 521, 522.

[0202] Configuring the variable capacitor cell 530 in this manner can reduce variation of the cell's capacitance in the presence of an RF input signal at the RF input RF_{IN}.

[0203] Although the variable capacitor cell 530 of Figure 14B can have a smaller capacitance relative to the variable capacitor cell 520 of Figure 14A for a given bias voltage level, the variable capacitor cell 530 of Figure 14B can have a higher voltage handling capability relative to the variable capacitor cell 520 of Figure 14A.

[0204] The variable capacitor cell 530 of Figure 14B shows an anti-series configuration in which the cathodes of the first and second variable capacitors 521, 522 electrically connected to one another and the anodes of the first and second variable capacitors 521, 522 are electrically connected to the RF input RF_{IN} and the RF output RF_{OUT}, respectively. However, the teachings herein are also applicable to anti-series configurations in which the anodes of the first and second variable capacitors 521, 522 are electrically connected to one another and the cathodes of the first and second variable capacitors 521, 522 are electrically connected to the RF input RF_{IN} and the RF output RF_{OUT}, respectively.

[0205] For example, such a configuration can be more robust against damage from electrostatic discharge (ESD) events. For instance, the anodes of the first and second variable capacitors 521, 522 can be associated with gates of MOS capacitors and the cathodes of the first and second variable capacitors 521, 522 can be associated with source and/or drain regions of MOS capacitors. Since, a MOS capacitor's source and drain regions typically can withstand a greater voltage relative to the MOS capacitor's gate region, an anti-series variable capacitor cell with cathodes electrically connected to input and output pins may exhibit a greater robustness to ESD events or other overvoltage conditions relative to an anti-series variable capacitor cell with anodes electrically connected to input and output pins.

[0206] Figure 15A is a schematic diagram of a metal oxide semiconductor (MOS) variable capacitor cell 560 according to one embodiment. The MOS variable capacitor cell 560 includes a first MOS capacitor 571 and a second MOS capacitor 572. The MOS variable capacitor cell 560 further includes an RF input RF_{IN} and an RF output RF_{OUT}.

[0207] Electrical connections between the MOS variable capacitor cell 560 and a bias voltage generation circuit 575 have been illustrated in Figure 8A. Although not illustrated in Figure 8A, the bias voltage generation circuit 575 can be used to bias additional MOS variable capacitor cells.

[0208] The RF input RF_{IN} is electrically connected to a gate of the first MOS capacitor 571 and to a source and drain of the second MOS capacitor 572. Additionally, the RF output RF_{OUT} is electrically connected to a gate of the second MOS capacitor 572 and to a source and drain of the first MOS capacitor 571.

[0209] As shown in Figure 15A, the bias voltage generation circuit 575 can be used to bias the first and second MOS capacitors 571, 572 at a first bias voltage level V_{B1} or at a second bias voltage level V_{B2}. In one embodiment, the first and second MOS capacitors 571, 572 operate in accumulation when biased at the first bias voltage level V_{B1} and operate in inversion when biased at the second bias voltage level V_{B2}.

[0210] Biasing the first and second MOS capacitors 571, 572 in this manner can improve linearity relative to a configuration in which the first and second MOS capacitors 571, 572 are biased at a bias voltage level selected from a continuous tuning voltage range. For example, a MOS capacitor can exhibit a change in capacitance in response

to changes in an applied RF signal, and a magnitude of the capacitance change can vary with the MOS capacitor's bias voltage level.

[0211] Figure 15B is a schematic diagram of a MOS variable capacitor cell 570 according to another embodiment. The MOS variable capacitor cell 570 includes first and second MOS capacitors 571, 572. Electrical connections between the MOS variable capacitor cell 570 and the bias voltage generation circuit 575 have been illustrated in Figure 15B.

[0212] The MOS variable capacitor cell 570 of Figure 15B is similar to the MOS variable capacitor cell 560 of Figure 15A, except that the MOS variable capacitor cell 570 of Figure 15B implements the first and second MOS capacitors 571, 572 in an anti-series configuration, rather than in an anti-parallel configuration.

[0213] For example, in the illustrated configuration, the gate of the first MOS capacitor 571 is electrically connected to the RF input RF_{IN}, and the gate of the second MOS capacitor 572 is electrically connected to the RF output RF_{OUT}. Additionally, the source and drain of the first MOS capacitor 571 are electrically connected to the source and drain of the second MOS capacitor 572. As shown in Figure 15B, the bias voltage generation circuit 575 can be used to bias the first and second MOS capacitors 571, 572 at the first bias voltage level V_{B1} or at the second bias voltage level V_{B2}.

[0214] Although Figure 15B illustrates an anti-series configuration in which the cathodes of the first and second MOS capacitors are electrically connected to one another, the teachings herein also applicable to anti-series configurations in which the anodes of the first and second MOS capacitors are electrically connected to one another. For example, in another embodiment, the source and drain of the first MOS capacitor 571 are electrically connected to the RF input RF_{IN}, and the source and drain of the second MOS capacitor 572 are electrically connected to the RF output RF_{OUT}. Additionally, the gate of the first MOS capacitor 571 is electrically connected to the gate of the second MOS capacitor 572.

[0215] Figure 16A is a graph 600 of gain versus frequency for one example of a bandpass filter. The graph 600 includes a gain versus frequency plot 601. As shown in Figure 16A, the bandpass filter can include a first stop band 603, a second stop band 604, and a pass band 602. The graph 600 can represent a gain versus frequency response of a fixed filtering structure, such as a SAW filter.

[0216] Figure 16B is a graph 610 of gain versus frequency for one embodiment of a tunable filter. The graph 610 of Figure 16B is similar to the graph 600 of Figure 16A, except that the graph 610 further includes a first tunable resonator gain versus frequency plot 612, a second tunable resonator gain versus frequency plot 613, and a third tunable resonator gain versus frequency plot 614. The capacitance of the tunable resonator can be controlled to tune the resonator's frequency response. The gain versus frequency plots 612-614 of Figure 16B illustrate various possible gain versus frequency plots associated with different tunings. However, a tunable resonator can be tuned in other ways.

[0217] As shown in Figure 16B, a tunable resonator can be used to tune a filter to a single channel, rather than to a whole pass band 602 suitable for passing a particular frequency band. The tunable resonator can provide lower insertion loss and/or higher frequency selectivity relative to certain fixed bandpass filters, which can have a fixed performance. Additionally, the tunable resonator can operate with more band gap, since the tunable resonator can be tuned to a bandwidth that is smaller than the pass band 602. For instance, in one example of LTE operating with single-mode, the channel bandwidth could be around 3 – 20 MHz, and thus may be, for instance, a factor of 3 to 5 times smaller than the pass band.

[0218] The Q-factor of a tunable resonator can be inversely proportional to bandwidth. Accordingly, a tuned resonator can be tuned to a relatively narrow bandwidth and can operate with high Q-factor. Thus, the tunable resonator's herein can be tuned to narrow bandwidths to operate with high Q-factor and low insertion loss.

[0219] Figure 16C is a graph 620 of gain versus frequency for another embodiment of a tunable filter.

[0220] The graph 620 of Figure 16C is similar to the graph 610 of Figure 16B, except that the graph 620 illustrates a configuration in which a tunable filter has been tuned to two carrier-aggregated channels for higher performance. The graph 620 includes a first tunable resonator gain versus frequency plot associated with a first channel frequency 622a and a second channel frequency 622b. Additionally, the graph 620 includes a second tunable resonator gain versus frequency plot associated with a third channel frequency 623a and fourth channel frequency 623b. Furthermore, the graph 620 includes a third tunable resonator

gain versus frequency plot associated with a fifth channel frequency 624a and a sixth channel frequency 624b. The gain versus frequency plots of Figure 16C illustrate various possible gain versus frequency plots. However, a tunable resonator can be tuned in other ways.

[0221] As shown in Figure 16C, a tunable resonator can be used to tune a filter to two or more carrier-aggregated channels. The illustrated tunable resonator operates with a bandwidth that is less than the pass band 602, rather than to a whole pass band 602 suitable for passing a particular frequency band.

[0222] Figure 17A is a first graph 700 of gain versus frequency for another embodiment of a tunable filter. Figure 17B is a second graph 710 of gain versus frequency for another embodiment of a tunable filter.

[0223] The first graph 700 and the second graph 710 can represent gain versus frequency plots of one example of tunable filters for a programmable duplexer. The first graph 700 illustrates a first gain versus frequency plot 701 of a first tunable filter. The first plot 701 includes a first marker 702 at a frequency of about 2.655 GHz, where the gain is about -1.217 dB in this example. The second graph 710 illustrates a second gain versus frequency plot 711 of a second tunable filter. The second plot 711 includes a second marker 712 at a frequency of about 2.655 GHz, where the gain is about -1.498 dB in this example.

[0224] In certain LTE applications, more rejection and/or isolation can be desired on one end of the duplexer to provide higher TX/RX isolation. The tunable filters herein can be tuned asymmetrically by selectively tuning a resonator to provide more rejection on one side of the duplexer at the cost of an increase in insertion loss.

[0225] Capacitance and/or inductance values of a tunable filter can be selected in a variety of ways.

[0226] In one embodiment, a tunable filter includes an inductor and a capacitor electrically connected as a tunable resonator. Additionally, for a first inductance value L_1 and a first capacitance value C_1, the tunable filter has a first resonant frequency F_1 about equal to $\frac{1}{2\pi\sqrt{L_1 * C_1}}$. Additionally, for a second inductance value L_2 and a second capacitance value

C_2, the tunable filter has a second resonant frequency F_2 about equal to $\frac{1}{2\pi\sqrt{L_2 * C_2}}$. Additionally, the square of the ratio of F_2 to F_1 can be given by Equation 3 below.

Equation 3

$$\left(\frac{F_2}{F_1}\right)^2 = \frac{C_1}{C_2} * \frac{L_1}{L_2}$$

[0227] In one embodiment, F_{MAX} corresponds to a highest resonance frequency (HRF) in a given band sequence, F_{MIN} corresponds to a lowest resonance frequency (LRF) in a given band sequence, C_{MAX} corresponds to a highest capacitance for LRF, and C_{MIN} corresponds to a lowest capacitance for HRF. In certain configurations, a square of the ratio of F_{MAX} to F_{MIN} can be given by Equation 4 below.

Equation 4

$$\left(\frac{F_{MAX}}{F_{MIN}}\right)^2 = \frac{C_{MAX}}{C_{MIN}} * \frac{L_1}{L_2}$$

[0228] In certain embodiments, Equation 4 can be used to select a tuning range of a variable capacitor used in a tunable filter. For example, Equation 4 can be used to select C_{MAX} and C_{MIN} once F_{MAX} and F_{MIN} have been determined. Although one example of capacitance sizing has been described, a tunable resonators can have capacitance values selected or sized in other ways.

[0229] Figure 18 is a schematic diagram of a tunable filter 800 according to another embodiment. The tunable filter 800 includes a substrate 801, on which a surface mount technology (SMT) inductor or surface mount inductor 802 has been attached. Additionally, a semiconductor die or IC 803 has been placed on the substrate 801 adjacent to the SMT inductor 802. The illustrated tunable filter 800 illustrates a configuration in which a vector inductor has been omitted in favor of using an SMT inductor.

[0230] The IC 803 includes a variable capacitor array 804 and a bias voltage generation circuit 805, which can be implemented as described earlier with respect to Figures 12-15B. The SMT inductor 802 and the variable capacitor array 804 have been electrically

connected using the conductor 807 to operate as a tunable resonator. Although Figure 18 illustrates the SMT inductor 802 and the variable capacitor array 805 electrically connected as a series resonator, the teachings herein are also applicable to configurations in which an SMT inductor and variable capacitor array are electrically connected as a parallel resonator.

[0231] Additional details of the tunable filter 800 can be similar to those described earlier.

[0232] Figure 19 is a schematic diagram of another embodiment of an RF system 900. The RF system 900 includes a multi-chip module (MCM) 901, which has been attached to a phone board 902. The MCM 901 includes a laminated substrate 904, which includes a vector inductor 906 formed therein. The MCM 901 further includes a semiconductor die or IC 907, which includes a variable capacitor 903 fabricated therein. The MCM 901 further includes encapsulation used to protect the IC 907.

[0233] As shown in the Figure 19, a plurality of conductive balls have been used to provide electrical connections between the MCM 901 and the phone board 902. For example, a first conductive ball 908a can serve as a first RF input for the MCM 901, and a second conductive ball 908b can serve as a first RF output for the MCM 901.

[0234] In certain configurations herein, a tunable filter can be implemented as a MCM. Additionally, the MCM can include tunable resonators including vector inductors and/or variable capacitor arrays. For example, a vector inductor can be integrated into a laminated substrate of the MCM, and the vector inductor can be electrically connected with a variable capacitor array or other variable capacitor to operate as a series resonator or as a parallel resonator.

[0235] Additional details of the RF system 900 can be similar to those described earlier.

Conclusion

[0236] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." The word "coupled", as generally used herein, refers to two or

more elements that may be either directly connected, or connected by way of one or more intermediate elements. Likewise, the word "connected", as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0237] Moreover, conditional language used herein, such as, among others, "can," "could," "might," "can," "e.g.," "for example," "such as" and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0238] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0239] The teachings of the invention provided herein can be applied to other systems, not only the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0240] While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

WHAT IS CLAIMED IS:

1. A tunable filter comprising:

a laminated substrate comprising a first vector inductor, wherein the first vector inductor comprises:

a stack of conductors comprising two or more conductors arranged on different conductive layers of the laminated substrate, wherein each of the different conductive layers is separated by a dielectric, wherein the two or more conductors are electrically connected to one another along a first side of the stack, and wherein the two or more conductors are electrically connected to one another along a second side of the stack opposite the first side; and

a semiconductor die attached to the laminated substrate, wherein the semiconductor die comprises a first variable capacitor,

wherein the first variable capacitor and the first vector inductor are electrically connected to operate as a first tunable resonator.

2. The tunable filter of claim 1, wherein adjacent conductors in the stack are mutually coupled to one another with a coupling coefficient of at least 0.9.

3. The tunable filter of claim 1, wherein each of the conductors in the stack have substantially the same shape and are adjacent to each other.

4. The tunable filter of claim 1, wherein at least one of the first side or second side is tapered to compensate for differences in mutual coupling between the two or more conductors of the stack.

5. The tunable filter of claim 1, wherein the variable capacitor comprises a first variable capacitor array and a bias voltage generation circuit configured to bias the first variable capacitor array to control a capacitance of the first variable capacitor array, wherein

the first variable capacitor array comprises a first plurality of metal oxide semiconductor (MOS) variable capacitor cells.

6. The tunable filter of claim 5, wherein the first plurality of MOS variable capacitor cells comprises a first MOS variable capacitor cell comprising a first MOS capacitor and a second MOS capacitor, wherein the first MOS capacitor and the second MOS capacitor are electrically connected in anti-series.

7. The tunable filter of claim 5, wherein the first plurality of MOS variable capacitor cells comprises a first MOS variable capacitor cell comprising a first MOS capacitor and a second MOS capacitor, wherein the first MOS capacitor and the second MOS capacitor are electrically connected in anti-parallel.

8. The tunable filter of claim 1, wherein the first vector inductor comprises a first terminal on a first side of the laminated substrate and a second terminal on a second side of the laminated substrate opposite the first side of the laminated substrate, wherein the first terminal is electrically connected to the first side of the stack, wherein the second terminal is electrically connected to the second side of the stack.

9. The tunable filter of claim 1, wherein the first vector inductor and the first variable capacitor are electrically connected in series with one another.

10. The tunable filter of claim 9, wherein each of the conductors in the stack have a substantially rectangular shape when viewed from above the stack.

11. The tunable filter of claim 1, wherein the first vector inductor and the first variable capacitor are electrically connected in parallel with one another.

12. The tunable filter of claim 11, wherein each of the conductors in the stack have a curved shape when viewed from above the stack.

13. The tunable filter of claim 1,

wherein the semiconductor die further comprises a second variable capacitor,

wherein the laminated substrate further comprises a second vector inductor, wherein the second variable capacitor and the second vector inductor are electrically connected to operate as a second tunable resonator.

14. The tunable filter of claim 13,

wherein the laminated substrate further comprises a first ground isolation structure positioned between first vector inductor and the second vector inductor.

15. The tunable filter of claim 13,

wherein the semiconductor die further comprises a third variable capacitor and a fourth variable capacitor,

wherein the laminated substrate further comprises a third vector inductor and a fourth vector inductor, wherein the third variable capacitor and the third vector inductor are electrically connected to operate as a third tunable resonator, wherein the fourth variable capacitor and the fourth vector inductor are electrically connected to operate as a fourth tunable resonator.

16. The tunable filter of claim 15,

wherein the first vector inductor and the first variable capacitor are electrically connected in series between a radio frequency input and an intermediate node,

wherein the second vector inductor and the second variable capacitor are electrically connected in series between a radio frequency output and the intermediate node,

wherein the third vector inductor and the third variable capacitor are electrically connected in series between a ground node and the intermediate node, and

wherein the fourth vector inductor and the fourth variable capacitor are electrically connected in series between the ground node and the intermediate node.

17. The tunable filter of claim 15,

wherein the first vector inductor and the first variable capacitor are electrically connected in parallel between a radio frequency input and an intermediate node,

wherein the second vector inductor and the second variable capacitor are electrically connected in parallel between a radio frequency output and the intermediate node,

wherein the third vector inductor and the third variable capacitor are electrically connected in parallel between a ground node and the intermediate node, and

wherein the fourth vector inductor and the fourth variable capacitor are electrically connected in parallel between the ground node and the intermediate node.

18. The tunable filter of claim 15,

wherein the laminated substrate further comprises a first ground isolation structure positioned between first vector inductor and the fourth vector inductor.

wherein the laminated substrate further comprises a second ground isolation structure between the second vector inductor and the fourth vector inductor,

wherein the laminated substrate further comprises a third ground isolation structure between the second vector inductor and the third vector inductor, and

wherein the laminated substrate further comprise a fourth ground isolation structure between the fourth vector inductor and the first vector inductor.

19. The tunable filter of claim 1, wherein the tunable filter comprises a multi-chip module, wherein the laminated substrate comprises a substrate of the multi-chip module.

20. The tunable filter of claim 1, wherein the stack of conductors comprises at least three conductors.

21. A radio frequency system comprising:

a phone board; and

a multi-chip module attached to the phone board, wherein the multi-chip module comprises:

a laminated substrate comprising a first vector inductor integrated therein, wherein the first vector inductor comprises a stack of conductors comprising two or more conductors arranged on different conductive layers of the laminated substrate, wherein each of the different conductive layers is separated by a dielectric, wherein the two or more conductors are electrically connected to one another along a first side of the stack, and wherein the two or more conductors are electrically connected to one another along a second side of the stack opposite the first side; and

a semiconductor die attached to the laminated substrate, wherein the semiconductor die comprises a first variable capacitor,

wherein the first variable capacitor and the first vector inductor are electrically connected to operate as a first tunable resonator.

22. The RF system of claim 20, wherein the multi-chip module comprises a plurality of electrical connections to the phone board on a first side of the laminated substrate, wherein the semiconductor die is attached on a second side of the laminated substrate opposite the first side, and wherein the vector inductor comprises a first terminal on the first side of the laminated substrate and a second terminal on the second side of the laminated substrate.

23. A tunable filter comprising:

a substrate;

a first surface mount inductor attached to the substrate; and

a semiconductor die attached to the substrate, wherein the semiconductor die comprises a first variable capacitor array and a bias voltage generation circuit configured to bias the first variable capacitor array to control a capacitance of the first variable capacitor array, wherein the first variable capacitor array comprises:

a first plurality of metal oxide semiconductor (MOS) variable capacitor cells, wherein the first plurality of MOS variable capacitor cells comprises a first MOS variable capacitor cell comprising a first MOS capacitor and a second MOS capacitor, wherein the first MOS capacitor and the second MOS capacitor are arranged in an anti-series configuration or in an anti-parallel configuration,

wherein the first variable capacitor array and the first surface mount inductor are electrically connected to operate as a first tunable resonator.

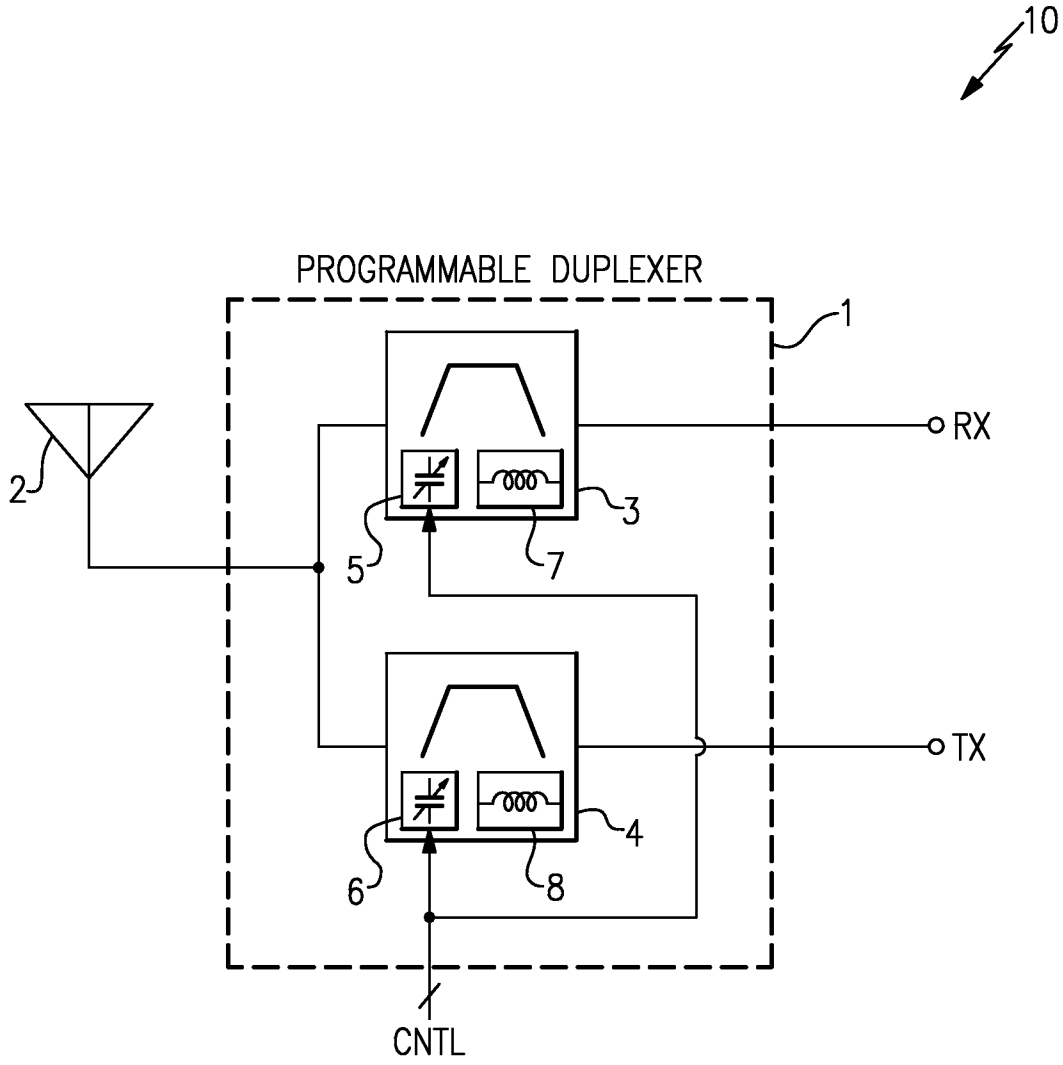


FIG.1

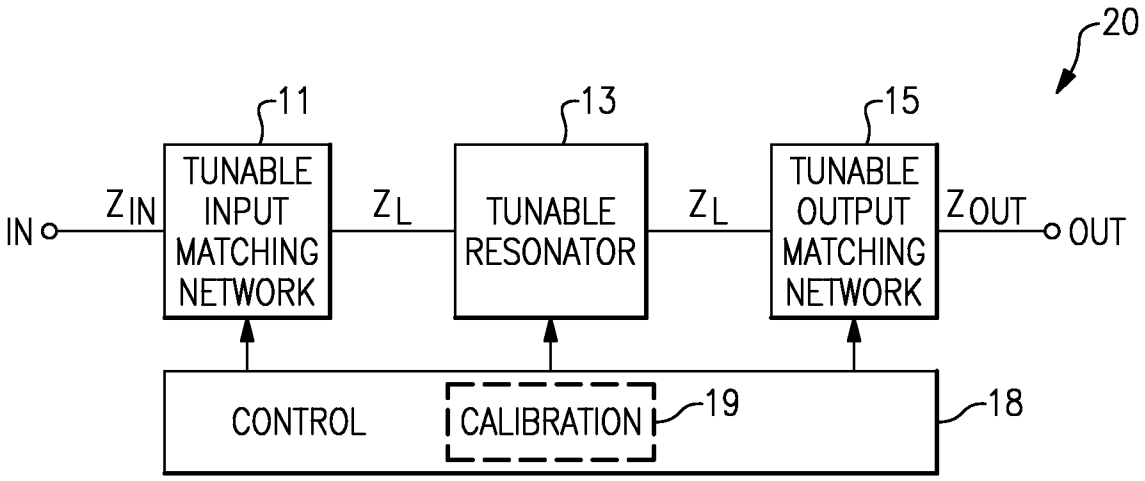

20
11
13
15
TUNABLE INPUT MATCHING NETWORK
TUNABLE RESONATOR
TUNABLE OUTPUT MATCHING NETWORK
IN
ZIN
ZL
ZL
ZOUT
OUT
CONTROL
CALIBRATION
19
18

FIG.2A

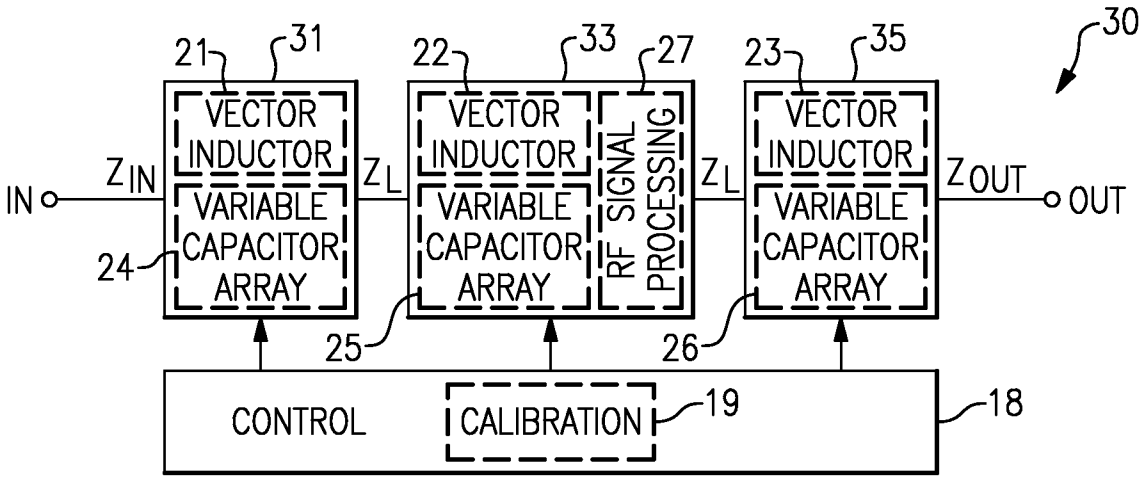

30
21
31
22
33
27
23
35
VECTOR INDUCTOR
VARIABLE CAPACITOR ARRAY
RF SIGNAL PROCESSING
IN
ZIN
ZL
ZL
ZOUT
OUT
24
25
26
CONTROL
CALIBRATION
19
18

FIG.2B

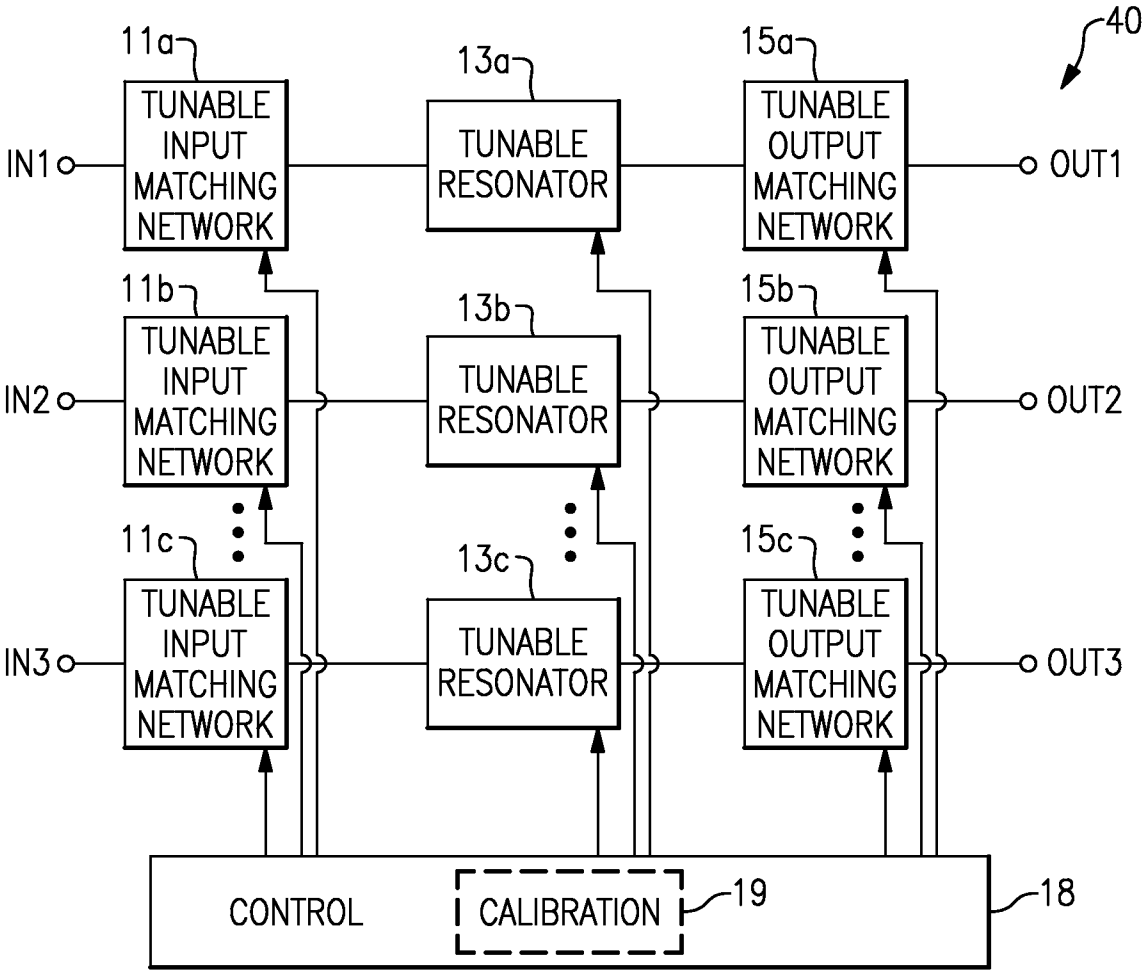

40
11a
TUNABLE INPUT MATCHING NETWORK
13a
TUNABLE RESONATOR
15a
TUNABLE OUTPUT MATCHING NETWORK
IN1
OUT1
11b
TUNABLE INPUT MATCHING NETWORK
13b
TUNABLE RESONATOR
15b
TUNABLE OUTPUT MATCHING NETWORK
IN2
OUT2
11c
TUNABLE INPUT MATCHING NETWORK
13c
TUNABLE RESONATOR
15c
TUNABLE OUTPUT MATCHING NETWORK
IN3
OUT3
CONTROL
CALIBRATION
19
18

FIG.2C

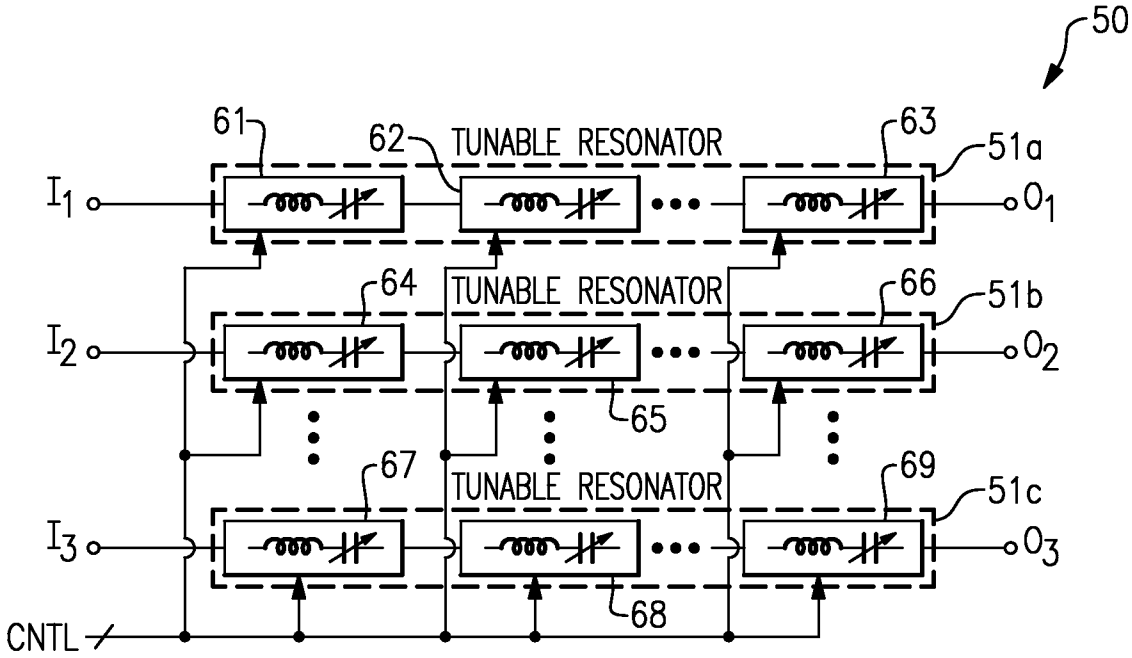

50
61
62
TUNABLE RESONATOR
63
51a
I1
O1
64
TUNABLE RESONATOR
66
51b
I2
O2
65
67
TUNABLE RESONATOR
69
51c
I3
O3
68
CNTL

FIG.3A

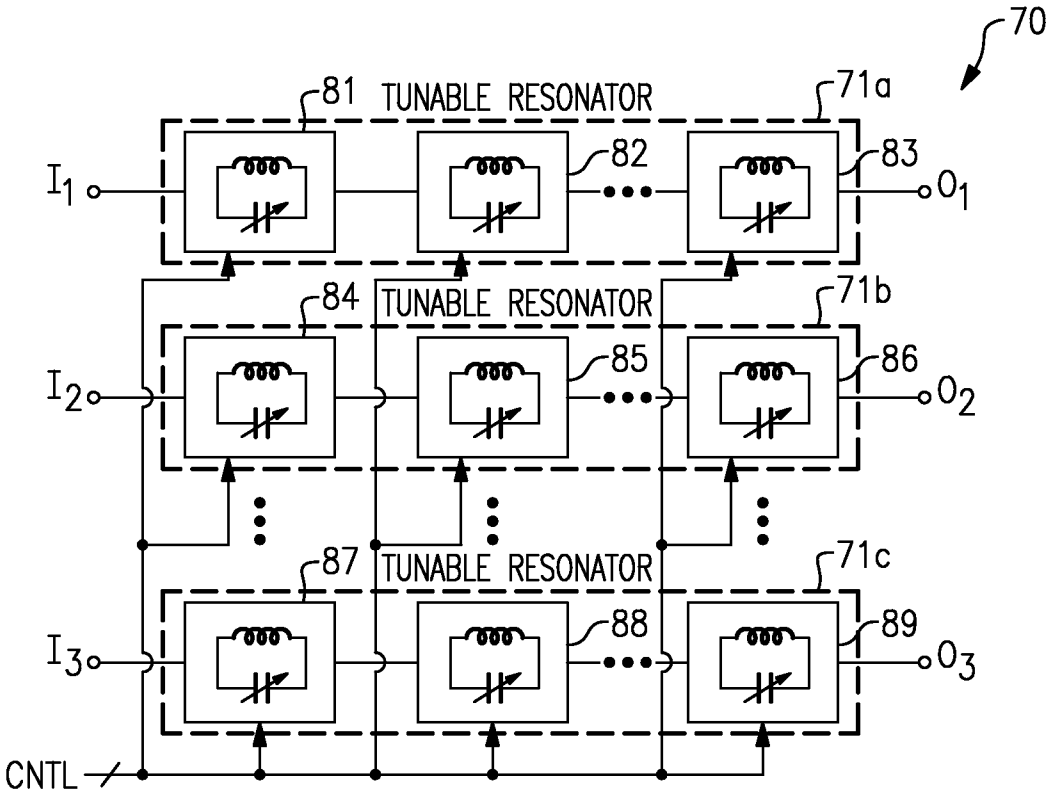

70
81
TUNABLE RESONATOR
71a
82
83
I1
O1
84
TUNABLE RESONATOR
71b
85
86
I2
O2
87
TUNABLE RESONATOR
71c
88
89
I3
O3
CNTL

FIG.3B

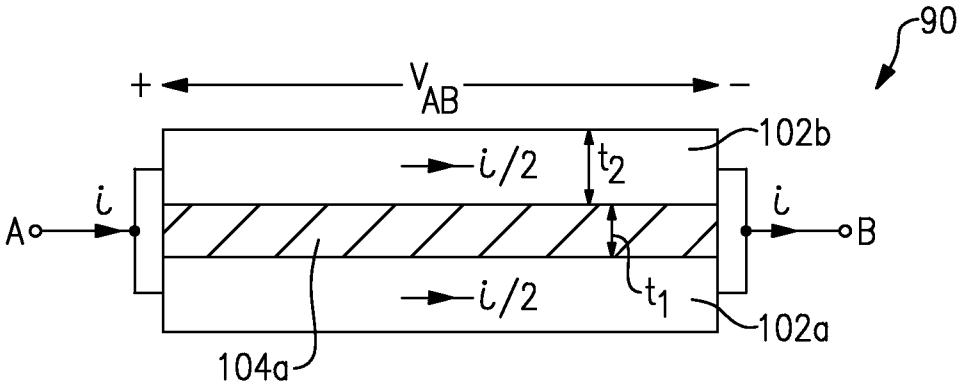

90
+
V_{AB}
–
102b
t_2
$i/2$
i
A
i
B
t_1
$i/2$
102a
104a

FIG.4A

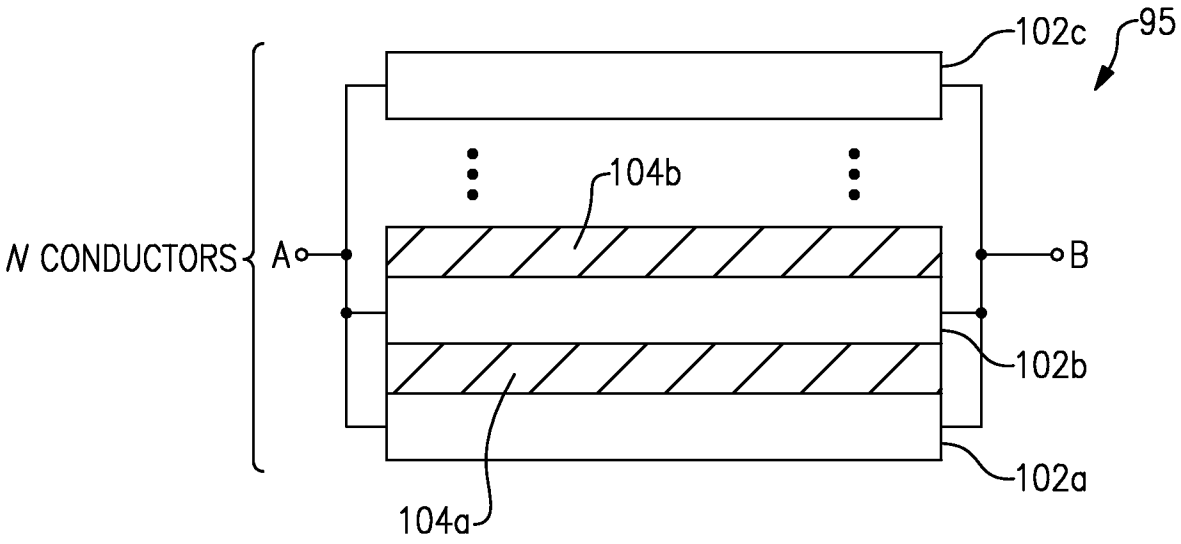

102c
95
104b
N CONDUCTORS
A
B
102b
102a
104a

FIG.4B

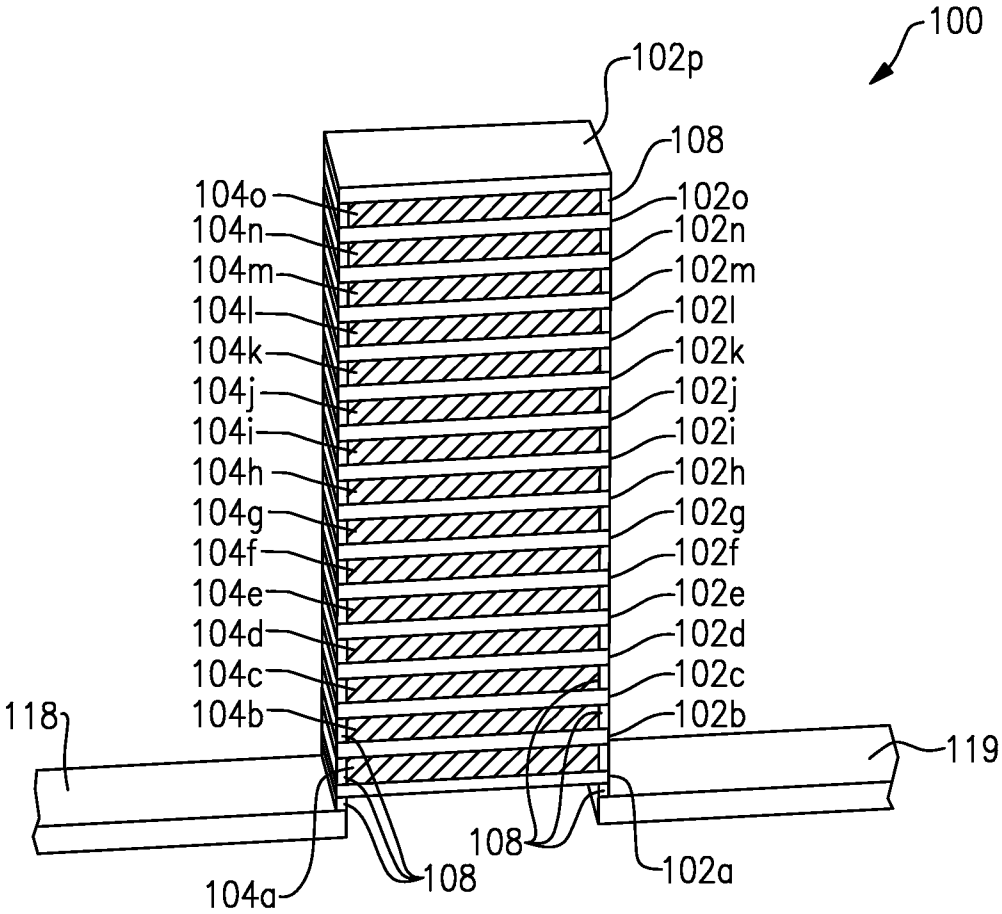

100
102p
108
104o
104n
104m
104l
104k
104j
104i
104h
104g
104f
104e
104d
104c
104b
102o
102n
102m
102l
102k
102j
102i
102h
102g
102f
102e
102d
102c
102b
118
119
108
108
102a
104a

FIG.5A

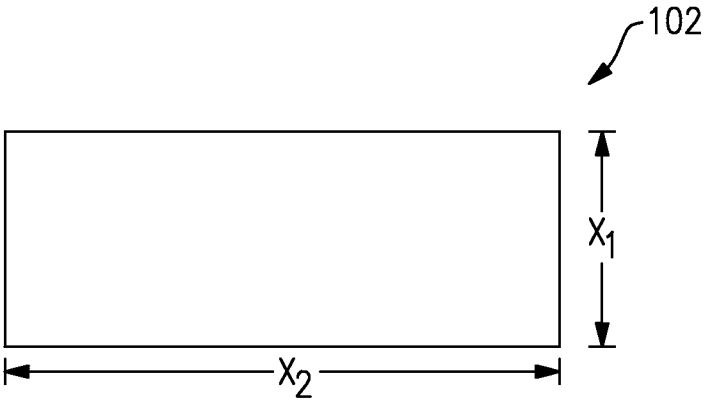

102
X_1
X_2

FIG.5B

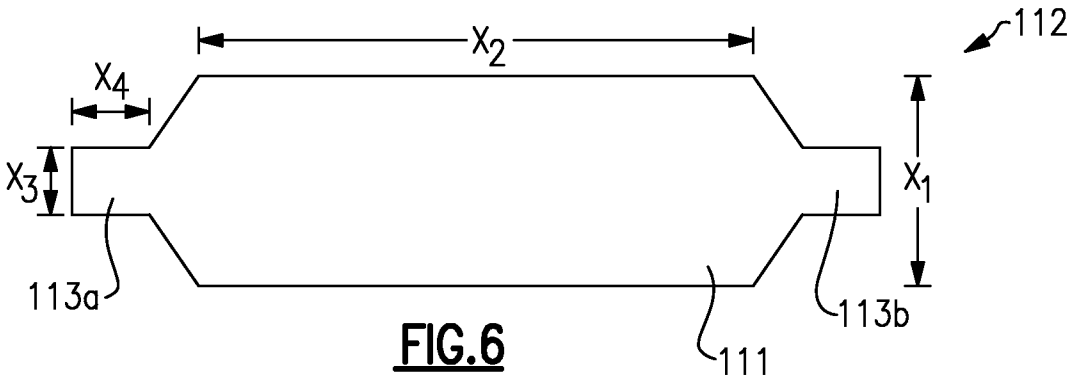


FIG.6

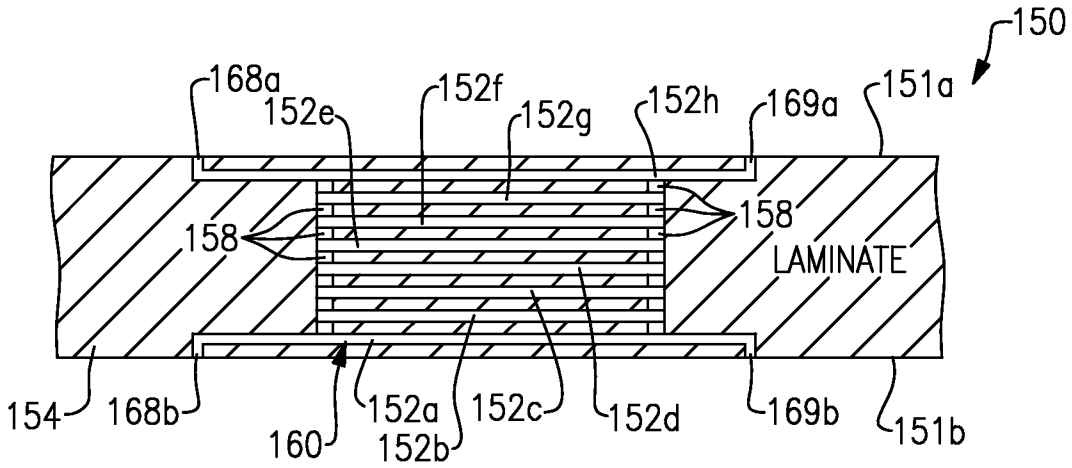


FIG.7A

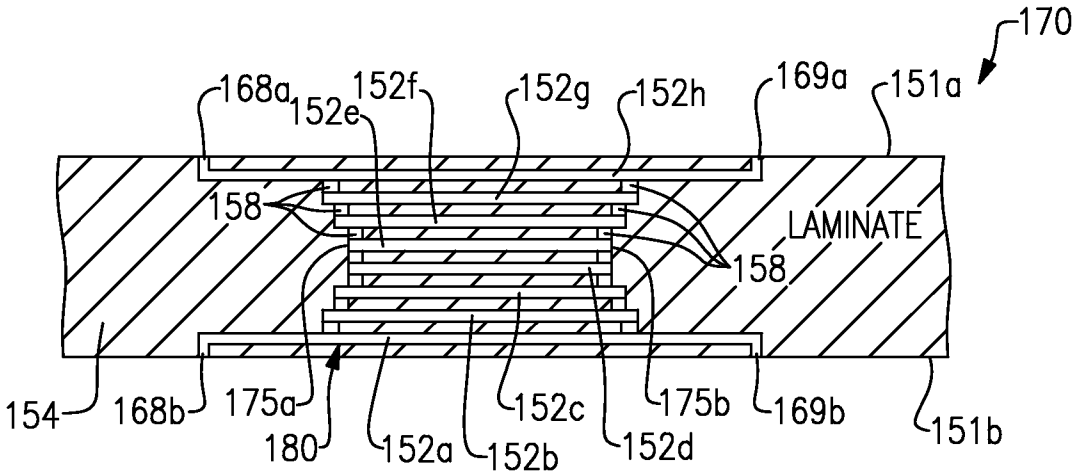


FIG.7B

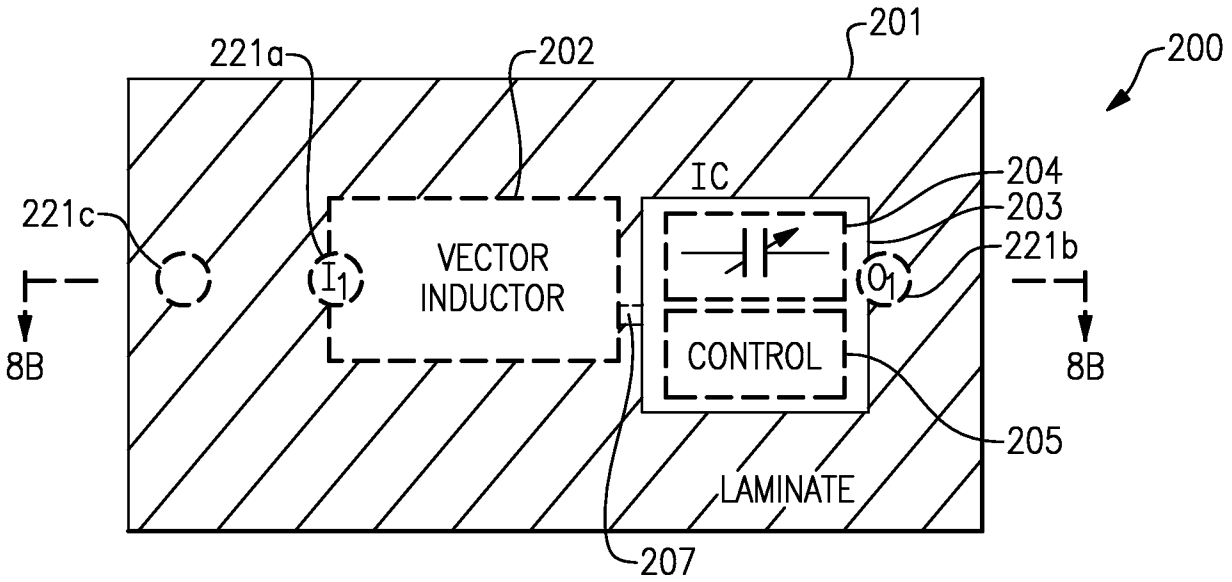


FIG.8A

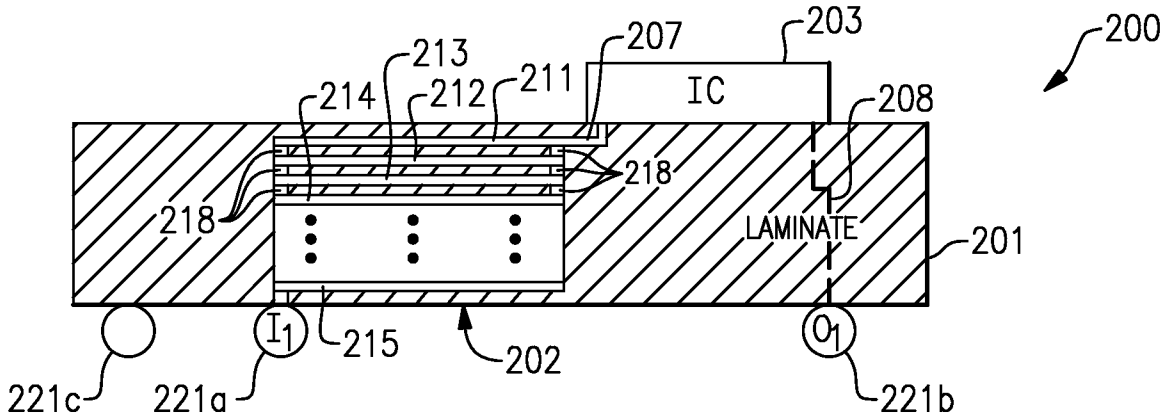


FIG.8B

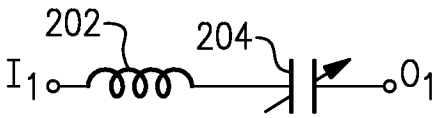


FIG.8C

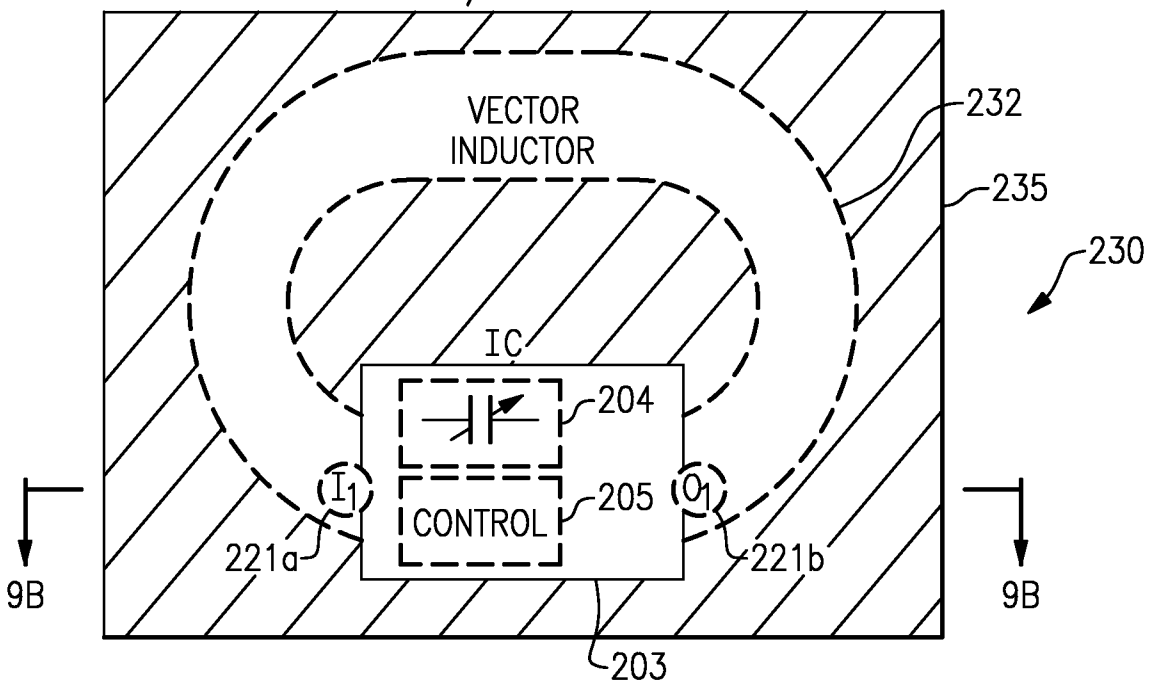


FIG.9A

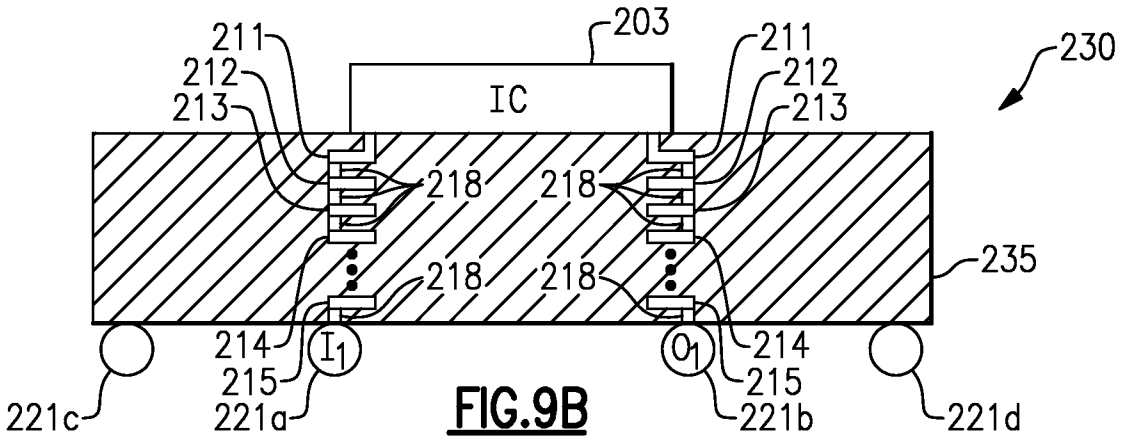


FIG.9B

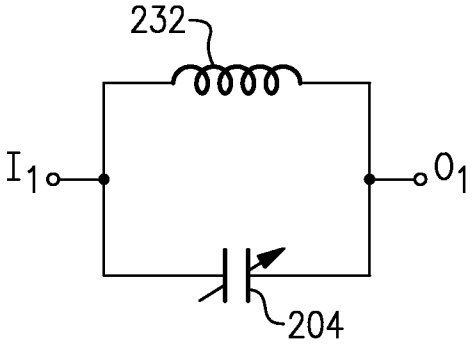


FIG.9C

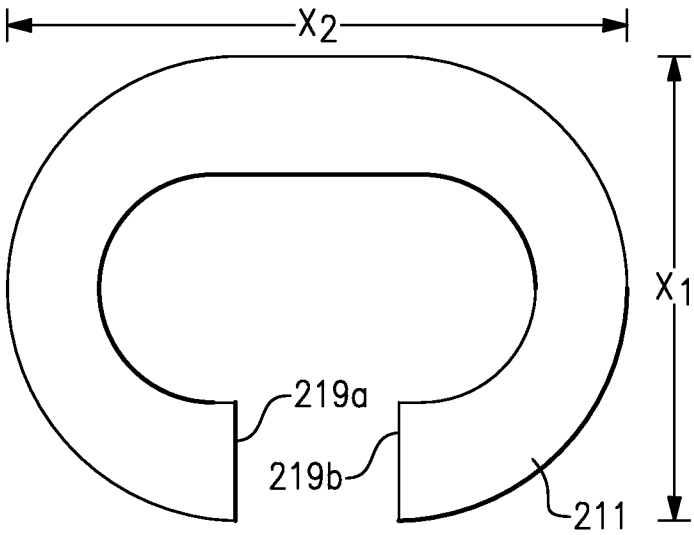


FIG.9D

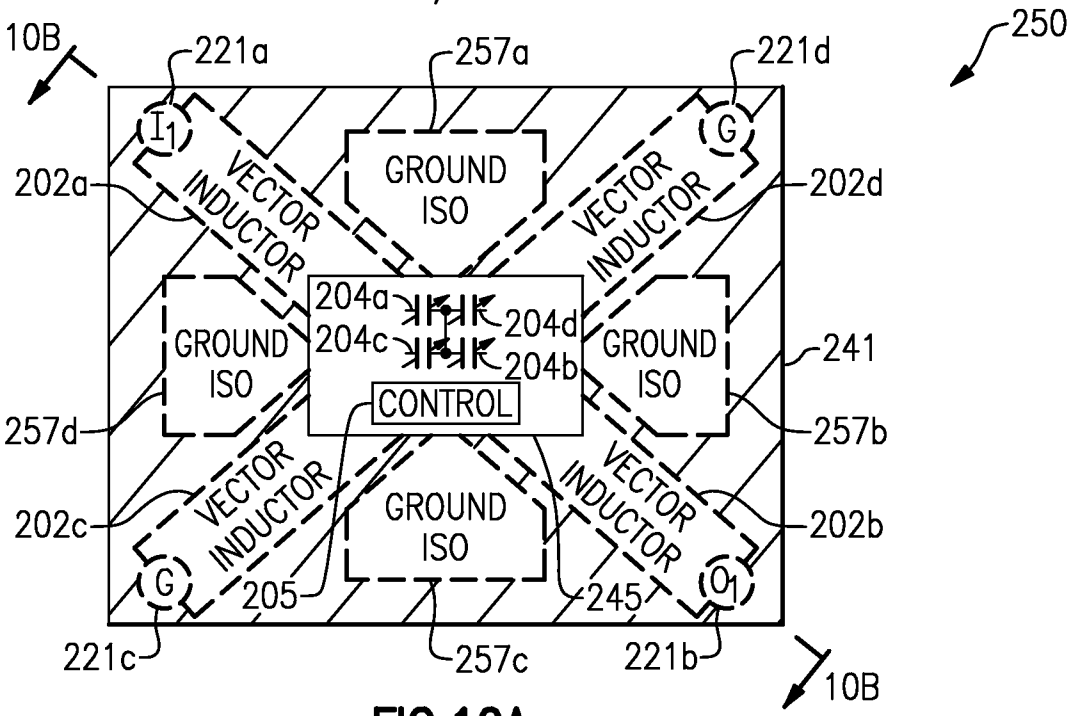


FIG.10A

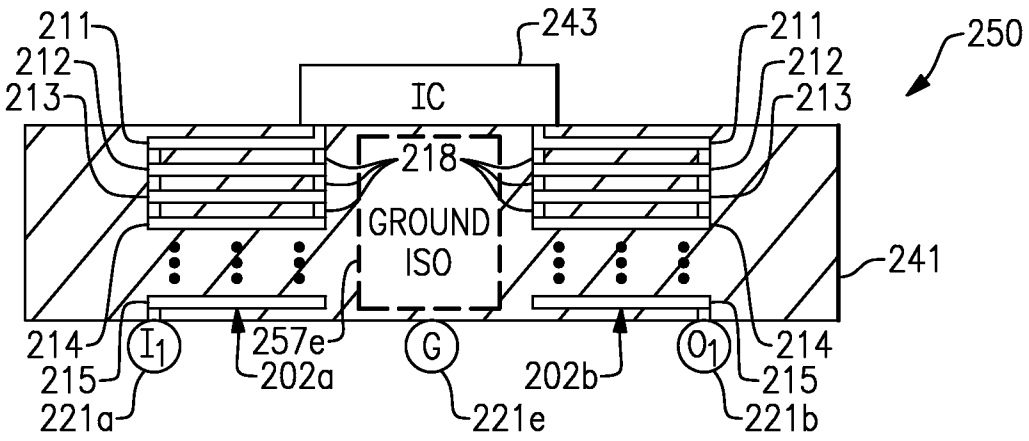


FIG.10B

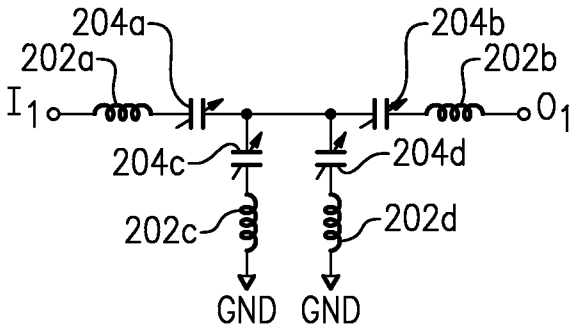


FIG.10C

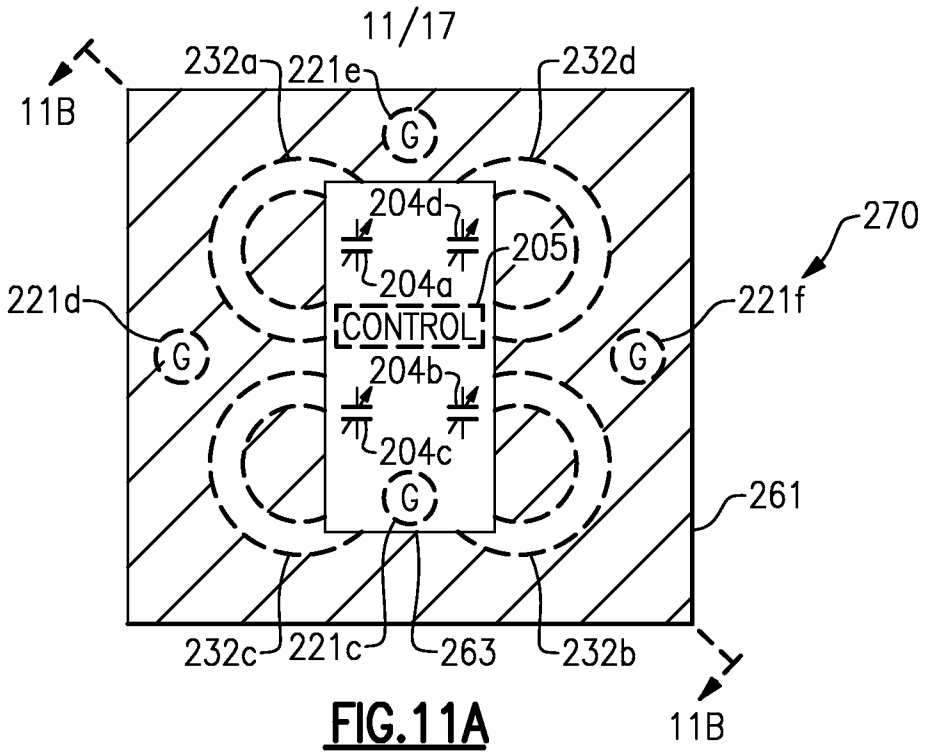


FIG.11A

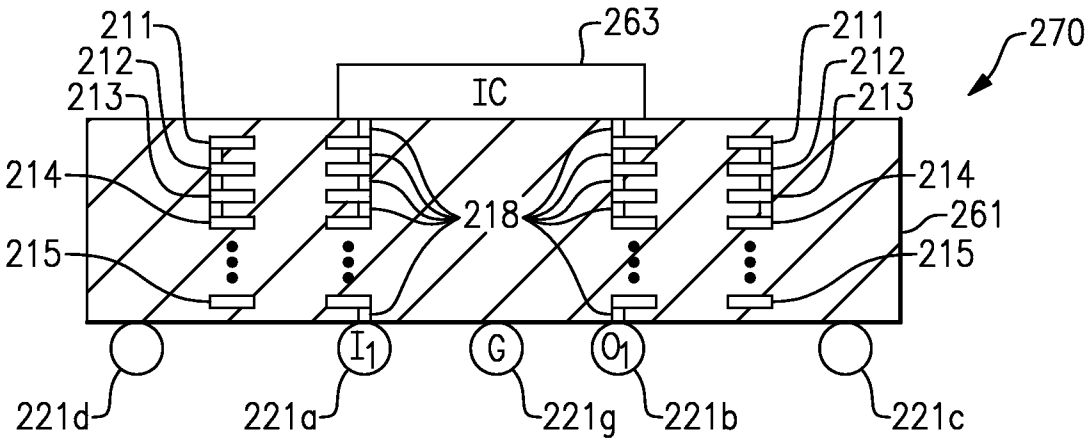


FIG.11B

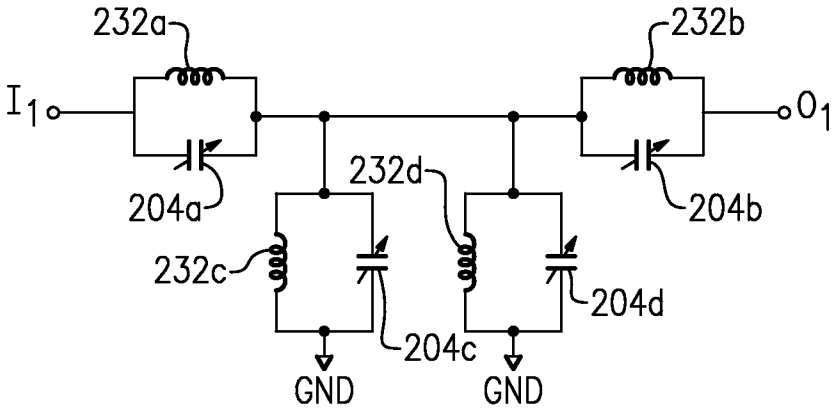


FIG.11C

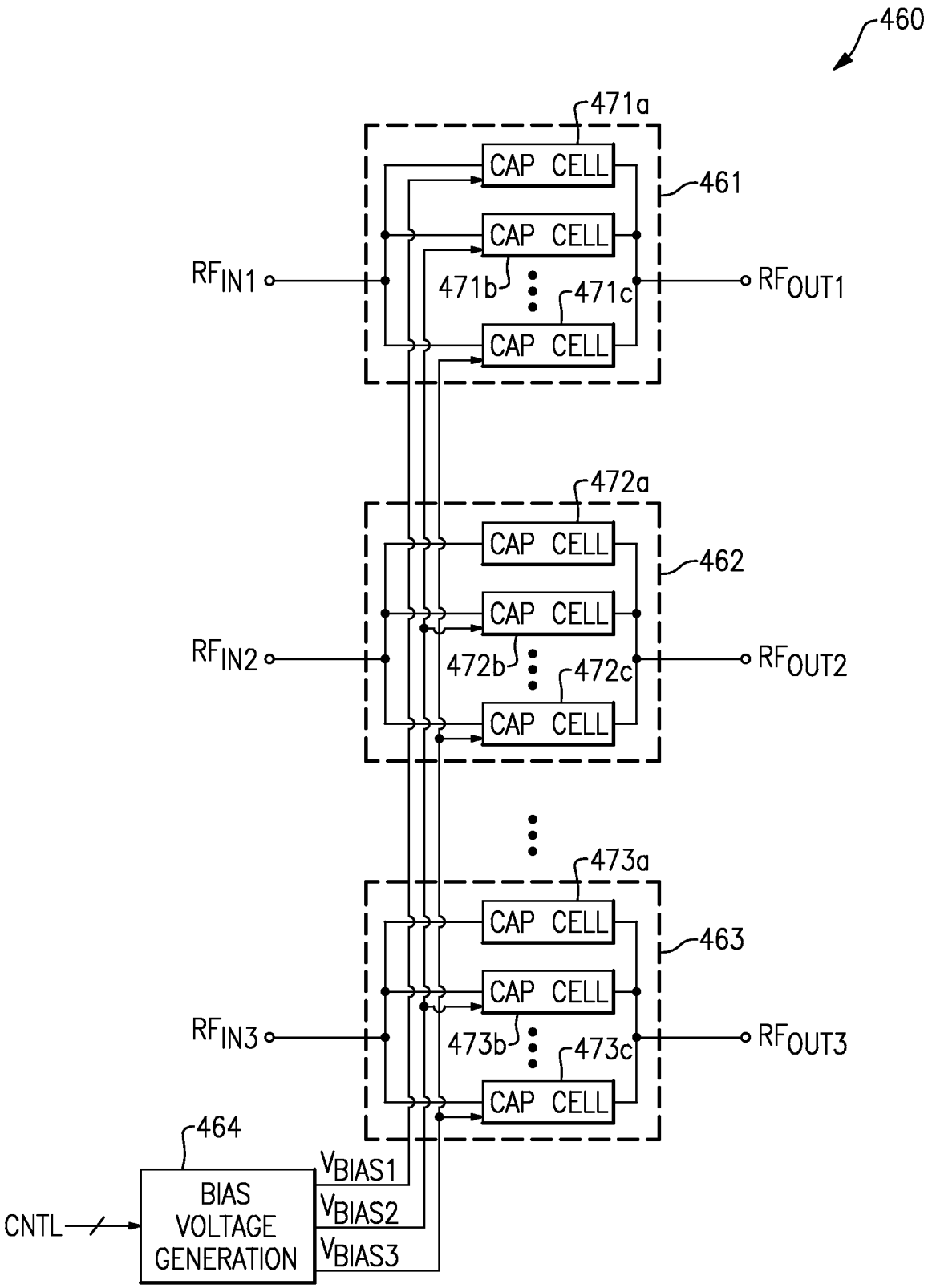

460
471a
CAP CELL
CAP CELL
CAP CELL
461
RFIN1
471b
471c
RFOUT1
472a
CAP CELL
CAP CELL
CAP CELL
462
RFIN2
472b
472c
RFOUT2
473a
CAP CELL
CAP CELL
CAP CELL
463
RFIN3
473b
473c
RFOUT3
464
CNTL
BIAS VOLTAGE GENERATION
VBIAS1
VBIAS2
VBIAS3

FIG.12

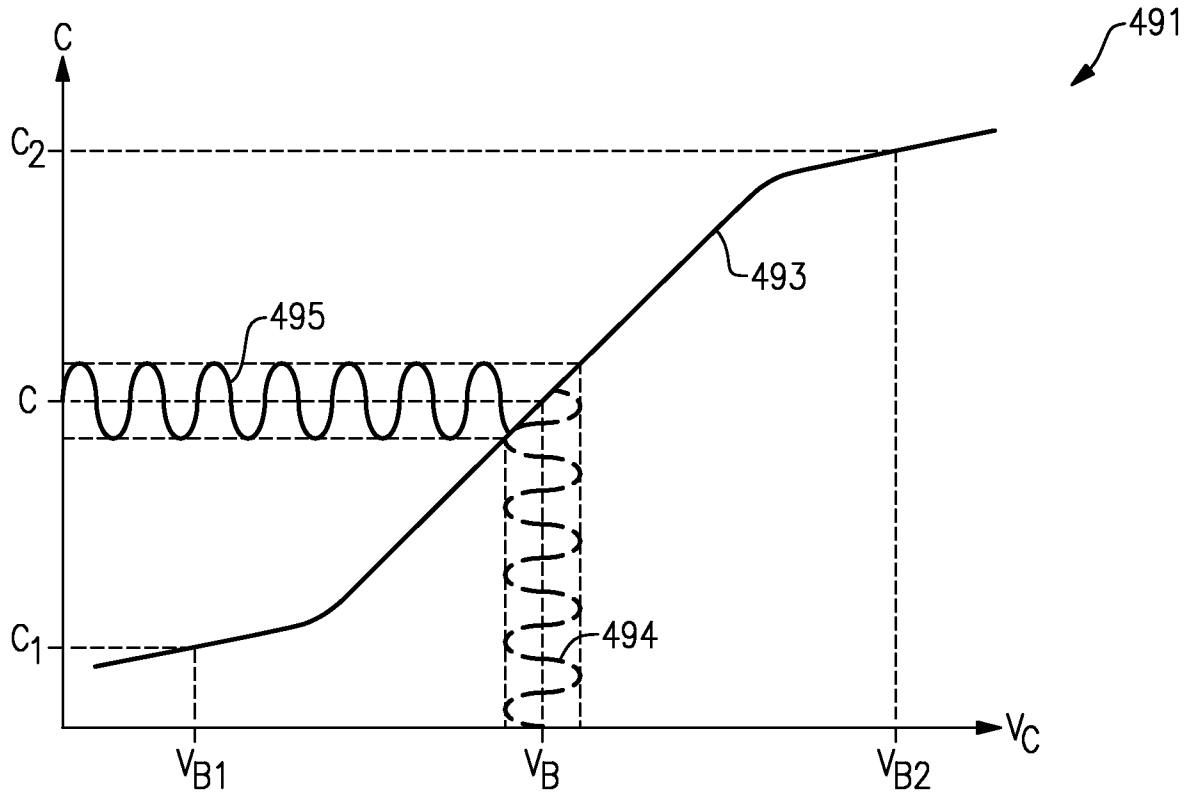


FIG.13A

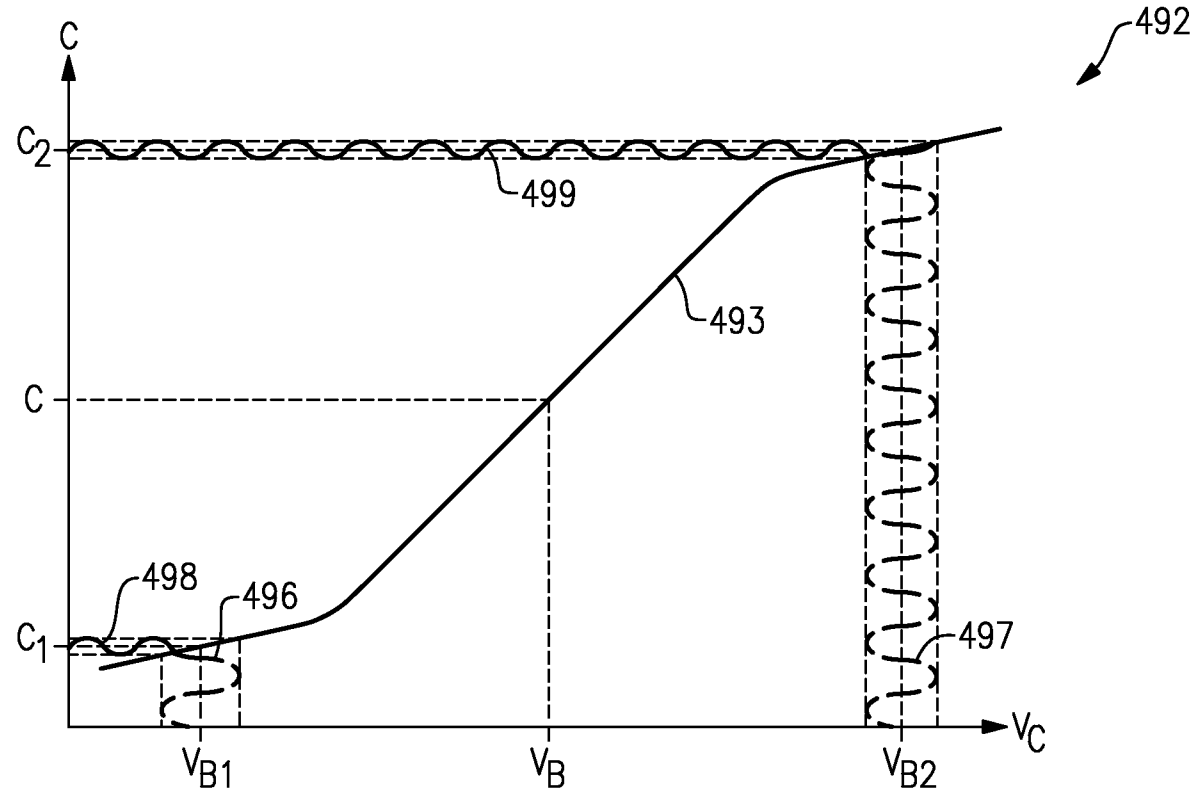


FIG.13B

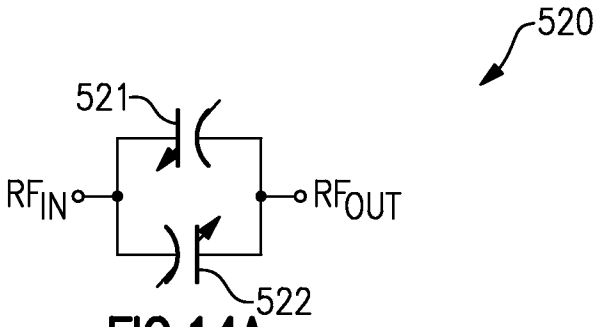


FIG.14A

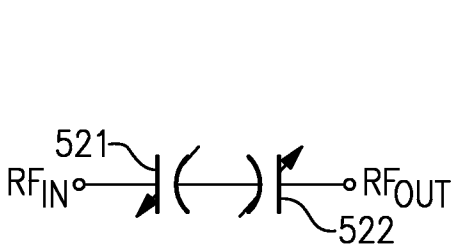


FIG.14B

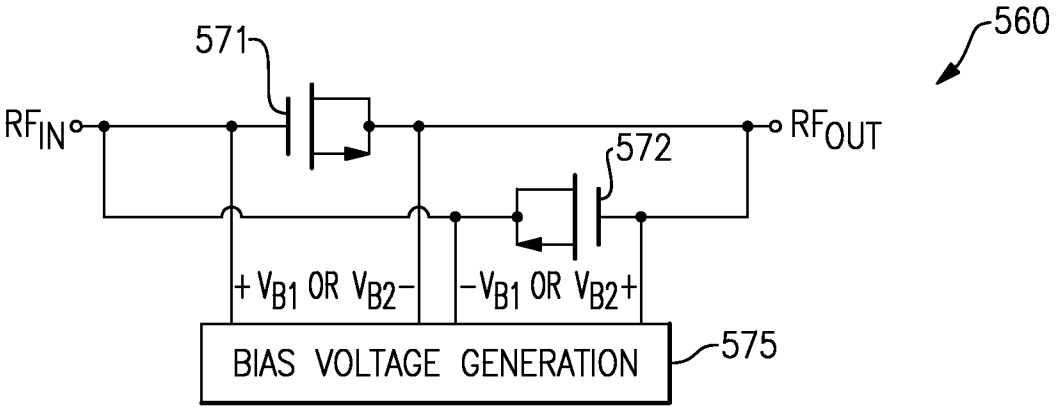


FIG.15A

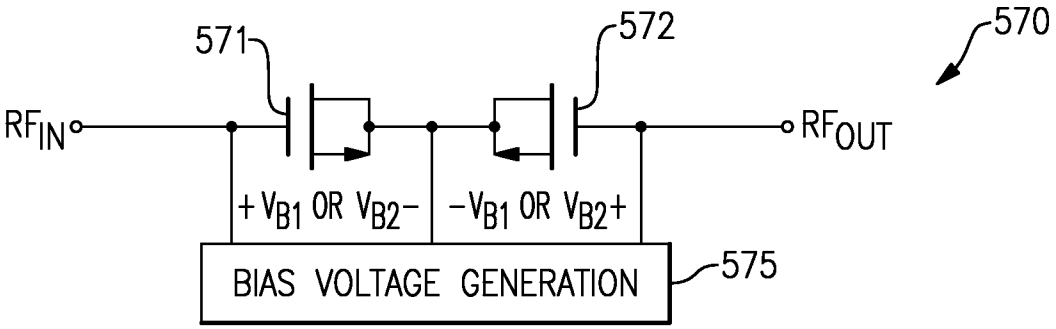


FIG.15B

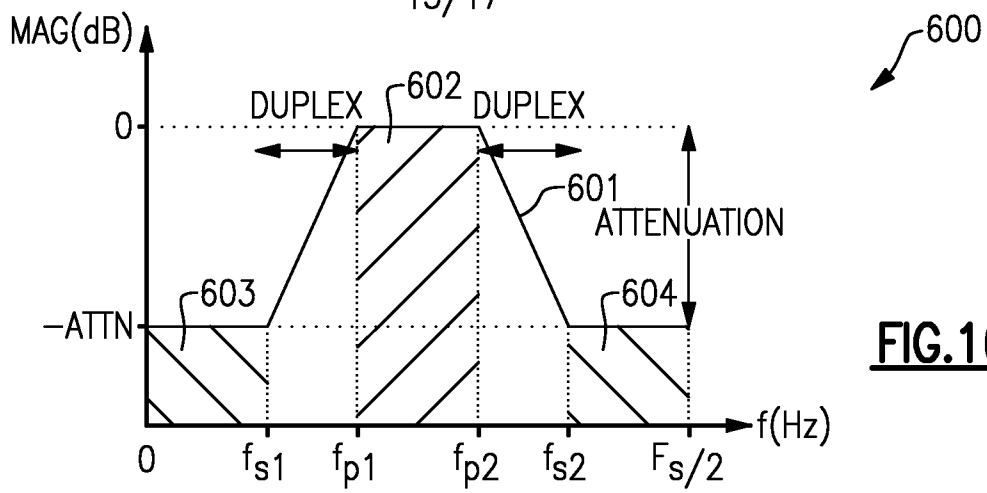


FIG.16A

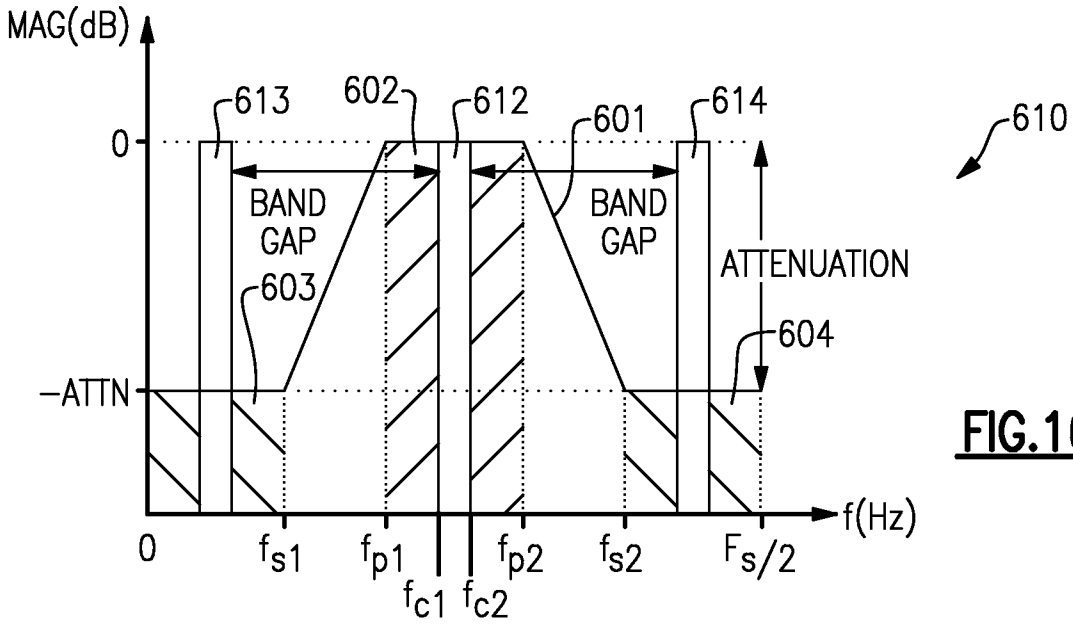


FIG.16B

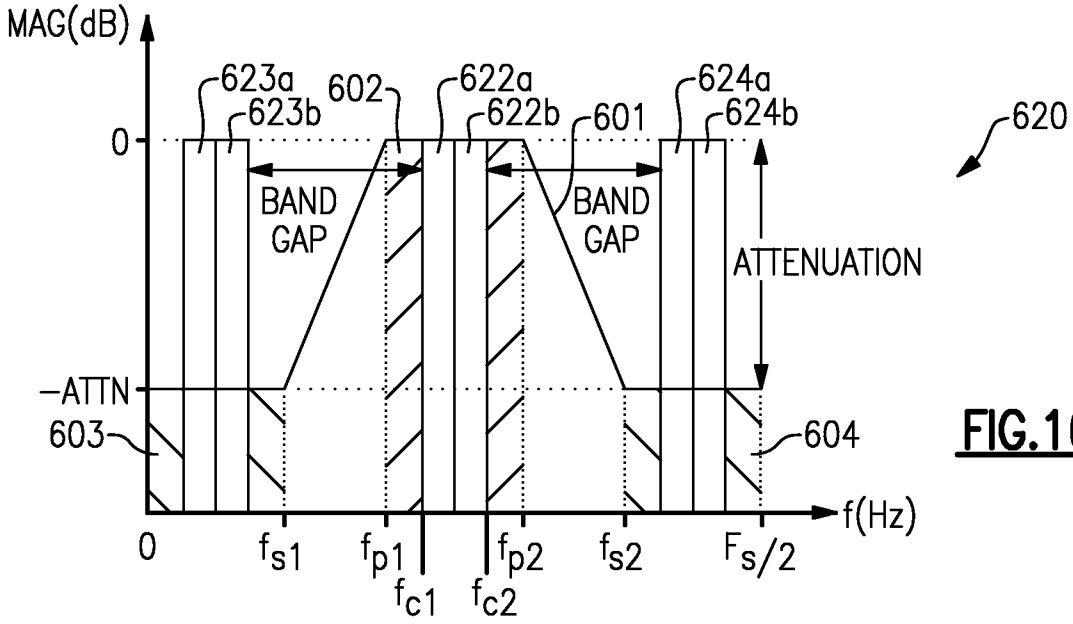


FIG.16C

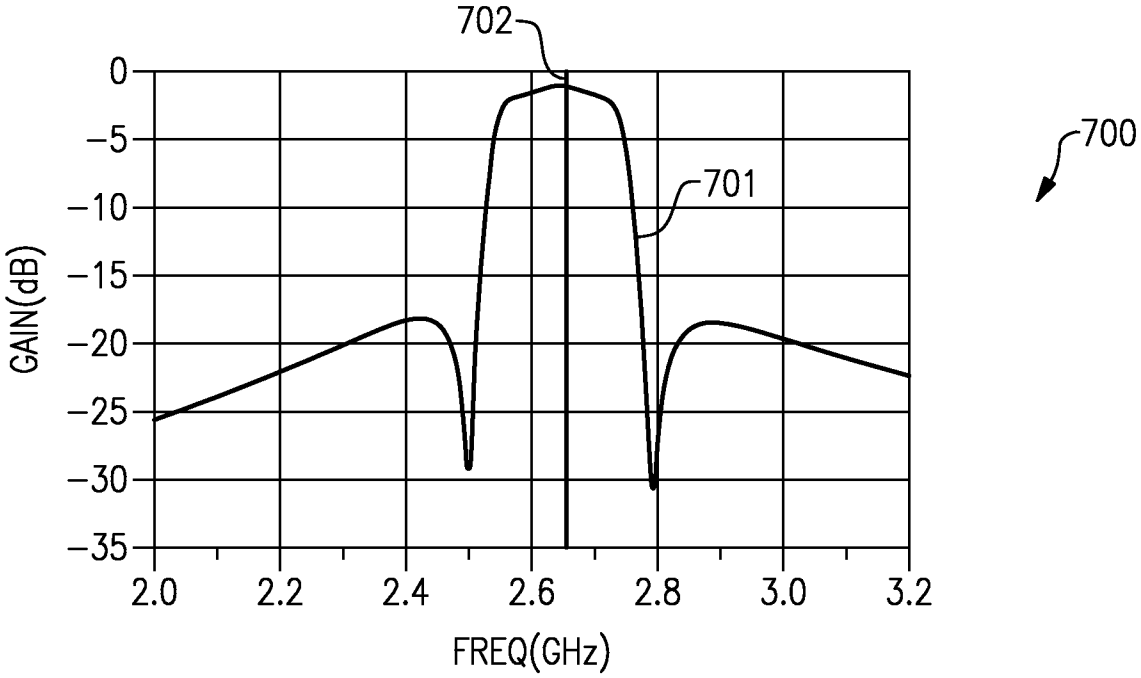


FIG.17A

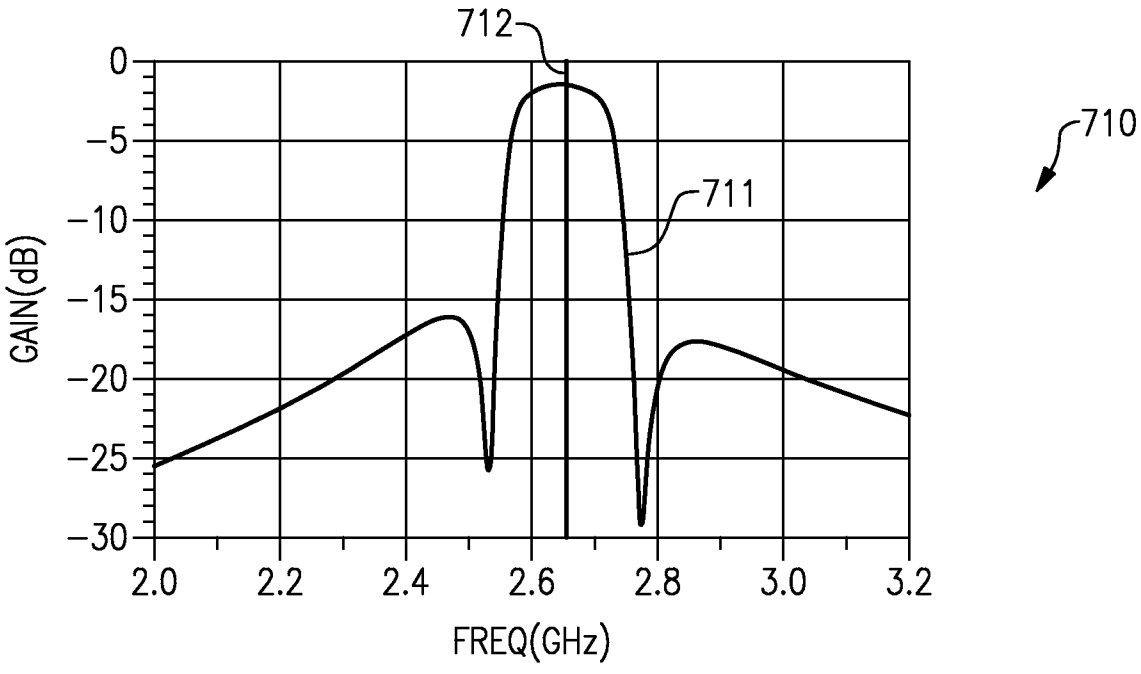


FIG.17B

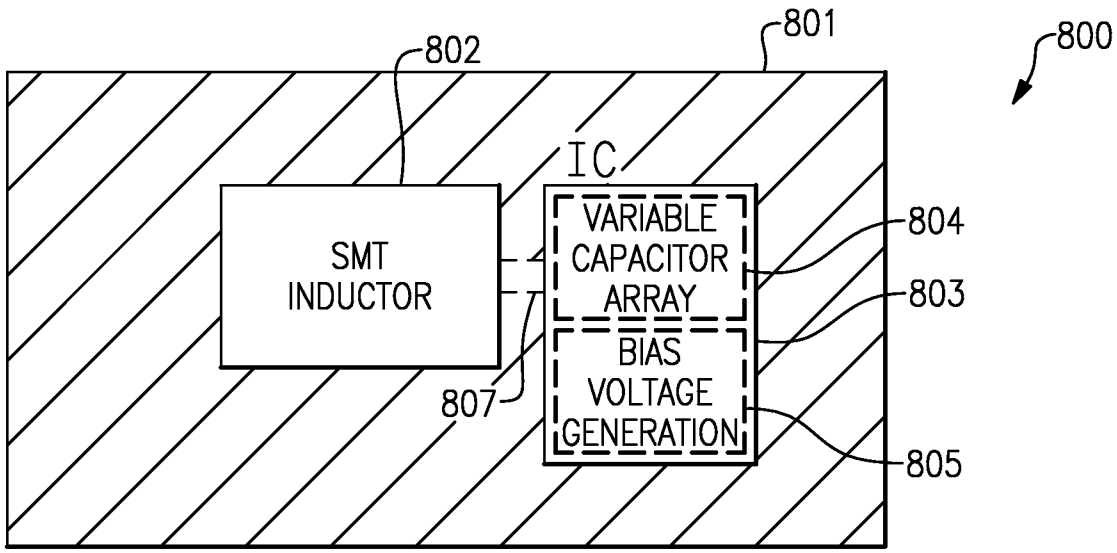

800
801
802
IC
SMT
INDUCTOR
VARIABLE
CAPACITOR
ARRAY
BIAS
VOLTAGE
GENERATION
804
803
805
807

FIG.18

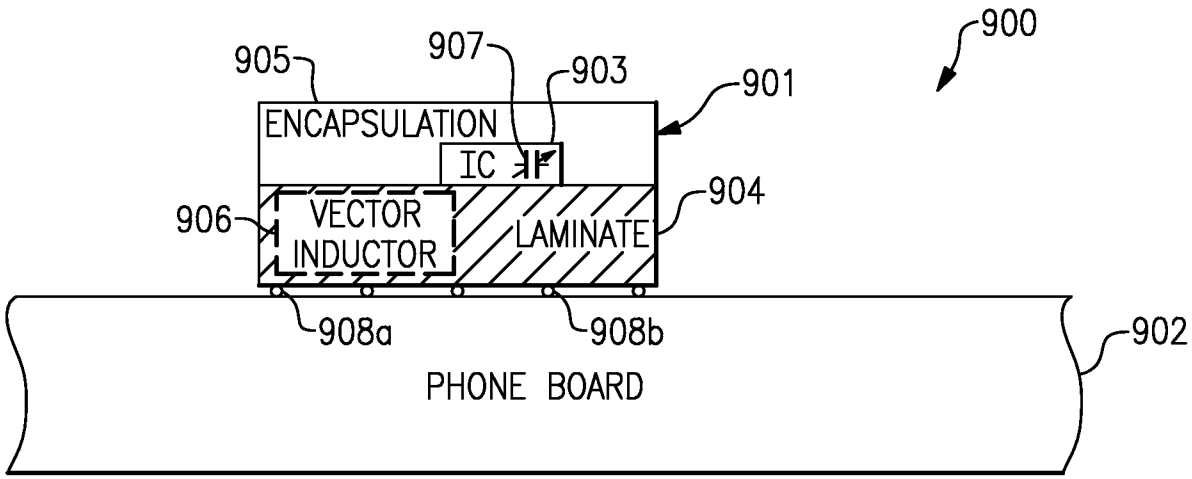

900
905
907
903
901
ENCAPSULATION
IC
904
906
VECTOR
INDUCTOR
LAMINATE
908a
908b
902
PHONE BOARD

FIG.19

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/059018

A. CLASSIFICATION OF SUBJECT MATTER

H03H 7/12(2006.01)i, H03H 7/46(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03H 7/12; H03H 9/15; H03K 5/00; H03B 5/12; H03H 7/01; H03H 7/46

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: filter, tunable, laminate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2009-0273416 A1 (HIROSHI NAKATSUKA et al.) 05 November 2009 See paragraphs [0009], [0100]-[0105]; and figures 1A-5.	23
A		1-22
Y	US 2006-0103456 A1 (KOUROS AZIMI et al.) 18 May 2006 See paragraph [0027]; and figures 1, 2.	23
A	US 2010-0039189 A1 (TETSUO TANIGUCHI) 18 February 2010 See paragraphs [0041]-[0076]; and figures 2-5.	1-23
A	US 2014-0285286 A1 (WISPRY, INC.) 25 September 2014 See paragraphs [0025]-[0032]; and figures 1-4B.	1-23
A	US 2008-0042771 A1 (SEON-HO HAN et al.) 21 February 2008 See paragraphs [0030]-[0048]; and figures 4, 5.	1-23

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 February 2016 (19.02.2016)	**19 February 2016 (19.02.2016)**

Name and mailing address of the ISA/KR	Authorized officer
International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea	KIM, Do Weon
Facsimile No. +82-42-472-7140	Telephone No. +82-42-481-5560

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/059018

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009-0273416 A1	05/11/2009	CN 101501990 A	05/08/2009
		CN 101501990 B	14/03/2012
		EP 2051377 A1	22/04/2009
		EP 2051377 A4	28/03/2012
		JP 04691163 B2	01/06/2011
		US 7986198 B2	26/07/2011
		WO 2008-016075 A1	07/02/2008
US 2006-0103456 A1	18/05/2006	US 7199651 B2	03/04/2007
US 2010-0039189 A1	18/02/2010	CN 101682307 A	24/03/2010
		CN 101682307 B	27/03/2013
		EP 2148438 A1	27/01/2010
		EP 2148438 A4	21/07/2010
		JP 04356803 B2	04/11/2009
		KR 10-1026712 B1	08/04/2011
		KR 10-2009-0121337 A	25/11/2009
		TW 200908430 A	16/02/2009
		TW I359527 B	01/03/2012
		US 7907034 B2	15/03/2011
		WO 2008-143071 A1	27/11/2008
US 2014-0285286 A1	25/09/2014	WO 2014-145662 A2	18/09/2014
		WO 2014-145662 A3	06/11/2014
US 2008-0042771 A1	21/02/2008	KR 10-0821126 B1	11/04/2008
		KR 10-2008-0011616 A	05/02/2008
		TW 200807886 A	01/02/2008
		US 7688155 B2	30/03/2010