

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
21 August 2008 (21.08.2008)

(10) International Publication Number
WO 2008/100324 A3

- (51) **International Patent Classification:**
H01L 25/065 (2006.01)
- (21) **International Application Number:**
PCT/US2007/071370
- (22) **International Filing Date:**
15 June 2007 (15.06.2007)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
11/453,885 16 June 2006 (16.06.2006) US
11/538,567 4 October 2006 (04.10.2006) US
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- (81) **Designated States (unless otherwise indicated, for every kind of national protection available):** AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) **Designated States (unless otherwise indicated, for every kind of regional protection available):** ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) **Title:** METHOD FOR ACHIEVING VERY HIGH BANDWIDTH BETWEEN THE LEVELS OF A CACHE HIERARCHY IN 3-DIMENSIONAL STRUCTURES, AND A 3- DIMENSIONAL STRUCTURE RESULTING THEREFROM

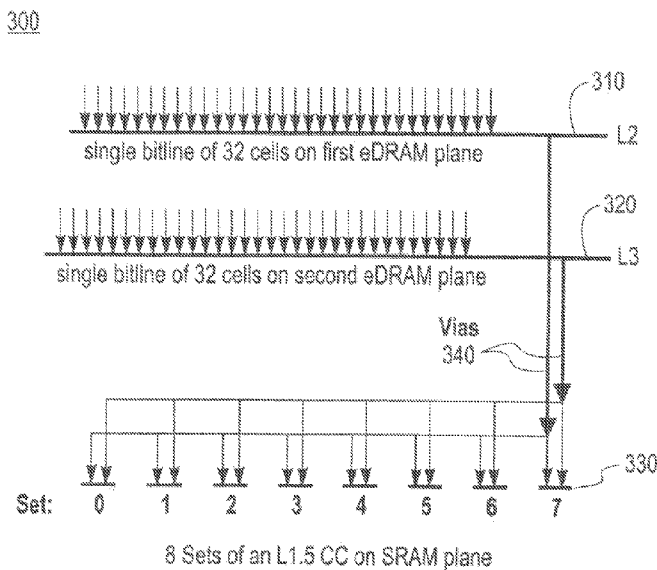


Fig. 3

(57) **Abstract:** A method of electronic computing, and more specifically, a method of design of cache hierarchies in 3-dimensional chips, and a cache hierarchy resulting therefrom, including a physical arrangement of bits in cache hierarchies implemented in 3 dimensions such that the planar wiring required in the busses connecting the levels of the hierarchy is minimized. In this way, the data paths between the levels are primarily the vias themselves, which leads to very short, hence fast and low power busses.

WO 2008/100324 A3



Published:

- *with international search report (Art. 21(3))*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(88) Date of publication of the international search report:
13 January 2011

(15) Information about Correction:

Previous Correction:
see Notice of 22 May 2009

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2007/071370

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L25/065
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 175 160 B1 (PANICCIA MARIO [US] ET AL) 16 January 2001 (2001-01-16) column 1, line 60 - column 2, line 3 column 2, line 65 - column 3, line 11 column 3, line 27 - line 45 figure 3.	1-31
A	----- KIMURA M: "BRIDGING THE GAP BETWEEN PACKAGES AND CHIPS: 10MUM SUPER SONNECT TECHNOLOGY", SOLID STATE TECHNOLOGY, PENNWELL CORPORATION, TULSA, OK, US, vol. 43, no. 11, 1 November 2000 (2000-11-01), page 56,58,60, XP000976042, ISSN: 0038-111X the whole document ----- -/--	1-31

 Further documents are listed in the continuation of Box C. See patent family annex.

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Date of the actual completion of the international search

18 November 2010

Date of mailing of the international search report

25. 11. 2010

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INTERNATIONAL SEARCH REPORT

International application No

PCT/US2007/071370

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>US 2006/113653 A1 (XIAOQI SHERRY [US] ET AL ZHU SHERRY XIAOQI [US] ET AL) 1 June 2006 (2006-06-01) paragraph [0004] paragraph [0019] - paragraph [0020] figures 2,3</p> <p style="text-align: center;">-----</p>	1-31
A	<p>KARNEZOS M: "ADVANTAGES OF SYSTEM ON A PACKAGE AND SYSTEM ON A CHIP", ELECTRONIC PACKAGING AND PRODUCTION, CAHNERS PUBLISHING CO, NEWTON, MASSACHUSETTS, US, vol. 41, no. 8, 1 July 2001 (2001-07-01), pages 32-34,36, XP001093552, ISSN: 0013-4945 the whole document</p> <p style="text-align: center;">-----</p>	1-31

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2007/071370

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6175160	B1	16-01-2001	NONE

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