PATENT SPECIFICATION (11) 1 569 284

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(21) Application No. 44508/76 (22) Filed 26 Oct. 1976
(31) Convention Application No. 7534087
(32) Filed 7 Nov. 1975 in
(33) France (FR)
(44) Complete Specification published 11 June 1980
(51) INT CL³ H04L 11/20
(52) Index at acceptance
H4P PS

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(54) DATA PACKET SWITCHING SYSTEM

(71) We, TELECOMMUNICATIONS RADIOELECTRIQUES ET TELEPHONIQUES T.R.T. a French Body Corporate of 88 rue Brillat Savarin, 75013 Paris, France, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a data packet switching system, of use more particularly but not exclusively for the formation of long-range binary data transmission networks for telecommunication.

Data transmission between the users of any one network proceeds of course either on a real time or delayed time basis. The corresponding switching centres use two different switching techniques-line or circuit switching for real time transmission and message switching for delayed time transmission.

Each of the two techniques has its advantages including:

For line switching, short trunking time, no restriction on format, dialogue, transparency of the network;

For message switching, maximum load management, spreading of traffic peaks, multiple routing, transmission between incompatible terminals.

Each system also has its particular disadvantages.

In message switching systems the switching centres have stores for storing data temporarily until the addressee is available.

Data packet switching is related to message switching. The latter, which is already in use in the U.S.A. (ARPA), also uses shared time and consists of dividing the message into packets or mini-messages each having a destination address and of routing the packets through the network by means of an identifying marker. The packets corresponding to a single message or collection of data can travel by different routes according to the instantaneous rout availability. At each of the centres passed through the packet is written into a fast store, processed and immediately retransmitted. The packet is erased from the store immediately acknowledgement of its receipt has been received from the destination centre.

The flexibility of packet switching is such that it enables the network to be used in optimum conditions.

Packet switching networks carry data which are regrouped in packets on their journey between a single origin and a single address. Packets from various origins and for various destinations travel consecutively along the link lines between the nodes of the network. At their passage through the nodes the packets can be temporarily stored, processed and oriented.

There are packet switching networks using the virtual circuit method in which each packet has a communication number. The consultation of a table present in each of the stores of the switching centres indicates the characteristics of the communication. The communication number allows the sequence in which packets are transmitted to be controlled. In this method a call between two users or subscribers passes through the same phases as for line switching—i.e.:

Trunking—i.e., writing of characteristics into stores,
Communication between subscribers,
Release.

The simplicity of the procedure for routing received packets by consulting a directly accessible table helps to speed up switching performances considerably.

There is no difficulty in restoring the packets into the order in which they were formed, and so there is no need to have special storage facilities at the departure point from the network for the sake of onwards transmission to the addressee.

This invention relates to a data packet switching system using virtual addressing. In such systems, which are used on specialised networks, switching is performed by telecommunications computers which simultaneously analyse the packet markers and provide routing.

Relatively cheap computers are arranged hierarchically so as to share traffic and to exchange information. However, an increase in the number of simultaneous communications leads to an at least proportional increase in the number of computers, with an appreciable increase in the first and operating costs of the network. If the number of computers is limited, serious problems of distributing the common resources arise very soon; also, a limited system cannot cope with the traffic peaks occurring when a large number of subscribers are connected to a network simultaneously.

In the system according to this invention, separate elements are responsible for switching functions and for the functions of trunking and supervising calls. This separation of functions is known in telephone self-switching units but is not used in any data transmission network. The amount of equipment required is reduced since the available equipment is used better.

It is another object of the invention to provide a communications system of the kind hereinbefore defined, of use for forming a network having a large number of subscribers with very heavy traffic to be switched. The technology is accordingly adapted at all levels to the work to be done. For instance, repetitive operations are provided by wired logic circuits whereas more complex operations are peformed by means of recorded programs. The system also makes the greatest possible use of micro-programming, the microprograms being written into programmable dead stores having a fragmented structure.

This system aims at meeting the following criteria:

Network transparency for subscribers,

Semi-real time—i.e., information line transit time should be short enough for instantaneous dialogue to be possible.

Adaptation to subscriber's procedures, as compared with known message switching systems in which the messages must be of a particular format,

Reliability thanks to the presence of spare units,

Adaptability—i.e., the possibility of gradual extension of the network without modification of its basic structure.

According to the present invention there is provided a data packet switching system including transmission lines and switching centres, wherein the data packets are directed by virtual addressing and wherein each switching centre comprises at least one control unit and at least one line switching module connected on a bus loop, the control unit including a store which provides virtual addressing and determines the connections to be made.

Other features and advantages of the invention will become apparent from the following description of an embodiment with reference to the accompaning drawings wherein:—

Figure 1 shows a switching centre unit;

Figure 2 shows a small switching centre;

Figure 3 shows a switching link;

Figure 4 shows a synchronous line adapter ALS;

Figure 5 shows a synchronous line unit ULS;

Figure 6 shows a processor common to the synchronous line units ULS, to the asynchronous line units ULA and to the packet processing stage PP;

Figure 7 shows the executive element of the synchronous line unit ULS;

Figure 8 is a schematic view of the arrangement of a packet processor;

Figure 9 shows the input-output supervisor of the packet processor;

Figure 10 shows the store adaptation circuit, and

Figure 11 shows the connector of a packet processor PP to the time bus B.T.

In the system according to this invention the basic unit providing connecting and switching functions will be referred to as a switching centre. The aim of switching centre is to arrange for the connection of synchronous or asynchronous lines and to make the necessary adaptations before transmission to the switching unit in accordance with a predetermined procedure and in the required format.

Referring to Figure 1, each switching centre comprises at least one switching module 1 and at least one modular control unit 2. All the switching modules 1 will

hereinafter be referred to as the switching chain 3. In the case of synchronous lines the modules are connected to MODEMS. The modules 1 and the control units 2 communicate with one another via a time bus loop 4. As previously stated, the switching modules interconnect subscribers in accordance with instructions given by the control unit. A control unit 2 consists of a mini-processor 21, an extensible addressing store 22 and a peripheral unit 23 used only for maintenance services. As will be described hereinafter, the processing capacity of a switching unit can be increased by the use of a larger number of control units, the system being by its nature modular.

Figure 2 shows a small centre containing one switching module and one control unit. All the switching centres are of identical construction, the only variation being in the number of components and in the programs, in accordance with the jobs allotted to each particular centre.

A switching module (Figure 2) consists of:

At least one synchronous line adapter ALS,

At least one asynchronous line unit ULA,

A switching link consisting of at least one synchronous line unit ULS and at least one packet processor PP.

Referring to Figure 8 and Figure 2 the packet processor PP consists of a data input and output stage 51, a mini-processor 36 and a store matching circuit 53. Circuit 53 communicates via an interface AM with a main store MM adapted for considerable extension. These stages will be described hereinafter.

The block schematic diagram of Figure 3 shows a fitted-up switching link in which all elements are duplicated for reliabilty. The switching module is connected to the time bus by time bus connection stage CBT. The control unit UC, which does not form part of the link, includes a programmable computer of the universal mini-computer kind. The same kind of computer is used for maintenace at local control points PCL and for operating the system. The size of the control units depends upon the number of calls to be trunked whereas the size of the switching modules depends upon the number of connections and upon the switching throughput.

Brief description of the functions of the stages of a switching module (Figure 3).

A synchronous line adapter ALS serves for encoding at T.T.L. level the data coming from the MODEMS for transmission to the line unit ULS and vice versa. One adapter can regroup up to 8 lines. It provides electrical matching to network characteristics, demultiplexes data at transmission and performs the converse operations at reception;

The synchronous line unit ULS receives trains of bits from the ALS to which it is connected. The ULS forms the characters, makes redundancy checks and transmits them to the packet processor PP after processing. In the opposite direction the ULS receives from the packet processor to which it is connected characters which it serialises in bits which it transmits to the ALS. These operations are performed under the supervision of a skilled processor and operators.

Just by way of example, a synchronous line unit can be connected to 16 synchronous line matchers and can therefore manage up to 128 lines, so that a data input and output traffic of greater than 1 M bits can be handled;

The asynchronous line unit ULA serves to manage exchanges with parallel junctions JP and to process the characters so as to present to the packet processor PP an interface identical to the interface presented by the ULS;

The packet processor PP receives characters from the line units, shapes, analyses and switches the data packets, restores the frames formed by a bunch of packets and transmits the characters to the line units.

Two sub-assemblies of the packet processor operate in parallel, namely:

The entry-output sub-assembly 51 (Figure 8) which manages exchanges either with the line units or with another switching unit, performs very repetitive operations of entering or extracting characters as a buffer store: the processor itself analyses the frames and packets.

These two sub-assemblies utilize the store access circuit SAM 53 (Figure 8) to gain access to the common store.

The store matching interface AM (Figure 8) manages exchanges of words, e.g., of a length of 16 bits, between the packet processors PP and the common store MM. It has a safety feature for addressing and for data.

The common store MM consists e.g. of store boxes MOS.

A time bus connector is a means of providing information exchanges between

the packet processor PP and the control unit within the same link or between different links.

According to a feature of the system according to this invention, data are exchanged by pulse code modulation (PCM). A 40-channel time bus has a handling capacity of 80 M bits/s.

Every connector can connect all the packet processors and all the control units to a time bus of the system-i.e., all the time bus connectors (C.B.T.) have the same structure.

Simple and repetitive functions, such as restoration of transmitted characters and serialization of characters for transmission, are performed by wired microprograms for the sake of high processing capacity. Functions which are simple but which call for parameters, such as recognition of particular characters, parity calculations and redundancy code calculations, are performed by wired logic under the control of a processor. Specialised functions such as frame analysis and packet processing are performed by specialised processors executing a program contained in a fast store. More general functions such as call trunking, system supervision and network management are performed by universal calculators.

The ways in which the network—i.e., the lines and switching units—may be used derive from the following principles:

Existence of multiline links,
Virtual circuit method,
Regulation of flux at links and virtual circuits,
Semi-matching routing,
Reservation of buffer stores.

A multiline link is a group of connected lines and equipment considered as a data channel, so that data can pass along an available channel in the event of some other route being interrupted. Bits regrouped into frames are transmitted via the first free line. Indications of data flux are given at two levels.

At link level a frame is addressed from A to B only if it can be received by B. Frame receipt acknowledgements which initiate release of the store resources are provided more rapidly because of the use of multiline networks.

At virtual circuit level the network controls the maximum rate of packet acceptance in dependence upon the rate of progress of previous packets.

Routing is the mechanism determining the route to be taken by the data at the time when the call is trunked. Routing is shared in thresholds. There are a number of routes from any one switching unit for reaching any one subscriber. The principle of routing is to follow a priority itinerary determined by the quantity of data, i.e. whether or not it is below a particular threshold, and then within the determined itinerary to use itineraries of consecutively decreasing order of priority within the same threshold band. Costing, i.e. determining the data rate allocated to each priority level, the itineraries calls for knowledge of data formed by adjacent switching units.

The extent of "look-ahead" is the number of packets receivable at the end B before their transmission over a particular line. This factor is therefore defined by the availability of storage capacities at transit points.

The reserved store volume is a means of ensuring buffer store availability. For economic reasons the buffer stores actually used vary along the path of a call.

Synchronous Line Matcher

Figure 4 is a diagrammatic view of a synchronous line matcher ALS for TTL encoding of the data coming from line junctions such as e.g. the CCITT standard V 24 or V 35 line junctions. The data are collected bit by bit for transmission over the network or are restored bit by bit at reception. Concentration and shaping of the data are performed progressively in the various stages.

The synchronous line matcher provides electrical matching and the multiplexing or demultiplexing of data, according as it is transmitting or receiving. A number of matchers ALS, e.g. 16, are connected to a synchronous line unit ULS (Fig. 3) via a common bus and each separately via a calling channel.

Referring to Figure 4, the stage 25 is the stage which is connected to the clock of the MODEMS by connections 114, 115. A decoder 25*a* counts the clock pulses to give the card number—i.e., the number of the synchronous line matcher which is transmitted to the interface stage with the line unit 26. From stage 26 the data are transferred to the ULS via a 14-wire channel, 8 wires serving for data transmission

and the others for service signal transmissions (two wires for clock signals and four wires for the card number). The ULS must know not only the card or ALS number but also the number of the line connected to it. The line number and data are transmitted to the NOLI (line number) channel.

Via a line H the stage 25 distributes sync pulses which open the gates of stages 24 or 27 according as the event is a write-in (EC) into the MODEM by the stage 24, which is connected to the MODEMS by the lines 103, or a read-out (LE) by the stage 27 which is connected to the MODEMS by the connections 104. The data then go along the lines D connected to the line NOLI.

Stage 24 comprises a demultiplexer which transmits the data bit by bit to the MODEMS, and stage 27 comprises a buffer store which provides a brief storage of the received bits before the reading thereof by the ULS. The interface 26 also comprises a number of silo registers which make it possible to wait for the ULS to become available without loss of information.

Synchronous Lines Unit

Figure 5 is a block schematic diagram of a synchronous line unit. Whereas the synchronous lines matcher ALS arranges for the transmission of data bits between the MODEMS and the network, the synchronous lines unit regroups the bits to form characters and transmits them after processing to the packet processor PP. Conversely, at transmission the ULS receives characters coming from a subscriber through the network by way of the processors PP. As Figure 5 shows, the ULS consists of 7 separate items, a transmission bus 45 and a reception bus 44.

From left to right in Figure 5 the various elements are:

An interface element 26 with the line matchers;

A character restoration and transmission element 31;

An interface element 32 with the packet processor PP;

A parity redundance calculating element 33;

A line storage element 34;

A sequence analysing and transcoding element 35;

A processing element 36.

The processing element 36 is provided to link together the consecutive operations of different elements, recognise and analyese events and perform arithmetical and logic operation on octets.

The element 36 can carry out four kinds of instruction:

Arithmetical and logic operations;

Transfers between internal and/or external registers;

Connections which may or may not be conditional;

Operations controlling specialized registers.

Figure 6 is a diagrammatic view showing the arrangement of the processor 36, the same having two parts which operate simultaneously;

An instruction reader 37 (Fig. 6) extracts the next instruction to be performed from the program store 38, such instruction being placed in a register 39 and performed by an executive element 40;

The next instruction is read while the executive element carries out the pending instruction.

This kind of arrangement is known as the "look-ahead" program.

The instructions reader 37 comprise a program counter 41 which addresses store 38, a buffer register 39 which stores the instruction read in the store, an instructions decoder 42 and a condition muliplexer 43 which, if the tested condition exists, causes a connection. In this event the multiplexer 43 initiates a change of the instruction in the program counter 41. The processor 36 works on each of the lines consecutively and a special link 27 interconnects the register NOLI containing the line number, the line store unit 34, the parity unit 33 and the character transmission restoration stage 31.

Figure 7 shows the executive element 40 which operates with an operand read bus and with an operand write bus. The element 40 controls *inter alia* transfer operations between the two buses.

Connected in parallel between the read bus 44 and the write bus 45 are the following items:

A processor store 46, in the form of a register unit so addressed by the instruction INS as to transmit the content of the registers to the read bus or to receive data from the write bus, the capacity of store 46 being e.g. 32 octets;

A transfer operator 47 (Fig. 7) controlling transfers from the read bus 44 to the write bus 45;

A work register 48 which is loaded by the read bus 44, when the instruction orders it and whose contents can be transferred as second operand to the stage 50;

An arithmetical operator 50 whose first operand is given by the read bus and whose second operand can, where applicable, be taken from the work register 48;

A prom type dead store 49 containing the constants which are used in the processor and which can also enter the stage 50 as second operand, and

An accumulator 51 transmitting the result to the write bus upon termination of the instruction.

Other elements are not shown and are mainly a clock which outputs calls to the condition multiplexer 43 (Figure 6) and a safety monostable periodically reset by the processor. Non-resetting of the monostable causes a signal to be transmitted over a fault wire.

The element 40 operates as follows:

The instruction which is read in the program store 38 (Figure 6) is decoded in the instructions reader 37;

According to the nature of the instruction, one of the transmitter registers outputs its information to the read bus 44;

An operation (a transfer or an arithmetical operation) occurs either in stage 47 or in operator 50;

At the next cycle—i.e., 50 ns later—the result appears on the write bus 45 and a receiving register takes this information into account.

Simultaneously, the next instruction is sampled in the program store 38 and the program counter 41 advances by one unit. As a rule, the advance is a single step, but when there are various connections the advance is determined by the instruction.

In one particular case there are seven kinds of instruction which lead, in the case of the first type, to arithmetical and logic operations on an octet between a constant and the contents of a register R of store 46.

The other kinds of instruction are means of peforming the various operations required.

Operation of the synchronous lines unit described with reference to Figures 5 to 7 is as follows.

Upon each reception of a bit by the ALS, the same generates a calling signal for the ULS, such signal being received by the interface unit with the line matcher 26, more particularly by a wired-logic call encoder. The interface unit stores the number of the calling ALS and transmits a transfer authorisation thereto. The bit then enters the ULS and goes to the character restoration unit 31. The same contains the line number corresponding to the transmitting line, the line number being established by the interface 26 by concatenation of the matcher number and of the line number in the matcher as transmitted by the ALS.

The character restoration unit 31 uses stores directly addressed by calling-line numbers which belong to unit 31. So that the required kind of treatment may be known and the received character stored, the unit 31 can:

Count the consecutive bits in the 1 state so as to recognise the flags;

Detect sync characters;

Store characters during reception in the line stores 34;

Detect the end of the characters, and

Test the transverse parity of the character where necessary and inform the processor of the reconstituted characters and the line they have come from by way of the silo register (first in—first out).

The processor samples the characters received in the latter register and uses the sequence analyser 35 by action on a register forming the input interface of analyser 35. The same detects the individual characters by addressing a dead store and encodes the identified character. The resulting code, together with a line sequence signal from the processor, addresses another store which supplies the processor 36 with the necessary instructions for executing the required action.

The parity operator 33 operates e.g. on 2 or 3-octet stores directly addressed by the line number. Each such store contains the cyclic redundancy character being calculated. For each character, a sequence is triggered and each bit is introduced into the computing logic. The parity operator is loaded and tested by the processor. The data thus processed are subsequently transmitted to the packet processor PP.

For the latter transmission the ULS has an interface stage 32 comprising silo registers absorbing traffic peaks. The ULS therefore addresses to the packet processor:

Information about the nature of the call;
The number of the calling line, and
An octet contents indicator which can be either a data octet (received character) or a service octet. Service data include flag data, begin-packet data, redundancy calculation data and so on.

As regards performances, the ULS takes the form of two systems operating simultaneously and in parallel, one system serving to exchange bits with the ALS while the other, which consists of operators controlled by a speciallised processor, processes and prepares data which have been received or which are to be transmitted.

In the opposite direction—i.e., transmission—the packet processor transmits to the synchronous lines unit octets to be transmitted to the lines and service information of the kind just referred to. Transmission of bits to the ALS proceeds by the calling thereof, the calls being collected by the interface 26 which acts on the unit 31. Transmission of bits to the ALS proceeds by sampling in the line stores of unit 31. These characters were placed in the stores by the processor upon their arrival from the packet processor.

In one embodiment of the invention, through the agency of the parity computing unit 33 and sequence analyser 35, 16 line matchers, corresponding to 128 lines, can be connected to each ULS.

Asynchronous Line Unit

The function of these units is to provide a connection between parallel junctions and a packet processor PP. The asynchronous line units (ULA) act in the same way for the asynchronous lines as do the ULS for the synchronous lines and are of substantially similar construction. On reception they manage the wires of the parallel junctions connected to them, differentiate between procedure characters and the specific characters of some data character users, recognize particular sequences, make longitudinal and transverse parity checks, transcode received characters, trunk calls and release the same in the event of the silences exceeding a critical time.

On transmission they manage the wires of the parallel junctions connected to them, prepare the starts and ends of messages and transmit the longitudinal parity. They comprise a processing unit identical to the one described with reference to the synchronous line unit. The ULA system is similar to the ULS system except for the interface of parallel junctions at which the received characters and the corresponding line number are transmitted to the ULA data processor by way of a silo register.

Packet Processor

A packet processor PP receives characters from the synchronous and asynchronous line units, forms, analyses and switches packets, restores frames and transmits characters to the line units. The packet processor accordingly uses a general store MM which in one embodiment is common to two packet processors of the same kind when an emergency or standby processor is used for the sake of reliability. The switching of packets between line units belonging to different modules calls for exchanges between the general stores of such modules, the exchanges being performed by the packet processor of the particular module concerned by way of a time bus also serving for exchanges between packet processors and control units.

Figure 8 is a block schematic diagram of a packet processor. The same basically comprises a system 51 of output and inputs, the system 51 being connected to the line units and carrying out the simplest and most repetitive operations so as to reduce the work of the processor 36 which is identical to the processors used in the synchronous and asynchronous line units.

The system 51 stores words coming from the line units in a common store, transmits words therein to the line units, seizes a buffer store available at the start of reception of a packet and allots such store thereto, initiates calls to the processor and wait-lists.

In addition to the elements 51, 36 the packet processor comprises a program store 52 and a store access circuit 53. Operations other than those just referred to in the functions of the input and output supervisor proceed under the control of the processor, the same being free from restrictions associated with the response time to calls, such restrictions arising from the need not to lose any incoming character and from the need to cause no delay in the transmission of outgoing characters.

The store access circuit 53 is embodied by a system of fast stores and an associated logic. It can be actuated both by the processor 36 and by the input and output checker 51. It permits direct addressing of tables contained in the central store MM, such tables being arranged in line numbers, logical channel numbers, packet numbers, link numbers and so on.

Figure 9 is a diagrammatic view of the input and output checker, which comprises three functional units:

A register system 60 for connecting the line units exchange bus 70 and the time bus connector CBT 71 with the data transmission store bus 72;

A silo register 61 acting as a buffer store between the UL/CBT exchange bus and the packet processing processor 36 (bus 73), and

A time base 62 adapted to perform a number of sequences of instructions controlling the store access circuit 53, the sequences being recorded in a dead store 63.

A stage 75 connects the processor to the time bus connector.

The input and output checker operates as follows:

When a call enters the checker, the same proceeds to acquire and keep the two octets coming from the line unit in the registers 601 and 603 or, in the case of link-to-link transfers by way of the time bus connector, in the stores 602, 604. Associated with the latter octets are two bits denoting the kind of information received which can be either information for keeping directly in a buffer of a general store of information for communication to the processor 36 via the silo register 61 or information for selecting and performing one of the instruction sequences, contained in the dead store 63, of time base 62 of the input and output checker. The instructions are performed by the store access circuit 53 and are a means of allotting central store positions and wait-listing the filled positions for analysis. The input and output checker associated with the store access circuit 53 therefore operates like a channel triggered by the line unit and reporting to the processor. The number of events to be communicated by the checker to the processor is limited as compared with the number of data items it processes directly.

Conversely, in the event of a call coming from a line unit the checker transmits two octets which it removes from a buffer store by way of registers 605, 606.

In the event of a call coming from the time bus two octets are also transmitted by way of stores 607, 608. An octet counter 64 counts backwards at each character transmission to the time bus, so that the checker can recognize the emptying of a buffer store and start looking in a transmission wait-list row for the contents of the next buffer store to be transmitted.

The processor 36 of the packet processor PP is identical to the processors described with reference to the synchronous line unit ULS and mentioned as forming part of the asynchronous line unit ULA. However, a larger volume of implementation orders is addressed to the processor 36 and to the others since the work it has to perform is more varied than the work which has to be performed by the other processors, the processor 36 having to manage the frames, analyse received packets, wait-list outgoing analysed packets, process and transmit packets ready to be received and clear the buffer stores.

The speed at which these functions are performed depends upon the store access circuit 53 to be described hereinafter. The processor receives operations requests from the input and output checker 51 by way of a silo register 54 which smooths out the traffic. According to a feature of the invention, very repetitive programs are stored in fast dead stores whereas less frequently used programs are stored in a read-write store RWM. Processor 36 also has fast line stores which are addressed directly by the number of the calling line at the rate of e.g. 8 octets per 512 lines. In one actual switching system a packet processor can control 512 synchronous and asynchronous lines. Switching rates of the order of 2 000 000 bauds are possible.

Figure 10 shows the store access circuit 53 of Figure 8. Circuit 53 comprises a system of associated registers and logic operators communicating with one another and with the store by way of data buses 80 and addresses the store 61. The buses 80, 81 do not input directly to the main store MM but are connected to a store-matching interface AM. The actual circuit 53 comprises a unit 82 of marker groups. A marker is defined either by the time base stage 62 of the checker 51 or by an instruction from the processor 36. A group is defined by the line number of the stage 51 or by a register Pr filled by the processor 36. The markers contain e.g. the management indexes of the packets per line or per route link. Unit 83 is a unit

containing the current address of the buffer store which can be addressed by line number and is a means of introducing or removing buffer-stored consecutive characters. Incrementation of these current addresses is performed directly in circuit 53 by adder 84. Unit 85 comprises a number of markers, e.g. 128, which can be either markers Sj addressed directly by the operand *j* of the instruction, e.g. markers of the table of free buffer stores, or markers Spr addressed by a register *pr* 86 filled directly by the processor or markers Wj addressed directly by the operand *j* or the instruction and adapted to be post-indexed by the operand *d* of the instruction or markers Wpr adapted to be post-indexed by the instruction operand *d*. Stages 87, 88 are multiplexers. Via the registers 89, 94 the processor 36 has direct access to the store. Registers 90, 91 form a unit performing the logical *or* operation between the contents of register 80 and a store word. The result is entered into register 92 and addresses the store. The stores 90, 91 are a means of directly addressing the classified tables by logic channel number.

A marker 93 of which one part, AI, is filled by an initial address coming from the store and whose other part 91 is filled by the processor 36 is post-indexed by the instruction operand *d*. The element 93 is a means of addressing e.g. overflow or indirect access tables. The units and registers just described are actuated either by a special instruction of the processor or, for some of such units and registers, by instructions of the checker 51.

Store Matchers

The store matchers encode calls from the packet processors and permit use of the store if the same is available. They supervise the store cards by decoding the address high weights so as to identify the individual car selection rows. When the stores used are MOS tables they generate the timing and refreshement signals, they calculate write and read data redundancies in a Hamming code, they check the address parity bits at read-out and possibly produce a warning signal when any card of the store is wrong.

Common Stores

Advantageously, the common stores used are MOS stores, channel N of 4 k/bit per box. The access time is approximately 200 ns and the cycle time is 400 ns. Reliability of the stores in increased by the use of a code which detects and automatically corrects simple errors. Each 22-bit store word is broken down into 16 data bits, 5 self-correcting code bits and a parities bit of the address where the word is disposed, so that the instructions row can be checked. According to a feature of the invention, a store card has 88 Mos store boxes and the integrated addressing and read circuits. With 4 k/bit boxes, the data capacity of a card is 16 k 22-bit words.

Time Bus Connector

The time bus is a means for the transmission of data and service signals between two packet processors of a single module for signalling exchanges, more commonly between one packet processor of the modules and another packet processor of a different module for packet exchange, between a packet processor and a control unit for the exchange of signalling packets and faults or between two control units UC for updatings.

Information packet exchanges proceed on the basis of a technique similar to the pulse code modulation (PCM) technique used in telephony, where a common bus sequentially connects a receiver during a unit time interval. As a rule, two different calls correspond to two consecutive unit time intervals. Trunking of the calls is managed by a scanning logic circuit which distributes the information necessary for the connection of the transmitters and receivers to a connecting bus which is connected to the time bus. Each unit time interval or time slot is allotted to a packet processor or to a control unit which, according to the traffic, are considered as transmitters or receivers.

The module packet processors are physically connected to time bus connectors. As previously stated, the packet processors are provided in duplicate, one processor being in operation, the other coming into operation in the event of the first becoming faulty. Information indicating that such faults exist and information for reshaping a module are regrouped in registers of the time bus connector and transmitted to the time bus.

The Table given hereinafter represents the structure of a frame i.e., of a

scanning cycle. The time bus is basically a loop to which the packet processors are connected by way of time bus connectors of the kind to be described hereinafter.

The single Table is in the form of rows corresponding to physical lines and columns representing development of transmissions in time.

Row Bp is the parity bit row and rows B0 to B7 carry the information octets in parallel. Rows B8, B9 are frame sync rows. Row CBT represents the appearance of the timing signals in time and the last line of the Table represents either the receiving packet processor or a control unit.

Each channel is allotted to a receiving packet processor PPO to PPM. A channel comprises three octets which present consecutively to the time bus. The first octet contains identification bits of the packet processor or of the transmitting control unit. The octets 1, 2 carry the information which it is required to switch.

Each time slot lasts e.g. 150 microseconds and is sufficient for the transfer of 1 octet. 15 packet processors and 1 control unit are scanned during each frame, the traffic of one control unit being statistically equal to approximately 1/16th of the traffic of the packet processors. At switching the first octet transmitted indicates what the number is of the transmitter and also, by means of the bit B0, whether the channel is clear or busy and, by means of the bits B1, B2 whether what is occurring is a buffer store start X or a message end Y. The octets 1, 2 are then transmitted to the packet processor concerned.

The time switching used here has considerable advantages over the physical switching provided by a cross-bar type device, since the traffic which the system can accept can be increased readily by using multiple time buses.

Bp		⊗	⊗	⊗	⊗	⊗	⊗					⊗	⊗	⊗	⊗	⊗	⊗
B0	DATA ITEMS	UGEmet.	Y	X	occ			UGEmet.	Y	X	occ			UGEmet.	Y	X	occ
B1		OCTET 1						OCTET 1						OCTET 1			
B2		OCTET 2						OCTET 2						OCTET 2			
B3																	
B4																	
B5																	
B6																	
B7																	
B8/9	Sync frame	0	1	1		1	1	1						1	1	1	1	1	1
CBT	Time bus Connector timer	H	H	H		H	H	H						H	H	H	H	H	H
	Receiving UG's	pp0				pp1								pp4			ppX		
														x = 0..n					

Figure 11 shows a time bus connector CBT connected in parallel with the actual time bus 95. At its input 96 the connector receives the timing signals of the time bus. In the connector the time bus 95 goes consecutively through an amplifier 97, a receive register 98, a multiplexer 100 and a second amplifier 97*a*.

A pilot station 99 controlling the operation of the system has been shown in diagrammatic form *promemoria* and is disposed anywhere on the loop 4 (shown in Fig. 1) formed by the bus.

The timing pulses arriving at 96 enter a receiving channel 101 which identifies the channel number Kr. This stage takes the form e.g. of a 48-position shift register which advances in proportion as the timining signals arrive. The output signal of stage 101 is applied simultaneously to a code comparator 102 and to a multiplexer 103. Comparator 102 compares the received code with the code stored in stage 104, which is a stage for identifying the module connected via the time bus connector. Comparator 102 opens the gates if the code number received at a given time corresponds to the module number, otherwise the gates stay closed and nothing occurs. The stage 104*a* is an amplifier.

Data coming from the bus 95 are multiplexed with the code of channel KR in multiplexer 103, then entered in a silo register 105 which concatenates the data with the kind of call coming from a wired logic circuit 106. The data are therefore placed in wait rows and are transmitted to the packet processor on the exchange bus 107 via an amplifier 106 only when the same is opened at 108. The transmission route 95, 103, 105—107 relates solely to reception by a packet processor of data coming from the time bus. In the opposite direction data are sampled from bus 107 by two registers 109, 110, whereafter the octets 1, 2 are transferred to stores 111, 112 whereas the octet O is multiplexed in 113 with the number of the channel KR. If the result of the code comparison in 102 is positive, the contents of stores 111, 112 are transferred to multiplexer 100 and thence to time bus 95 where they will be recognised by the destination packet processor as previously stated.

The SILO registers 105 and stores 111, 112 are used to present data to the receiving element at predetermined times; as in the other stages they are a means of introducing and removing the data asynchronously.

The symmetrical standby or spare components are not shown.

Means for supervising and maintaining the network which will not be described correspond to each switching centre. The actual control units can be embodied by minicomputers having an appropriate logic facility. Such computers are already commercially available and do not form part of the invention.

The switching system according to this invention makes it possible to take full advantage of equipment possibilities.

Modifications can of course be made to the embodiments hereinbefore described, *inter alia* by the substitution of equivalent technical means, without departure from the scope of this invention.

WHAT WE CLAIM IS:—

1. A data packet switching system including transmission lines and switching centres, wherein the data packets are directed by virtual addressing and wherein each switching centre comprises at least one control unit and at least one line switching module connected on a bus loop, the control unit including a store which provides virtual addressing and determines the connections to be made.

2. A system according to Claim 1 wherein a switching centre comprises a group of identical switching modules and a group of identical control units, the number of each kind of unit depending upon the maximum processing capacity of the centre, all the units of a centre being sequentially connected by way of a time bus.

3. A system according to Claim 2 wherein each switching module has provision for the concentration in stages of the data between the line interface and the time bus interface, the line interface working on binary bits while the time bus interface works on data packets.

4. A system according to Claim 1 wherein each switching module comprises at least one line unit which receives bits to reconstitute characters and *vice versa*, and a packet processor which receives characters and forms data packets and *vice versa*.

5. A system according to Claim 4 wherein each line unit and each packet processor comprises an identical fast computer operating sequentially on the data which have been received or which are to be transmitted over a line.

6. A system according to Claim 1 wherein a switching module comprises a general store, a packet processor and at least one line unit connected to the packet processor and to a line group.

7. A system according to Claim 1 wherein a synchronous line unit is connected to a synchronous line matching group which is in turn connected to modems which multiplex the data received from the lines and *vice versa*.

8. A system according to Claim 4 wherein the packet processor is connected to the general store by way of a store-matching circuit containing markers for directly addressing predetermined positions of the store.

9. A system according to Claim 1 wherein simple and repetitive functions are performed by wired logic circuits;

simple functions which require external signals are performed by logic circuits under the control of a processor;

specialised functions are performed by specialized processes, and

the general functions of call trunking are performed by universal computers.

10. A system according to Claim 1, characterised in that all the elementary circuits are provided in duplicate, failure of any circuit causing reconfiguration of the system with the simultaneous transmission of a warning signal.

11. A System according to Claim 1 substantially as hereinbefore described with reference to, and as shown in the accompanying drawings.

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Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1980
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1569284 COMPLETE SPECIFICATION
6 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

Fig.1.

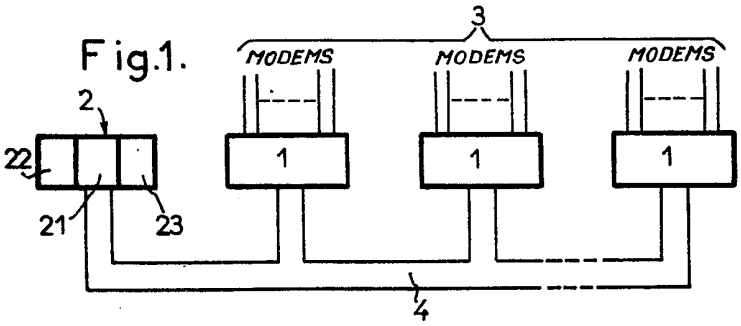


Fig.2.

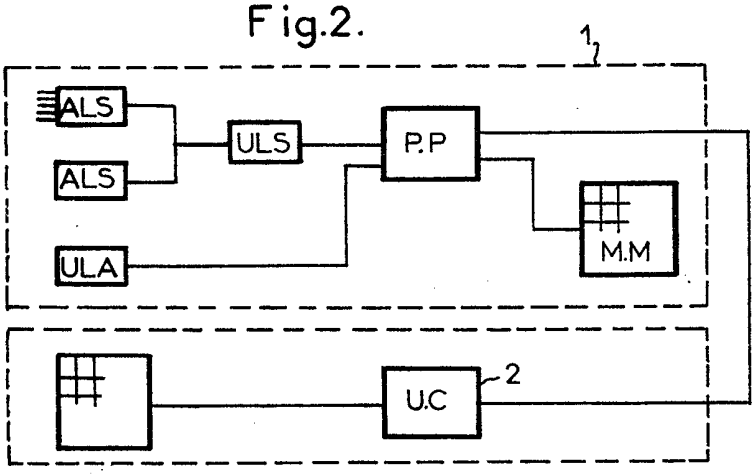
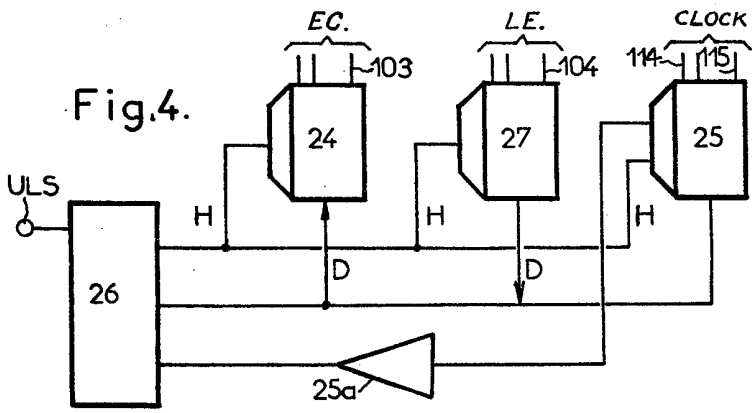
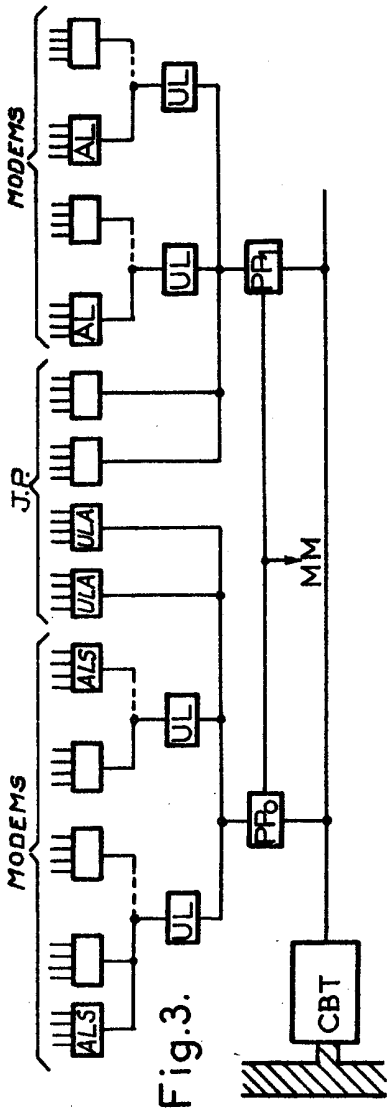


Fig.4.




MODEMS
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UL
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ULA
ULA
MODEMS
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UL
ALS
PP1
PP6
MM
CBT

Fig.3.

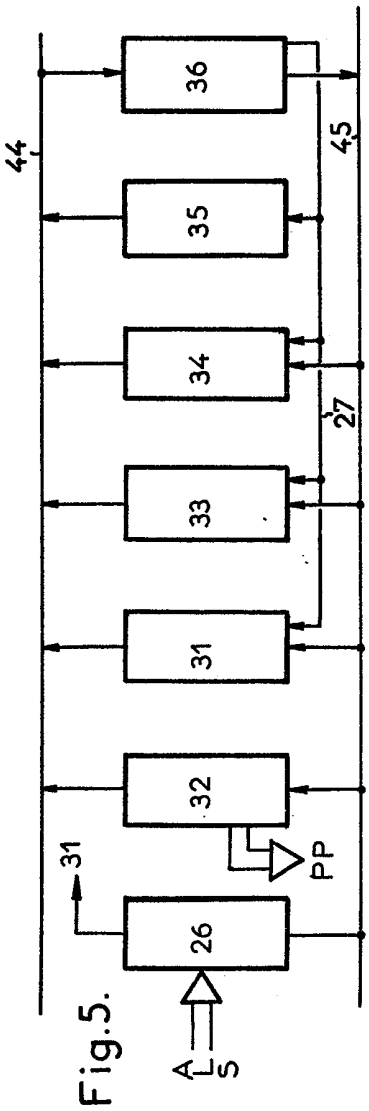
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Fig.5.

Fig.6.

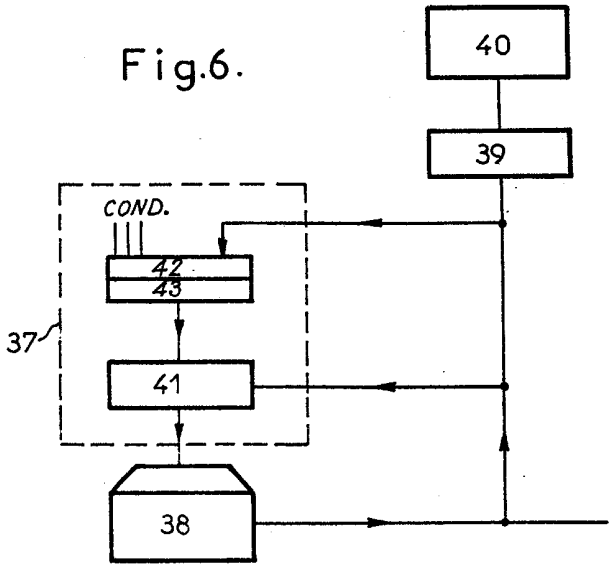

Fig.7.

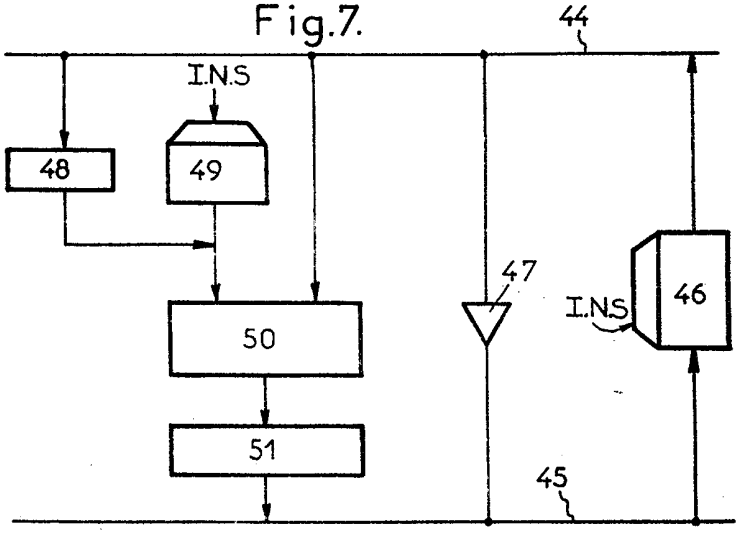

Fig.8.

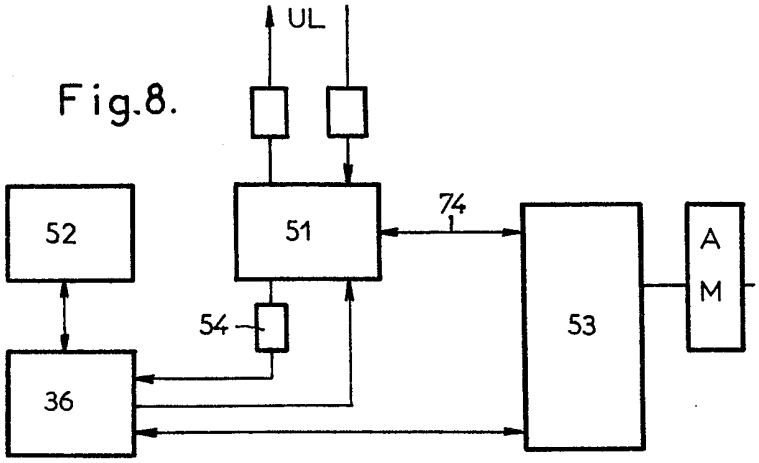
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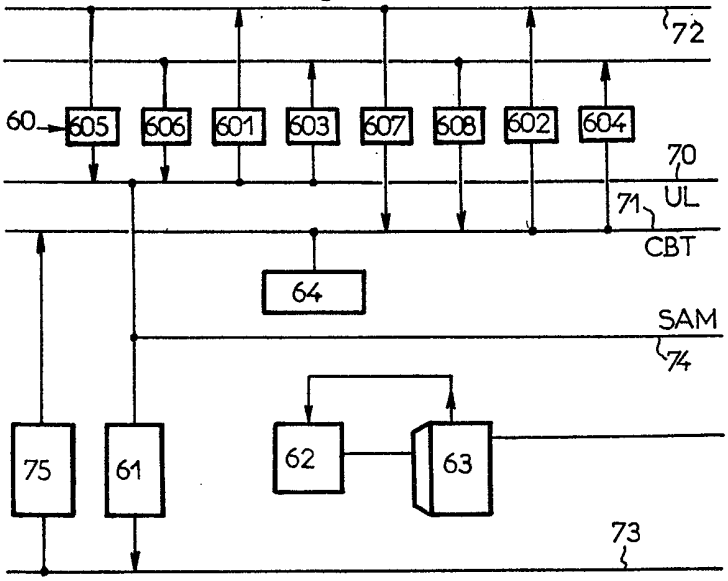
Fig.9.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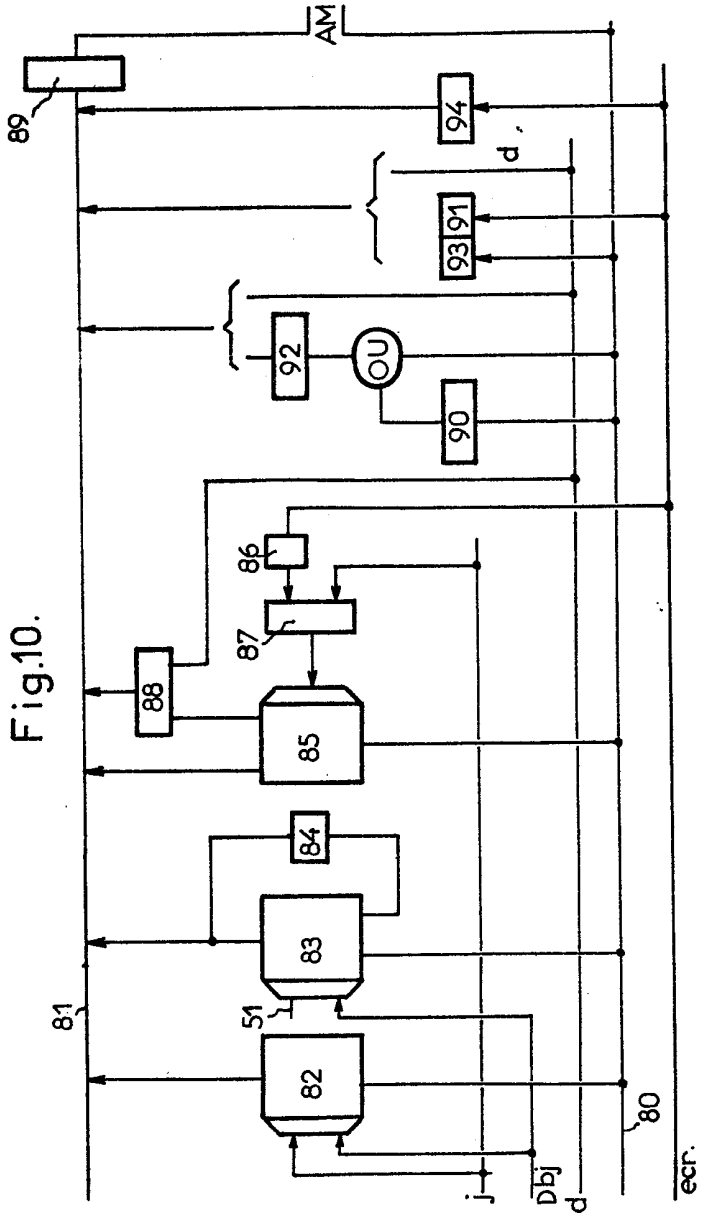
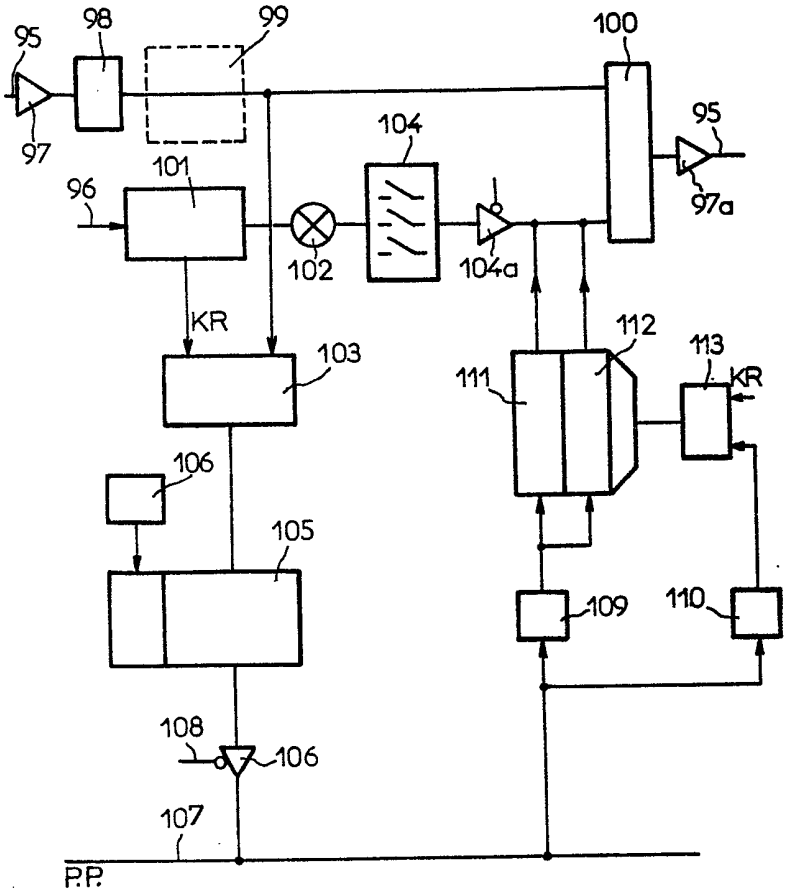


Fig.10.

Fig.11.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